Advanced Information
Preliminary Datasheet

OV9656 Color CMOS SXGA (1.3 MegaPixel) CAMERACHIP™ Sensor with OmniPixel® Technology

General Description

The OV9656 CAMERACHIP™ image sensor is a low voltage CMOS device that provides the full functionality of a single-chip SXGA (1280x1024) camera and image processor in a small footprint package. The OV9656 provides full-frame, sub-sampled, scaled or windowed 8-bit/10-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 15 frames per second (fps) in SXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, white pixel canceling, noise canceling, and more, are also programmable through the SCCB interface. In addition, OmniVision CAMERACHIP sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable color image.

Note: The OV9656 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable apps
- Standard SCCB interface
- Output support for Raw RGB, RGB (GRB 4:2:2, RGB565/555), YUV (4:2:2) and YCbCr (4:2:2) formats
- Supports image sizes: SXGA, VGA, CIF, and any size scaling down from CIF to 40x30
- VarioPixel® method for sub-sampling
- Automatic image control functions including Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Band Filter (ABF), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, gamma, sharpness (edge enhancement), lens correction, white pixel canceling, noise canceling, and 50/60 Hz luminance detection
- Supports LED and flash strobe mode
- Supports scaling

Ordering Information

Product	Package
OV09656-VL1A (Color, lead-free)	28-pin CSP2

Applications

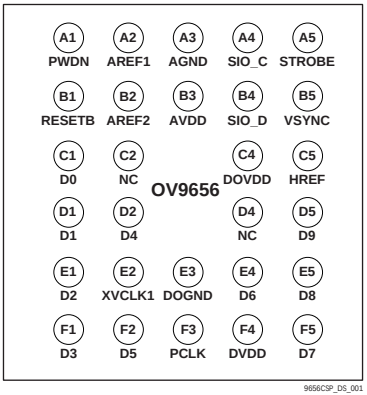
- Cellular and Picture Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

Active Array Size		1280 x 1024
Power Supply	**Core**	1.8VDC ± 10%
	Analog	2.45 to 3.0VDC
	I/O	1.7V to 3.3V[a]
Power Requirements	**Active**	90 mW typical (15fps SXGA YUV format)
	Standby	<20 µA
Temperature Range	**Operation**	-30°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB565/555 • GRB 4:2:2 • Raw RGB Data
Lens Size		1/4"
Chief Ray Angle		25° non linear
Maximum Image Transfer Rate	**SXGA**	15 fps
	VGA, CIF and down scaling	30 fps
Sensitivity		1.1 V/(Lux • sec)
S/N Ratio		42 dB
Dynamic Range		50 dB
Scan Mode		Progressive
Maximum Exposure Interval		1050 x t_{ROW}
Gamma Correction		Programmable
Pixel Size		3.18 µm x 3.18 µm
Dark Current		15 mV/s at 60°C
Well Capacity		10 K e
Fixed Pattern Noise		<0.03% of $V_{PEAK-TO-PEAK}$
Image Area		4.17 mm x 3.29 mm
Package Dimensions		5145 µm x 6145 µm

a. I/O power should be 2.45V or higher when using the internal regulator for Core (1.8V); otherwise, it is necessary to provide an external 1.8V for the Core power supply.

Figure 1 OV9656 Pin Diagram (Top View)



Functional Description

Figure 2 shows the functional block diagram of the OV9656 image sensor. The OV9656 includes:

- Image Sensor Array (1300 x 1028 active image array)
- Analog Signal Processor
- A/D Converters
- Digital Signal Processor (DSP)
- Output Formatter
- Timing Generator
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram

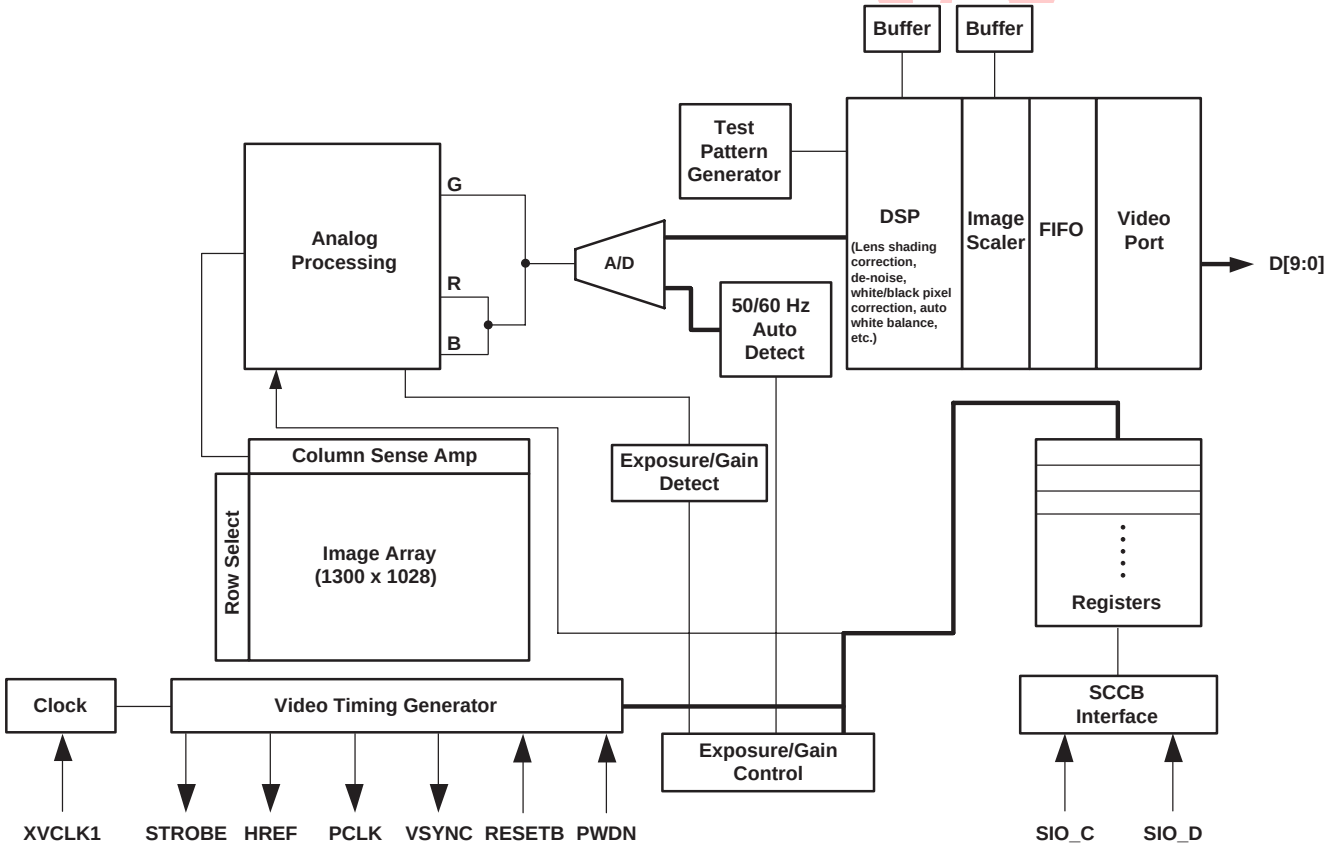


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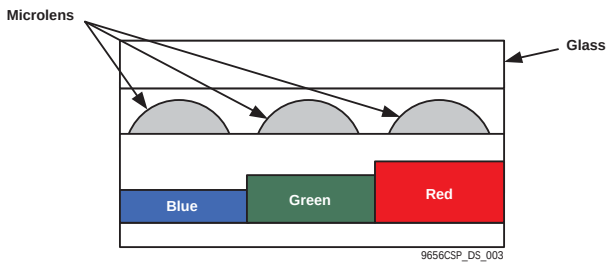
Image Sensor Array

The OV9656 sensor has an active image array of 1300 columns by 1028 rows (1,336,400 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)

A/D Converters

After the Analog Processing block, the bayer pattern Raw signal is fed to two 10-bit analog-to-digital (A/D) converters via two multiplexers, one for the G channel and one shared by the BR channels. These A/D converters operate at speeds up to 12 MHz and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit
- White pixel canceling
- De-noise

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Scaling Image Output

The OV9656 is capable of scaling down the image size from VGA to 40x30. By using register bits COM14[1] (0x3E), COM16[0] (0x41), and registers POIDX (0x72), XINDX (0x74), and YINDX (0x75), the user can output the desired image size. At certain image sizes, HREF is not consistent in a frame.

Strobe Mode

The OV9656 has a Strobe mode that allows it to work with an external flash and LED.

Digital Video Port

Register bits COM2[1:0] increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP sensor operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Location	Name	Pin Type	Function/Description
A1	PWDN	Function (default = 0)	Power Down Mode Selection - active high, internal pull-down resistor. 0: Normal mode 1: Power down mode
A2	AREF1	V_{REF}	Internal voltage reference - connect to ground through 1µF capacitor
A3	AGND	Power	Analog ground
A4	SIO_C	Input	SCCB serial interface clock input
A5	STROBE	Output	Flash strobe signal output
B1	RESETB	Input	Clears all registers and resets them to their default values 0: Reset mode 1: Normal mode
B2	AREF2	V_{REF}	Voltage reference
B3	AVDD	Power	Analog power supply
B4	SIO_D	I/O	SCCB serial interface data I/O
B5	VSYNC	Output	Vertical sync output
C1	D0	Output	Output bit[0] - LSB for 10-bit Raw RGB data only
C2	NC	—	No connection
C4	DOVDD	Power	Digital power supply for I/O
C5	HREF	Output	HREF output
D1	D1	Output	Output bit[1] - for 10-bit RGB only
D2	D4	Output	Output bit[4]
D4	NC	—	No connection
D5	D9	Output	Output bit[9] - MSB for 10-bit Raw RGB data and 8-bit YUV or RGB565/RGB555
E1	D2	Output	Output bit[2] - LSB for 8-bit YUV or RGB565/RGB555
E2	XVCLK1	Input	System clock input
E3	DOGND	Power	Digital ground
E4	D6	Output	Output bit[6]
E5	D8	Output	Output bit[8]
F1	D3	Output	Output bit[3]
F2	D5	Output	Output bit[5]
F3	PCLK	Output	Pixel clock output
F4	DVDD	Power	Power supply for digital core logic
F5	D7	Output	Output bit[7]

NOTE:
D[9:2] for 8-bit YUV or RGB565/RGB555 (D[9] MSB, D[2] LSB)
D[9:0] for 10-bit Raw RGB data (D[9] MSB, D[0] LSB)

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-C}	3 V
	V_{DD-IO}	3 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+0.5V
Lead-free Temperature, Surface-mount process		245ºC

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	–	2.45	2.5	3.0	V
V_{DD-C}	DC supply voltage – Core	–	1.62	1.8	1.98	V
V_{DD-IO}	DC supply voltage – I/O power	–	1.7	–	3.3	V
I_{DDA}	Active (Operating) Current	See Note [a]		20		mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current			10		µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 2.5V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 7.5 fps YUV output, no I/O loading

b. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 2.5V
$I_{DDS-SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to a PWDN pin-initiated Standby

c. Standard Output Loading = 25pF, 1.2KΩ

Table 4 Functional and AC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			18	dB
	Red/Blue Adjustment Range		12		dB
Inputs (PWDN, CLK, RESETB)					
f_{CLK}	Input Clock Frequency	10	24	48	MHz
t_{CLK}	Input Clock Period	21	42	100	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESETB}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB Timing (see Figure 4)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and D[9:0] (see Figure 5, Figure 6, and Figure 7)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	D[9:0] Setup time	15			ns
t_{HD}	D[9:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-C} = 1.8V, V_{DD-A} = 2.5V, V_{DD-IO} = 2.5V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 2.5V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

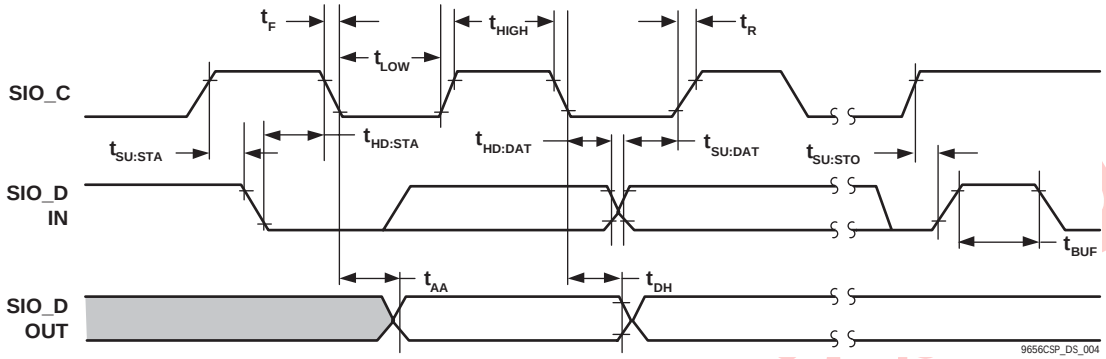


Figure 5 Horizontal Timing

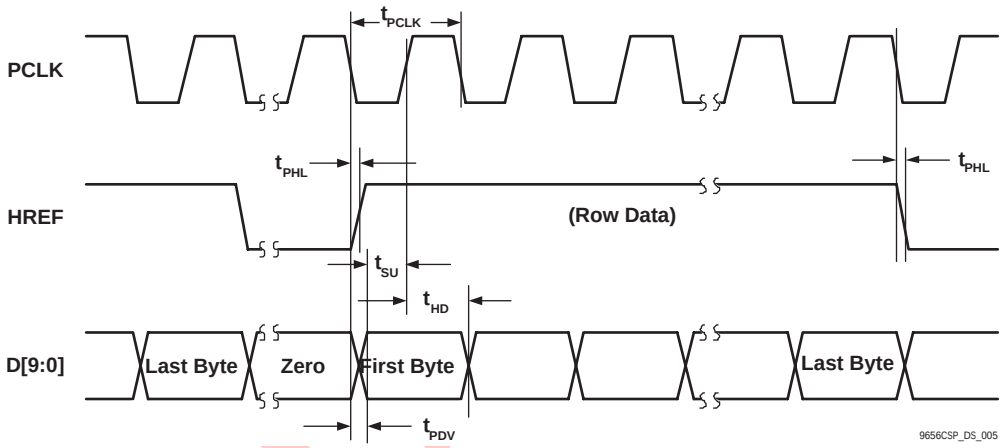
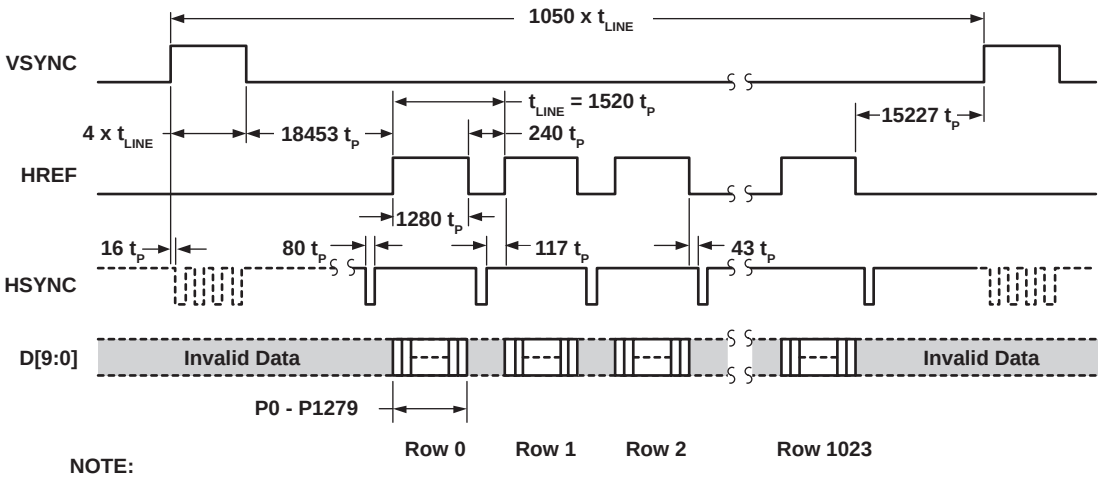


Figure 6 SXGA Frame Timing



NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

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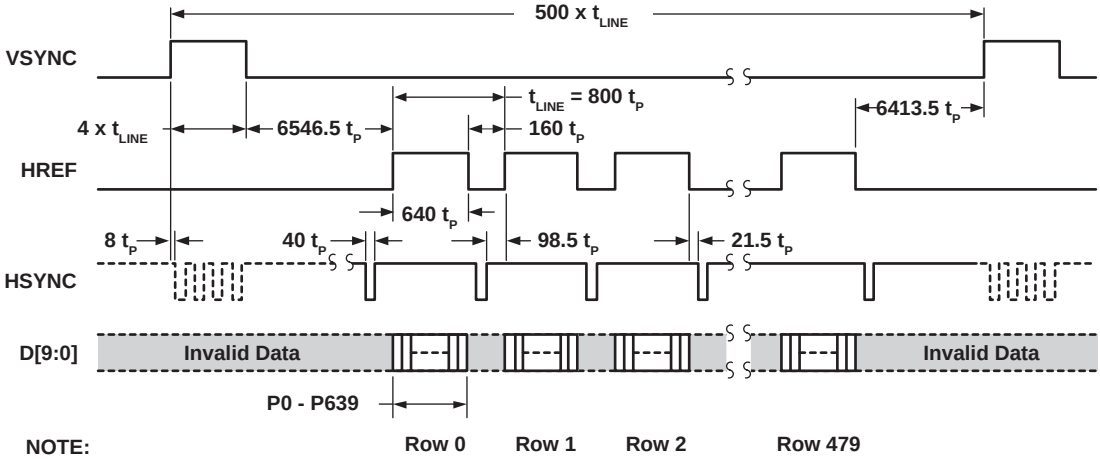
Figure 7 VGA Frame Timing



NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

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Figure 8 RGB 565 Output Timing Diagram

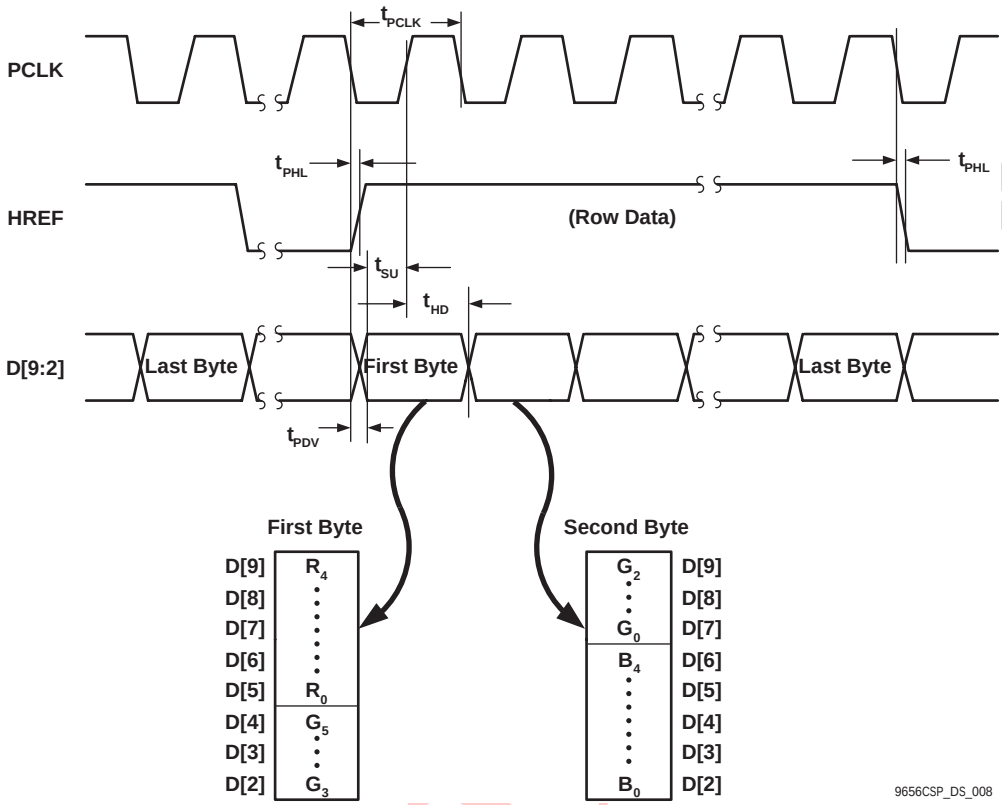
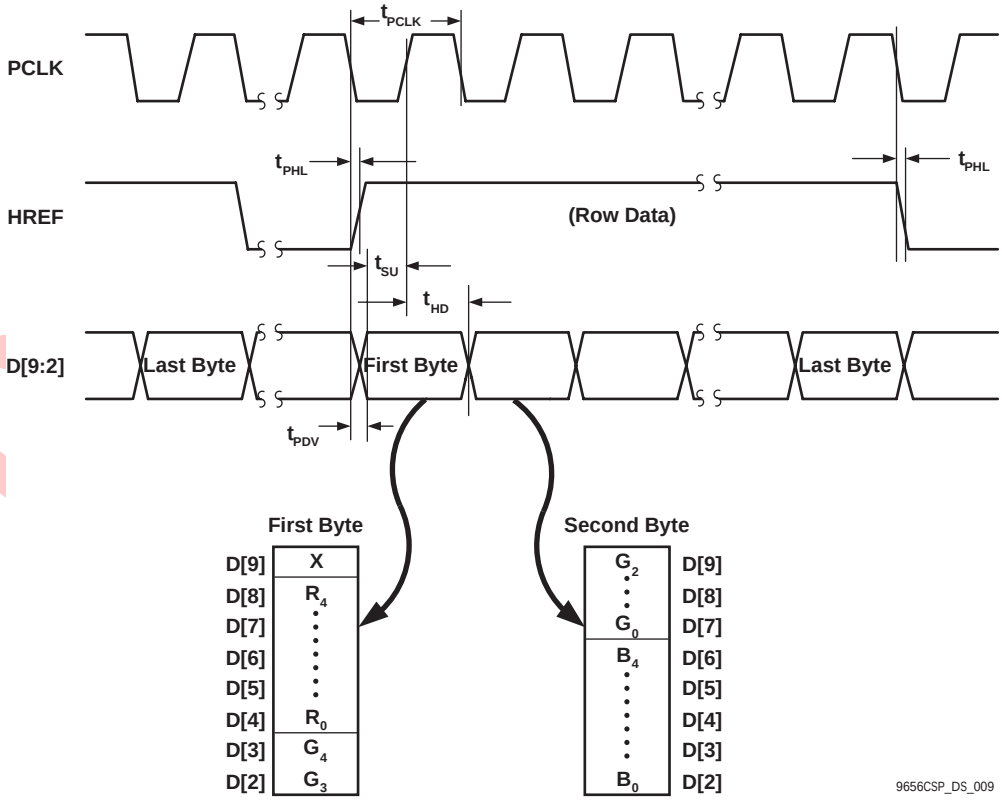


Figure 9 RGB 555 Output Timing Diagram



Register Set

Table 5 provides a list and description of the Device Control registers contained in the OV9656. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 60 for write and 61 for read.

Table 5 Device Control Register List (Sheet 1 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC[7:0] – Gain control gain setting • Range: [00] to [FF]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF]
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF]
03	VREF	12	RW	Vertical Frame Control Bit[7:6]: AGC[9:8] (see register GAIN for AGC[7:0]) Bit[5:3]: VREF end low 3 bits (high 8 bits at VSTOP[7:0] Bit[2:0]: VREF start low 3 bits (high 8 bits at VSTRT[7:0]
04	COM1	00	RW	Common Control 1 Bit[7]: Reserved Bit[6]: CCIR656 format Bit[5:4]: Reserved Bit[3:2]: HREF skip option 00: No skip 01: YUV/RGB skip every other row for YUV/RGB, skip 2 rows for every 4 rows for Raw data 1x: Skip 3 rows for every 4 rows for YUV/RGB, skip 6 rows for every 8 rows for Raw data Bit[1:0]: AEC low 2 LSBs (see registers AECH for AEC[15:10] and AEC for AEC[9:2])
05	BAVE	00	RW	U/B Average Level Automatically updated based on chip output format
06	GbAVE	00	RW	Y/Gb Average Level Automatically updated based on chip output format
07	GrAVE	00	–	Gr Average Level
08	RAVE	00	RW	V/R Average Level Automatically updated based on chip output format
09	COM2	01	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Soft sleep mode Bit[3:2]: Reserved Bit[1:0]: Output drive capability 00: 1x 01: 2x 10: 2x 11: 4x
0A	PID	96	R	Product ID Number MSB (Read only)

Table 5 Device Control Register List (Sheet 2 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0B	VER	57 (for REV5) 56 (for REV4)	R	Product ID Number LSB (Read only)
0C	COM3	00	RW	Common Control 3 Bit[7]: Color bar output Bit[6]: Output data MSB and LSB swap Bit[5:4]: Reserved Bit[3]: Pin selection 1: Change RESETB pin to EXPST_B (frame exposure mode timing) and change PWDN pin to FREX (frame exposure enable) Bit[2]: RGB 565 format option 0: RGB 565 format 1: Output data average Bit[1]: Reserved Bit[0]: Single frame output (used for Frame Exposure mode only)
0D	COM4	00	RW	Common Control 4 Bit[7:4]: Reserved Bit[3]: One-pin frame exposure option ON/OFF selection 0: OFF 1: ON Bit[2]: Tri-state option for output clock at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[1]: Tri-state option for output data at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[0]: Reserved
0E	COM5	01	RW	Common Control 5 Bit[7:5]: Reserved Bit[4]: Slam mode enable 0: Master mode 1: Slam mode (used for slave mode) Bit[3:1]: Reserved Bit[0]: Exposure step can be set longer than VSYNC time 1: In Normal mode, AEC changes by 1/16 and in Fast mode, AEC changes by double

Table 5 Device Control Register List (Sheet 3 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0F	COM6	46	RW	Common Control 6 Bit[7]: Output of optical black line option 0: Disable HREF at optical black 1: Enable HREF at optical black Bit[6]: BLC input selection 0: Use electrical black line as BLC signal 1: Use optical black line as BLC signal Bit[5:4]: Reserved Bit[3]: Enable bias for B/Gr/Gb/R channel Bit[2]: Output window setting auto/manual selection when mode is changed 0: Need to manually update window size when working mode changes 1: Auto change registers HSTART (0x17), HSTOP (0x18), VSTRT (0x19), and VSTOP (0x1A) when working mode changes Bit[1]: Reset all timing when format changes Bit[0]: Enable ADBLC option
10	AEC	40	RW	Exposure Value (middle 8-bits) Bit[7:0]: AEC[9:2] (see registers AECH for AEC[15:10] and COM1 for AEC[1:0])
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7]: Reserved Bit[6]: Use external clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar F(internal clock) = F(input clock)/(Bit[5:0]+1) • Range: [0 0000] to [1 1111]
12	COM7	02	RW	Common Control 7 Bit[7]: SCCB register reset 0: No change 1: Resets all registers to default values Bit[6:4]: Format control 000: Full resolution or 15fps VGA 110: 30fps VGA with VarioPixel® Bit[3:2]: Reserved Bit[1:0]: Output format selection 00: Raw RGB data 01: Raw RGB interpolation 10: YUV 11: RGB

Table 5 Device Control Register List (Sheet 4 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COM8	8F	RW	Common Control 8 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - Step size limit (used only in fast condition and COM5[0] is low) 0: Fast condition change maximum step is VSYNC 1: Unlimited step size Bit[5]: Banding filter ON/OFF Bit[4]: Reserved Bit[3]: Enable "AEC time can be less than 1 line" option Bit[2]: AGC Enable Bit[1]: AWB Enable Bit[0]: AEC Enable
14	COM9	4A	RW	Common Control 9 Bit[7]: Reserved Bit[6:4]: Automatic Gain Ceiling - maximum AGC value 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x Bit[3]: Exposure timing can be less than limit of banding filter when light is too strong Bit[2]: Data format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than the Exposure Gap Bit[0]: Reserved
15	COM10	00	RW	Common Control 10 Bit[7]: Set pin definition 1: Set RESETB to SLHS (slave mode horizontal sync) and set PWDN to SLVS (slave mode vertical sync) Bit[6]: HREF changes to HSYNC Bit[5]: PCLK output option 0: PCLK always output 1: No PCLK output when HREF is low Bit[4]: PCLK reverse Bit[3]: HREF reverse Bit[2]: Reset signal end point option Bit[1]: VSYNC negative Bit[0]: HSYNC negative

Table 5 Device Control Register List (Sheet 5 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
16	REG16	04	RW	Register 16 Control Bit[7:6]: CCIR656 format SAV position option Bit[5:4]: Automatically add dummy frame option 00: Add dummy frame when gain is greater than 2x 01: Add dummy frame when gain is greater than 4x 10: Add dummy frame when gain is greater than 8x Bit[3:2]: Reserved Bit[1]: Enable output "AA" and "55 at blanking period Bit[0]: Reserved
17	HSTART	1A	RW	Output Format - Horizontal Frame (HREF column) start high 8-bit (low 3 bits are at HREF[2:0])
18	HSTOP	BA	RW	Output Format - Horizontal Frame (HREF column) end high 8-bit (low 3 bits are at HREF[5:3])
19	VSTRT	01	RW	Output Format - Vertical Frame (row) start high 8-bit (low 3 bits are at VREF[2:0])
1A	VSTOP	B1	RW	Output Format - Vertical Frame (row) end high 8-bit (low 3 bits are at VREF[5:3])
1B	PSHFT	00	RW	Data Format - Pixel Delay Select (delays timing of the D[9:0] data relative to HREF in pixel units) • Range: [00] (no delay) to [FF] (256 pixel delay which accounts for whole array)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	MVFP	00	RW	Mirror/VFlip Enable Bit[7:6]: Reserved Bit[5]: Mirror 0: Normal image 1: Mirror image Bit[4]: VFlip enable 0: VFlip disable 1: VFlip enable Bit[3:0]: Reserved
1F	LAEC	00	RW	Reserved
20	BOS	80	RW	B Channel ADBLC Result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
21	GBOS	80	RW	Gb channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range

Table 5 Device Control Register List (Sheet 6 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
22	GROS	80	RW	Gr channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
23	ROS	80	RW	R channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
24	AEW	78	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	AEB	68	RW	AGC/AEC - Stable Operating Region (Lower Limit)
26	VPT	D4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: High nibble of upper limit Bit[3:0]: High nibble of lower limit
27	BBIAS	80	RW	B Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
28	GbBIAS	80	RW	Gb Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
29	PREGAIN	00	RW	RGB Channel Pre-gain Bit[7:6]: Reserved Bit[5:4]: G channel pre-gain Bit[3:2]: R channel pre-gain Bit[1:0]: B channel pre-gain
2A	EXHCH	00	RW	Dummy Pixel Insert MSB Bit[7:4]: 4 MSB for dummy pixel insert in horizontal direction Bit[3:2]: HSYNC falling edge delay 2 MSB Bit[1:0]: HSYNC rising edge delay 2 MSB
2B	EXHCL	00	RW	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction
2C	RBIAS	80	RW	R Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
2D	ADVFL	00	RW	LSB of insert dummy lines in vertical direction (1 bit equals 1 line)

Table 5 Device Control Register List (Sheet 7 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2E	ADVFH	00	RW	MSB of insert dummy lines in vertical direction
2F	YAVE	00	RW	Y/G Channel Average Value
30	HSYST	08	RW	HSYNC Rising Edge Delay (low 8 bits)
31	HSYEN	30	RW	HSYNC Falling Edge Delay (low 8 bits)
32	HREF	A4	RW	HREF Control Bit[7:6]: HREF edge offset to data output Bit[5:3]: HREF end 3 LSB (high 8 MSB at register HSTOP) Bit[2:0]: HREF start 3 LSB (high 8 MSB at register HSTART)
33	CHLF	00	RW	Array Current Control • Range: [00] to [FF]
34	AREF1	3F	RW	Array Reference Control • Range: [00] to [FF]
35	AREF2	00	RW	Array Reference Control • Range: [00] to [FF]
36	AREF3	F9	RW	Array Reference Control • Range: [00] to [FF]
37	ADC1	04	RW	ADC Control 1 Bit[7:4]: Reserved Bit[3]: ADC range adjustment 0: 1x range 1: 1.5x range Bit[2:0]: ADC range adjustment 000: 0.8x 100: 1x 111: 1.2x
38	ADC2	12	RW	ADC Reference Control • Range: [00] to [FF]
39	AREF4	50	RW	Analog Reference Control • Range: [00] to [FF]

Table 5 Device Control Register List (Sheet 8 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3A	TSLB	8C	RW	Line Buffer Test Option Bit[7:6]: PCLK output delay option 00: No delay 01: 2 ns 10: 4 ns 11: 6 ns Bit[5]: Output bit-wise reverse Bit[4]: UV output value 0: Use normal UV output 1: Use fixed UV value set in registers MANU and MANV as UV output instead of chip output Bit[3:2]: YUV output sequence 00: Y U Y V 01: Y V Y U 10: V Y U Y 11: U Y V Y Bit[1]: 50/60 Hz banding filter auto detection Bit[0]: Reserved
3B	COM11	05	RW	Common Control 11 Bit[7]: Night mode 0: Night mode disable 1: Night mode enable - Frame rate will adjust based on COM11[6:5] before AGC gain increases more than 2. Also, ADVFH and ADVFL will be automatically updated. Bit[6:5]: Night mode insert frame option 00: Normal frame rate 01: 1/2 frame rate 10: 1/4 frame rate 11: 1/8 frame rate Bit[4:1]: Reserved Bit[0]: Reserved (for REV4 sensors) Bit[0]: Clear registers ADVFL (0x2D) and ADVFH (0x2E) when COM11[7] = 0 (for REV5 sensors)
3C	COM12	0C	RW	Common Control 12 Bit[7]: HREF option 0: No HREF when VREF is low 1: Always has HREF Bit[6:5]: Reserved Bit[4]: Night mode speed selection 0: Normal 1: Fast Bit[3]: Contrast expand center selection 0: Use manually entered value at CNST2 (0x57) as center value 1: Use average value of last frame as center value Bit[2:0]: Reserved

Table 5 Device Control Register List (Sheet 9 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3D	COM13	99	RW	Common Control 13 Bit[7]: Gamma selection for signal 0: No gamma function 1: Gamma used for Raw data before interpolation Bit[6]: Reserved Bit[5]: VSYNC shift option 1: VSYNC will shift back 9 lines and width will change to 2 lines Bit[4]: Reserved Bit[3]: Enable Y channel delay option 0: Delay UV channel 1: Delay Y channel Bit[2:0]: Output Y/UV delay
3E	COM14	00	RW	Common Control 14 Bit[7:4]: Reserved Bit[3]: Black pixel correction ON/OFF selection 0: OFF 1: ON Bit[2]: White pixel correction ON/OFF selection 0: OFF 1: ON Bit[1]: Zoom function ON/OFF selection 0: OFF 1: ON Bit[0]: Reserved
3F	EDGE	02	RW	Edge Enhancement Adjustment Bit[7:5]: Reserved Bit[4:0]: Edge enhancement factor
40	COM15	C0	RW	Common Control 15 Bit[7:6]: Data format - output full range enable 0x: Output range: [10] to [F0] 10: Output range: [01] to [FE] 11: Output range: [00] to [FF] Bit[5:4]: RGB 555/565 option (must set COM7[2] high) x0: Normal RGB output 01: RGB 565 11: RGB 555 Bit[3:0]: Reserved
41	COM16	40	RW	Common Control 16 Bit[7:2]: Reserved Bit[1]: Color matrix coefficient double option Bit[0]: Scaling down ON/OFF selection 0: Normal 1: Scaling down

Table 5 Device Control Register List (Sheet 10 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
42	COM17	08	RW	Common Control 17 Bit[7]: De-noise option 0: De-noise strength fixed 1: De-noise strength auto adjust Bit[6]: Edge enhancement option 0: Fixed 1: Edge enhancement strength auto adjust Bit[5]: Reserved Bit[4]: Auto digital gain enable Bit[3]: Reserved Bit[2]: Select single frame out Bit[1]: Tri-state output after single frame out Bit[0]: Banding filter selection 0: 60 Hz banding filter 1: 50 Hz banding filter
43-4E	RSVD	XX	–	Reserved
4F	MTX1	40	RW	Matrix Coefficient 1
50	MTX2	34	RW	Matrix Coefficient 2
51	MTX3	0C	RW	Matrix Coefficient 3
52	MTX4	17	RW	Matrix Coefficient 4
53	MTX5	29	RW	Matrix Coefficient 5
54	MTX6	40	RW	Matrix Coefficient 6
55	BRTN	00	RW	Brightness Adjustment
56	CNST1	40	RW	Contrast Control Coefficient
57	CNST2	80	RW	Contrast Control Coefficient

Table 5 Device Control Register List (Sheet 11 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
58	MTXS	1E	RW	Matrix Coefficient Sign Bit[7:6]: Reserved Bit[5]: Matrix coefficient 6 sign 0: Plus 1: Minus Bit[4]: Matrix coefficient 5 sign 0: Plus 1: Minus Bit[3]: Matrix coefficient 4 sign 0: Plus 1: Minus Bit[2]: Matrix coefficient 3 sign 0: Plus 1: Minus Bit[1]: Matrix coefficient 2 sign 0: Plus 1: Minus Bit[0]: Matrix coefficient 1 sign 0: Plus 1: Minus
59	AWBOP1	91	RW	AWB Control Option 1
5A	AWBOP2	94	RW	AWB Control Option 2
5B	AWBOP3	AA	RW	AWB Control Option 3
5C	AWBOP4	71	RW	AWB Control Option 4
5D	AWBOP5	8D	RW	AWB Control Option 5
5E	AWBOP6	0F	RW	AWB Control Option 6
5F	BLMT	F0	RW	AWB Blue Component Gain Limit
60	RLMT	F0	RW	AWB Red Component Gain Limit
61	GLMT	F0	RW	AWB Green Component Gain Limit
62	LCC1	00	RW	Lens Correction Option 1
63	LCC2	00	RW	Lens Correction Option 2
64	LCC3	10	RW	Lens Correction Option 3
65	LCC4	80	RW	Lens Correction Option 4
66	LCC5	00	RW	Lens Correction Control Bit[7:4]: Reserved Bit[3:1]: Lens correction parameter output Bit[0]: Lens correction enable
67	MANU	80	RW	Manual U Value (effective only when register TSLB[4] is high)
68	MANV	80	RW	Manual V Value (effective only when register TSLB[4] is high)
69	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Sheet 12 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
6A	BD50MAX	00	RW	50 Hz Banding Filter Maximum Step Setting
6B	DBLV	0A	RW	Band Gap Reference Adjustment Bit[7:6]: PLL frequency selection 00: Bypass PLL 01: 4x 10: 6x 11: 8x Bit[5]: Reserved Bit[4]: Bypass internal regulator for DVDD Bit[3:0]: Band gap reference adjustment
6C-6F	RSVD	XX	–	Reserved
70	DNSTH	02	RW	De-noise Function Threshold Adjustment
71	RSVD	XX	–	Reserved
72	POIDX	00	RW	Pixel Output Index Bit[7]: Reserved Bit[6]: Vertical pixel output option 0: Use pixel average data 1: Drop unused pixel data Bit[5:4]: Vertical pixel output index 00: Normal 01: Output 1 line for every 2 lines 10: Output 1 line for every 4 lines 11: Output 1 line for every 8 lines Bit[3]: Reserved Bit[2]: Horizontal pixel output option 0: Use pixel average data 1: Drop unused pixel data Bit[1:0]: Horizontal pixel output index 00: Normal 01: Output 1 line for every 2 pixels 10: Output 1 line for every 4 pixels 11: Output 1 line for every 8 pixels
73	PCKDV	01	RW	Pixel Clock Output Selection Bit[7:4]: Reserved Bit[3:0]: Pixel clock output frequency adjustment
74	XINDX	3A	RW	Horizontal Scaling Down Coefficients
75	YINDX	35	RW	Vertical Scaling Down Coefficients
76-79	RSVD	XX	–	Reserved
7A	SLOP	24	RW	Gamma Curve Highest Segment Slope - calculated as follows: SLOP[7:0] = (FF - GAM15[7:0] + 1) x 40/30
7B	GAM1	04	RW	Gamma Curve 1st Segment Input End Point 0x010 Output Value
7C	GAM2	07	RW	Gamma Curve 2nd Segment Input End Point 0x020 Output Value

Table 5 Device Control Register List (Sheet 13 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
7D	GAM3	10	RW	Gamma Curve 3rd Segment Input End Point 0x040 Output Value
7E	GAM4	28	RW	Gamma Curve 4th Segment Input End Point 0x080 Output Value
7F	GAM5	36	RW	Gamma Curve 5th Segment Input End Point 0x0A0 Output Value
80	GAM6	44	RW	Gamma Curve 6th Segment Input End Point 0x0C0 Output Value
81	GAM7	52	RW	Gamma Curve 7th Segment Input End Point 0x0E0 Output Value
82	GAM8	60	RW	Gamma Curve 8th Segment Input End Point 0x100 Output Value
83	GAM9	6C	RW	Gamma Curve 9th Segment Input End Point 0x120 Output Value
84	GAM10	78	RW	Gamma Curve 10th Segment Input End Point 0x140 Output Value
85	GAM11	8C	RW	Gamma Curve 11th Segment Input End Point 0x180 Output Value
86	GAM12	9E	RW	Gamma Curve 12th Segment Input End Point 0x1C0 Output Value
87	GAM13	BB	RW	Gamma Curve 13th Segment Input End Point 0x240 Output Value
88	GAM14	D2	RW	Gamma Curve 14th Segment Input End Point 0x2C0 Output Value
89	GAM15	E5	RW	Gamma Curve 15th Segment Input End Point 0x340 Output Value
8A	RSVD	XX	–	Reserved
8B	COM18	04	RW	Common Control 18 Bit[7:4]: Reserved Bit[3]: Zoom mode under VGA timing Bit[2:0]: Reserved
8C	COM19	0C	RW	Common Control 19 Bit[7:4]: Reserved Bit[3:2]: UV adjust option Bit[1]: Reserved Bit[0]: UV average ON/OFF
8D	COM20	00	RW	Common Control 20 Bit[7:5]: Reserved Bit[4]: Color bar test mode Bit[3:0]: Reserved
8E-91	RSVD	XX	–	Reserved
92	DMLNL	00	RW	Frame Dummy Line LSBs
93	DMLNH	00	RW	Frame Dummy Line MSBs
94-9C	RSVD	XX	–	Reserved
9D	LCC6	00	RW	Lens Correction Option 6
9E	LCC7	00	RW	Lens Correction Option 7
9F-A0	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Sheet 14 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
A1	AECH	40	RW	Exposure Value - AEC MSB 5 bits Bit[7:6]: Reserved Bit[5:0]: AEC[15:10] (see registers AEC for AEC[9:2] and COM1 for AEC[1:0])
A2	BD50	9D	RW	1/100s Exposure Setting for 50 Hz Banding Filter
A3	BD60	83	RW	1/120s Exposure Setting for 60 Hz Banding Filter
A4	COM21	78	RW	Common Control 21 Bit[7:4]: Reserved Bit[3:0]: Digital gain value
A5	RSVD	80	–	Reserved
A6	GREEN	86	RW	AWB Green Component Gain Setting
A7	VZST	10	RW	VGA Zoom Mode Vertical Start Line
A8	REFA8	01	RW	Analog Reference Control
A9	REFA9	00	RW	Analog Reference Control
AA-AB	RSVD	XX	–	Reserved
AC	BLC1	84	RW	Black Level Control 1
AD	BLC2	84	RW	Black Level Control 2
AE	BLC3	84	RW	Black Level Control 3
AF	BLC4	84	RW	Black Level Control 4
B0	BLC5	04	RW	Black Level Control 5
B1	BLC6	00	RW	Black Level Control 6
B2	BLC7	01	RW	Black Level Control 7
B3	BLC8	0F	RW	Black Level Control 8
B4	CTRLB4	00	RW	Bit[7:4]: Reserved Bit[3:2]: UV adjust start selection Bit[1]: UV adjust slope selection Bit[0]: UV adjust ON/OFF selection
B5-B6	RSVD	XX	–	Reserved
B7	FRSTL	EE	RW	One-Pin Frame Exposure Reset Time Control Low 8 Bits
B8	FRSTH	EE	RW	One-Pin Frame Exposure Reset Time Control High 8 Bits
B9-BB	RSVD	XX	–	Reserved
BC	ADBOFF	40	RW	ADC B channel offset setting
BD	ADROFF	40	RW	ADC R channel offset setting
BE	ADGbOFF	40	RW	ADC Gb channel offset setting
BF	ADGrOFF	40	RW	ADC Gr channel offset setting

Table 5 Device Control Register List (Sheet 15 of 15)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
C0-C3	RSVD	XX	–	Reserved
C4	COM23	00	RW	Common Control 23 Bit[7]: Strobe enable 1: Start Strobe mode Bit[6]: Strobe output pulse polarity control Bit[5:4]: Reserved Bit[3:2]: Xenon mode strobe pulse width 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines Bit[1:0]: Strobe mode 00: Xenon mode 01: LED1&2 mode 10: LED1&2 mode 11: LED3 mode ***Notes:*** *1 When in LED1&2 mode, registers ADVFL (0x2D) and ADVFH (0x2E) will serve as pulse width control* *2 Only detect bit 7 rising edge to start sequence* *3 Clear bit 7 after initiating*
C5	BD60MAX	2E	RW	60 Hz Banding Filter Maximum Step Setting
C6	RSVD	XX	–	Reserved
C7	COM24	80	RW	Common Control 24 Bit[7:3]: Reserved Bit[2:0]: Pixel clock frequency selection
C8-CF	RSVD	XX	–	Reserved

NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.

Package Specifications

The OV9656 uses a 28-pin Chip Scale Package 2 (CSP2). Refer to Figure 10 for package information, Table 6 for package dimensions and Figure 11 for the array center on the chip.

Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 10 OV9656 Package Specifications

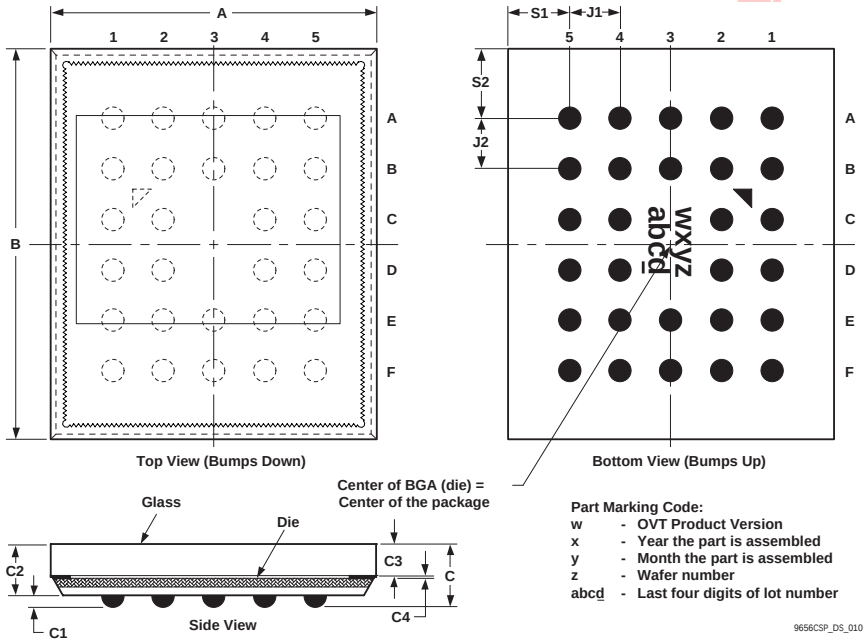
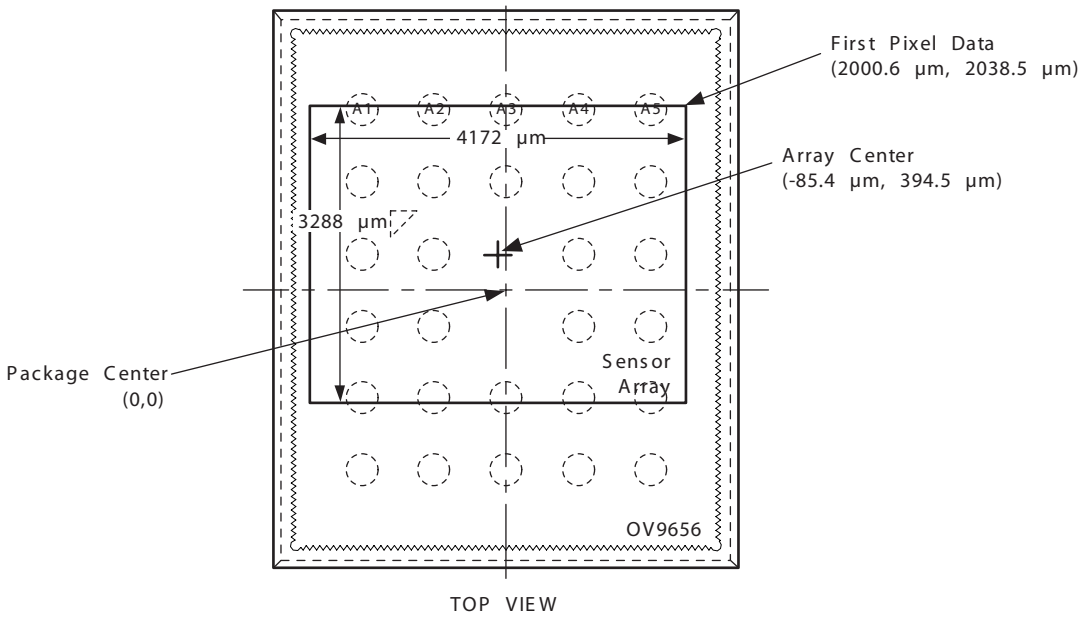


Table 6 OV9656 Package Dimensions

Parameter	Symbol	Min	Nominal	Max	Unit
Package Body Dimension X	A	5120	5145	5170	µm
Package Body Dimension Y	B	6120	6145	6170	µm
Package Height	C	945	1005	1065	µm
Ball Height	C1	150	180	210	µm
Package Body Thickness	C2	780	825	870	µm
Cover Glass Thickness	C3	475	500	525	µm
Airgap Between Cover Glass and Sensor	C4	30	45	60	µm
Ball Diameter	D	320	350	380	µm
Total Pin Count	N		28 (2 NC)		
Pin Count X-axis	N1		5		
Pin Count Y-axis	N2		6		
Pins Pitch X-axis	J1		800		µm
Pins Pitch Y-axis	J2		800		µm
Edge-to-Pin Center Distance Analog X	S1	942.5	973	1002.5	µm
Edge-to-Pin Center Distance Analog Y	S2	1042.5	1073	1102.5	µm

Sensor Array Center

Figure 11 OV9656 Sensor Array Center



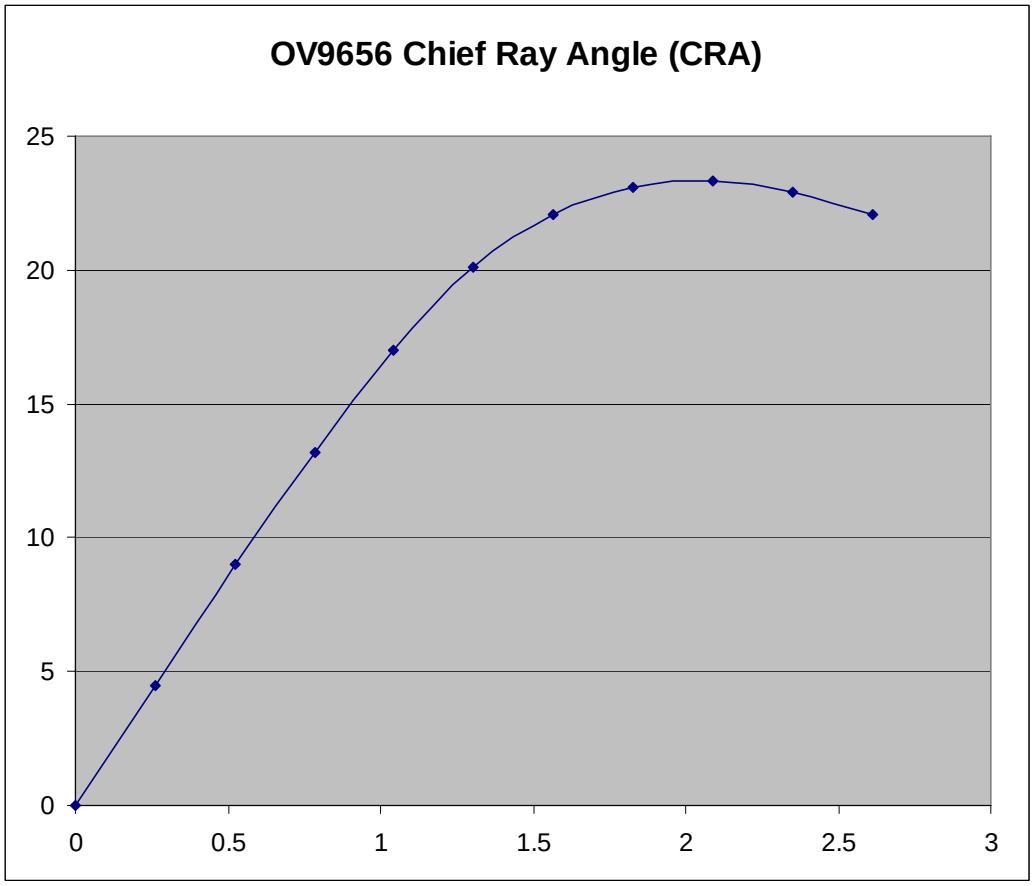
NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A5 oriented down on the PCB.

9656CSP_DS_011

Chief Ray Angle

Figure 12 OV9656 Chief Ray Angle



IR Reflow Ramp Rate Requirements

OV9656 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 13 IR Reflow Ramp Rate Requirements

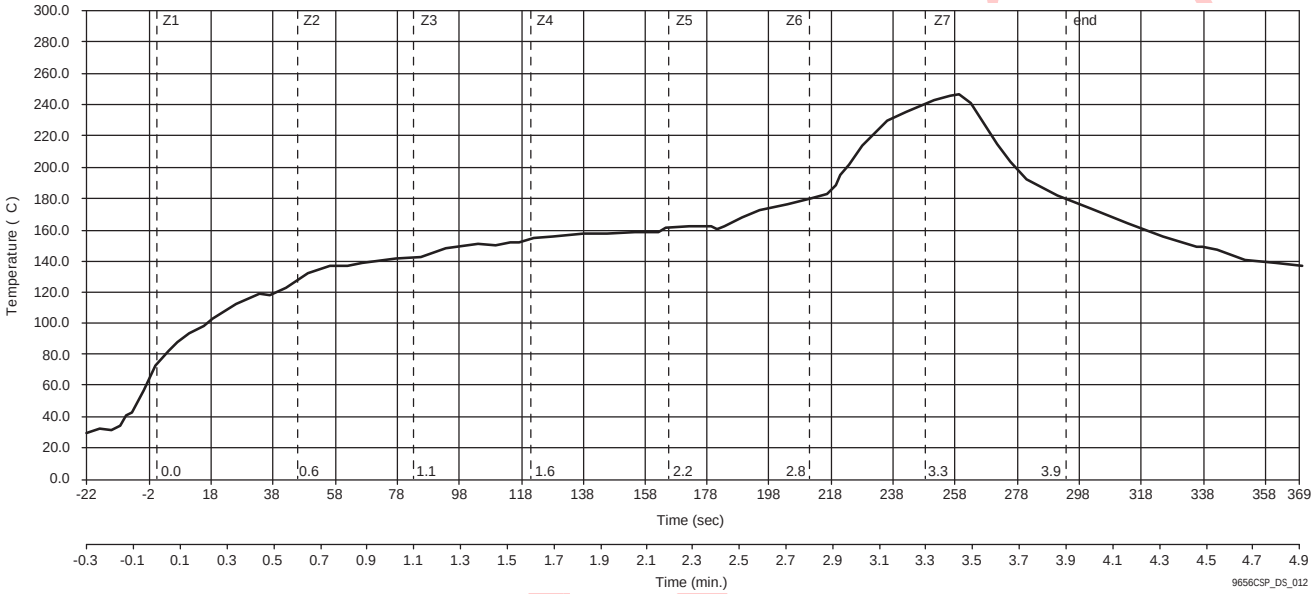


Table 7 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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