DM13A-E

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Low Power 16-bit Constant Current LED Driver

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DM13A-E

Low Power 16-bit Constant Current LED Driver

General Description

DM13A-E is a constant-current sink driver specifically designed for LED display applications. The device incorporates shift registers, data latches, and constant current circuitry on the silicon CMOS chip. The maximum output current value of all 16 channels is adjustable by a single external resistor.

Features

- Minimum constant-current outputs: 0.3mA
- Low minimum output voltage: 0.31V@0.4mA
- Maximum output voltage: 5.5V
- Maximum clock frequency: 25MHz
- Power supply voltage: 3.3V to 5V
- Overshooting stress elimination
- Ghost elimination
- In-rush current control
- Bit-to-bit skew : ± 0.7 %@0.8mA
  ± 1.1 %@4.5mA
  ± 2 %@15mA
- Chip-to-chip skew : ± 1.4 %@15mA
- Package and pin assignment compatible to conventional LED drivers (DM13A exclude QFN24)

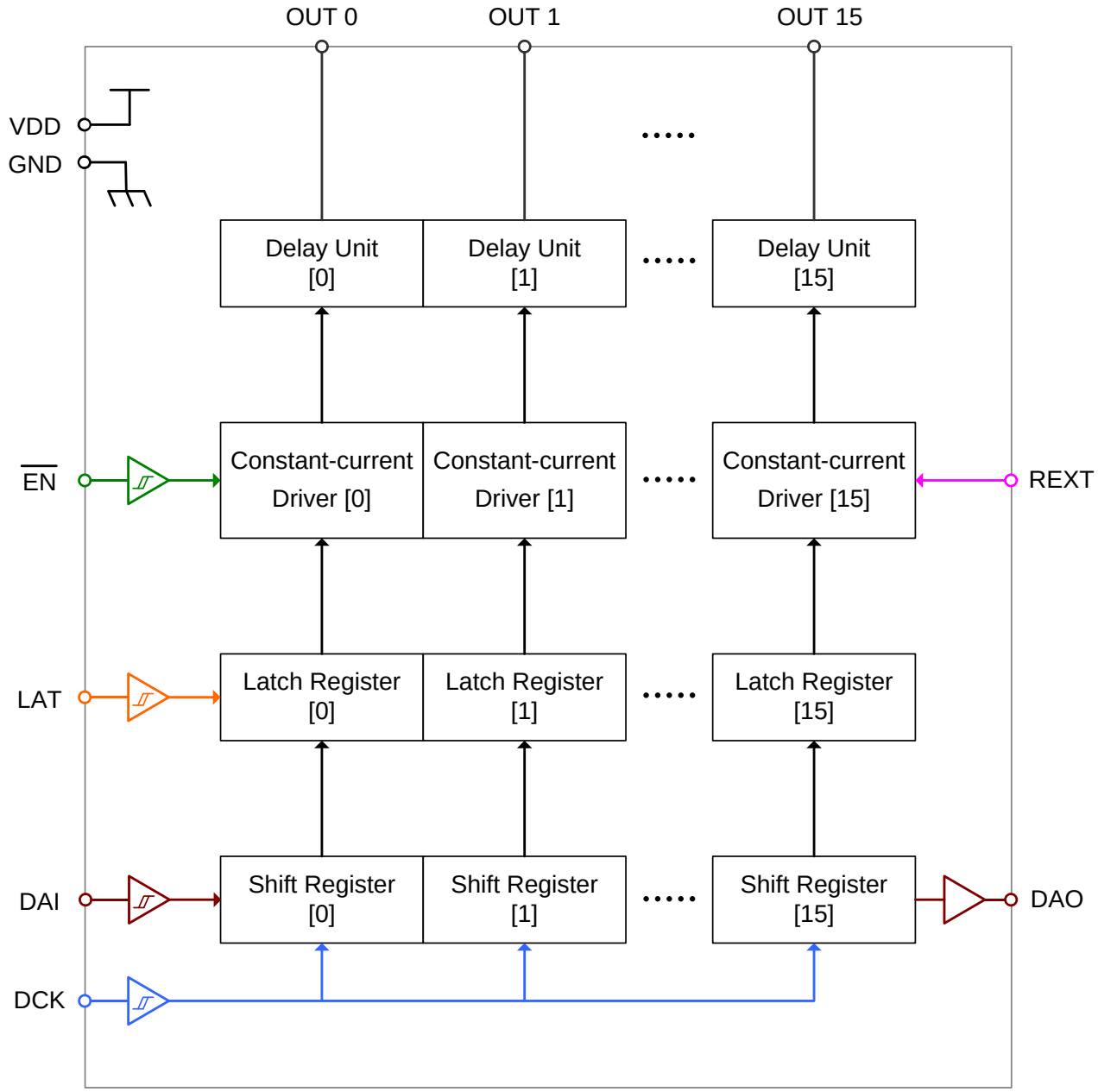
Applications

- Indoor LED Video Display

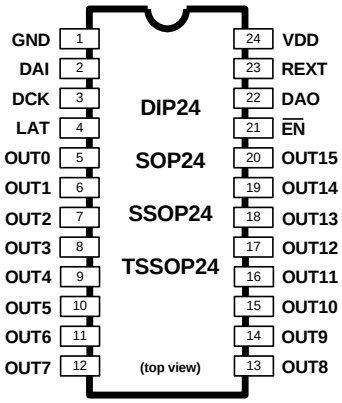
Package Types

- DIP24, SOP24, SOP24B, SSOP24, QFN24

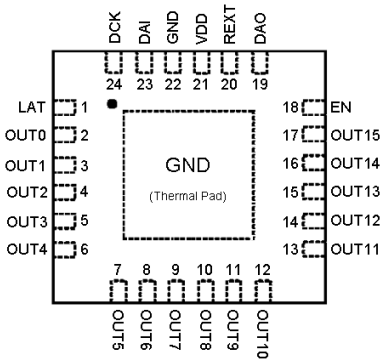
Block Diagram



Pin Connection



QFN24

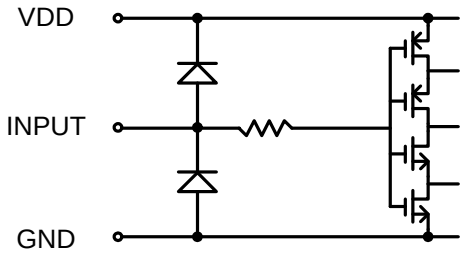


Pin Description

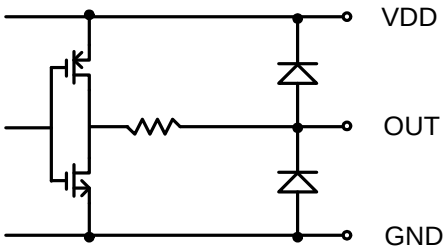
PIN No.	PIN NAME	FUNCTION
DIP24/SOP24/SSOP24:1 QFN24:22,thermal pad	GND	Ground terminal.
DIP24/SOP24/SSOP24: 2 QFN24:23	DAI	Serial data input terminal.
DIP24/SOP24/SSOP24: 3 QFN24:24	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
DIP24/SOP24/SSOP24: 4 QFN24:1	LAT	Input terminal of data strobe. Data on shift register goes through at the high level of LAT (level trigger). Otherwise, data is latched.
DIP24/SOP24/SSOP24: 5~20 QFN24:2~17	OUT0~15	Sink constant-current outputs (open-drain).
DIP24/SOP24/SSOP24: 21 QFN24:18	$\overline{\text{EN}}$	Output enable terminal: **'H'** for all outputs are turned off , **'L'** for all outputs are active.
DIP24/SOP24/SSOP24: 22 QFN24:19	DAO	Serial data output terminal.
DIP24/SOP24/SSOP24: 23 QFN24:20	REXT	External resistors connected between REXT and GND for output current value setting.
DIP24/SOP24/SSOP24: 24 QFN24:21	VDD	Supply voltage terminal.

Equivalent Circuit of Inputs and Outputs

1. DCK, DAI, LAT, $\overline{EN}$ terminals



2. DAO terminals



Maximum Ratings[*1](Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 6.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	30	mA
Output Voltage	VOUT	-0.3 ~ 5.5	V
Input Clock Frequency	FDCK	25	MHz
GND Terminal Current	IGND	480	mA
Power Dissipation (4 layer PCB)	PD	2.5 (PDIP24 : Ta=25°C)	W
		2.03(SOP24B : Ta=25°C)	
		1.57 (SOP24 : Ta=25°C)	
		1.38 (SSOP24 : Ta=25°C)	
		3.37 (QFN24 : Ta=25°C)	
Thermal Resistance	Rth(j-a)	50.0 (PDIP24)	°C/W
		61.4 (SOP24B)	
		79.2 (SOP24)	
		90.2 (SSOP24)	
		37 (QFN24)	
Operating Temperature	Top	-20 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	—	3.3	5.0	5.5	V
Output Voltage	VOUT	Driver On@0.4mA	0.31	—	0.5VDD	V
Output Voltage	VOUT	Driver Off	—	—	5.5	
Output Current	IO	OUTn	0.3	—	30	mA
	IOH	VOH = VDD – 0.2 V	+1	—	—	
	IOL	VOL = 0.2 V	—	—	–1	
Input Voltage	VIH	VDD = 3.3 V ~ 5.5V	0.8VDD	—	VDD	V
	VIL		0.0	—	0.2VDD	
Input Clock Frequency	FDCK	Single Chip Operation	—	—	25	MHz
LAT Pulse Width	tw LAT	VDD = 5.0V&3.3V	15	—	—	ns
DCK Pulse Width	tw DCK		15	—	—	
Set-up Time for DAI	tsetup(D)		10	—	—	
Hold Time for DAI	thold(D)		10	—	—	
Set-up Time for LAT	tsetup(L)		10	—	—	
Hold Time for LAT	thold(L)		10	—	—	

[*1] Stress beyond those listed under “Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; it’s not implied functional operation condition. Exposure to “Maximum Ratings” conditions for extended periods may affect device reliability and life time.

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.8VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.2VDD	
Output Current Skew (Channel-to-Channel)*1	IOL1	VOUT = 0.5V Rrext = 22KΩ		±0.7	±1.5	%
		VOUT = 0.5V Rrext = 4KΩ		±1.1	±1.8	
		VOUT = 0.5V Rrext = 1KΩ		±2	±3	
Output Current Skew (Chip-to-Chip) *2	IOL2	VOUT = 0.5V Rrext = 22KΩ		±2.8	±6	%
		VOUT = 0.5V Rrext = 4KΩ		±1.8	±4	
		VOUT = 0.5V Rrext = 1KΩ		±1.4	±3	
Output Voltage Regulation	% / VOUT	VOUT = 0.5 V ~ 3 V (DC) Rrext = 4 KΩ	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VDD	VDD = 3.3 V ~5 V (DC) Rrext = 4 KΩ	—	±0.1	±0.5	
Output Current Ripple (due to output voltage ripple)	IRIP1	VOUT=1.5V±0.1V@5MHz Rrext = 4 KΩ		±0.5	±1	%
Output Current Ripple (due to supply voltage ripple)	IRIP2	VDD=4V±0.1V@5MHz Rrext = 4 KΩ		±0.7	±1.2	
Average Output Current Skew (due to supply voltage ripple)	IAO	VDD=4V±0.1V@5MHz Rrext = 4 KΩ		±0.1	±0.5	
Supply Current	$I_{DD(off)}$	power on all pins are open unless VDD and GND	—	4	7	mA
	$I_{DD(off)}$	input signal is static Rrext = 4K Ω all outputs turn off	—	4.5	8	
	$I_{DD(on)}$	input signal is static Rrext = 4K Ω all outputs turn on	—	4.5	8	

*1 Channel-to-channel skew is defined as the ratio between (any I_{OUT}) of chip and (the average Iout) of chip.

Equation: $Skew_{(IOL1)}=\{(I_{OUTn})/[\ (I_{OUTmax} + I_{OUTmin})/2]\}-1$

*2 Chip-to-chip skew is defined as the ratio between (the average of OUT0 to OUT15) and (the reference Iout).

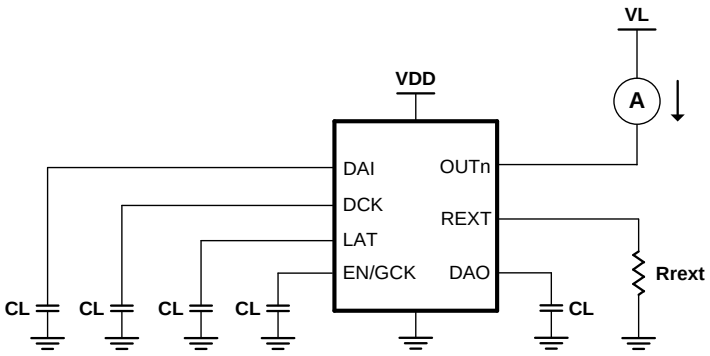
Equation: $Skew_{(IOL2)}=\{[(I_{OUT0}+I_{OUT1}+\ldots\ldots I_{OUT14}+I_{OUT15})/16]/(I_{ref.})\}-1$; I_{ref} refer to page 10

Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	EN-to-OUT0	tpLH	VIH = VDD VIL = GND Rrext = 4KΩ VL = 5.0 V CL*1 = 13 pF	—	30	—	ns
	LAT-to-OUT0			—	25	—	
	DCK-to-DAO			—	20	—	
Propagation Delay ('H' to 'L')	EN-to-OUT0	tpHL		—	32	—	
	LAT-to-OUT0			—	19	—	
	DCK-to-DAO			—	20	—	
Output Current Rise Time		tor		—	28	—	
Output Current Fall Time		tof		—	14	—	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+1)}$)		tod		—	1.5	—	

Switching Characteristics (VDD = 3.3V, Ta = 25°C unless otherwise noted)

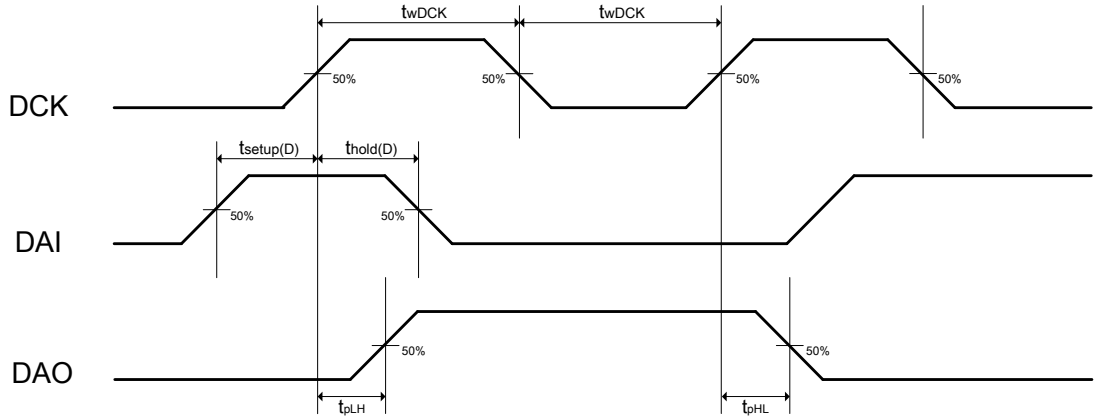
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	EN-to-OUT0	tpLH	VIH = VDD VIL = GND Rrext = 4KΩ VL = 5.0 V CL*1 = 13 pF	—	37	—	ns
	LAT-to-OUT0			—	32	—	
	DCK-to-DAO			—	27	—	
Propagation Delay ('H' to 'L')	EN-to-OUT0	tpHL		—	34	—	
	LAT-to-OUT0			—	19	—	
	DCK-to-DAO			—	31	—	
Output Current Rise Time		tor		—	34	—	
Output Current Fall Time		tof		—	16	—	
Output Delay Time		tod		—	3	—	



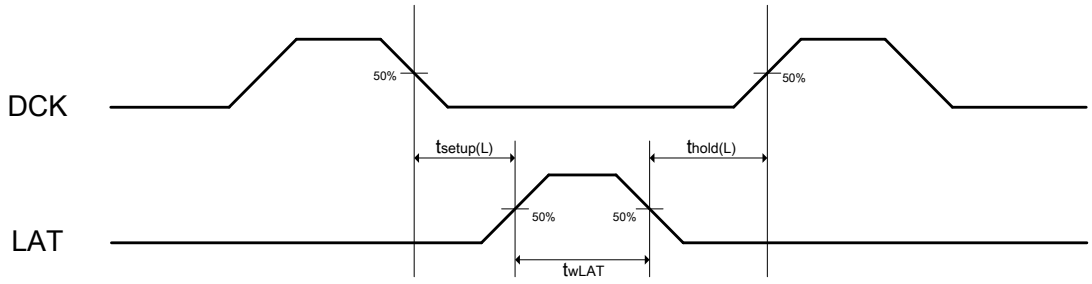
Switching Characteristics Test Circuit **1**

Timing Diagram

1. DCK-DAI, DAO

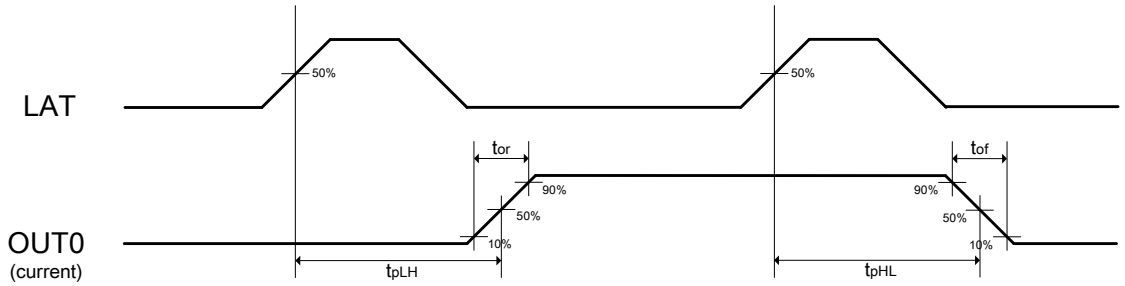


2. DCK-LAT

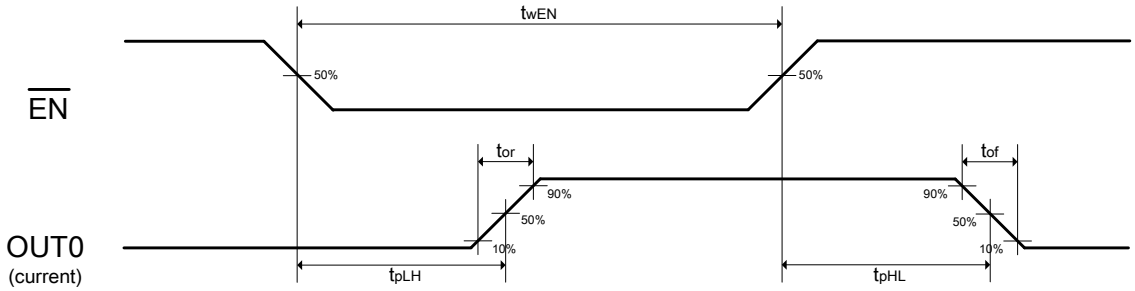


*[1] CL means the probe capacitance of oscilloscope

3. LAT-OUT0

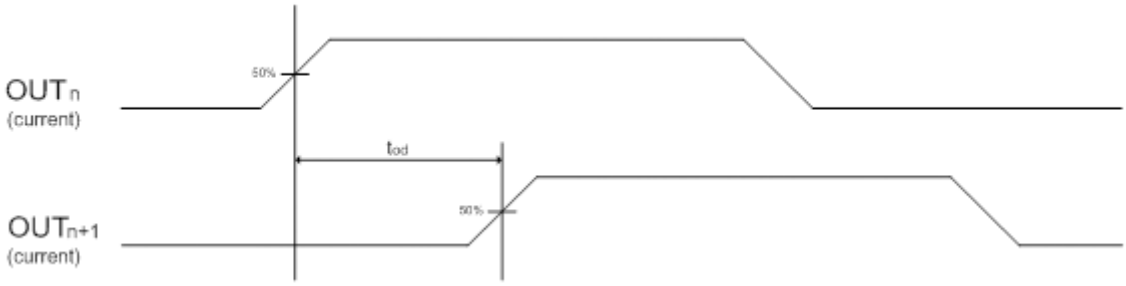


4. $\overline{EN}$-OUT0



OUT_{n+1}-OUT_n n+1 & n refer to “Outputs Delay”

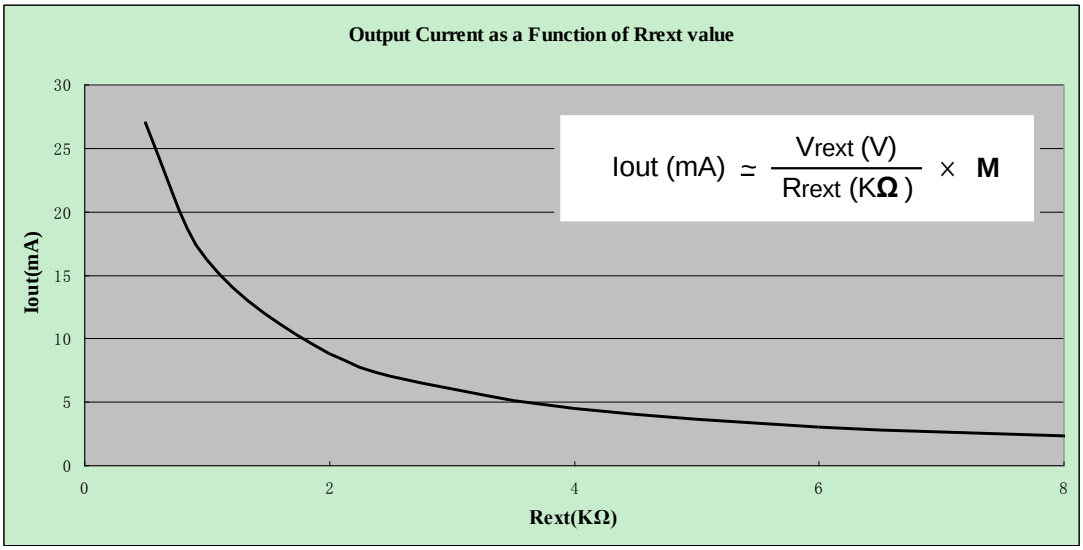
5.

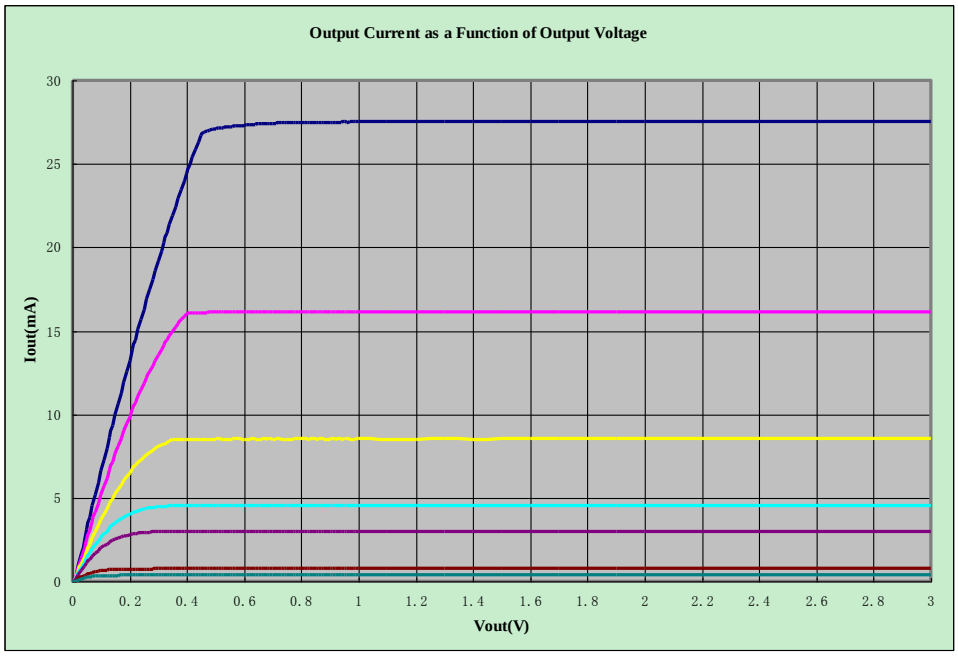


Constant-Current Output

Constant-current value of each output channel is set by an external resistor connected between the REXT pin and GND. Varying the resistor value can adjust the current scale ranging from 0.3mA to 25mA. The reference voltage of REXT terminal (Vrext) is approximately 1.25V.

Rrext(kΩ)	47	22	6	4	2	1	0.5
Iout(mA)	0.383	0.82	3	4.5	8.8	16.3	27.3
M	14.4	14.4	14.4	14.4	14.1	13	10.9



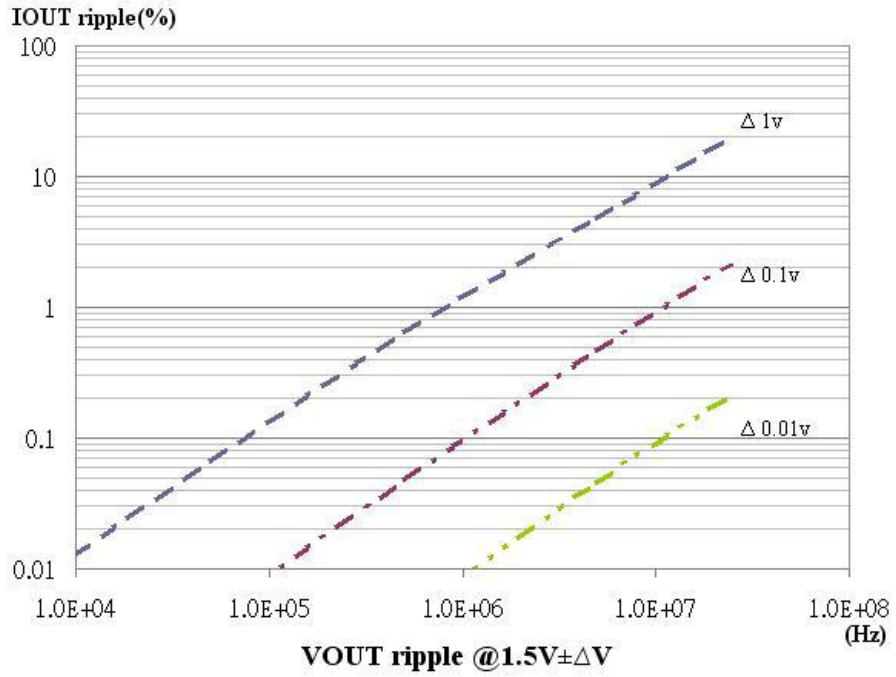


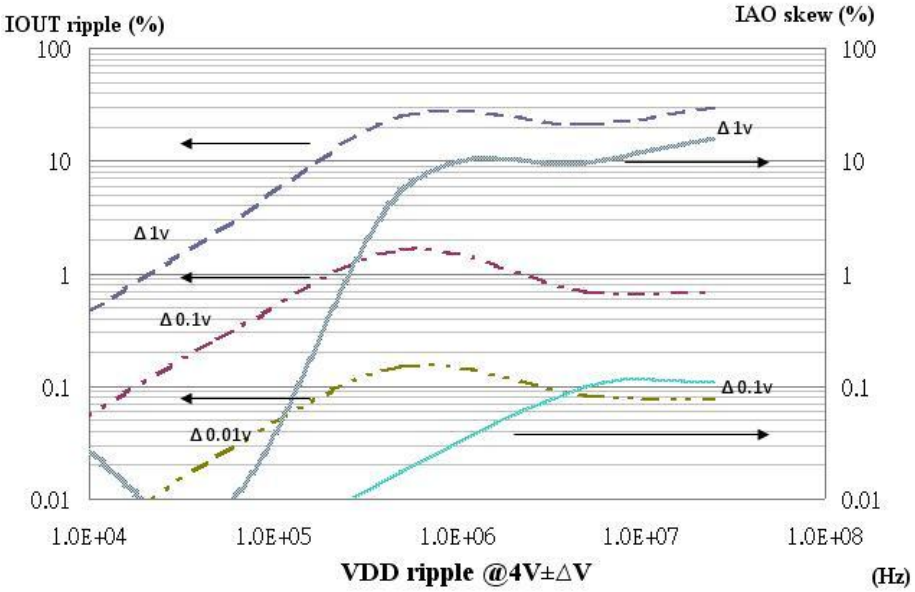
In order to get constant current characteristics, a suitable output voltage is necessary. Users can get related information about the minimum output voltage above.

Output Current Ripple

Output current ripple is due to output voltage or supply voltage ripple. The value of output current ripple is related to frequency and amplitude of voltage ripple. If the amplitude of voltage ripple is too big at high frequency, then it will skew the average output current. In order to ensure the stability of output current, capacitance Cvdd/Cvled are suggested to be installed between VDD/VLED and GND. The suggested value of Cvdd/Cvled is 1uF at 5MHz of outputs switching

(V)

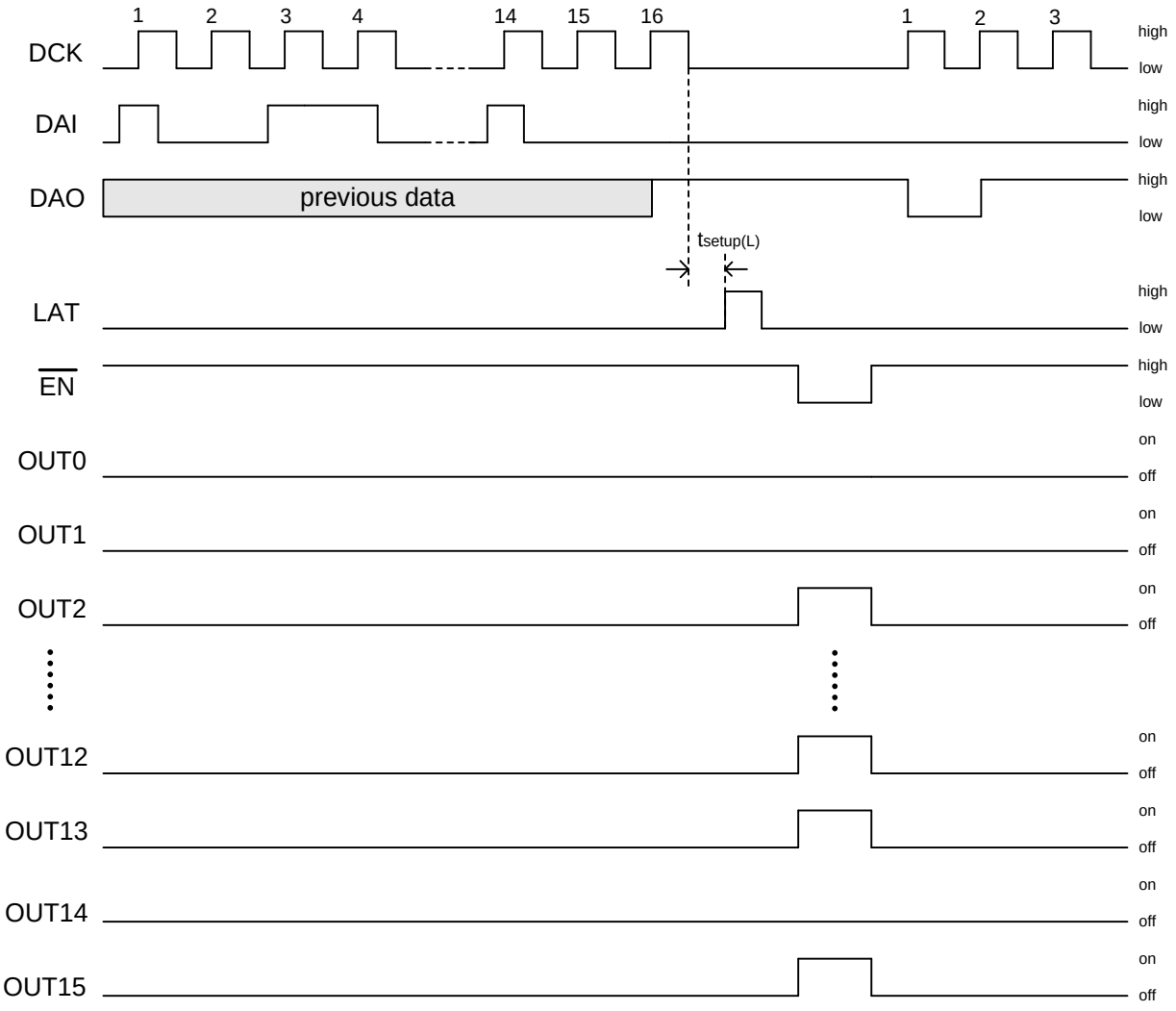




Serial Data Interface

The serial-in data (DAI) will be clocked into 16 bit shift register on the rising edge of the clock (DCK). The data **'1'** represents the corresponding current output **is turned on**, while the data **'0'** turns current output off. The data will be transferred into the 16 bit latch register when the strobe signal (LAT) is **'H'** (level trigger); otherwise, the data will be held. The serial-out data output (DAO) will be shifted out on the rising edge of the clock. All outputs are turned off while enable terminal

(EN) is kept at high level and they become active when EN is held low.



Outputs Delay

DM13A-E has approximately 3ns among drivers in 4 groups to prevent in-rush current when drivers are turned on. Drivers are grouped in the following:

Timing index	Channels
N	0/2/4/6

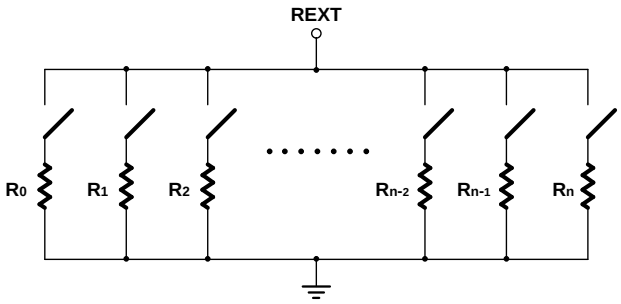
N+1	9/11/13/15
N+2	1/3/5/7
N+3	8/10/12/14

Overshooting Stress & Ghost Image Elimination

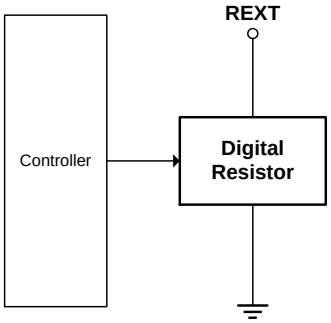
DM13A-E facilitates ghost elimination and voltage overshoot reduction (< 5.5V) by pulling driver outputs to Vdd in a smooth way when drivers are turned off.

Global Brightness Control

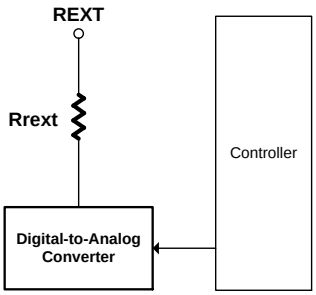
Despite of the availability of global brightness control in DM13A-E, three types of external circuitries are recommended to achieve brightness control as following diagram. They all adjust the current through REXT pin.



Global Brightness Control with Resistor Ladder



Global Brightness Control
with Digital Resistor



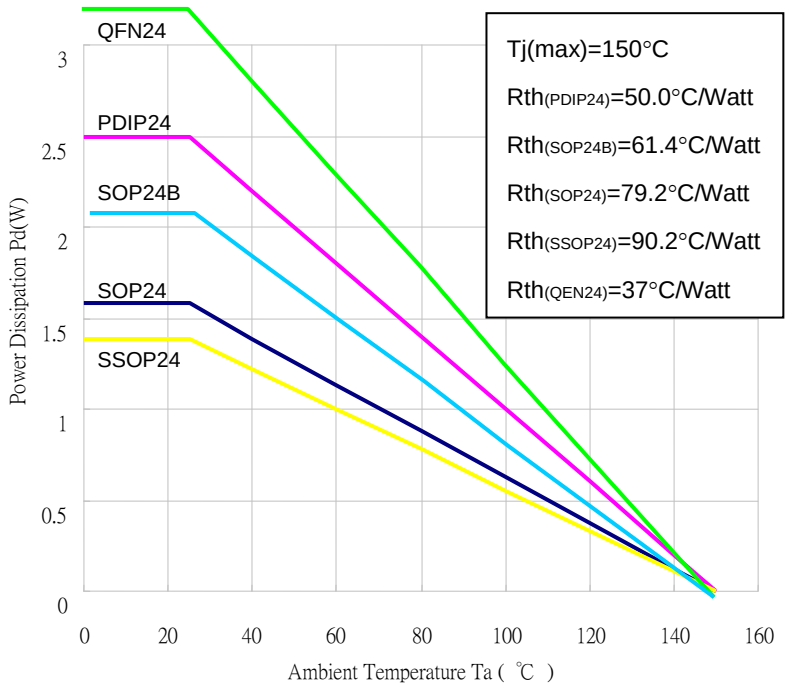
Global Brightness Control
with D/A converter

Power Dissipation

The maximum allowable power dissipation of a semiconductor chip is limited by its package and ambient temperature. It can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(℃) - Ta(ambient\ temperature)(℃)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(℃/Watt)}$$

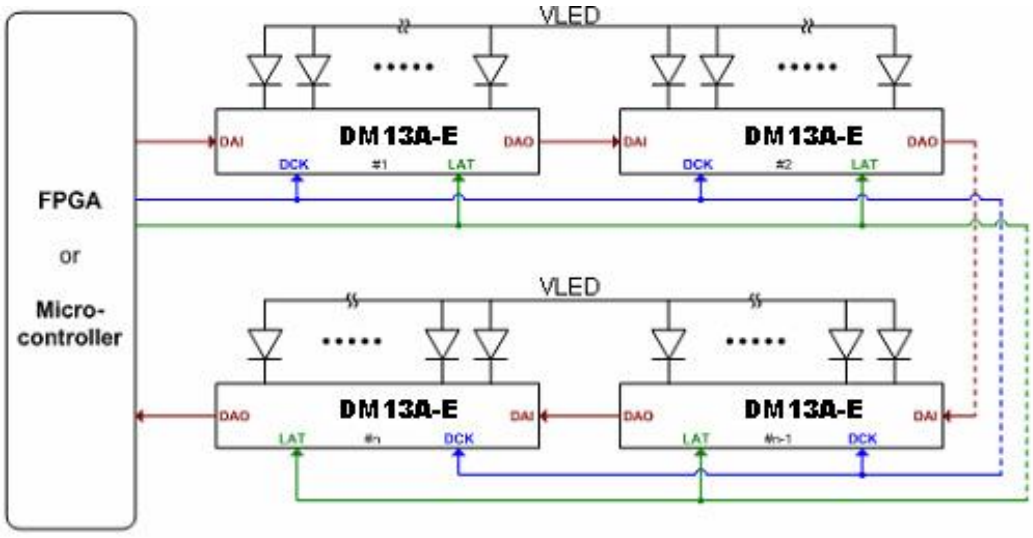
The relationship between power dissipation and operating temperature for various package types can be refered to the figure below:



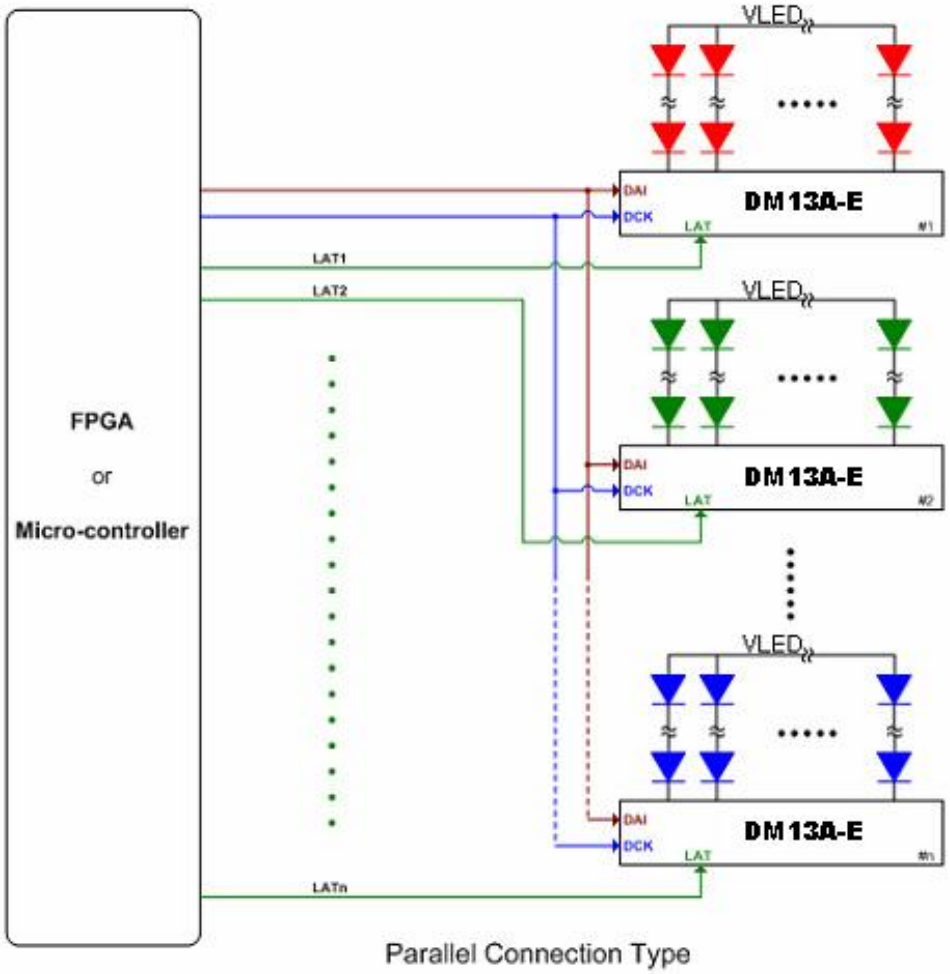
The power consumption of DM13A-E can be determined by the following equation and should be less than the maximum allowable power dissipation:

$$Pd(W) = V_{CC}(V) \times I_{DD}(A) + Vout0 \times Iout0 \times Duty0 + \cdots\cdots + Vout15 \times Iout15 \times Duty15 \leq Pd(max)(W)$$

Typical Application



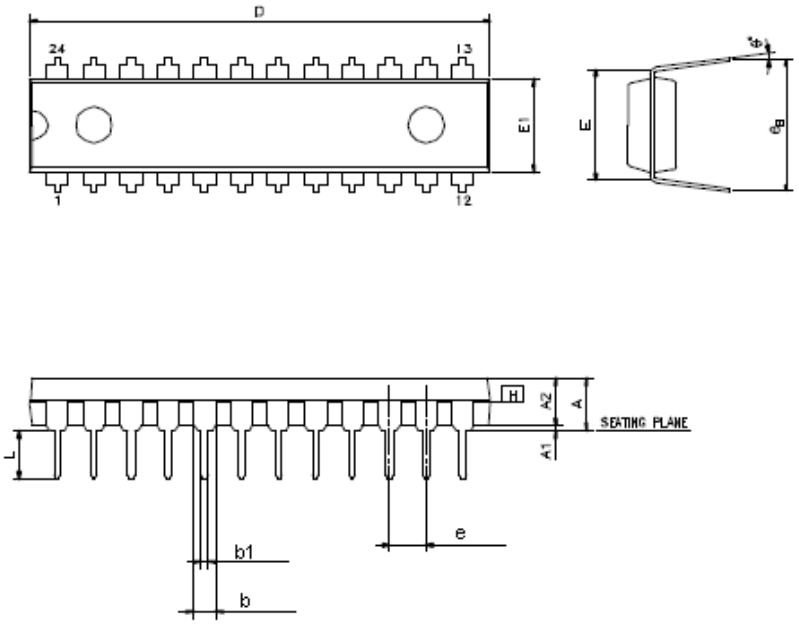
Serial Connection Type



Parallel Connection Type

Package Outline Dimension

DIP24

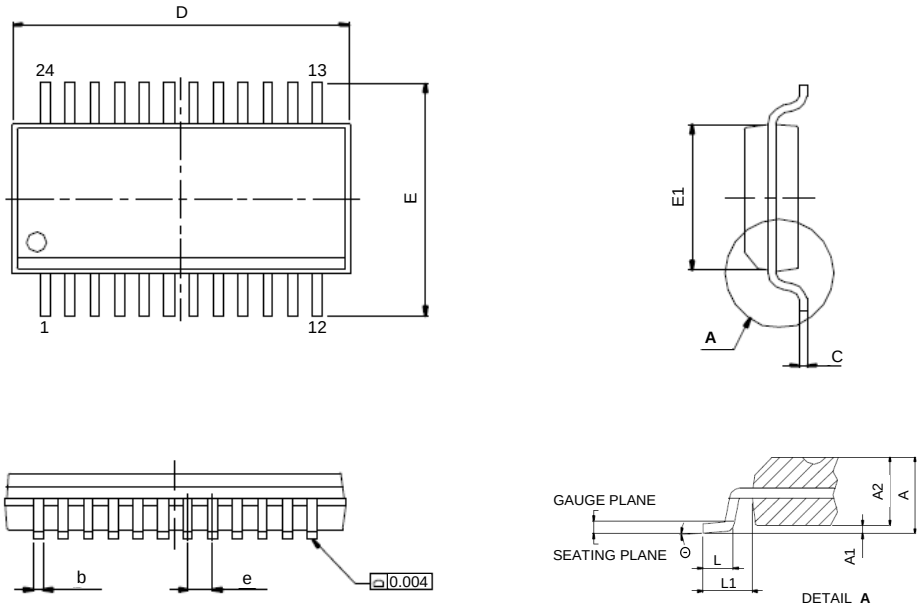


DIMENSIONS IN MM

SYMBOLS	MIN.	TYP.	MAX.
A	-	-	5.334
A1	0.381	-	-
A2	3.175	3.302	3.429
b	-	1.524	-
b1	-	0.480	-
D	31.242	-	32.512
E	7.620 BSC		
E1	6.426	-	6.680
e	-	2.540	-
eB	8.500	-	9.525
L	2.921	-	3.810
θ°	0	-	15

Package Outline Dimension

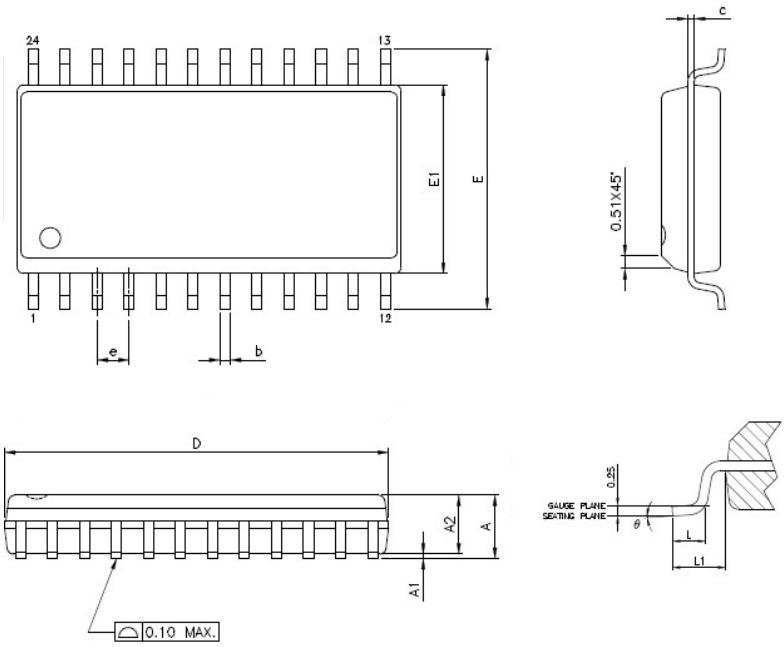
SSOP24



SYMBOLS	MIN.	TYP.	MAX.
A	1.346	1.626	1.753
A1	0.102	0.152	0.254
A2	-	-	1.499
b	0.203	-	0.305
C	0.178	-	0.254
D	8.560	8.661	8.738
E	5.791	5.994	6.198
e	0.635 BSC		
E1	3.810	3.912	3.988
L	0.406	0.635	1.270
L1	1.041 BSC		
θ°	0	-	8

Package Outline Dimension

SOP24

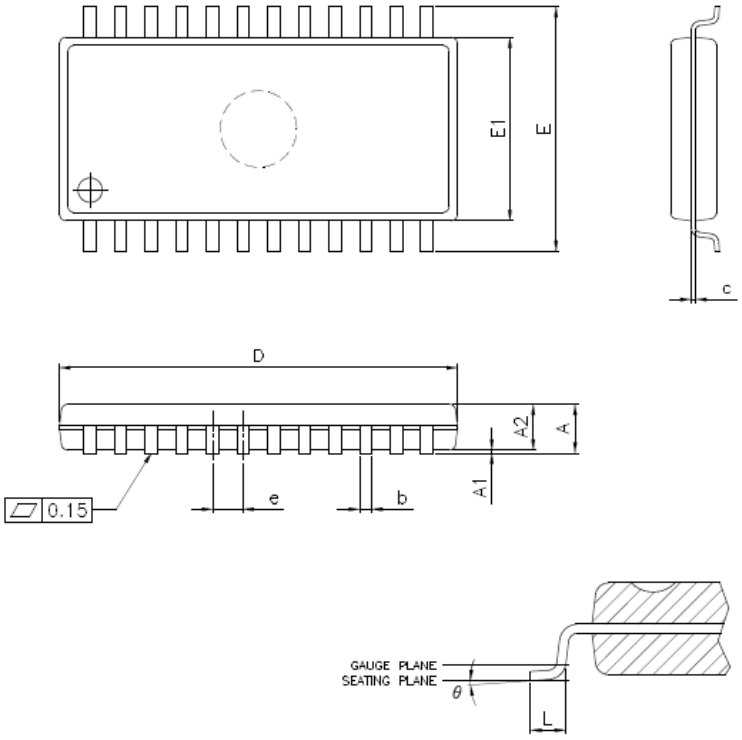


DIMENSIONS IN MM

SYMBOLS	MIN.	TYP.	MAX.
A	-	-	2.650
A1	0.100	-	0.300
A2	2.050	-	-
b	0.310		0.510
c	0.200	-	0.330
D	15.240	-	15.700
E1	7.500BSC		
e	1.270 BSC		
E	10.300BSC		
L1	1.40REF		
L	0.400	-	1.270
θ°	0	-	8

Package Outline Dimension

SOP24B

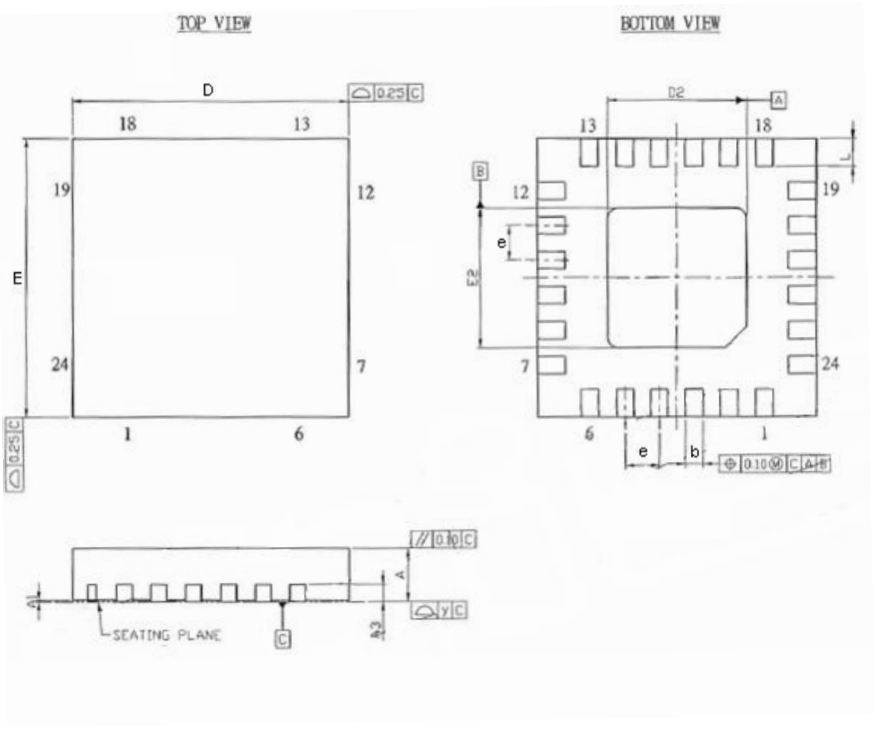


DIMENSIONS IN MM

SYMBOLS	MIN.	TYP.	MAX.
A	-	-	1.900
A1	0.050	0.100	0.200
A2	1.300	1.500	1.700
b	0.300	0.400	0.500
c	0.100	0.150	0.250
D	12.800	13.000	13.200
E	7.700	8.000	8.300
e	1.000 BSC		
E1	5.800	6.000	6.200
L	0.250	0.450	0.650
θ°	0	-	10

Package Outline Dimension

QFN24



DIMENSIONS IN MM

SYMBOLS	MIN.	TYP.	MAX.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3		0.203 REF	
b	0.180	0.250	0.300
D	3.900	4.000	4.100
D2	1.900	2.000	2.100
E	3.900	4.000	4.100
E2	1.900	2.000	2.100
e		0.500 BSC	
L	0.300	0.400	0.500
y	-	-	0.080

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.

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