Overview

TM512-AX is a LED drive chip of DMX512 differential parallel protocol, with optional 1/2/3/4-channel high-precision constant current output and decoding forwarding function. It can perform 800Kbps data output by converting into a single wire via DO port. The coding form of output data contains two options: return-to-zero code and return-to-one code. DO output data can directly control the 800 Kbps IC of our company. 192 channels of data can be forwarded. TM512-AX decoding technology can accurately decode DMX512 signals, compatible with and able to expand DMX512 protocol signals. TM512-AX can perform complete adaptive decoding for DMX512 signals within the transmission frequency of 200Kbps-500Kbps, without the need for rate setting, addressing up to 4,096 channels. TM512-AX has built-in E2PROM, without the need for external connection, supporting on-line code writing. The chip provides 4 voltage-withstand high-precision constant current output channels (30V, up to 60mA) and sets output current via 1 external resistor. TM512-AX has the PWM reverse polarity underclocking output function, which fits for plug-in triode and MOS tube for current expansion driving. With a high port refresh rate, the picture refresh rate is greatly improved. Moreover, TM512-AX can short out multiple constant current output interfaces to expand current driving capability. It is mainly designed for construction decoration and stage-lighting effect LED illuminating systems. The abnormity of one chip does not affect the normal operation of other chips. The maintenance is simple and convenient. The product boasts excellent performance and reliable quality. The features of TM512-AX products and the respective matching ICs of our company are as shown in the following table:

Product name	DO output coding form	DO forwarding rate	TM series matching ICs
TM512-AL	Return-to-zero code	800Kbps	TM1804, TM1809, TM1812, etc.
TM512-AH	Return-to-one code	800Kbps	TM1913, TM1909, TM1912, TM1925, TM1926, etc.

Features

- Compatible with and able to expand DMX512(1990) signal protocol
- Control mode: differential parallel, addressing up to 4,096 channels
- Complete adaptive decoding for DMX512 signals within the transmission rate of 200Kbps-500Kbps
- With built-in E2PROM, without the need for external connection
- Separate address series code writing wire for one-time auto code writing, supporting installation first and then code writing
- E2 address code dual backup mode, part of E2 damage does not affect address code reading
- PWM reverse polarity underclocking output function, port refresh rate after underclocking is 500Hz
- PWM 256 gray level control
- Picture refresh rate over 2KHz
- With built-in 5V voltage-regulator tube
- OUTR/OUTG/OUTB/OUTW output withstand voltage over 30V
- OUTR/OUTG/OUTB/OUTW four-bit constant current output channels
- With external output constant current adjustable resistance, the current range for each channel is 3-60mA
- ±3% current difference value between channels, ±3% current difference value between chips
- Supporting the data reading mode of 1/2/3/4-set of fields
- White light for power on self test, blue light after code writing succeeds
- Output channels delay step by step to lower surge current interference
- Industrial grade design, stable performance
- Packaging mode: SOP16

Field of application

Point light sources, line lamps, wash wall lamps, stage-lighting systems, indoor and outdoor video walls, decorative lighting systems

Block diagram for internal structure

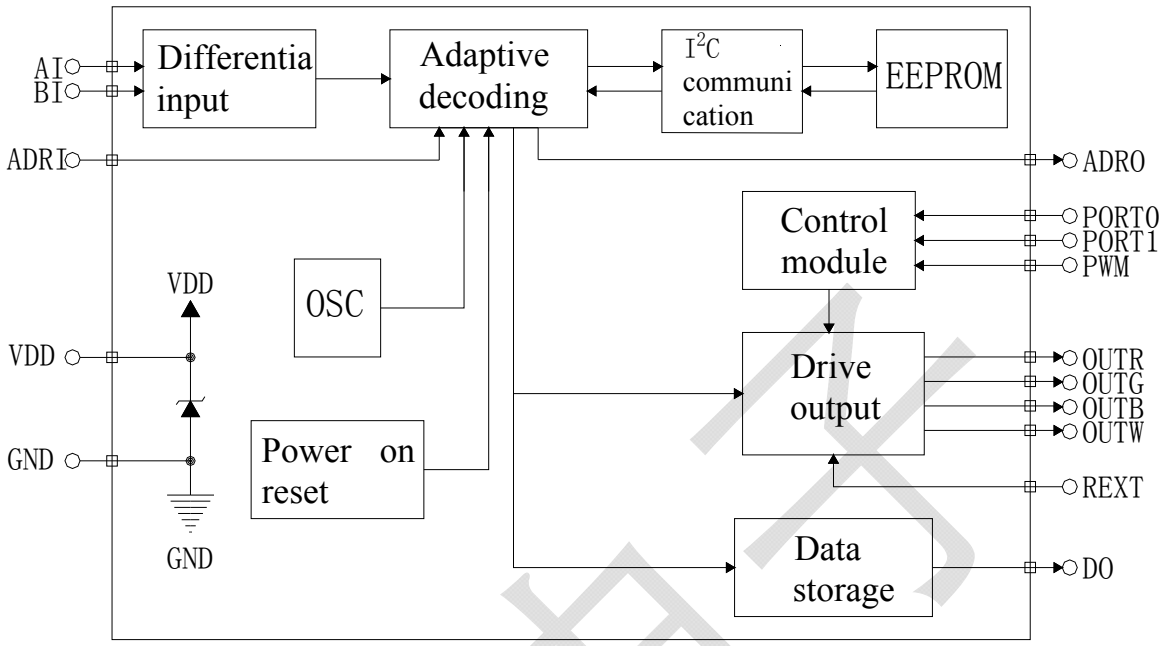


Figure 1

Pin configuration

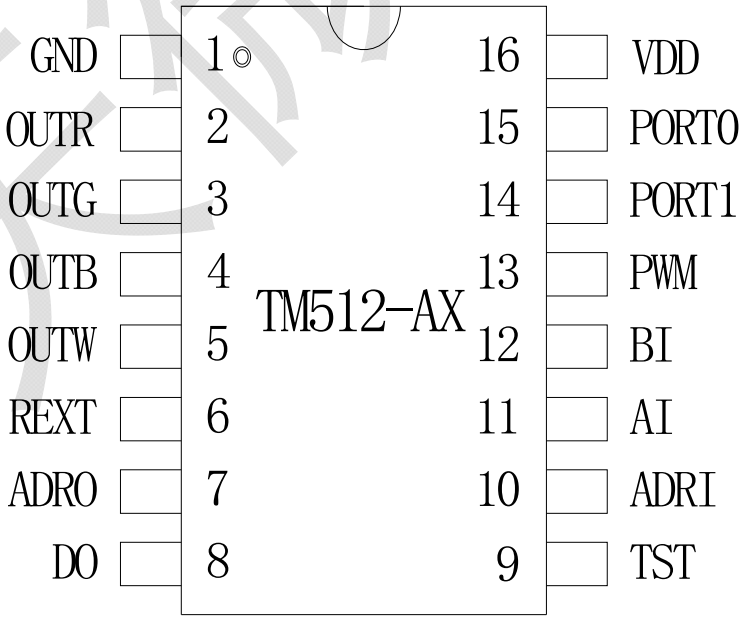


Figure 2

Pin function

Pin name	Pin number	I/O	Function description
VDD	16	--	Positive pole of power supply
GND	1	--	Negative pole of power supply
OUTR/OUTG/OUTB/ OUTW	2～5	O	PWM output port
REXT	6	I	Constant current feedback end, with grounding resistance to adjust output current
ADRO	7	O	Address code writing wire output
DO	8	O	Decode-and-forward channel, able to control the 18 and 19 series ICs of our company
TST	9	I	Test pin, built-in and pull-down
ADRI	10	I	Address code writing wire input, built-in and pull-up
AI	11	I	Differential signal, positive
BI	12	I	Differential signal, negative
PWM	13	I	Output polarity selection, generally suspended, output polarity is opposite after connecting VDD, meanwhile, port refresh rate is dropped to 500Hz
PORT1	14	I	Field selection, built-in and pull-down
PORT0	15	I	Field selection, built-in and pull-down

Input/output equivalent circuit

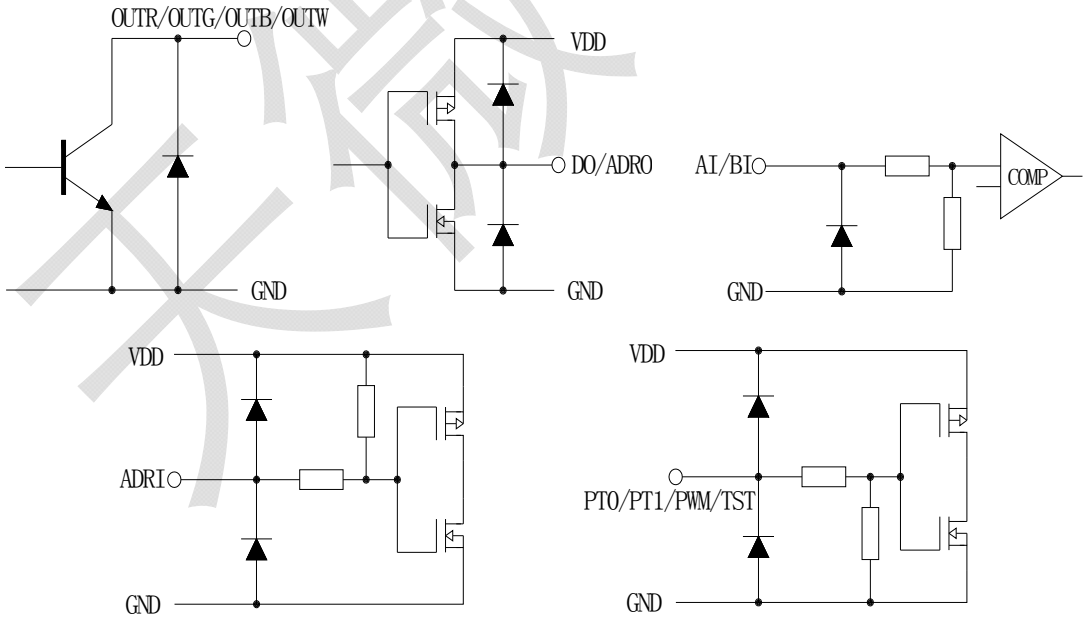


Figure 3

Integrated circuit is an electrostatic sensitive device which tends to generate a lot of static electricity when used in a dry season or dry environment. Electrostatic discharge may damage integrated circuit. Titan Micro Electronics suggests taking all appropriate preventive measures for integrated circuit. Improper operation and welding might cause ESD damage or performance reduction and chip operation failure.

Operating conditions

1. Limiting operating conditions

Tested under 25℃, VDD = 5V, unless otherwise specified		TM512-AX	Unit
Parameter name	Parameter symbol	Limit value	
Logic supply voltage	Vdd	+5.5～+6.5	V
Output port withstand voltage	Vout	30	V
Logic input voltage	Vi	−0.5～Vdd+0.5	V
Operating temperature	Topt	−40～ +85	℃
Storage temperature	Tstg	−55～ +150	℃
Antistatic electricity	ESD	3000	V
Packaging power consumption	Pd	400	mW

(1) When the chip works for a long time under the above limit parameters, it may cause device reliability reduction or permanent damage. Titan Micro Electronics does not suggest any parameter reaching or exceeding the limit value in practical use.

(2) All voltage values are comparatively tested in a systematic way.

2. Recommended operating conditions

Tested under -40℃-+85℃, VDD = 5V, unless otherwise specified			TM512-AX			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
Logical supply voltage	Vdd	--	--	5.5	--	V
High level input voltage	Vih	--	0.7Vdd	--	Vdd	V
Low level input voltage	Vil	—	0	—	0.3Vdd	V
Output port withstand voltage	Vout				30	V

Chip parameters

1. Electrical characteristics

Tested under -40℃-+85℃, VDD = 4.5V-5.5V, GND = 0, unless otherwise specified			TM512-AX			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
Low level output current	Iol	Vo =0.4V，DO，ADRO	10	-	-	mA
High level output current	Ioh	Vo =4V，DO，ADRO	10	-	-	mA
Input current	Ii		-	-	±1	μA
Differential input common mode voltage	Vcm				12	V
Differential input current	Iab	VDD=5V			28	μA
Differential input threshold voltage	Vth	0V<Vcm<12V	-0.2		0.2	V
Differential input hysteresis voltage		Vcm=0V		70		mV
Differential input impedance	Rin			270		KΩ
Output pin current	Isink	OUTR, OUTG, OUTB, OUTW (REXT grounding resistance 550Ω)	3		60	mA
High level input	Vih	ADRI	0.7Vdd	-		V

voltage						
Low level input voltage	Vil	ADRI	-	-	0.3Vdd	V
Current offset (between channels)	dIout	Vds=1V，Iout=17mA		±1.5	±3.0	%
Current offset (between chips)	dIout	Vds=1V，Iout=17mA		±3.0	±5.0	%
Voltage offset VS-Vds	%dVds	1V<Vds<3V		±0.1	±0.5	%/V
Voltage offset VS-Vdd	%dVds	4.5V<Vdd<5.5V		±1.0	±2.0	%/V
Dynamic current loss	IDDdyn	VDD=5V	No load		4	mA
Thermal resistance	Rth(j-a)			80	190	℃/W

Function description

1. Communication data protocol:

TM512-AX data reception is compatible with standard DMX512(1990) protocol and able to expand DMX512 protocol. TM512-AX can perform adaptive decoding for a data transmission rate of 200Kbps-500Kbps. The protocol waveform is as follows: the chip is AI and Bi differentially input. The figure shows the time sequence waveform of AI which is opposite to that of BI.

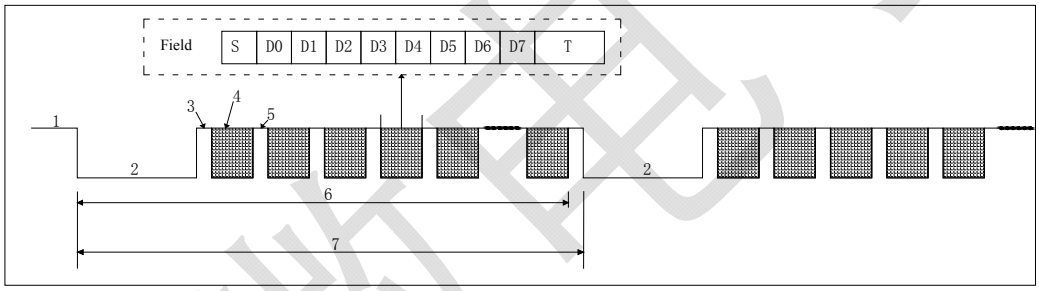


Figure 4

Symbol	Description	Min. value	Typical value	Max. value	Unit
	Bit rate	200	250	500	Kbps
	Bit time	5	4	2	μs
S	Start bit	5	4	2	μs
D0～D7	8 data bits	5	4	2	μs
T	2 stop bits	10	8	4	μs
1	Mark before reset	0		1000000	μs
2	Reset signal	88		1000000	μs
3	Mark after reset	8		1000000	μs
4	Field (note1)	55	44	22	μs
5	Span between fields	0		1000000	μs
6	Length of data packet	1024		1000000	μs
7	Reset signal interval	4096		1000000	μs

Note1: The field totally contains 11 bits, including 0 start bit, 8 data bits and 2 stop bits, wherein the 0 start bit is low level and the stop bits are high levels. If the data in the data bits is 0, the corresponding time period is low levels; if the data is 1, the corresponding time period is high level. The bit time for the 0 start bit, the stop bits and the data bits should be the same.

2. IC reception description:

1. When reset signal appears on AIBI wire, IC enters the reception-ready state, and the address counter resets.

2. The first field in the data packet is start field. Its 8 data bits must be "0000_0000". This field does not act as display data. The valid field used for display starts from the second field. The second field of DMX512 data packet is the first field of valid data. IC is self-adaptive to the data transmission rate of 200Kbps-00Kbps. Different rates correspond to different field durations. However, no matter the transmission rate is 200Kbps or 50Kbps, it only needs to ensure that the durations of all valid fields are same to that of the start field.

3. IC cuts out the corresponding field in DMX512 data packet according to the address in its E2. For example, if the chip address is 0000_0000_0000, it starts to cut out from the first valid field of the data packet; if the address is 0000_0000_0001, it starts to cut out from the second valid field. How many fields are used by the chip is set by PT1 and PT0.

PT1 (built-in and pull-down)	PT0 (built-in and pull-down)	Mode and number of fields cut out
0	0	3-field mode: 3 fields are cut out, respectively corresponding to R, G and B
0	1	4-field mode: 4 fields are cut out, respectively corresponding to R, G, B and W
1	0	2-field mode: 2 fields are cut out, respectively corresponding to RG and BW
1	1	1-field mode: 1 field is cut out, corresponding to RGBW

The 1-field mode and 2-field mode in the above table can achieve the current expansion function. For example, in the 1-field mode (generally monochrome application), the four output pins OUT/OUTR/OUTGB/OUTW can join up in parallel, when the maximum output current is up to 240mA. The said field selection is required only for data forwarding and current expansion. When current expansion is not required and under the point light source application (without the need for data forwarding), both PORT0 and PORT1 can be suspended from monochrome application and RGB trichromatic application.

4. When IC receives data, the interval of 2 reset signals cannot be less than 4ms. The frame frequency cannot be greater than 250Hz even though there are very few parallel connection points.

3. Precautions for the controller to send data:

1. As for standard DMX512(1990) protocol, if one subport of the controller connects 512 channels, that is to say, 170 pixel points, to achieve the refresh rate of 30Hz, the time width of each frame is 33.33ms and the time for transmitting 1bit is 4μs, the valid data time width will be 88+4μs*11bit*512 = 22.7ms and the time interval of each frame of data will be 33.33-22.7 = 10.63ms. In this time interval, the data line keeps at high level until the next reset signal.

2. TM512-AX requires the reset signal code interval of each data packet of the controller cannot be less than 4ms, i.e., the highest frame frequency cannot not be more than 250Hz, or else it may fail to display in a normal way.

4. Precautions for code writing:

1. On the code writer, there should be address writing terminal (PO) and A and B terminals. At code writing, AI and BI wires should be connected onto the A and B terminals of the code writer, and the A terminal of the code writer should be at high level and the B terminal of the same should be at low level. IC can perform normal code writing provided AI is at high level and BI is at low level.

2. After code writing, the blue light of the IC driver which has received the new address code is normally on, yet the newly written-in address code is not valid and all the newly encoded ICs still use the original address code. When the ICs are electrified again after powered off, the newly written-in address code will be valid. (In practical use, the lamp and the controller should be powered off. If the controller is not powered off, it is easy to cause incomplete outage of the first lamp directly connected with the code writing wire of the controller because of the charging by the controller via the code writing wire, hence the newly written-in address code is invalid.)

3. After code writing, do not take A and B wires down. Use the dedicated test program of the code writer to test, in a way to confirm if code writing is completely correct.

4. The address input end line on PO port of the code writer should be pulled out from the code writer after code writing, in order to avoid wrong code writing when the code writer is disordered. When the code writing wire is pulled out, it should be suspended and wrapped with insulating tape. There is no need of special ground connection.

5. Cautions for differential bus connection:

1. The controller should be common-grounded with ICs, and different ICs should also be common-grounded, in order to prevent excessive common mode voltage breaking down ICs. Shielding layer can be used as common-grounded wire for reliable connection of multiple IC nodes, to be reliably grounded at one point rather than grounded at double ends or multiple ends.

2. The protective resistors connected in parallel from AI and BI wires on the board to ICs should be consistent. The wiring mode of AI and BI wires on the board from bonding pad to ICs should try to be consistent.

3. AI and BI buses should try to adopt shielded twisted pair (especially in weak-current and heavy-current wiring duct sharing projects, nearby launching tower or the areas with more lightning) to reduce interference and lightning impulse. Cat. 5e shielded twisted pair can be used, but pay attention to purchase copper wire.

4. 485 node in 485 bus should try to reduce the distance with main line. It is generally suggested that 485 bus adopts hand-in-hand bus topology. Star configuration will produce reflected signals, which affect the quality of 485 communication. In the construction process, the distance between 485 node and 485 bus main line must be over 30cm. It is suggested to use 485 repeater as a bifurcation of 485 bus. If star topology is required to be used in the construction process, 485 concentrator should be used.

5. 485 bus will produce reflection echo signals along with the prolonging of transmission distance. If the transmission distance of 485 bus is long, it is suggested to connect a 120Ω terminal matching resistor on AI and BI wires at 485 communication terminal when construction is in process.

Constant current module

1. Output constant current setting:

OUTR, OUTG, OUTB and OUTW are constant current output. The maximum current can be up to 60mA. It is not suggested to set the current at the maximum value in practical application. The constant current value is determined by REXT grounding resistance. Current formula:

Iout = 48/(250+Rext) (1)

Rext = (48/Iout)-250 (2)

Rext is the resistor bridged between REXT pin and ground. Iout is the current output by OUTR, OUTG, OUTB and OUTW ports.

Current value (mA)	Rext resistance (Ω)
18	2416
20	2150
36	1083
60	550

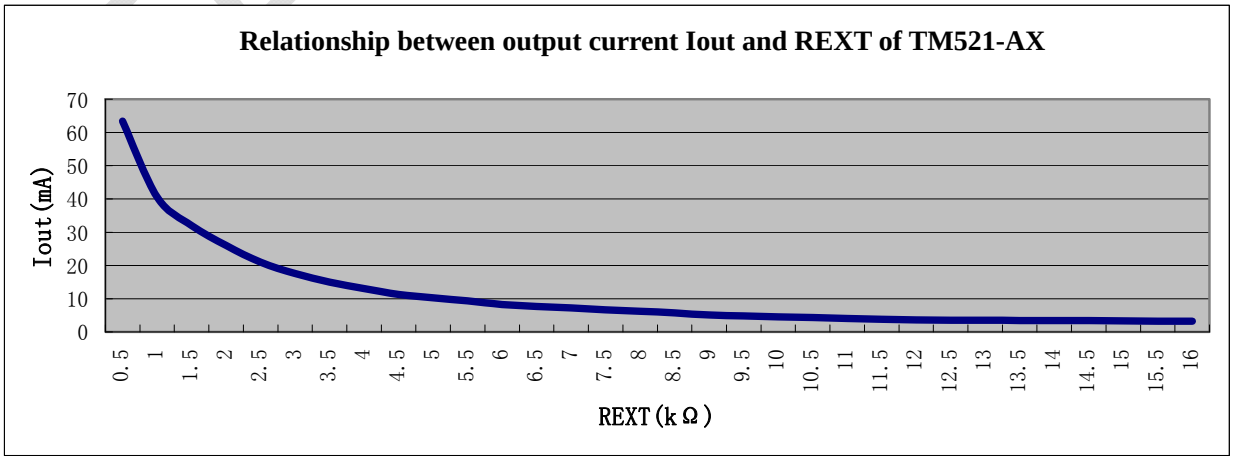


Figure 5

2. Constant current curve:

The constant-current characteristics of TM512-AX are outstanding. The current difference between channels and even between chips is very small.

(1) The current error between channels and between chips is less than ±3%.

(2) When the load end voltage changes, TM512-AX output current will not be affected, as shown in the following figure.

(3) As shown in the following figure, according to the curvilinear relationship between TM512-AX output port current I and the voltage Vds added on the port, if the current I is smaller, the Vds required under constant current is also smaller.

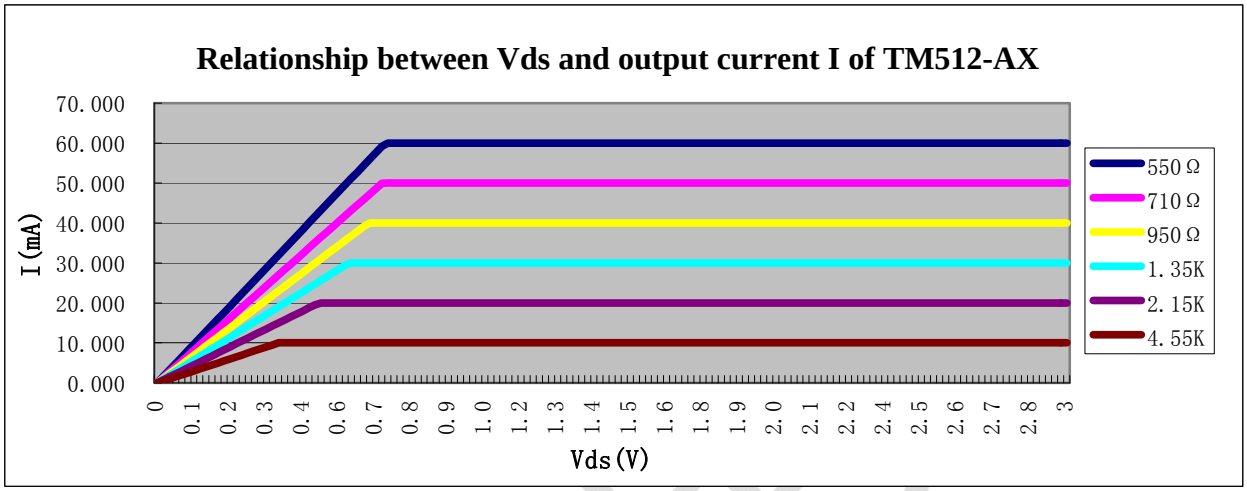


Figure 6

Application information

1. Application drawing 1: RGBW tetrachromatic application

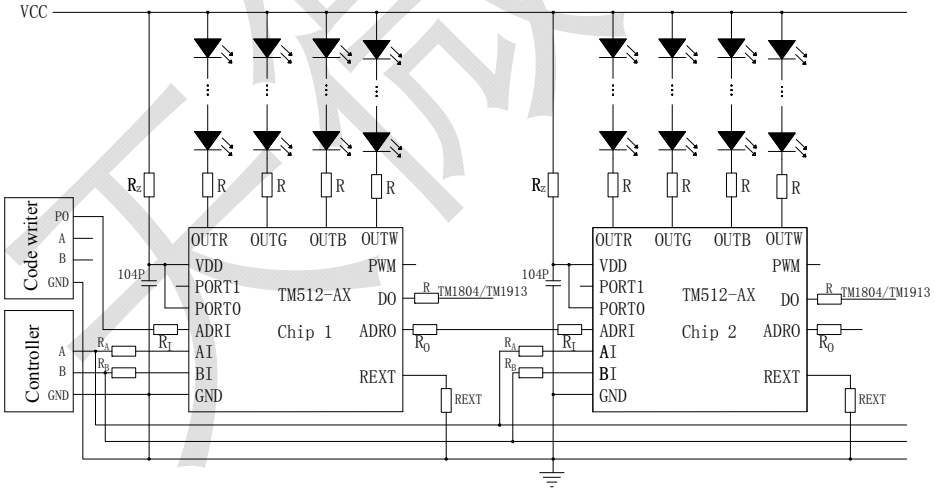


Figure 7

Notes: 1. Output high-precision constant current, up to 60mA for each channel which is connected with in parallel 4 sets of lamps to the largest extent (15mA/set).

2. Pay attention to the selection of divider resistor R to avoid excessive IC power consumption.

3. At code writing, IC should maintain that the level of AI is higher than that of BI. It is suggested to connect AI and BI buses to the A and B terminals of the code writer which provides the level of A higher than that of B.

4. REXT port must add grounding resistance to set output current. This port cannot be suspended.

2. Application drawing 2: RGB trichromatic application

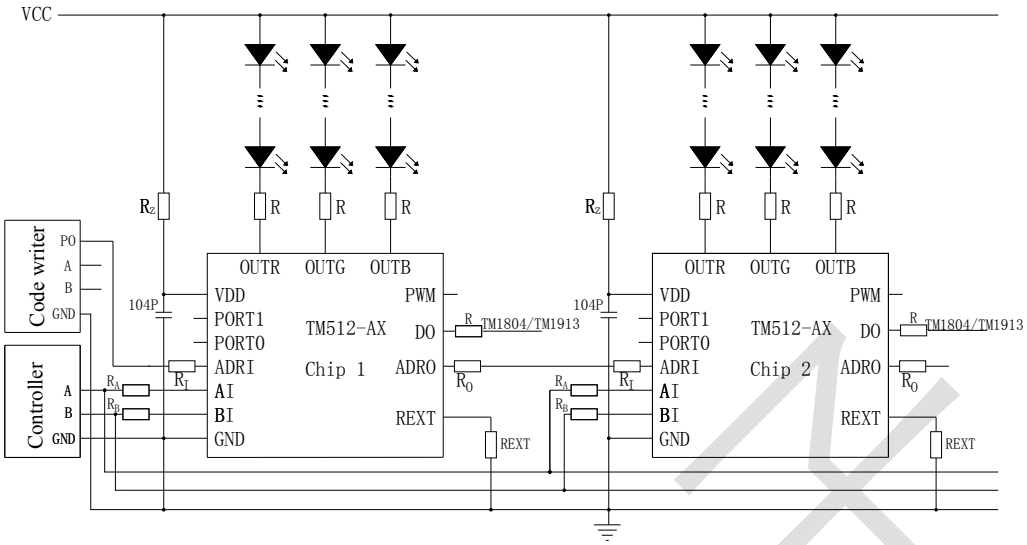


Figure 8

Notes: 1. Output high-precision constant current, up to 60mA for each channel which is connected with in parallel 4 sets of lamps to the largest extent (15mA/set).
2. Pay attention to the selection of divider resistor R to avoid excessive IC power consumption.
3. At code writing, IC should maintain that the level of AI is higher than that of BI. It is suggested to connect AI and BI buses to the A and B terminals of the code writer which provides the level of A higher than that of B.
4. REXT port must add grounding resistance to set output current. This port cannot be suspended.

3. Application drawing 3: dichromatic application

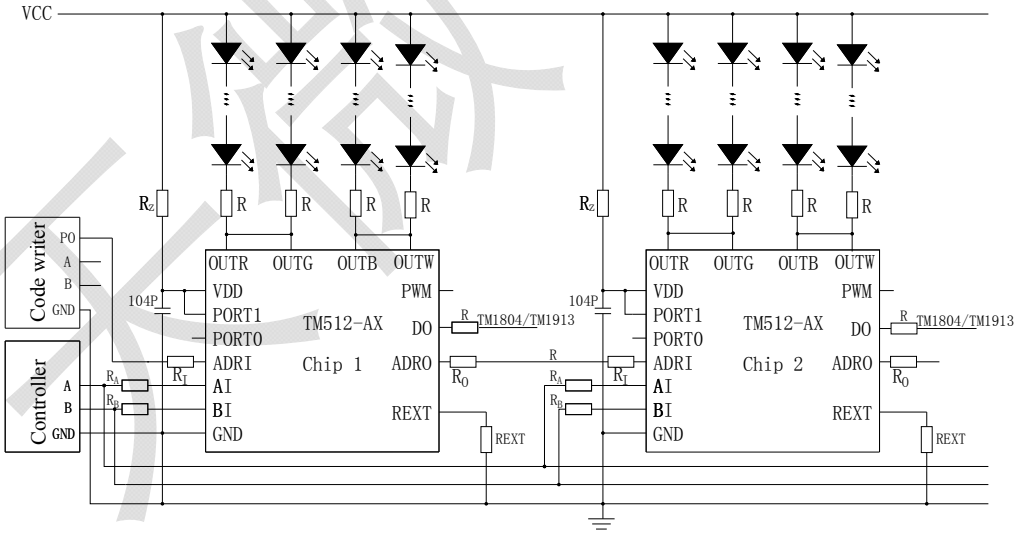


Figure 9

Notes: 1. At dichromatic application, the chip cuts out its own two bytes of data, channel OUTR has the same data with channel OUTG, and channel OUTB has the same data with channel OUTW. The figure shows the parallel current expansion application. When the 2 channels are connected in parallel, the maximum output current is 120mA.
2. Pay attention to the selection of divider resistor R to avoid excessive IC power consumption.
3. At code writing, IC should maintain that the level of A is higher than that of B. It is suggested to connect AI and BI buses to the A and B terminals of the code writer which provides the level of A higher than that of B.
4. REXT port must add grounding resistance to set output current. This port cannot be suspended.

4. Application drawing 4: monochrome application

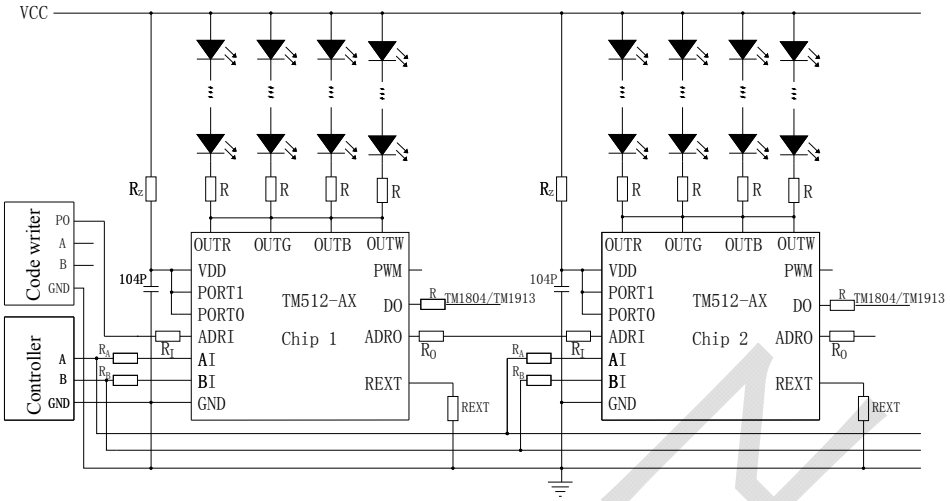
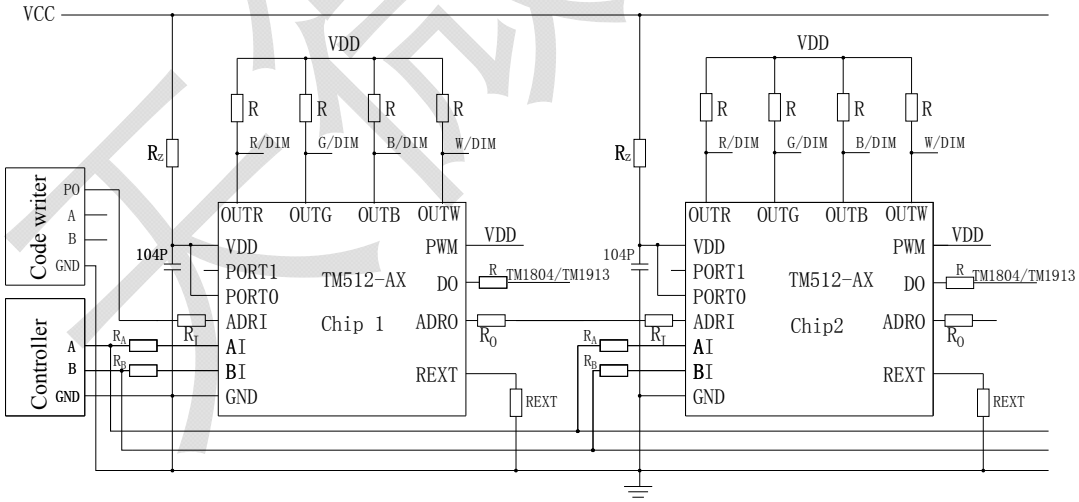


Figure 10

Notes: 1. At monochrome application, the chip cuts out its own one byte of data, and the 4 channels have the same data. The figure shows the parallel current expansion application. When the 4 channels are connected in parallel, the maximum output current is 240mA.

2. Pay attention to the selection of divider resistor R to avoid excessive IC power consumption.
3. At code writing, IC should maintain that the level of AI is higher than that of BI. It is suggested to connect AI and BI buses to the A and B terminals of the code writer which provides the level of A higher than that of B.
4. REXT port must add grounding resistance to set output current. This port cannot be suspended.

5. Application drawing 5: plug-in triode application (can also be connected with external MOS tube or high-power constant current drive)



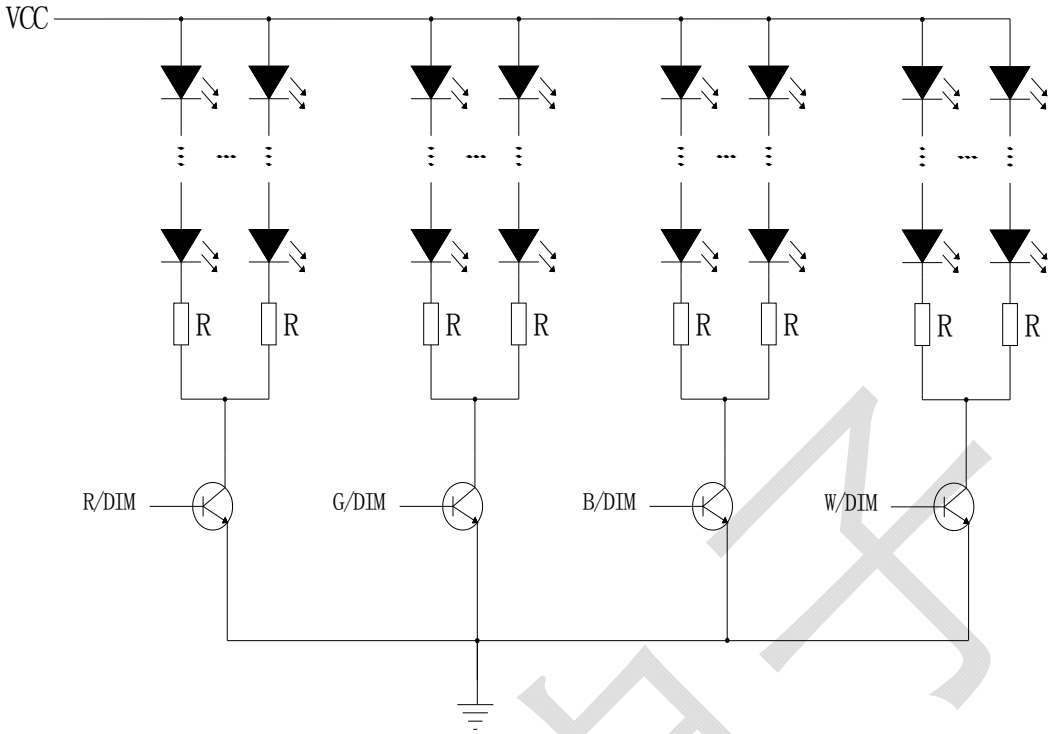


Figure 11

Notes: 1. When PWM pin connects VDD, it is reverse polarity underclocking constant voltage output, which is applicable to external NPN triode base (B), MOS tube or any high-power constant current drive IC with DIM (optical modulation end). At application, the output pin is pulled up to VDD and can also be pulled to other power supplies. The pull-up resistor is generally about 5K.

2. The above figure is the application drawing at 4-channel reverse polarity application. At other field reverse polarity application, pay attention to the selection of PORT0 and PORT1 ports.
3. At code writing, IC should maintain that the level of AI is higher than that of BI. It is suggested to connect AI and BI buses to the A and B terminals of the code writer which provides the level of A higher than that of B.
4. REXT can be suspended at reverse polarity application.

6. Tables of optional values for components

The table of optional values for R_Z is as follows:

VCC	24V	12V	5V
R_Z （Ω） R_Z (Ω)	1.8K～2.0K 1.8K-2.0K	650～800 650-800	51
R_I （Ω） R_I (Ω)	100	100	100
R_O （Ω） R_O (Ω)	100	100	100

The table of optional values for R_A / R_B is as follows:

Controller A port output voltage	12V	5V
R_A （Ω） R_A (Ω)	30K～50K 30K-50K	100～200 100-200
R_B （Ω） R_B (Ω)	30K～50K 30K-50K	100～200 100-200

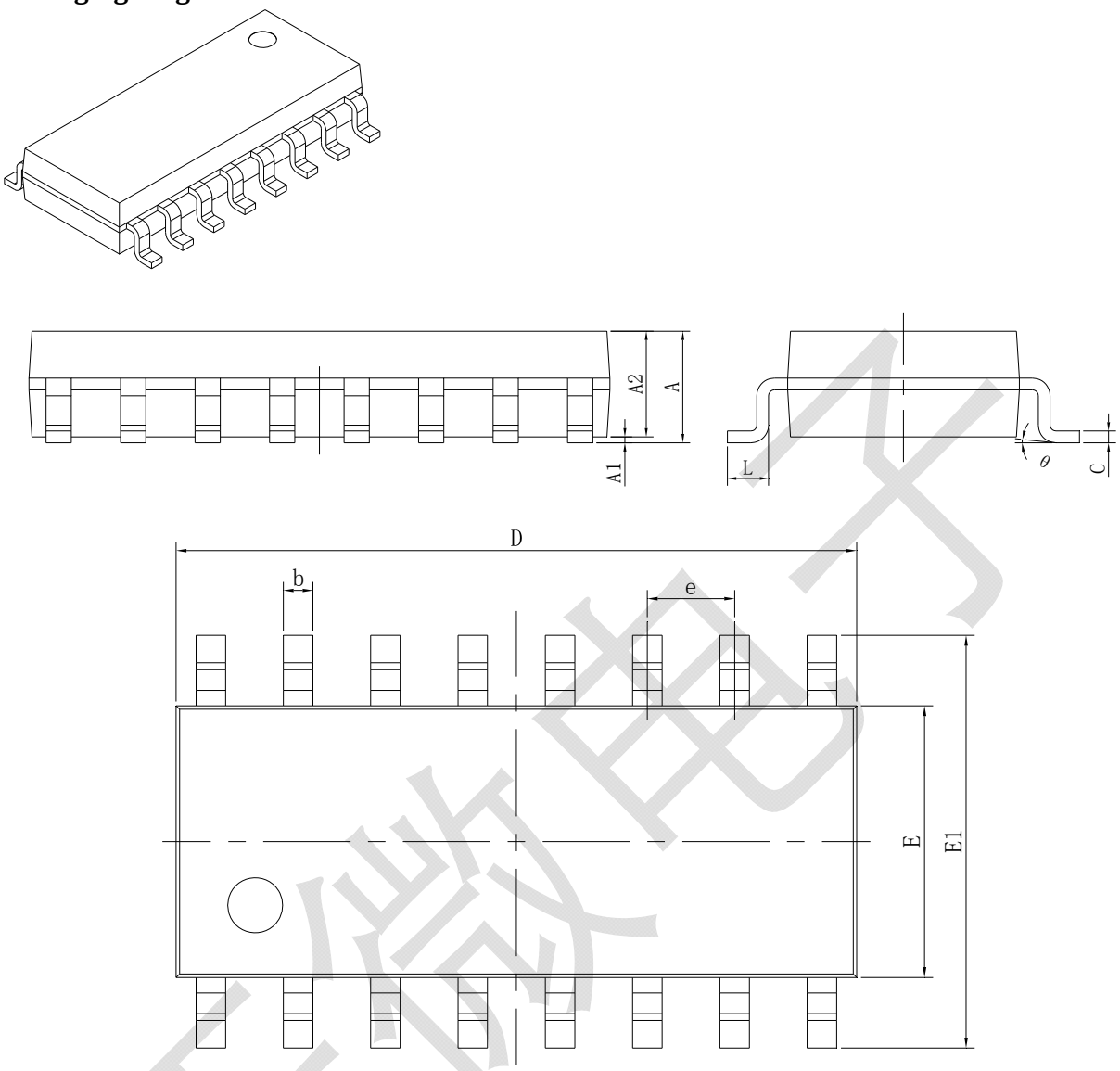
(1) Selection of VDD divider resistor Rz

It is suggested to set VDD current as 10mA and VDD steady voltage as 5.2V, hence Rz = (VCC-5.2)/0.01. For example, when VCC = 24V, Rz will be 1.88KΩ according to the formula.

(2) Value selection of light string resistor R

Since the long-term packaging power consumption of SOP16 cannot exceed 400mW, the IC power consumption should be set to be less than 400mW. With the increase of drive current, the output voltage Vout of the chip channel should be decreased, i.e., 400mW>5.2V*10mA+Vout*Iout*N (wherein, N is channel number, Vout is channel port voltage, and Iout is channel setting current), when N = 4 and Iout = 30mA, we get Vout<2.9V. And because Vout = VCC-M*VL-R*Iout (wherein M is the number of lamps connected in series on single channel, VL is the voltage drop of lamps), when VCC = 24V, VL = 2 and M = 8, we get R>170Ω. Besides, in order to output constant current, we should enable Vout>0.8Vm, hence R<240Ω. For the sake of achieving better output characteristics for the chip when the power consumption meets the requirements, it is suggested to select appropriate intermediate value for R.

Packaging diagram: SOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.30	1.70	0.051	0.067
A1	0.08	0.24	0.003	0.009
b	0.4TYP		0.016TYP	
c	0.25TYP		0.010TYP	
D	8.25	8.85	0.325	0.348
E	3.75	4.15	0.148	0.163
E1	5.70	6.30	0.224	0.248
e	1.27TYP		0.050TYP	
L	0.45	0.85	0.018	0.033
θ	0°	8°	0°	8°

(All specs and applications shown above are subject to change without prior notice.)