PAM8002

Ultra Low EMI, 3W Filterless Mono Class D Audio Power Amplifier with Anti-saturation

Key Features

- One-side Modulation Active Emissions Significantly Reduce EMI
- Unique Anti-saturation Technology with Maximum Output Power Setting Reduce Distortion and Protect Speaker to be Damaged
- High Efficiency up to 89% with an 8Ω Speaker
- 3W@10% THD Output with a 4Ω Load at 5V Supply
- Maximum Output Power Adjuastable
- Minimized "Click and Pop" Noises
- Superior Low Noise without Input
- Supply Voltage from 2.5V to 5.5 V
- Short Circuit Protection
- Thermal Shutdown
- Available in Space Saving Packages: 1.45mmx1.45mm WCSP9, MSOP-8L, Pb-Free Package

Applications

- Cellular Phones/Smart Phones
- MP4/MP3
- GPS
- Digital Photo Frame
- Electronic Dictionary
- Portable Game Machines

General Description

The PAM8002 is a 3W mono filterless class-D amplifier with high PSRR and differential input that reduce noise.

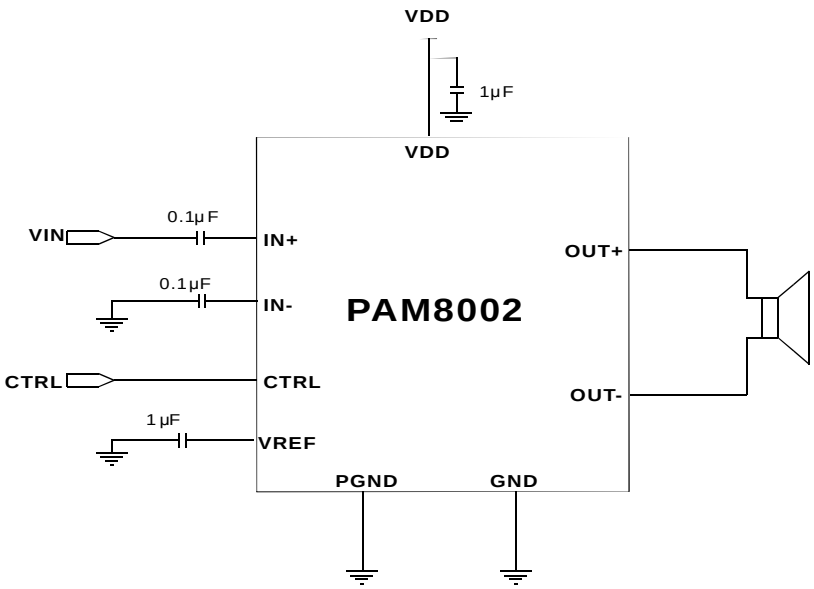
Features like 89% efficiency and small PCB area make the PAM8002 Class-D amplifier ideal for cellular handsets. The filterless architecture requires no external output filter, fewer external components, less PCB area and lower system costs, and simplifies application design.

The PAM8002 features anti-saturation function which detect output signal clip due to the over input level and keep the output non-saturation automatcally and the release time is selectable, that to get the excellent sound quality and prevent the speaker to be damaged. Additionally, the maximum output power is adjusted by one external resistor make the PAM8002 an flexible choice for kinks of application.

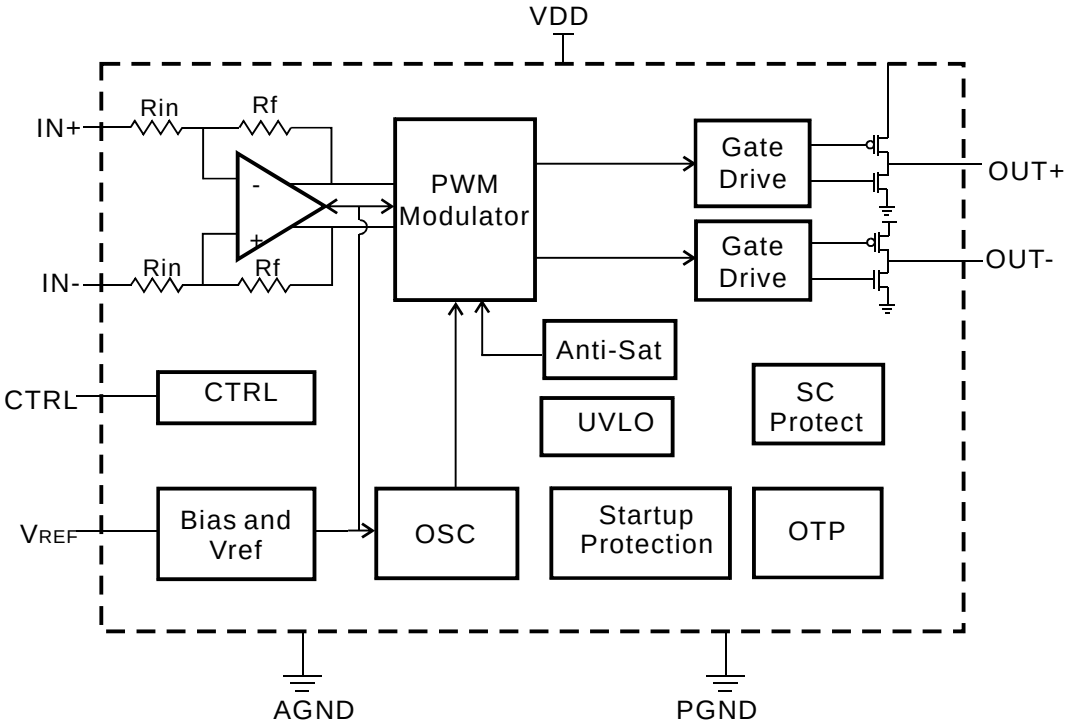
The PAM8002 features short circuit protection and over temperature protection.

The PAM8002 is available in tiny WCSP-9 and MSOP-8L packages.

Typical Application Circuit

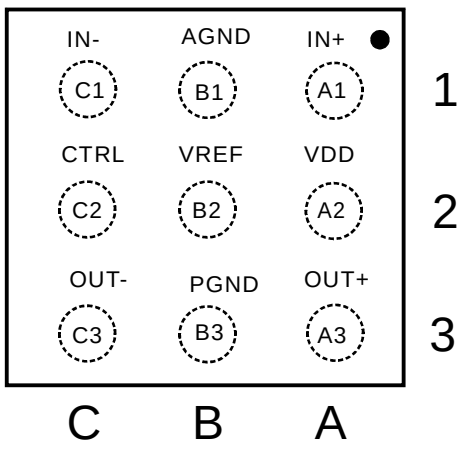


Block Diagram

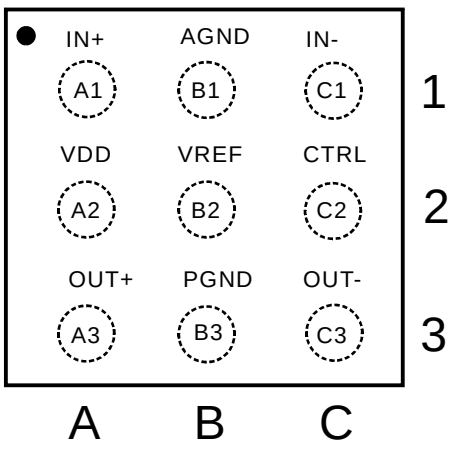


Pin Configuration & Marking Information

9 Ball WCSP
Top View



9 Ball WCSP
Bottom View

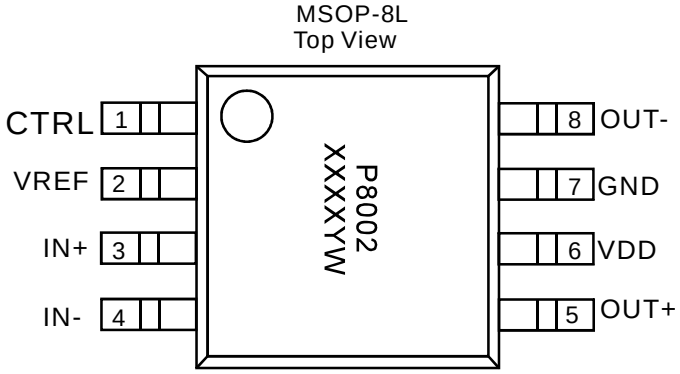


Marking

BF
YW

BF: Product Code of PAM8002
Y: Year
W: Week

Pin Configuration & Marking Information



X: Internal Code
Y: Year
W: Week

Pin Number	Pin name	Description
1	CTRL	CRTL terminal to set chip operation mode
2	V_{REF}	Common mode output
3	IN+	Positive differential input
4	IN-	Negative differential input
5	OUT+	Positive BTL output
6	VDD	Power supply
7	AGND	Analog Ground
8	OUT-	Negative BTL output

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage 6.0V
Input Voltage.....-0.3V to V_{DD}+0.3V
Storage Temperature.....-65°C to 150°C
Maximum Junction Temperature.....150°C
Soldering Temperature.....250°C,10 sec

Recommended Operating Conditions

Supply voltage Range.....2.5V to 5.5V
Ambient Temperature Range.....-40°C to 85°C
Junction Temperature Range.....-40°C to 125°C

Thermal Information

Parameter	Symbol	Package	Maximum	Unit
Thermal Resistance (Junction to ambient)	θ_{JA}	WCSP 1.45x1.45	90-220	°C/W
		MSOP-8	180	°C/W
Thermal Resistance (Junction to case)	θ_{JC}	MSOP-8	75	°C/W

Electrical Characteristic

T_A=25°C, V_{DD}=5V, V_{REF}=2.5V, Gain=24dB, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

Symbol	Parameter	Test Conditions		MIM	TYP	MAX	UNIT
V_{DD}	Supply Voltage			2.5		5.5	V
Po	Output Power Anti-saturation off	THD+N=10%,f=1kHz, R=4Ω	V_{DD}=5.0V	2.85	3.0		W
			V_{DD}=3.6V	1.5	1.65		
			V_{DD}=2.5V	0.7	0.8		
		THD+N=1%,f=1kHz, R=4Ω	V_{DD}=5.0V	2.50	2.65		W
			V_{DD}=3.6V	1.2	1.35		
			V_{DD}=2.5V	0.5	0.6		
		THD+N=10%,f=1kHz, R=8Ω	V_{DD}=5.0V	1.5	1.65		W
			V_{DD}=3.6V	0.7	0.85		
			V_{DD}=2.5V	0.35	0.4		
		THD+N=1%,f=1kHz, R=8Ω	V_{DD}=5.0V	1.2	1.35		W
			V_{DD}=3.6V	0.6	0.7		
			V_{DD}=2.5V	0.25	0.3		
Po	Output Power Anti-saturation active	THD+N<1%,f=1kHz, R=4Ω	V_{DD}=5.0V		2.2		
		THD+N<1%,f=1kHz, R=8Ω	V_{DD}=5.0V		1.5		
THD+N	Total Harmonic Distortion Plus Noise	V_{DD}=5.0V,Po=1W,R=4Ω	f=1kHz		0.1	0.2	%
		V_{DD}=3.6V,Po=0.5W,R=4Ω			0.1	0.2	
		V_{DD}=2.5V,Po=0.1W,R=4Ω			0.17	0.3	
		V_{DD}=5.0V,Po=0.5W,R=8Ω	f=1kHz		0.11	0.2	%
		V_{DD}=3.6V,Po=0.3W,R=8Ω			0.08	0.2	
		V_{DD}=2.5V,Po=0.1W,R=8Ω			0.11	0.2	
PSRR	Power Supply Ripple Rejection	V_{DD}=5V, Inputs ac-grounded with Cin=1μF	f=217Hz		-65		dB
			f=1kHz		-67		
SNR	Dynamic Range	V_{DD}=5V, THD=1%, R=8Ω	f=1kHz	85	95		
Vn	Output Noise	V_{DD}=5V Inputs ac-grounded	No A-weighting		100	150	μV
			A-weighting		70	100	
CMRR	Common Mode Rejection Ratio	V_{IC}=100mVpp,f=1kHz		40	65		dB

Electrical Characteristic (continued)

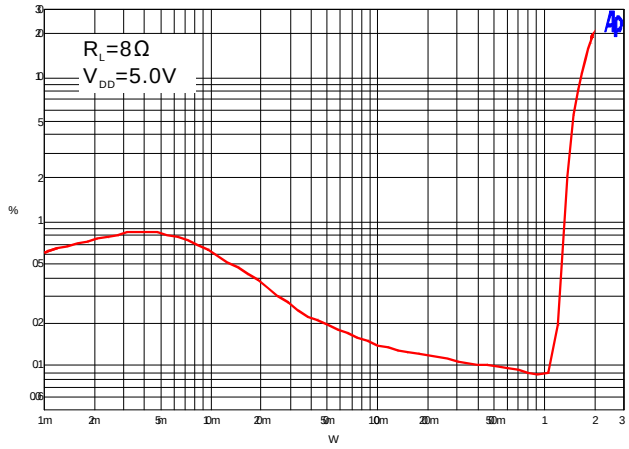
T_A=25°C, V_{DD}=5V, V_{REF}=2.5V, Gain=24dB, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

Symbol	Parameter	Test Conditions		MIM	TYP	MAX	UNIT
η	Efficiency	R_L=8Ω, THD=10%	f=1kHz	85	89		%
		R_L=4Ω, THD=10%		83	86		
I_Q	Quiescent Current	V_{DD}=5V	R =8Ω		5.6		mA
		V_{DD}=3.6V			4.4		
		V_{DD}=2.5V			3.0		
I_{SD}	Shutdown Current	V_{DD}=3V to 5V	V_{SD}=0.3V		0.5	1	μA
Rdson	Static Drain-to-source On-state Resistor	CSP package，High Side PMOS plus Low Side NMOS, I=500mA	V_{DD}=5V		280	350	mΩ
			V_{DD}=3.6V		300	375	
			V_{DD}=2.5V		350	400	
		MSOP/DFN package，High Side PMOS plus Low Side NMOS, I=500mA	V_{DD}=5V		365	420	mΩ
			V_{DD}=3.6V		385	450	
			V_{DD}=2.5V		450	500	
Rin	Internal Input Resistance				18		kΩ
fsw	Switching Frequency	V_{DD}= 5V		200	250	300	kHz
Gv	Closed-loop Gain	V_{DD}= 5V			24		dB
Vos	Output Offset Voltage	Input ac-ground, V_{DD}=5V			10	50	mV
T_{ON}	Turn-on time from Shutdown	V_{DD}=5V			32		mS

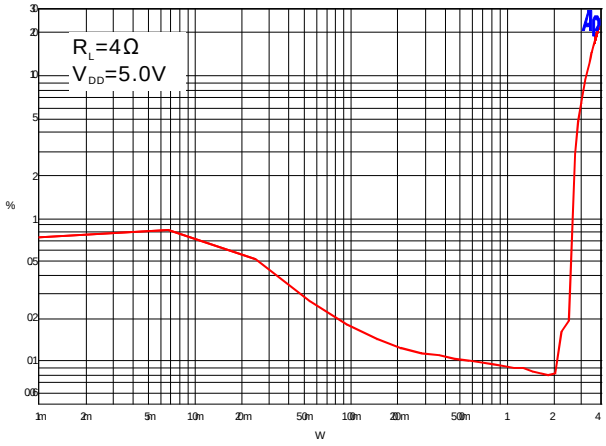
Typical Operating Characteristics

T_A=25°C, V_{DD}=5V, f=1kHz, Gain=24dB, unless otherwise noted.

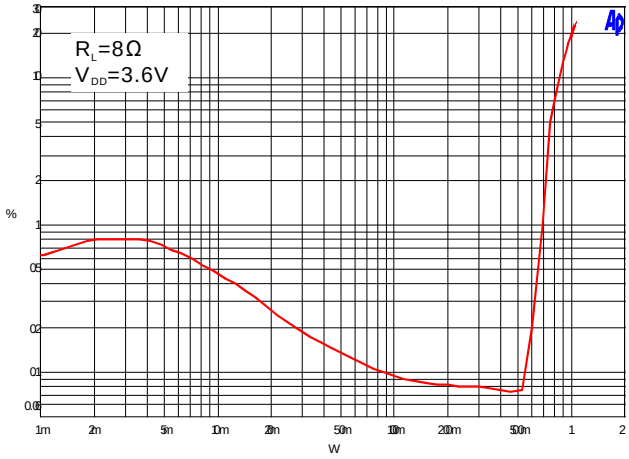
1. THD+N VS Output Power



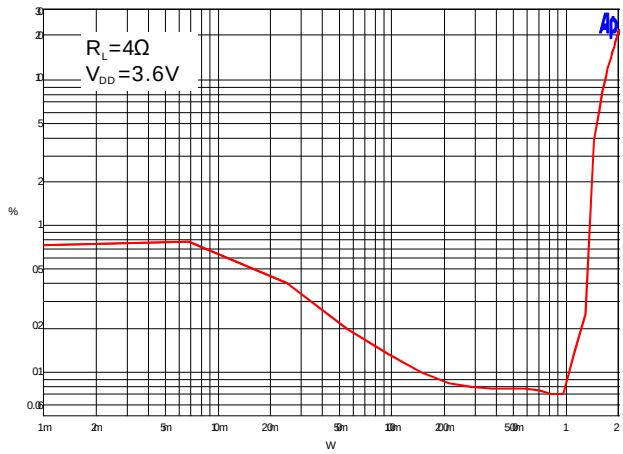
2. THD+N VS Output Power



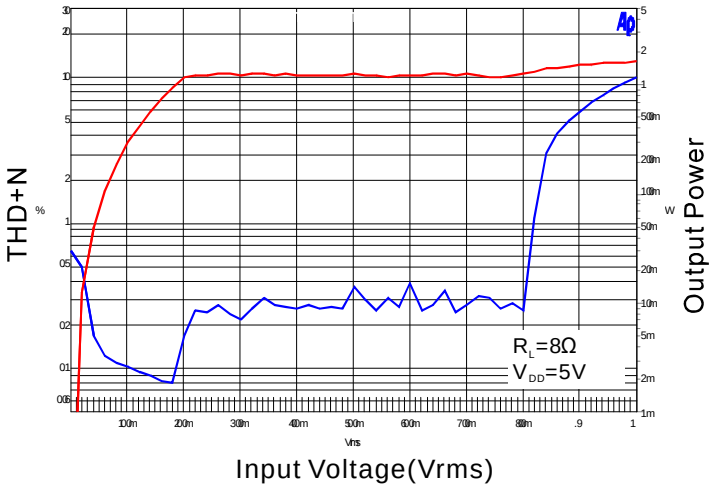
3. THD+N VS Output Power



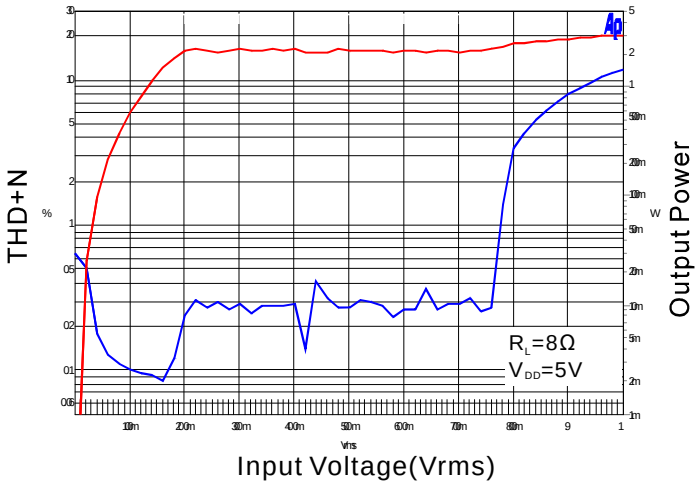
4. THD+N VS Output Power



5. THD+N VS Output Power(with anti-saturation)



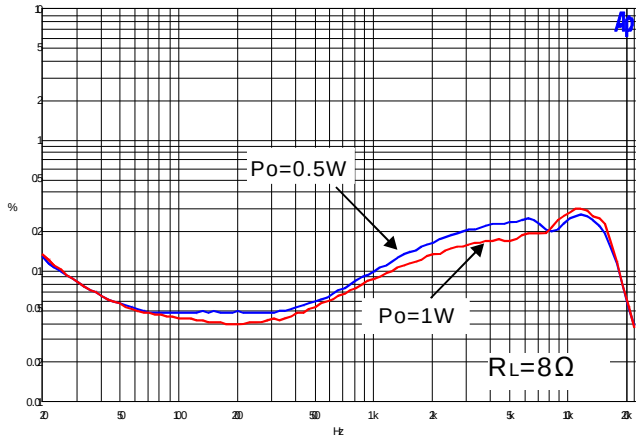
6. THD+N VS Output Power(with anti-saturation)



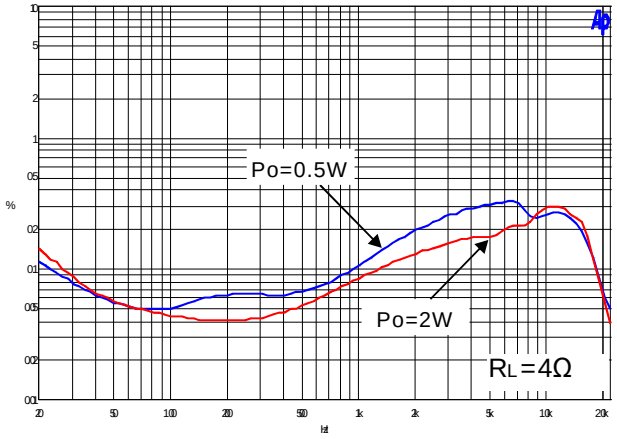
Typical Operating Characteristics

T_A=25°C, V_{DD}=5V, f=1kHz, Gain=24dB, unless otherwise noted.

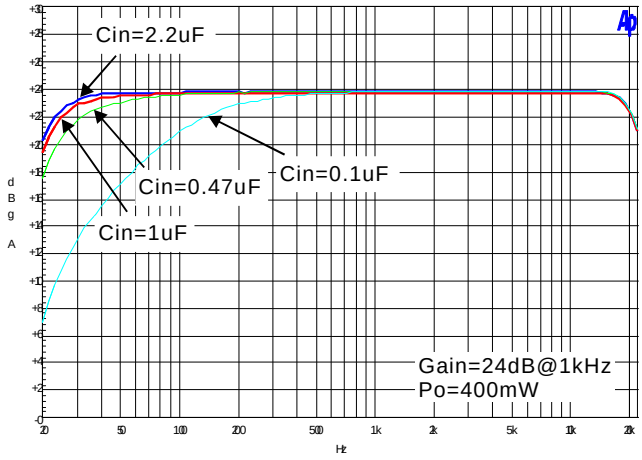
7. THD+N VS Frequency



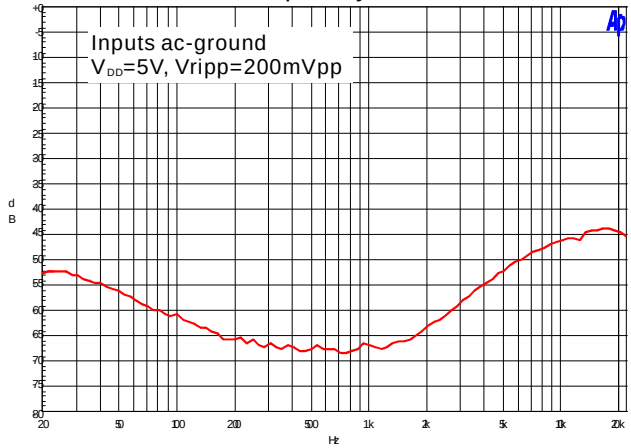
8. THD+N VS Frequency



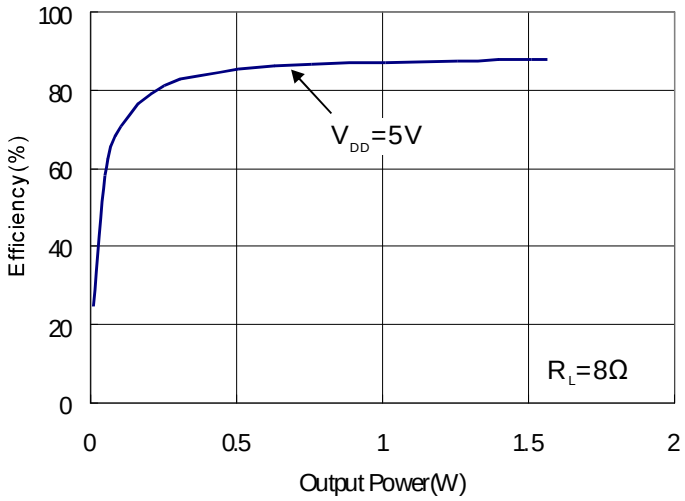
9. Frequency Response



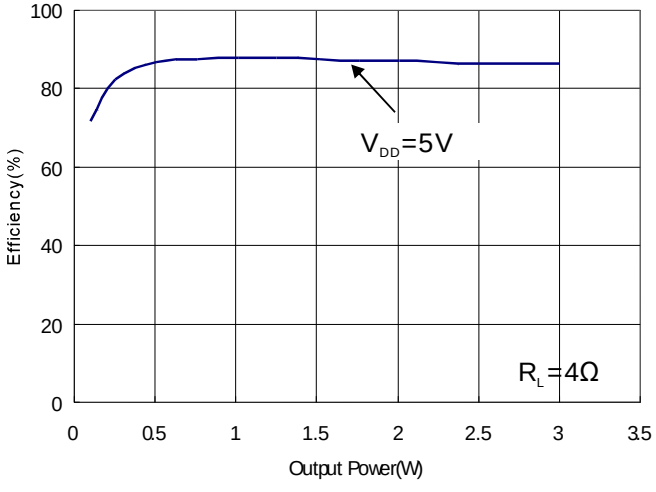
10. PSRR VS Frequency



11. Efficiency VS Output Power



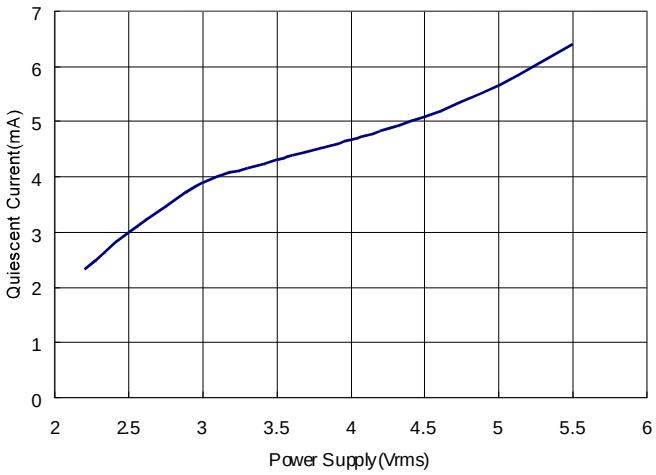
12. Efficiency VS Output Power



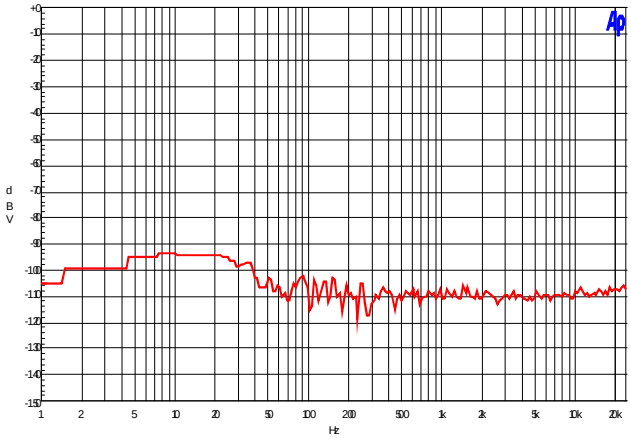
Typical Operating Characteristics

T_A=25°C, V_{DD}=5V, f=1kHz, Gain=24dB, unless otherwise noted.

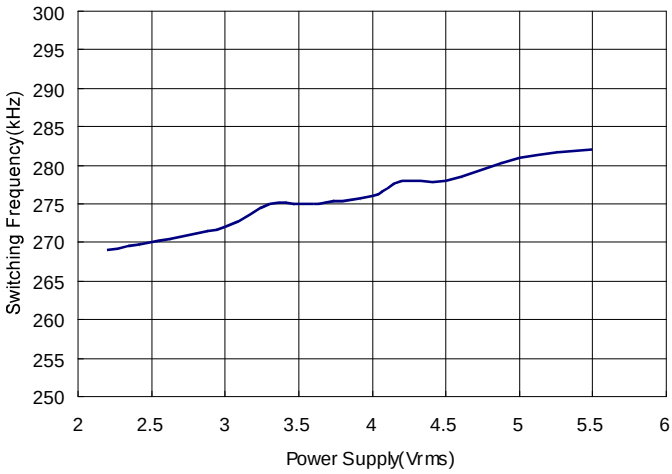
13. Quiescent Current vs Power Supply Voltage



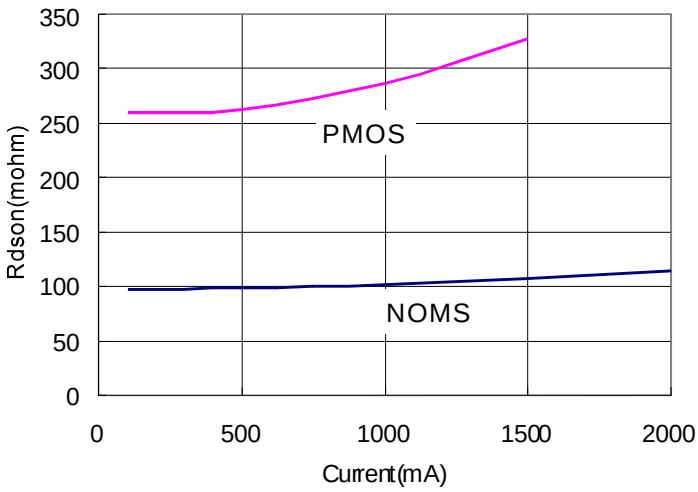
14. Noise FFT



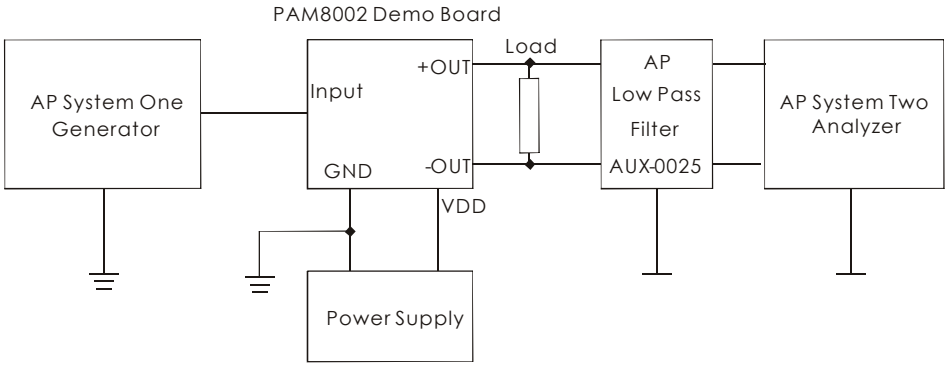
15. OSC Frequency



16. Rdson vs Supply Voltage



Test Setup for Performance Testing



Notes

1. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
2. Two 33µH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Application Information

Anti-saturation

The Anti-saturation feature provides continuous automatic gain adjustment to the amplifiier through an internal circuit. This feature enhances the perceived audio loudness and at the same time prevents speaker damage from occurring.

The Anti-saturation works by detecting the PWM output. The gain changes depending on the duty cycle, and the attack and release time. The gain changes constantly as the audio signal increases and/or decreases. The gain step size for the Anti-saturation is 0.4 dB. If the audio signal has near-constant amplitude, the gain does not change. Table 1 shows the Anti-saturation variable description.

Table 1. PAM8002 Anti-saturation Variable Description

VARIABLE	DESCRIPTION	Value
Gain	The pre-set gain of the device when the Anti-saturation is inactive. The fixed gain is also the initial gain when the device comes out of shutdown mode or when the Anti-saturation is disabled	24dB (Maximum)
Attack Time	The minimum time between two gain decrements. Mode 1	32uS
	The minimum time between two gain decrements. Mode 2	32uS
Release Time	The minimum time between two gain increments. Mode 1	256mS
	The minimum time between two gain increments. Mode 2	128mS

CTRL Terminal Function

4 modes, Anti-sat 1,Anti-sat 2, Anti-sat off and Shutdown, can be set by apply a DC voltage to CTRL terminal, the threshold voltage of each mode is listed in table 2.

Table 2. Mode Threshold Voltage

Mode	Function	Threshold Voltage
1	Anti-sat 1	1.2V ~ VDD
2	Anti-sat 2	0.8V ~ 1.1V
3	Anti-sat OFF	0.4V ~ 0.7V
4	Shutdown	0V ~ 0.3V

V_{REF} Terminal Function

PAM8002 internal common mode point, one 1uF capacitor is connected from this terminal to GND for good performance. The voltage value of V_{REF} sets the PAM8002 maximum output by an external resistor. Refer to Figue 1and Table 3 for the maximum power setting.

Figure 1

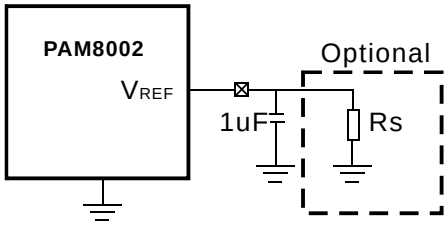


Table 3 Power Limitation Setting

Rs	V_{REF}	Anti-saturation Output Power
200K	0.6V	3.0W
100K	0.4V	2.0W
39K	0.2V	0.5W
18K	0.1V	0.2W

Application Information

Input Resistance (Ri)

The input resistors (Ri=Rin+Rex) set the gain of the amplifier according to Equation 1.

G=20 Log [2*150K/(Rin+Rex)] (DB)

Where Ri is a 18K internal resistor, Re is the external input resistor. Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the PAM8002 to limit noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2X(Ri=150k) or lower. Lower gain allows the PAM8002 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise. In addition to these features, higher value of Ri minimizes pop noise.

Input Capacitors (Ci)

In the typical application, an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form is a high-pass filter with the corner frequency determined in the follow equation:

$$f_C = \frac{1}{(2\pi RiCi)}$$

It is important to consider the value of Ci as it directly affects the low frequency performance of the circuit. For example, when Ri is 150kΩ and the specification calls for a flat bass response are down to 150Hz. Equation is reconfigured as followed:

$$Ci = \frac{1}{(2\pi Rif_c)}$$

When input resistance variation is considered, the Ci is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci, Ri + Rf) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at $V_{DD}/2$, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (C_s)

The PAM8002 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, is placed as close as possible to the device each VDD and PVDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination shown at Figure 1. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

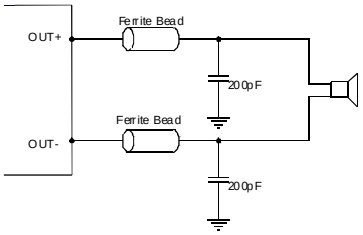


Figure 1: Ferrite Bead Filter to Reduce EMI

Shutdown operation

In order to reduce power consumption while not in use, the PAM8002 contains shutdown circuitry

amplifier off when logic low is placed on the $\overline{SD}$ pin. By switching the shutdown pin connected to GND, the PAM8002 supply current draw will be minimized in idle mode.

Under Voltage Lock-out (UVLO)

The PAM8002 incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 2.3V or below, the PAM8002 goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when reset the power supply or $\overline{SD}$ pin.

Short Circuit Protection (SCP)

The PAM8002 has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorts or output-to-GND shorts occur. When a short circuit occurs, the device immediately goes into shutdown state. Once the short is removed, the device will be reactivated.

Over Temperature Protection (OTP)

Thermal protection on the PAM8002 prevents the device from damage when the internal die temperature exceeds 135°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 30°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

POP and Click Circuitry

The PAM8002 contains circuitry to minimize turn-on and turn-off transients or “click and pops”, where turn-on refers to either power supply turn-on or device recover from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device will remain in mute mode until the reference voltage reach half supply voltage, 1/2 VDD. As soon as the reference voltage is stable, the device will begin full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

PCB Layout Guidelines

Grounding

It is recommended to use plane grounding or separate grounds. Do not use one line connecting power GND and analog GND. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. When these currents circulate elsewhere, they may get into the power supply, or the signal ground, etc, even worse, they may form a loop and radiate noise. Any of these instances results in degraded amplifier performance. The output noise ground that the logical returns for the output noise currents associated with class D switching must tie to system ground at the power exclusively. Signal currents for the inputs, reference need to be returned to quite ground. This ground only ties to the signal components and the GND pin. GND then ties to system ground.

Power Supply Line

As same to the ground, VDD and PVDD need to be separately connected to the system power supply. It is recommended that all the trace could be routed as short and thick as possible. For the power line layout, just imagine water stream, any barricade placed in the trace (shown in figure 2) could result in the bad performance of the amplifier.

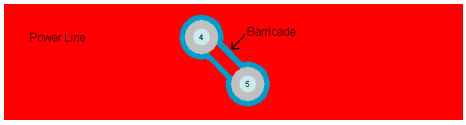


Figure 2: Power Line

Components Placement

Decoupling capacitors-As previously described, the high-frequency 1μF decoupling capacitors should be placed as close to the power supply terminals (VDD and PVDD) as possible. Large bulk power supply decoupling capacitors (10μF or greater) should be placed near the PAM8002 on the PVDD terminal.

Input resistors and capacitors need to be placed very close to input pins.

Output filter - The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance, and the capacitors used in the filters should be grounded to system ground.

Ordering Information

PAM8002 X X X

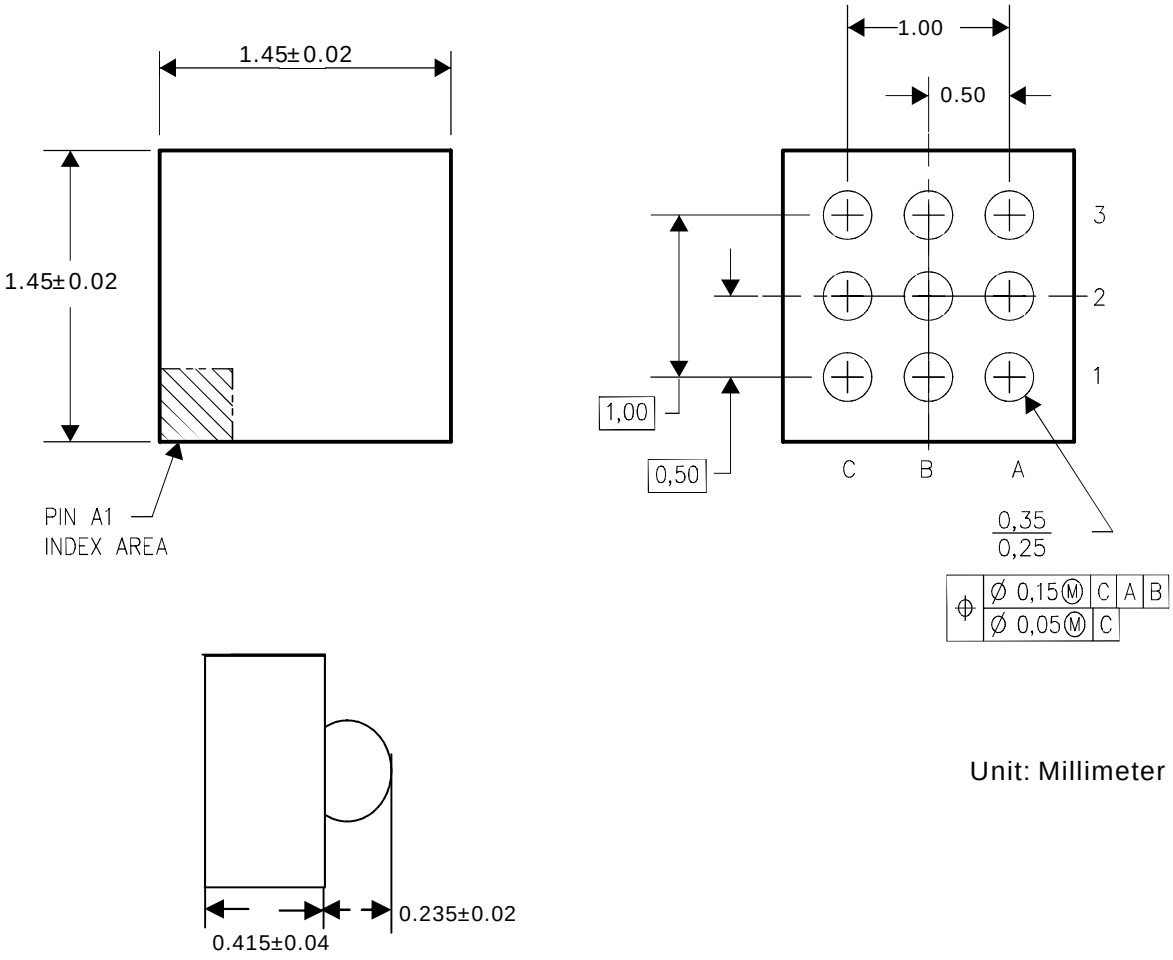
- Number of pins
- Package Type
- Pin Configuration

Pin Configuration	Package Type	Number of pins
A: A1: IN+ A2: VDD A3: OUT+ B1: AGND B2: VREF B3: PGND C1: IN- C2: CTRL C3: OUT- B: 1: CTRL 2: V_{REF} 3: IN+ 4: IN- 5: OUT 6: $\overline{VDD}$ 7: GND 8: OUT-	Z: WCSP S: MSOP	C: 8 N: 9

Part Number	Marking	Package Type	MOQ
PAM8002AZN	BF YW	WCSP 9	3,000 Units/ Tape & Reel
PAM8002BSC	P8002 XXXXYW	MSOP-8L	2,500 Units/ Tape & Reel

Outline Dimensions

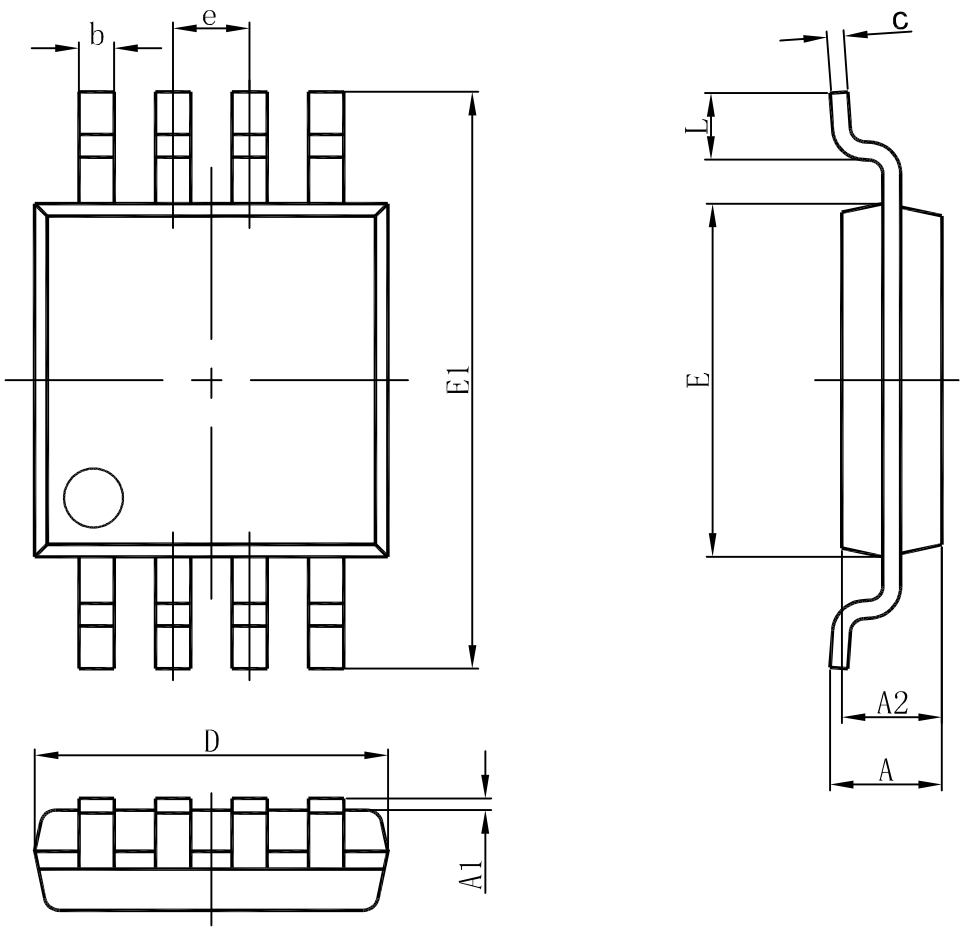
WCSP



Unit: Millimeter

Outline Dimensions

MSOP8



REF	Millimeter	
	Min	Max
A	--	1.10
A1	0.05	0.15
A2	0.78	0.94
b	0.22	0.38
c	0.08	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.75	5.05
e	0.65BSC	
L	0.40	0.70