HH1621

32 x 4 LCD Driver

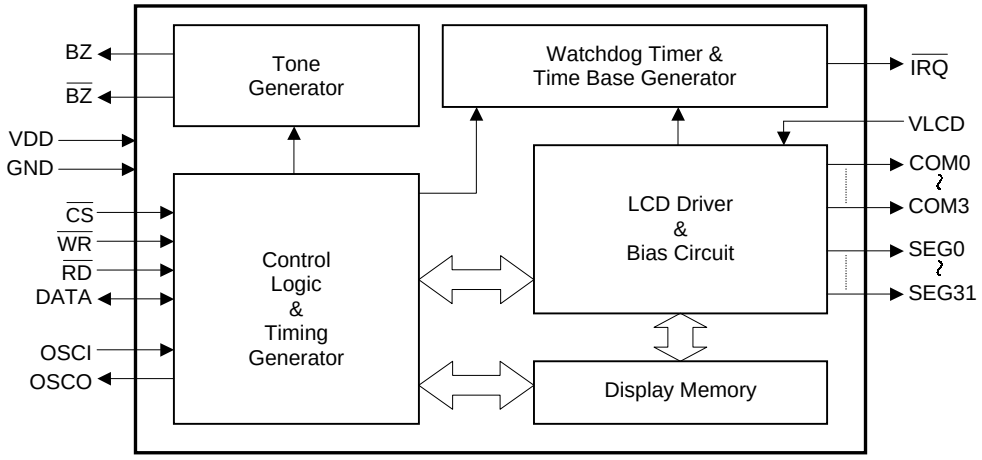
Features

- _ Operating voltage: 2.2V~5.2V
- _ Built-in 256kHz RC oscillator
- _ External 32.768kHz crystal or 256kHz frequency source input
- _ Selection of 1/2, 1/3 bias, and selection of 1/2, 1/3, 1/4 duty LCD applications
- _ Internal time base frequency sources
- _ Two selectable buzzer frequencies (2/4kHz)
- _ Built-in time base generator and WDT
- _ Time base or WDT overflow output
- _ Power down command available
- _ 8 kinds of time base/WDT clock sources
- _ Built-in 32x4 bit display RAM
- _ 3-wire serial interface.
- _ Internal LCD driving frequency source
- _ Software configuration
- _ Data mode and command mode instructions
- _ R/W address auto increment
- _ Three data accessing modes
- _ VLCD pin for adjusting LCD operating voltage

General Descriptions

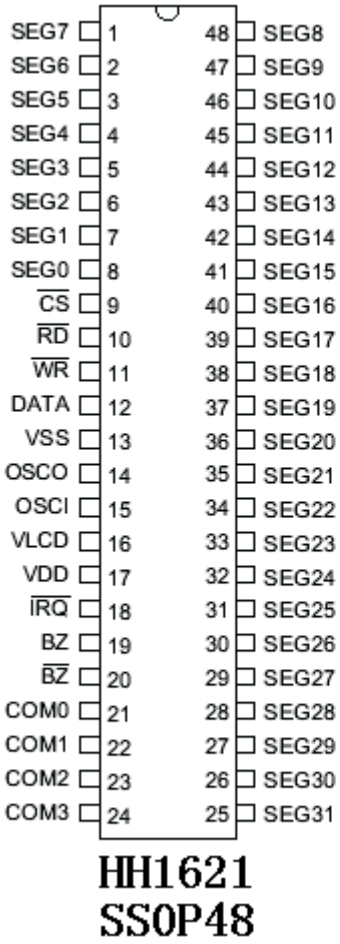
The HH1621 is a 128-pattern (32x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the HH1621 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the HH1621. The HH1621 contains a power down command to reduce power consumption.

Block Diagram

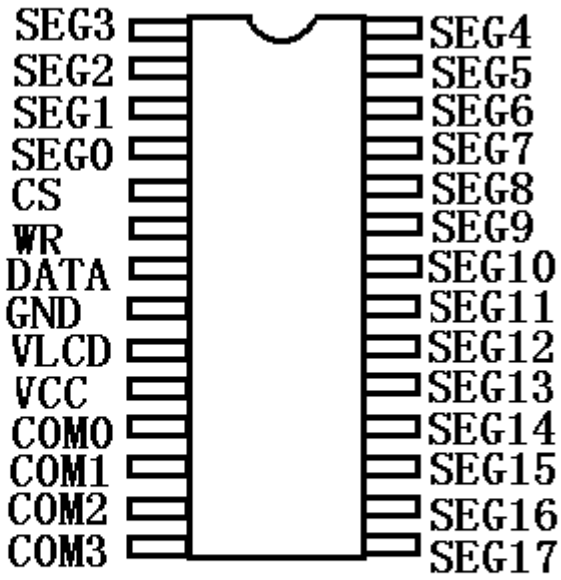


Note: $\overline{CS}$: Chip selection
BZ, $\overline{BZ}$: Tone outputs
$\overline{WR}$, $\overline{RD}$, DATA: Serial interface
$\overline{IRQ}$: Time base or WDT overflow output
COM0~COM3, SEG0~SEG31: LCD outputs

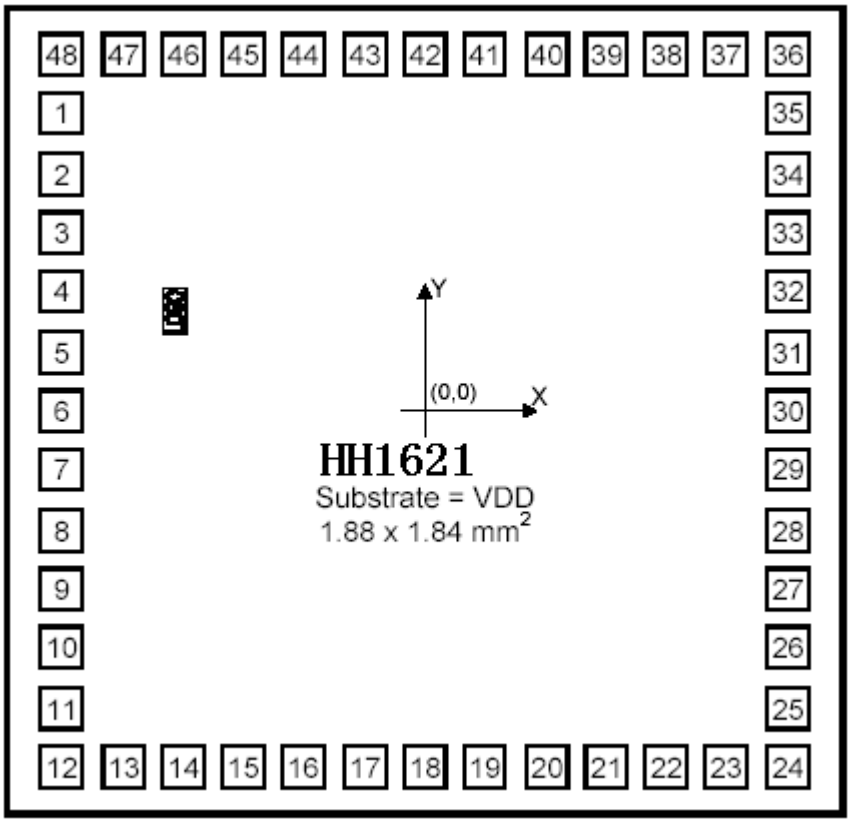
Pin Assignment



HH1621
SSOP48



HH28A1621
SDIP28
SOP28



Pad Assignment

Pad Coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	$\overline{CS}$	-960	1,039	17	SEG31	132	-1,039	33	SEG15	1,008	1,039
2	$\overline{RD}$	-1,019	415	18	SEG30	252	-1,039	34	SEG14	889	1,039
3	$\overline{WR}$	-1,019	295	19	SEG29	371	-1,039	35	SEG13	770	1,039
4	DATA	-1,019	109	20	SEG28	1,019	-1,028	36	SEG12	650	1,039
5	GND	-1,019	-16	21	SEG27	1,019	-909	37	SEG11	531	1,039
6	OSCO	-1,019	-135	22	SEG26	1,019	-789	38	SEG10	411	1,039
7	OSCI	-1,019	-624	23	SEG25	1,019	-670	39	SEG9	292	1,039
8	VLCD	-1,019	-746	24	SEG24	1,019	-551	40	SEG8	173	1,039
9	VDD	-1,019	-867	25	SEG23	1,019	-431	41	SEG7	53	1,039
10	$\overline{IRQ}$	-1,019	-1,039	26	SEG22	1,019	-312	42	SEG6	-66	1,039
11	BZ	-785	-1,039	27	SEG21	1,019	-192	43	SEG5	-185	1,039
12	$\overline{BZ}$	-577	-1,039	28	SEG20	1,019	-73	44	SEG4	-305	1,039
13	COM0	-392	-1,039	29	SEG19	1,019	46	45	SEG3	-424	1,039
14	COM1	-273	-1,039	30	SEG18	1,019	166	46	SEG2	-544	1,039
15	COM2	-141	-1,039	31	SEG17	1,019	284	47	SEG1	-663	1,039
16	COM3	-22	-1,039	32	SEG16	1,019	402	48	SEG0	-782	1,039

(Unit: µm)

Pad Descriptions

Pad No.	Pad Name	I/O	Function
1	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the HH1621 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HH1621 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the A3001NCE are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the HH1621 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with pull-high resistor
5	GND	—	Negative power supply, ground
6	OSCO	O	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if and on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
7	OSCI	I	
8	VLCD	I	LCD power input
9	VDD	—	Positive power supply
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
11,12	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
13~16	COM0~COM3	O	LCD common outputs
48~17	SEG0~SEG31	O	LCD segment outputs

Absolute Maximum Ratings

Supply Voltage……..……-0.3V ~ 5.5V
Input Voltage…… GND - 0.3V ~ V_{DD} + 0.3V
Storage Temperature……-50°C ~ 125°C
Operating Temperature……..-25°C ~ 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	150	325	μA
		5V		—	350	725	μA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	150	250	μA
		5V		—	225	475	μA
I_{DD3}	Operating Current	3V	No load/LCD ON External clock source	—	150	275	μA
		5V		—	275	500	μA
I_{STB}	Standby Current	3V	No load Power down mode	—	0.1	5	μA
		5V		—	0.3	10	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I_{OL1}	DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.5	1.2	—	mA
		5V	V_{OL}=0.5V	1.3	2.6	—	mA
I_{OH1}	DATA, BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	-0.4	-0.8	—	mA
		5V	V_{OH}=4.5 V	-0.9	-1.8	—	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	150	—	μA
		5V	V_{OL}=0.5V	150	250	—	μA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	-80	-120	—	μA
		5V	V_{OH}=4.5 V	-120	-200	—	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	60	120	—	μA
		5V	V_{OL}=0.5V	120	200	—	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	-40	-70	—	μA
		5V	V_{OH}=4.5 V	-70	-100	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	40	80	150	kΩ
		5V		30	60	100	kΩ

A.C. Characteristics

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	—	256	—	kHz
		5V		—	256	—	kHz
f_{SYS2}	System Clock	3V	Crystal oscillator	—	32.768	—	kHz
		5V		—	32.768	—	kHz
f_{SYS3}	System Clock	3V	External clock source	—	256	—	kHz
		5V		—	256	—	kHz
f_{LCD}	LCD Clock	—	On-chip RC oscillator	—	$F_{SYS1}/1024$	—	Hz
			Crystal oscillator	—	$F_{SYS2}/128$	—	Hz
			External clock source	—	$F_{SYS3}/1024$	—	Hz
t_{COM}	LCD Common Period		n: Number of COM	—	n/f_{LCD}	—	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	—		150	kHz
		5V		—		300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—		75	kHz
		5V		—		150	kHz
f_{TONE}	Tone Frequency		On-chip RC oscillator	—	2.0 or 4.0	—	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	3V	$\overline{CS}$	—	250	—	ns
		5V					
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	µs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	—	µs
			Read mode	3.34	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	3V	—	—	120	—	ns
		5V					
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					

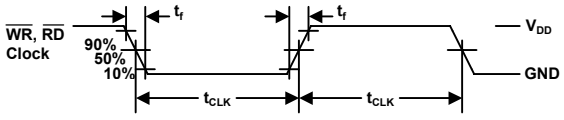


Figure 1

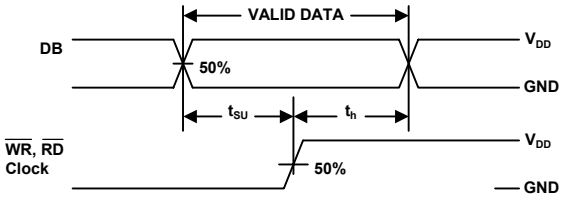


Figure 2

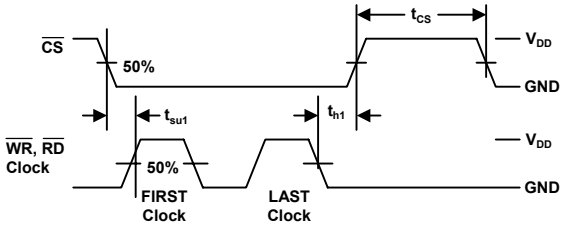


Figure 3

Functional Description

Display memory – RAM

The static display memory (RAM) is organized into 32x4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0	
SEG0					0
SEG1					1
SEG2					2
SEG3					3
SEG31					31
	D3	D2	D1	D0	Data / Addr

Address 6 bits
(A5, A4, …, A0)

Data 4 bits
(D3, D2, D1, D0)

RAM mapping

System oscillator

The HH1621 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the HH1621 is at the SYS DIS state.

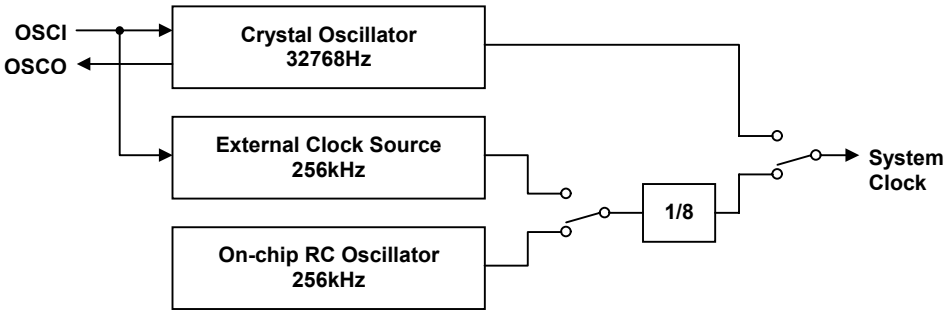
Time base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of and 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of and internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

$$f_{WDT} = \frac{32kHz}{2^n}$$

Where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the base time generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be



System oscillator configuration

executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of sys tem frequency the SYS DIS command

Name	Command Code	Function
LCD OFF	1 0 0 0 0 0 0 0 0 1 0 X	Turn off LCD outputs
LCD ON	1 0 0 0 0 0 0 0 0 1 1 X	Turn on LCD outputs
BIAS & COM	1 0 0 0 0 1 0 a b X c X	c=0:1/2 bias option
		c=1:1/3 bias option
		ab=00:2 commons option
		ab=01:3 commons option
		ab=10:4 commons option

turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the HH1621 will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.

Tone output

A simple tone generator is implemented in the HH1621. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, area pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ output will remain at low level.

LCD driver

The HH1621 is a 128 (32x4) patterns LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the HH1621suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 100, namely 100, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands; the HH1621 can be compatible with most types of LCD panels.

Command format

The HH1621 can be configured by the S/W setting. There are two mode commands to configure the HH1621 resources and to transfer the LCD display data. The configuration mode of the HH1621 is called command mode, and its command mode IC is 100. The command mode consists of system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode Ids and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

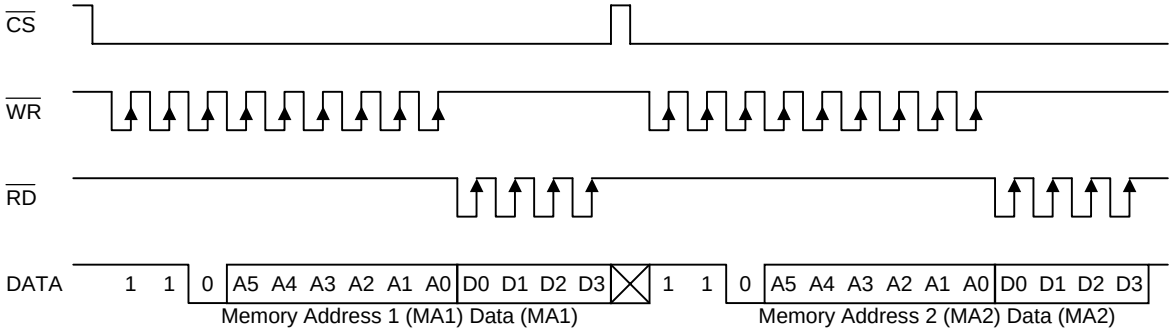
The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 100, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. Once the $\overline{CS}$ pin returns to "0" a new operation mode ID should be issued first.

Interfacing

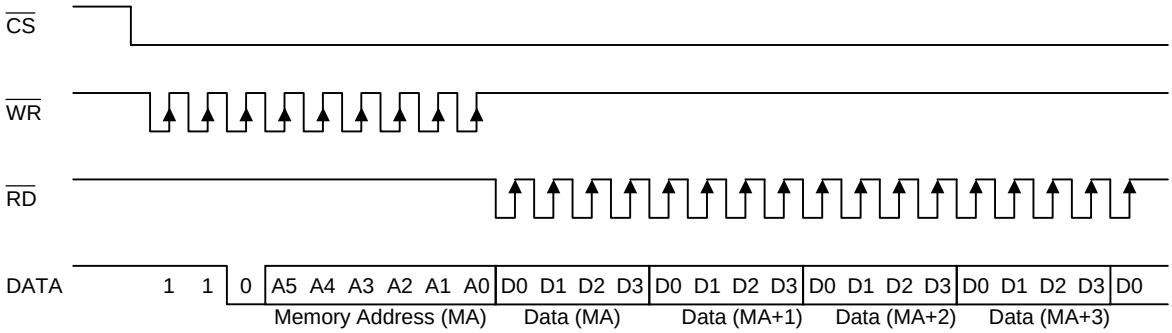
Only four lines are required to interface with the HH1621. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HH1621. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the HH1621 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HH1621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HH1621 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the HH1621. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the HH1621

Timing Diagrams

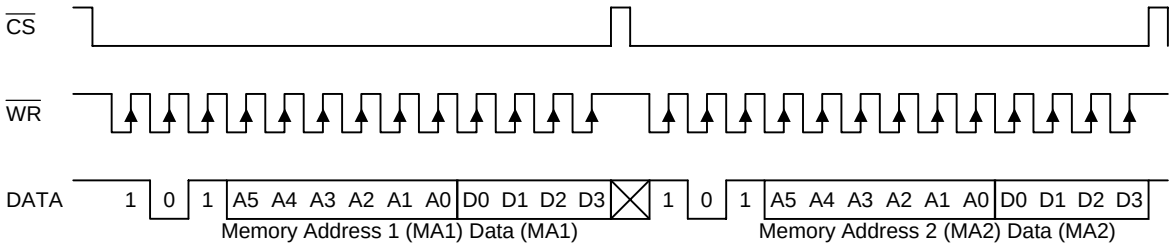
*READ mode (command code: **1 1 0**)*



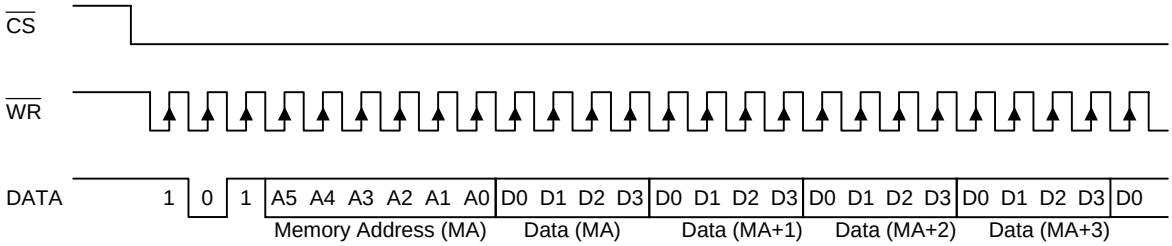
READ mode (successive address reading)



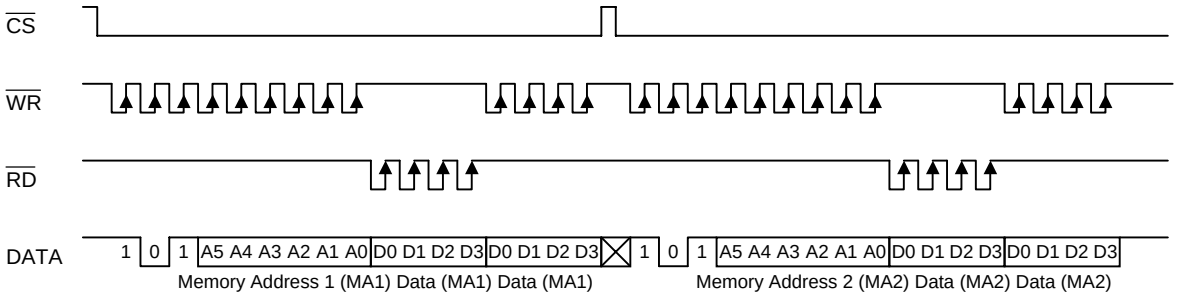
*WRITE mode (command code: **1 0 1**)*



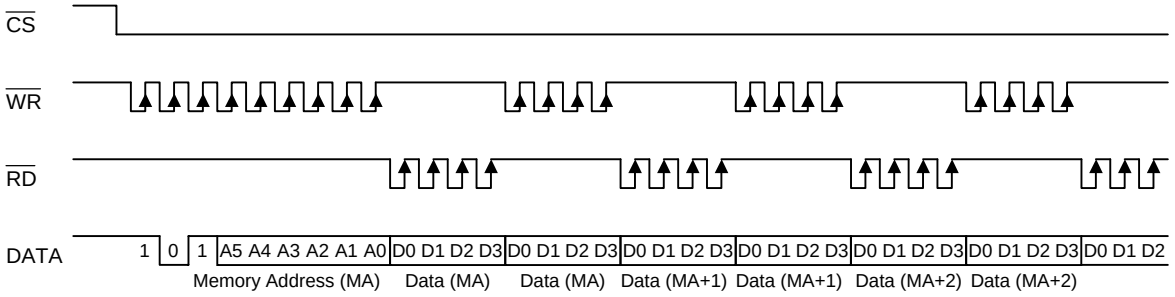
WRITE mode (successive address writing)



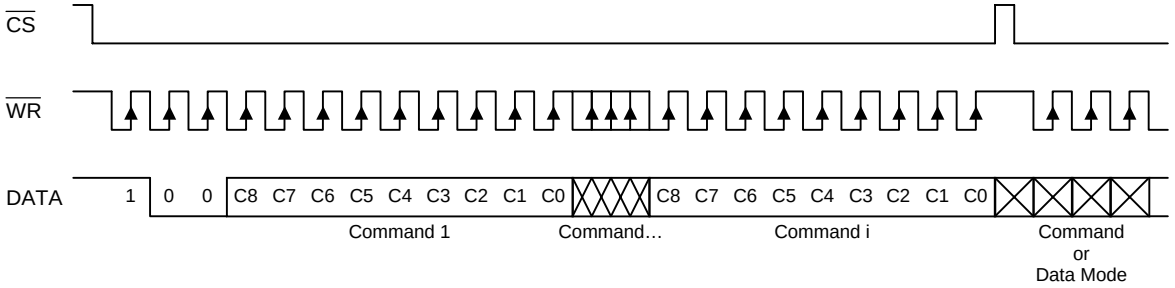
*READ-MODIFY-WRITE mode (command code: **1 0 1**)*



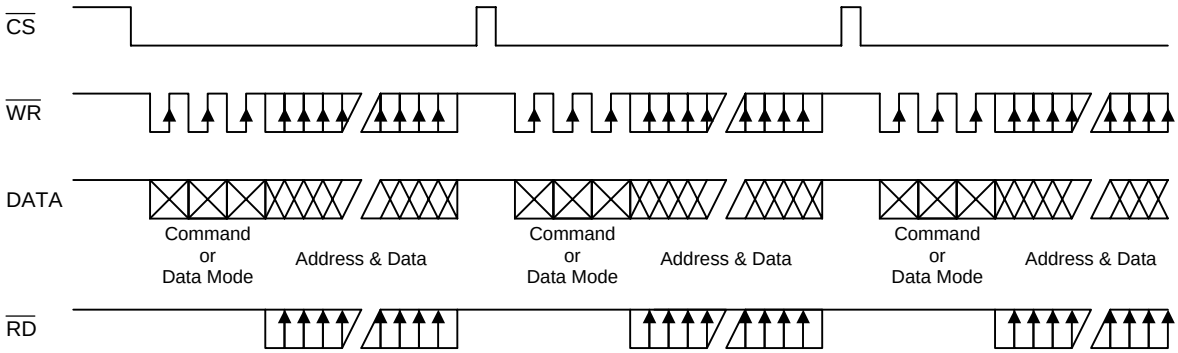
READ-MODIFY-WRITE mode (successive address accessing)



*Command mode (command code: **1 0 0**)*



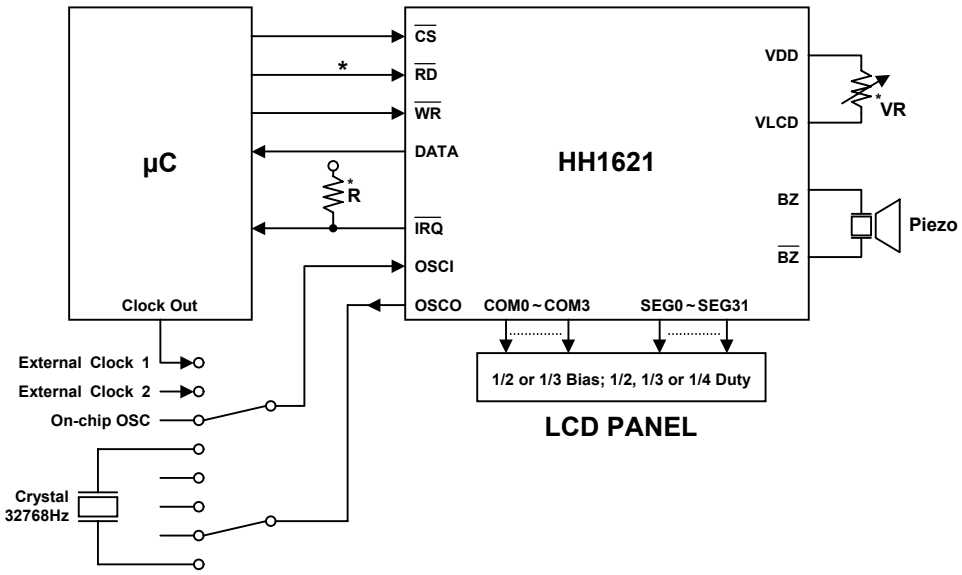
Mode (data and command mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the $\overline{RD}$ line and the falling edge of the next $\overline{RD}$ line.

Application Circuits

Host controller with a HH1621 display system



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the µC.

The voltage applied to V_{LCD} pin must be lower than V_{DD}.

Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=2.5kΩ±20%

Adjust R (external pull-high resistance) to fit user's time base clock.

Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LEC OFF	1 0 0	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	1 0 0	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	1 0 0	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	1 0 0	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	1 0 0	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	1 0 0	0001-10XX-X	C	System clock source, external clock source	Yes
EXT 256K	1 0 0	0001-11XX-X	C	System clock source, external clock source	
BLAS 1/2	1 0 0	0010-abX0-X	C	LCD 1/2 bias option ab=00:2 commons option ab=01:3 commons option ab=10:4 commons option	
BLAS 1/3	1 0 0	0010-abX1-X	C	LCD 1/3 bias option ab=00:2 commons option ab=01:3 commons option ab=10:4 commons option	
TONE 4K	1 0 0	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	1 0 0	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$ DIS	1 0 0	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	1 0 0	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	1 0 0	101X-X000-X	C	Time base/WDT clock Output: 1Hz The WDT time-out flag after: 4s	
F2	1 0 0	101X-X001-X	C	Time base/WDT clock Output: 2Hz The WDT time-out flag after: 2s	
F4	1 0 0	101X-X010-X	C	Time base/WDT clock Output: 4Hz	

Name	ID	Command Code	D/C	Function	Def.
				The WDT time-out flag after: 1s	
F8	1 0 0	101X-X011-X	C	Time base/WDT clock Output: 8Hz The WDT time-out flag after: 1/2s	
F16	1 0 0	101X-X100-X	C	Time base/WDT clock Output: 16Hz The WDT time-out flag after: 1/4s	
F32	1 0 0	101X-X101-X	C	Time base/WDT clock Output: 32Hz The WDT time-out flag after: 1/8s	
F64	1 0 0	101X-X110-X	C	Time base/WDT clock Output: 64Hz The WDT time-out flag after: 1/16s	
F128	1 0 0	101X-X111-X	C	Time base/WDT clock Output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	1 0 0	1110-0000-X	C		
NORMAL	1 0 0	1110-0011-X	C		Yes

Note: X: Don’t care

A5~A0: RAM addresses

D3~D0: RAM data

D/C: Data/command mode

Def.: Power on reset default

All the bold forms, namely 1 1 0, 1 0 1, and 1 0 0, are mode commands. Of these, 1 0 0 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HH1621 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HH1621

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