Feature

- Operating voltage: 2.4V~5.5V
- Internal 32kHz RC oscillator
- Bias: 1/3 or 1/4; Duty: 1/4 or 1/8
- Internal LCD bias generation with voltage-follower buffers
- I^2C interface
- Two selectable LCD frame frequencies: 80Hz or 160Hz
- Up to 16×8 bits RAM for display data storage
- Display patterns:
  – 20×4 patterns: 20 segments and 4 commons
  – 16×8 patterns: 16 segments and 8 commons
- Versatile blinking modes
- R/W address auto increment
- Internal 16-step voltage adjustment to adjust LCD operating voltage
- Low power consumption
- Provides V_{LCD} pin to adjust LCD operating voltage
- Manufactured in silicon gate CMOS process
- Package Type: 20/24/28-pin SOP, 16 NSOP and Chip.

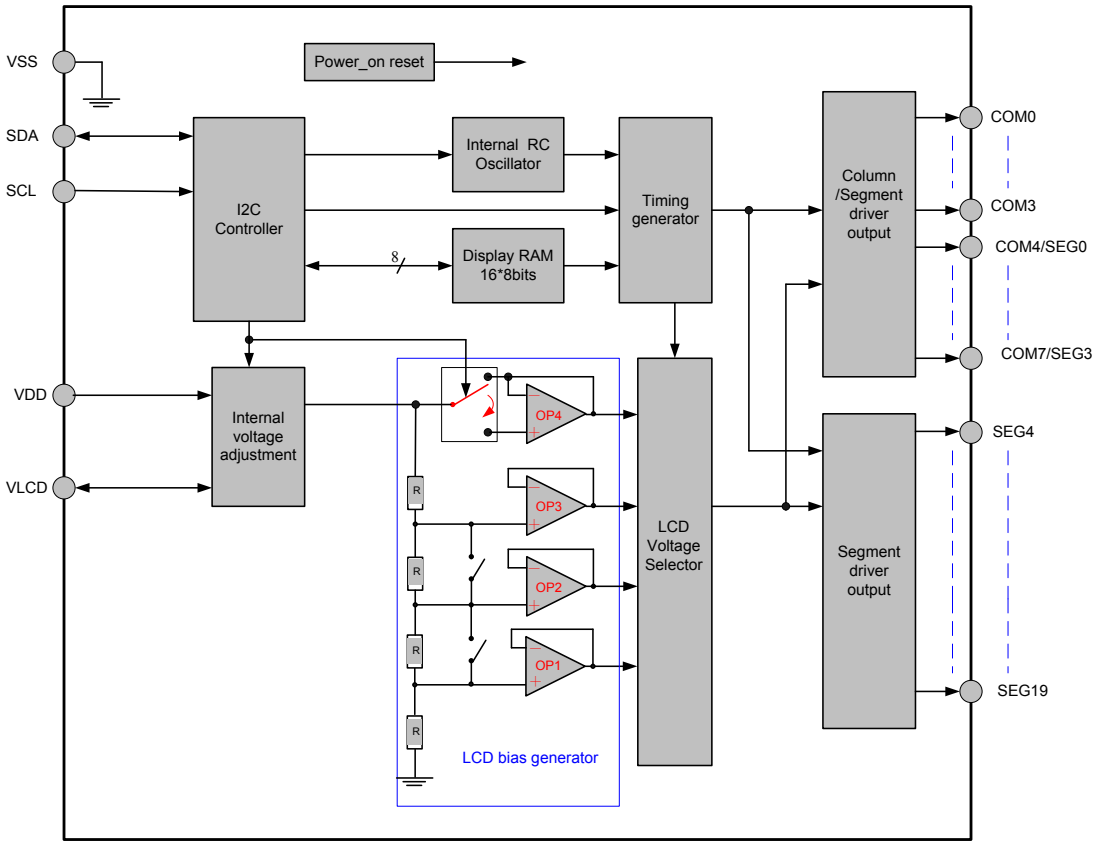
Applications

- Electronic meter
- Water meter
- Gas meter
- Heat energy meter
- Household appliance
- Games
- Telephone
- Consumer electronics

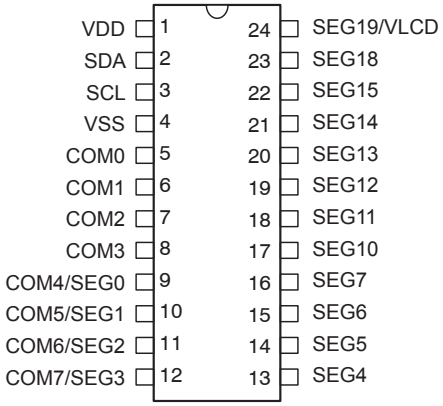
General Description

The HT16C21 device is a memory mapping and multi-function LCD controller/driver. The display segments of the device are 80 patterns (20 segments and 4 commons) or 128 patterns (16 segments and 8 commons). The software configuration feature of the HT16C21 device makes it suitable for multiple LCD applications including LCD modules and display subsystems. The HT16C21 device communicates with most microprocessors/microcontrollers via a two-line bidirectional I^2C interface.

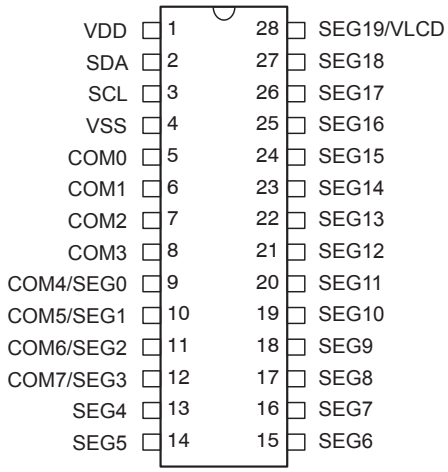
Block Diagram



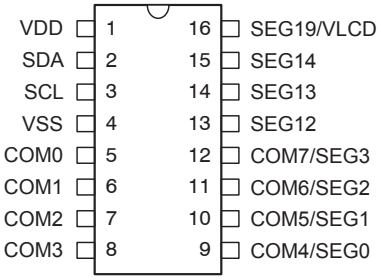
Pin Assignment



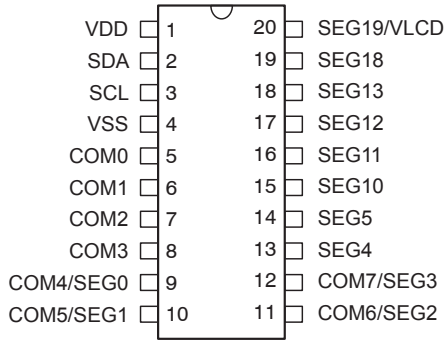
HT16C21
24 SOP-A



HT16C21
28 SOP-A

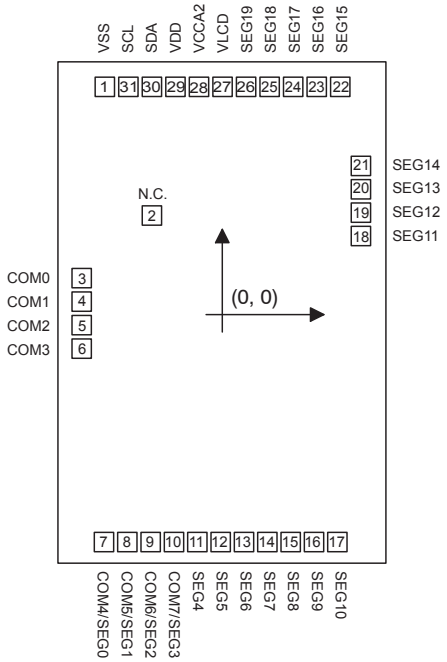


HT16C21
16 NSOP-A



HT16C21
20 SOP-A

Pad assignment for COB



Chip size: 1200 × 1846μm^2

Note: 1. The IC substrate should be connected to V_{SS} in the PCB layout artwork.
2. VDD (Pad29) and VCCA2 (Pad28) must be bonded together.
3. VLCD (Pad27) and SEG19 (Pad26) must be bonded together.

Pad Coordinates for COB

Unit: μm

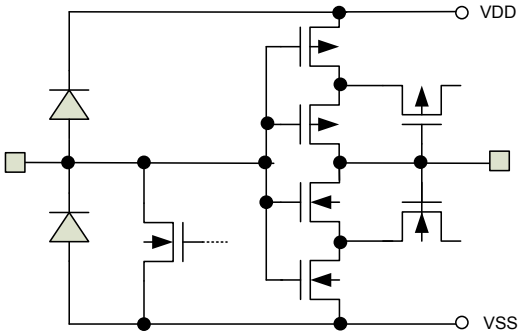
No	Name	X	Y	No	Name	X	Y
1	VSS	-423.6	819.9	17	SEG10	426.1	-825
2	N.C.	-251.74	351.435	18	SEG11	502	279.599
3	COM0	-502	134.752	19	SEG12	502	364.599
4	COM1	-502	49.752	20	SEG13	502	449.599
5	COM2	-502	-35.248	21	SEG14	502	534.599
6	COM3	-502	-120.248	22	SEG15	426.4	819.9
7	COM4/SEG0	-426.4	-825	23	SEG16	341.4	819.9
8	COM5/SEG1	-341.4	-825	24	SEG17	256.4	819.9
9	COM6/SEG2	-256.4	-825	25	SEG18	171.4	819.9
10	COM7/SEG3	-171.4	-825	26	SEG19	86.4	819.9
11	SEG4	-83.9	-825	27	VLCD	1.4	819.9
12	SEG5	1.1	-825	28	VCCA2	-83.6	819.9
13	SEG6	86.1	-825	29	VDD	-168.6	819.9
14	SEG7	171.1	-825	30	SDA	-253.6	819.9
15	SEG8	256.1	-825	31	SCL	-338.6	819.9
16	SEG9	341.1	-825				

Pin Description

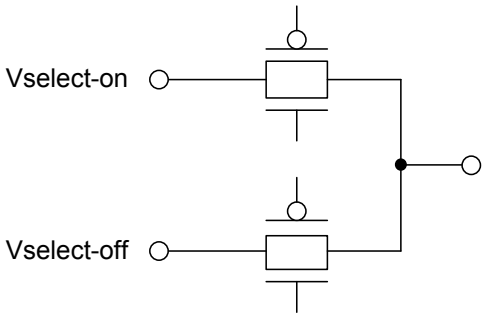
Pin Name	Type	Description
SDA	I/O	Serial data input/output for I²C interface
SCL	I	Serial clock input for I²C interface
VDD	—	Positive power supply.
VSS	—	Negative power supply, ground.
VLCD	—	• One external resistor is connected between the VLCD pin and the VDD pin to determine the bias voltage for the package with a VLCD pin. Internal voltage adjustment function is disabled. • Internal voltage adjustment function can be used to adjust the V_{LCD} voltage. If the VLCD pin is used as voltage detection pin, an external power supply should not be applied to the VLCD pin. • An external MCU can detect the voltage of the VLCD pin and program the internal voltage adjustment for the packages with a VLCD pin.
COM0~COM3	O	LCD common outputs.
COM4/SEG0~COM7/SEG3	O	LCD common/segment multiplexed driver outputs
SEG4~SEG19	O	LCD segment outputs.

Approximate Internal Connections

SCL, SDA (for schmit Trigger type)



COM0~COM7; SEG0~SEG19



Absolute Maximum Ratings

Supply voltage ..... V_{SS}−0.3V to V_{SS}+6.5V
Input voltage ..... V_{SS}−0.3V to V_{DD}+0.3V
Storage temperature .....-55°C to +150°C
Operating temperature .....-40°C to +85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{SS} = 0V; V_{DD} = 2.4 to 5.5V; Ta =-40~85°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	Operating Voltage	—	—	—	—	V_{DD}	V
I_{DD}	Operating Current	3V	No load, V_{LCD}=V_{DD}, 1/3bias, f_{LCD}=80Hz, LCD display on, internal system oscillator on, DA0~DA3 are set to "0000"	—	18	27	μA
		5V		—	25	40	μA
I_{DD1}	Operating Current	3V	No load, V_{LCD}=V_{DD}, 1/3bias f_{LCD}=80Hz, LCD display off, internal system oscillator on, DA0~DA3 are set to "0000"	—	2	5	μA
		5V		—	4	10	μA
I_{STB}	Standby Current	3V	No load, V_{LCD}=V_{DD}, LCD display off, internal system oscillator off	—	—	1	μA
		5V		—	—	2	μA
V_{IH}	Input High Voltage	—	SDA ,SCL	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input Low Voltage	—	SDA, SCL	0	—	0.3V_{DD}	V
I_{IL}	Input Leakage Current	—	V_{IN} = V_{SS} or V_{DD}	-1	—	1	μA
I_{OL}	Low Level Output Current	3V	V_{OL}=0.4V SDA	3	—	—	mA
		5V		6	—	—	mA
I_{OL1}	LCD COM Sink Current	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	—	μA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH1}	LCD COM Source Current	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA
I_{OL2}	LCD SEG Sink Current	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	—	μA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH2}	LCD SEG Source Current	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA

A.C. Characteristics

V_{SS} = 0V; V_{DD} = 2.4 to 5.5V; Ta =-40~85°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{LCD1}	LCD Frame Frequency	4V	1/4duty, Ta =25°C	72	80	88	Hz
f_{LCD2}	LCD Frame Frequency	4V	1/4duty, Ta =25°C	144	160	176	Hz
f_{LCD3}	LCD Frame Frequency	4V	1/4duty, Ta=- 40 to +85°C	52	80	124	Hz
f_{LCD4}	LCD Frame Frequency	4V	1/4duty, Ta=-40 to +85°C	104	160	248	Hz
t_{OFF}	V_{DD} Off Times	—	V_{DD} drop down to 0V	20	—	—	ms
t_{SR}	V_{DD} Slew Rate	—	—	0.05	—	—	V/ms

Note: 1. If the conditions of Power on Reset timing are not satisfied during the power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. If the V_{DD} voltage drops below the minimum voltage of operating voltage spec. during operating, the Power on Reset timing conditions must also be satisfied. That is, the V_{DD} voltage must drop to 0V and remain at 0V for 20ms (min.) before rising to the normal operating voltage.

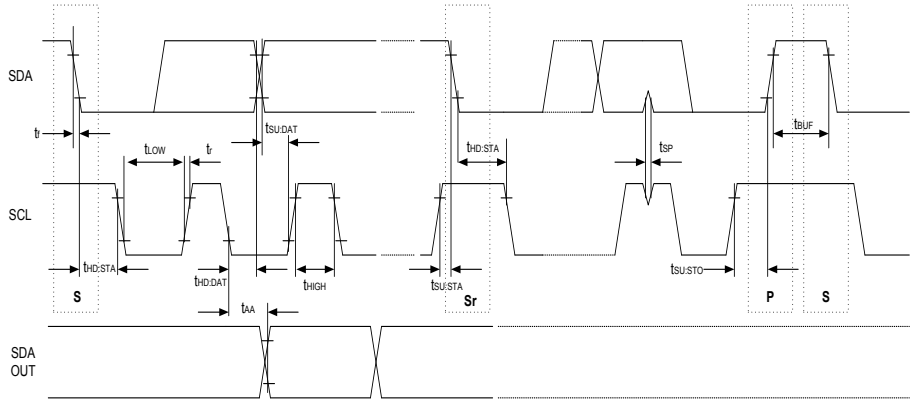
A.C. Characteristics – I²C Interface

Symbol	Parameter	Condition	V_{DD}=2.4V to 5.5V		V_{DD}=3.0V to 5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	kHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD: STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	4	—	0.6	—	μs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High Time	—	4	—	0.6	—	μs
$t_{SU: STA}$	Start Condition Setup Time	Only relevant for repeated START condition	4.7	—	0.6	—	μs
$t_{HD: DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU: DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R	SDA and SCL Rise Time	Note	—	1	—	0.3	μs
t_F	SDA and SCL Fall Time	Note	—	0.3	—	0.3	μs
$t_{SU: STO}$	Stop Condition Set-up Time	—	4	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns

Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

I²C Timing



Reset Timing

Functional Description

Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common/segment outputs are set to V_{LCD}.
- The drive mode 1/4 duty output and 1/3 bias is selected.
- The System Oscillator and the LCD bias generator are off state.
- LCD Display is off state.
- Internal voltage adjustment function is enabled.
- The Segment / VLCD shared pin is set as the Segment pin.
- Detection switch for the VLCD pin is disabled.
- Frame Frequency is set to 80Hz.
- Blinking function is switched off.

Data transfers on the I^2C interface should be avoided for 1 ms following power-on to allow completion of the reset action.

Display Memory – RAM Structure

The display RAM is static 16×8-bits RAM which stores the LCD data. Logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly, logic 0 indicates the 'off' state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the segments operated with respect to COM0. In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with COM1, COM2 and COM3 respectively. The following is a mapping from the RAM data to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
SEG13					SEG12					06H
SEG15					SEG14					07H
SEG17					SEG16					08H
SEG19					SEG18					09H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

RAM mapping of 20×4 display mode

Output	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	address
SEG4									00H
SEG5									01H
SEG6									02H
SEG7									03H
SEG8									04H
SEG9									05H
SEG10									06H
SEG11									07H
SEG12									08H
SEG13									09H
SEG14									0AH
SEG15									0BH
SEG16									0CH
SEG17									0DH
SEG18									0EH
SEG19									0FH
	D7	D6	D5	D4	D3	D2	D1	D0	Data

RAM mapping of 16×8 display mode

	MSB							LSB
LCD	D7	D6	D5	D4	D3	D2	D1	D0
LED	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0

Display data transfer format for I^2C interface

System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The System Clock frequency (f_{SYS}) determines the LCD frame frequency. During initial system power on the System Oscillator will be in the stop state.

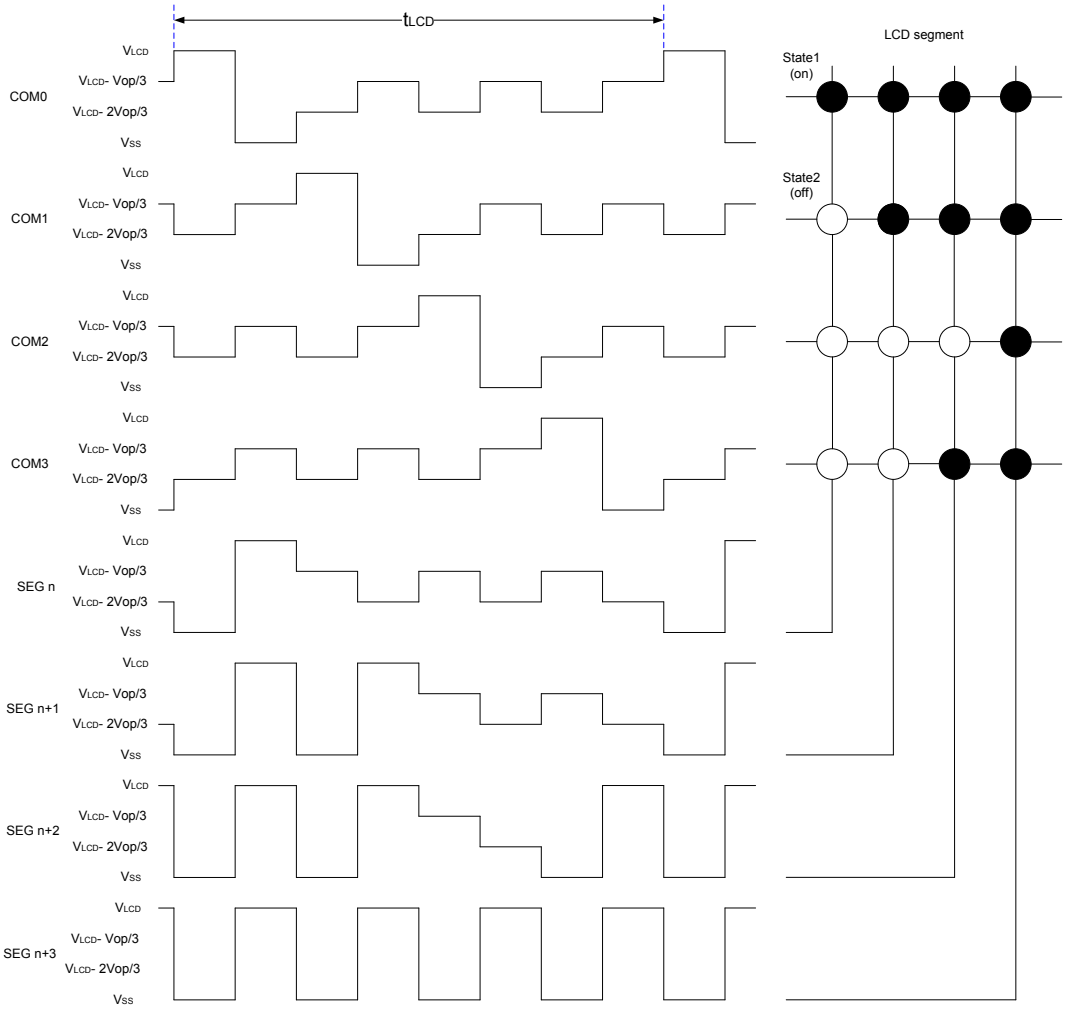
LCD Bias Generator

The full-scale LCD voltage (V_{OP}) is obtained from (V_{LCD} – V_{SS}). The LCD voltage may be temperature compensated externally through the Voltage supply to the V_{LCD} pin.

Fractional LCD biasing voltages, known as 1/3 or 1/4 bias voltage, are obtained from an internal voltage divider of four series resistors connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of circuits to provide a 1/3bias voltage level configuration.

LCD Drive Mode Waveforms

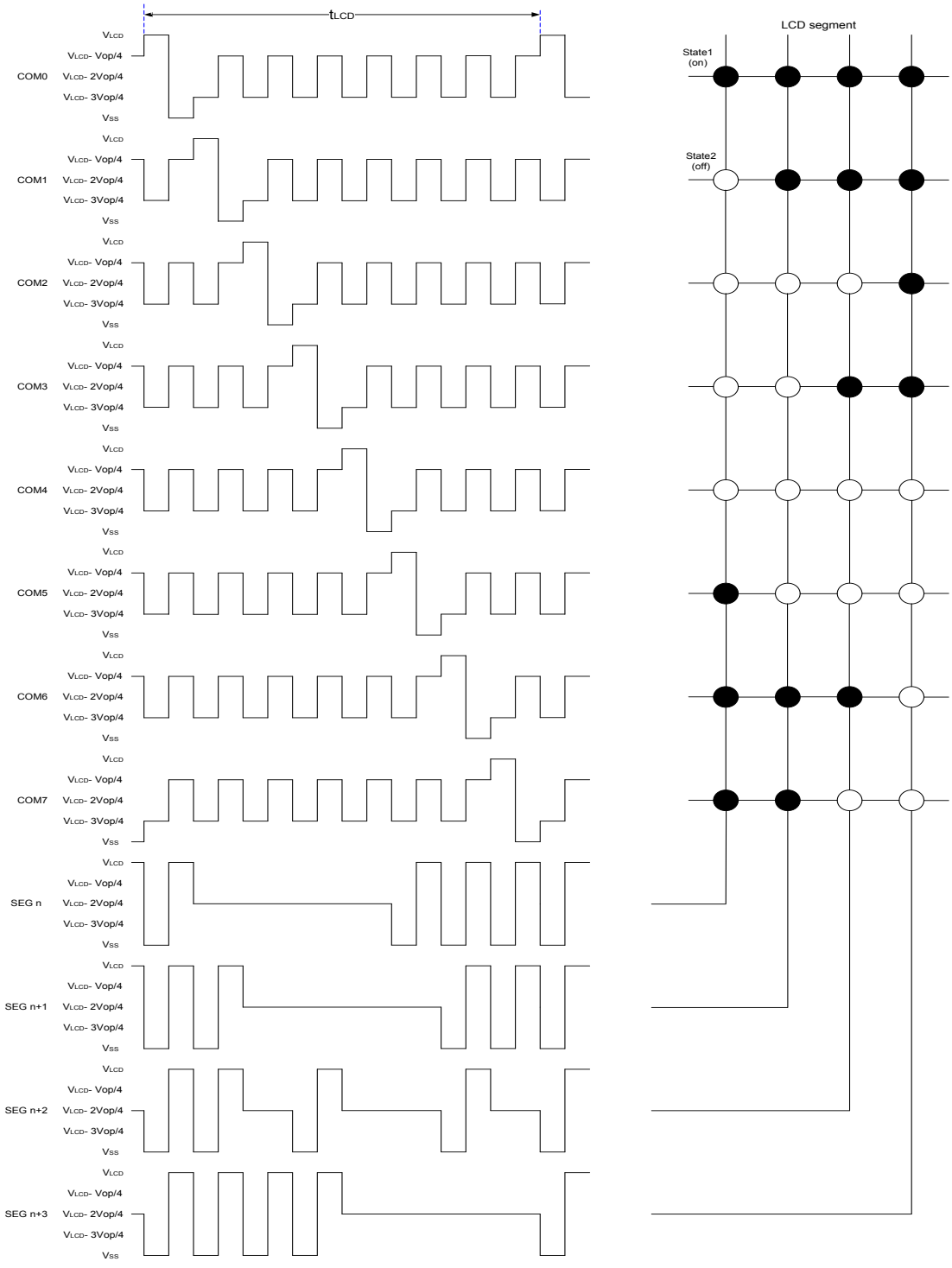
- When the LCD drive mode is selected as 1/4 duty and 1/3 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 duty drive mode with 1/3 bias (V_{OP} = V_{LCD}-V_{SS})

Note: $t_{LCD} = 1/f_{LCD}$

- When the LCD drive mode is selected as 1/8 duty and 1/4bias, the waveform and LCD display is shown as follows:



Waveforms for 1/8 duty drive mode with1/4 bias ($V_{OP} = V_{LCD} - V_{SS}$)

Note: $t_{LCD} = 1/f_{LCD}$

Segment Driver Outputs

The LCD drive section includes 20 segment outputs SEG0 ~ SEG19 or 16 segment outputs SEG4 ~ SEG19 which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit when less than 20 or 16 segment outputs are required.

Column Driver Outputs

The LCD drive section includes 4 column outputs COM0~COM3 or 8 column outputs COM0~COM7 which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit if less than 4 or 8 column outputs are required.

Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Address pointer command.

Blinker Function

The device contains versatile blinking capabilities. The whole display can be blinked at frequencies selected by the Blink command. The blinking frequency is a subdivided ratio of the system frequency. The ratio between the system oscillator and blinking frequencies depends on the blinking mode in which the device is operating, as shown in the following table:

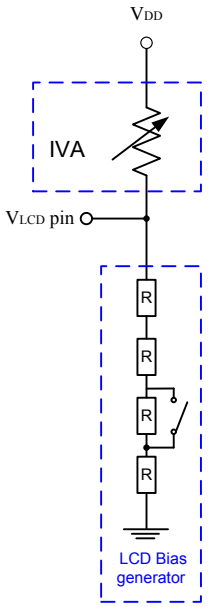
Blinking Mode	Operating Mode Ratio	Blinking Frequency (Hz)
0	0	Blink off
1	f_{SYS} / 16384Hz	2
2	f_{SYS} / 32768Hz	1
3	f_{SYS} / 65536Hz	0.5

Frame Frequency

The HT16C21 device provides two frame frequencies selected with Mode set command known as 80Hz and 160Hz respectively.

Internal VLCD Voltage Adjustment

- The internal V_{LCD} adjustment contains four resistors in series and a 4-bit programmable analog switch which can provide sixteen voltage adjustment options using the V_{LCD} voltage adjustment command.
- The internal V_{LCD} adjustment structure is shown in the diagram:



- The relationship between the programmable 4-bit analog switch and the V_{LCD} output voltage is shown in the table:

Bias / DA3~DA0	1/3	1/4	Note
00H	1.000*V_{DD}	1.000*V_{DD}	Default value
01H	0.944*V_{DD}	0.957*V_{DD}	
02H	0.894*V_{DD}	0.918*V_{DD}	
03H	0.849*V_{DD}	0.882*V_{DD}	
04H	0.808*V_{DD}	0.849*V_{DD}	
05H	0.771*V_{DD}	0.818*V_{DD}	
06H	0.738*V_{DD}	0.789*V_{DD}	
07H	0.707*V_{DD}	0.763*V_{DD}	
08H	0.678*V_{DD}	0.738*V_{DD}	
09H	0.652*V_{DD}	0.714*V_{DD}	
0AH	0.628*V_{DD}	0.692*V_{DD}	
0BH	0.605*V_{DD}	0.672*V_{DD}	
0CH	0.584*V_{DD}	0.652*V_{DD}	
0DH	0.565*V_{DD}	0.634*V_{DD}	
0EH	0.547*V_{DD}	0.616*V_{DD}	
0FH	0.529*V_{DD}	0.600*V_{DD}	

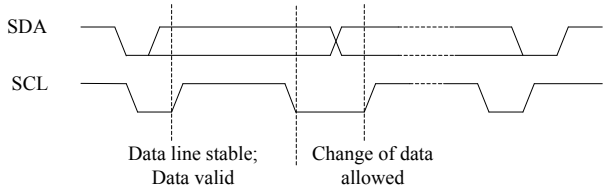
I²C Serial Interface

I²C Operation

The device supports I²C serial interface. The I2C interface is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7KΩ. When the I²C interface is free, both lines are high. Devices connected to the I²C interface must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the I²C interface is not busy.

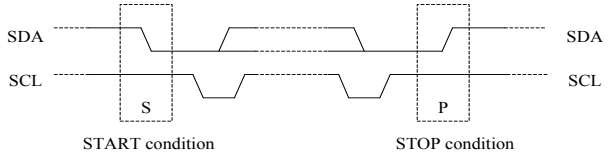
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low as shown in the diagram.



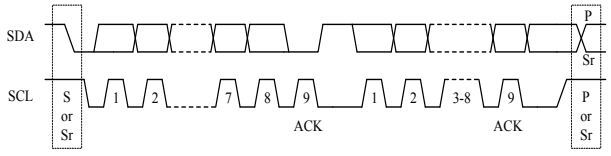
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The I²C interface is considered to be busy after the START condition. The I2C interface is considered to be free again a certain time after the STOP condition.
- The I²C interface stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START(S) and repeated START (Sr) conditions are functionally identical.



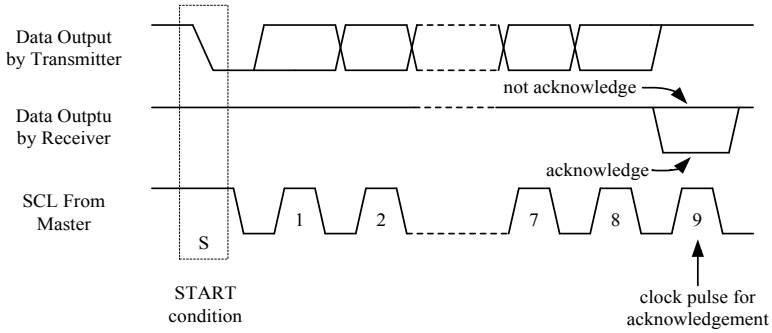
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



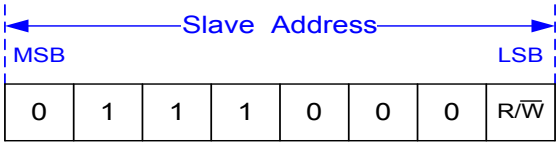
Acknowledge

- Each bytes of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level placed on the I^2C interface by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge, ACK, after the reception of each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Slave Addressing

- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/$\overline{W}$ bit is "1", then a read operation is selected. A "0" selects a write operation.
- The HT16C21 address bits are "0111000". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.

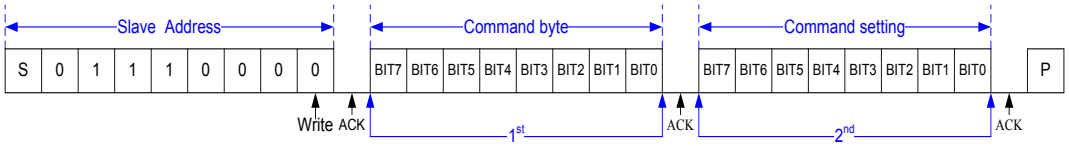


Write Operation

Byte Writes Operation

- **Command Byte**

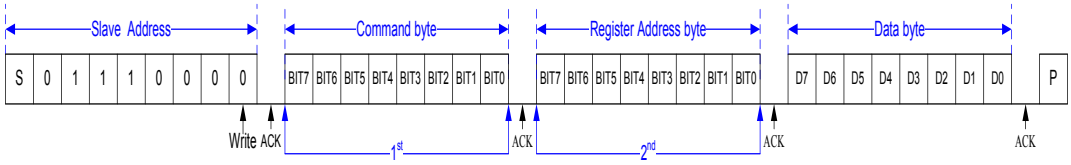
A Command Byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a command setting byte and a STOP condition for a command byte write operation.



Command Byte Write Operation

- **Display RAM Single Data Byte**

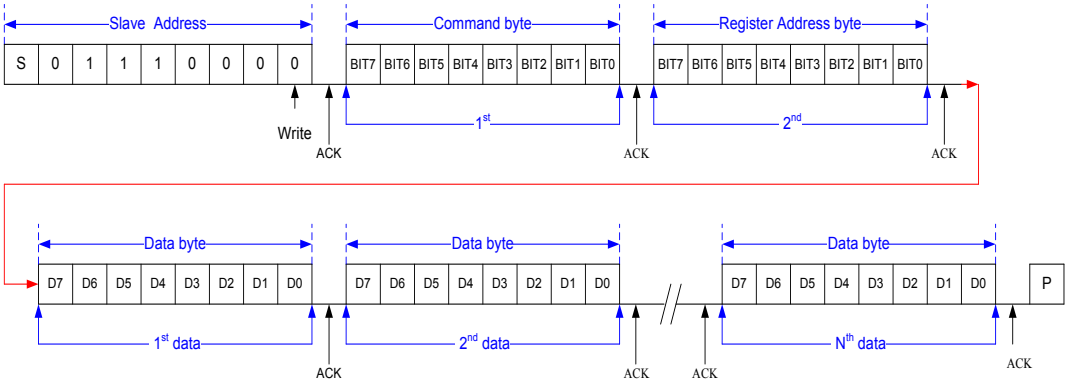
A display RAM data byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a valid Register Address byte, a Data byte and a STOP condition.



Display RAM Single Data Byte Write Operation

Display RAM Page Write Operation

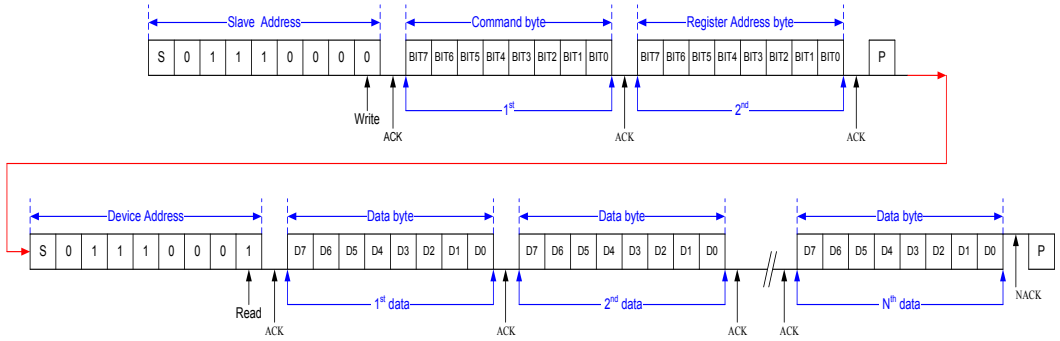
After a START condition the slave address with the R/$\overline{W}$ bit is placed on the I^{2}C interface followed with a command byte and the specified display RAM Register Address of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the internal address pointer will be incremented by 1 to indicate the next memory address location after the reception of an acknowledge clock pulse. After the internal address point reaches the maximum memory address, which is 09H for 1/4 duty drive mode or 0FH for 1/8 duty drive mode, the address pointer will be reset to 00H.



N Bytes Display RAM Data Write Operation

Display RAM Read Operation

- In this mode, the master reads the HT16C21 data after setting the slave address. Following the R/$\overline{W}$ bit (='0") is an acknowledge bit, a command byte and the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address transferred on the I²C interface followed by the R/$\overline{W}$ bit ('1"). Then the MSB of the data which was addressed is transmitted first on the I²C interface. The address pointer is only incremented by 1 after the reception of an acknowledge clock. That means that if the device is configured to transmit the data at the address of A_{N+1}, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum memory address, which is 09H for 1/4 duty drive mode or 0FH for 1/8 duty drive mode, the address pointer will be reset to 00H.
- This cycle of reading consecutive addresses will continue until the master sends a STOP condition.



Command Summary

Display Data Input Command

This command sends data from MCU to memory MAP of the HT16C21 device.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Display data input/ output command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	X	X	X	A3	A2	A1	A0	Display data start address of memory map	W	00H

Note:
- Power on status: The address is set to 00H.
- If the programmed command is not defined, the function will not be affected.
- For 1/4 duty drive mode after reaching the memory location 09H, the pointer will reset to 00H.
- For 1/8 duty drive mode after reaching the memory location 0FH, the pointer will reset to 00H.

Drive Mode Command

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Driver mode setting command	1st	1	0	0	0	0	0	1	0		W	
Duty and bias setting	2nd	X	X	X	X	X	X	Duty	Bias		W	00H

Note:

Bit		Duty	Bias
Duty	Bias		
0	0	1/4duty	1/3bias
0	1	1/4duty	1/4bias
1	0	1/8duty	1/3bias
1	1	1/8duty	1/4bias

- Power on status: The drive mode 1/4 duty output and 1/3 bias is selected.
- If the programmed command is not defined, the function will not be affected.

System Mode Command

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
System mode setting command	1st	1	0	0	0	0	1	0	0		W	
System oscillator and display on/off setting	2nd	X	X	X	X	X	X	S	E		W	00H

Note:

Bit		Internal System Oscillator	LCD Display
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

- Power on status: Display off and disable the internal system oscillator.
- If the programmed command is not defined, the function will not be affected.

Frame Frequency Command

This command selects the frame frequency.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Frame frequency command	1st	1	0	0	0	0	1	1	0		W	
Frame frequency setting	2nd	X	X	X	X	X	X	X	F		W	00H

Note:

Bit	Frame Frequency
F	
0	80Hz
1	160Hz

- Power on status: Frame frequency is set to 80Hz.
- If the programmed command is not defined, the function will not be affected.

Blinking Frequency Command

This command defines the blinking frequency of the display modes.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Blinking Frequency command	1st	1	0	0	0	1	0	0	0		W	
Blinking Frequency setting	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Note:

Bit		Blinking Frequency
BK1	BK0	
0	0	Blinking off
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

- Power on status: Blinking function is switched off.
- If the programmed command is not defined, the function will not be affected.

Internal Voltage Adjustment (IVA) Setting Command

The internal voltage (V_{LCD}) adjustment can provide sixteen kinds of regulator voltage adjustment options by setting the LCD operating voltage adjustment command.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Internal Voltage Adjustment (IVA) Setting	1st	1	0	0	0	1	0	1	0		W	
Internal Voltage Adjust control	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	● The Segment/VLCD shared pin can be programmed via the "DE" bit. ● The "VE" bit is used to enable or disable the internal voltage adjustment for bias voltage. ● The DA3~DA0 bits can be used to adjust the V_{LCD} output voltage.	W	30H

Note:

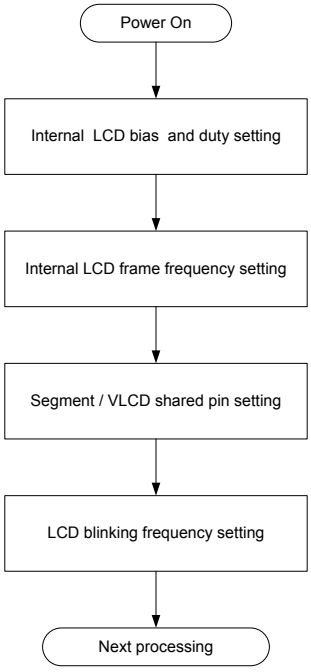
Bit		Segment / VLCD Shared Pin Select	Internal Voltage Adjustment	Note
DE	VE			
0	0	VLCD pin	off	● The Segment/VLCD pin is set as the VLCD pin. ● Disable the internal voltage adjustment function ● One external resister must be connected between VLCD pin and VDD pin to determine the bias voltage, and internal voltage follower (OP4) must be enabled by setting the DA3~DA0 bits as the value other than "0000". ● If the VLCD pin is connected to the VDD pin, the internal voltage follower (OP4) must be disabled by setting the DA3~DA0 bits as "0000".
0	1	VLCD pin	on	● The Segment/VLCD pin is set as the VLCD pin. ● Enable the internal voltage adjustment function. ● The VLCD pin is an output pin of which the voltage can be detected by the external MCU host.
1	0	Segment pin	off	● The Segment/VLCD pin is set as the Segment pin. ● Disable the internal voltage adjustment function. ● The bias voltage is supplied by the internal VDD power. ● The internal voltage-follower (OP4) is disabled automatically and DA3~DA0 don't care.
1	1	Segment pin	on	● The Segment/VLCD pin is set as the Segment pin. ● Enable the internal voltage adjustment function.

● Power on status: Disable the internal voltage adjustment and the Segment/VLCD pin is set as the Segment pin.
● When the DA0~DA3 bits are set to "0000", the internal voltage-follower (OP4) is disabled. When the DA0~DA3 bits are set to other values except "0000", the internal voltage follower (OP4) is enabled.
● If the programmed command is not defined, the function will not be affected.

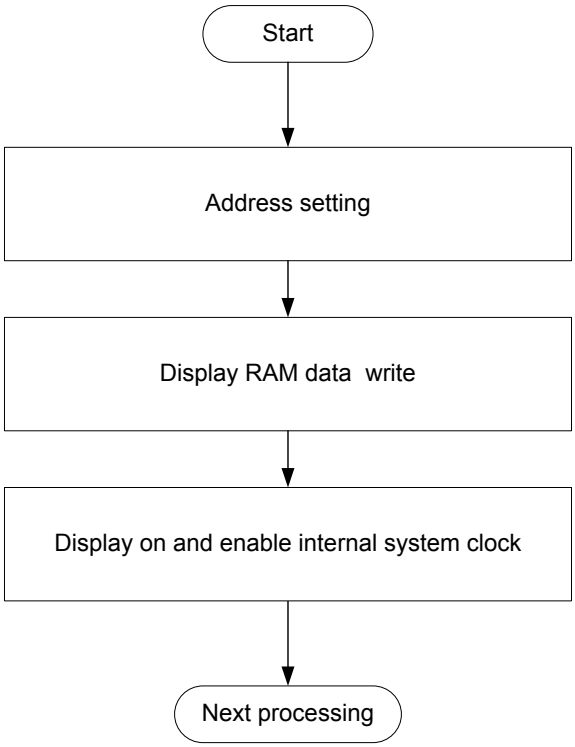
Operation Flow Chart

Access procedures are illustrated below by means of the flowcharts.

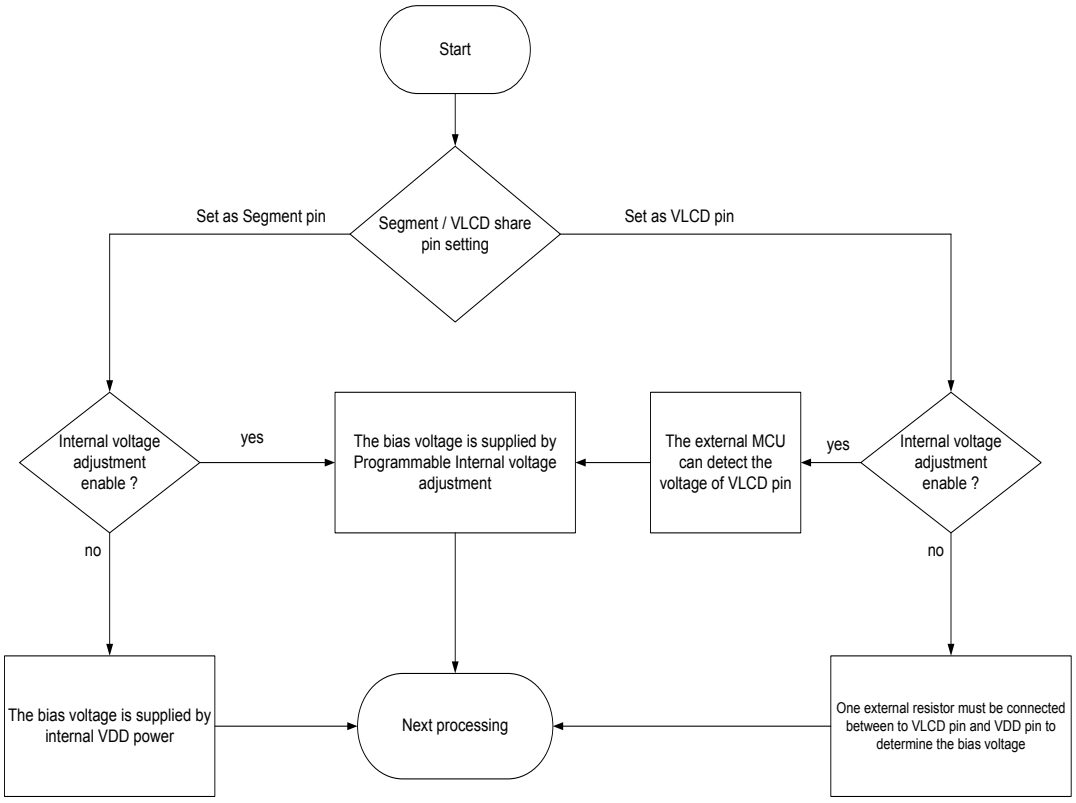
Initialization



Display Data Read/Write (Address Setting)



Segment / VLCD shared pin and internal voltage adjustment setting



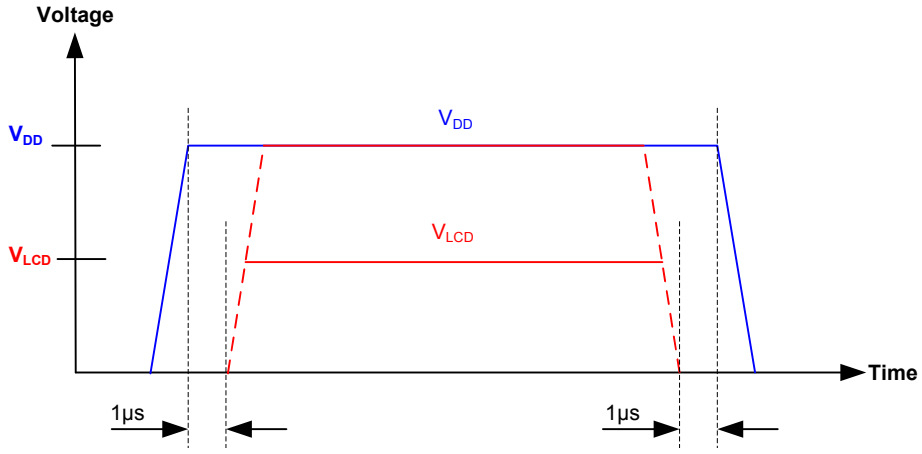
Power Supply Sequence

- If the power is individually supplied on the LCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

Holtek Power Supply Sequence Requirement:

1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.
2. Power-off sequence:
   Turn off the LCD driver power supply V_{LCD}. First and then turn off the logic power supply V_{DD}.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the V_{LCD} voltage is higher than the V_{DD} voltage.

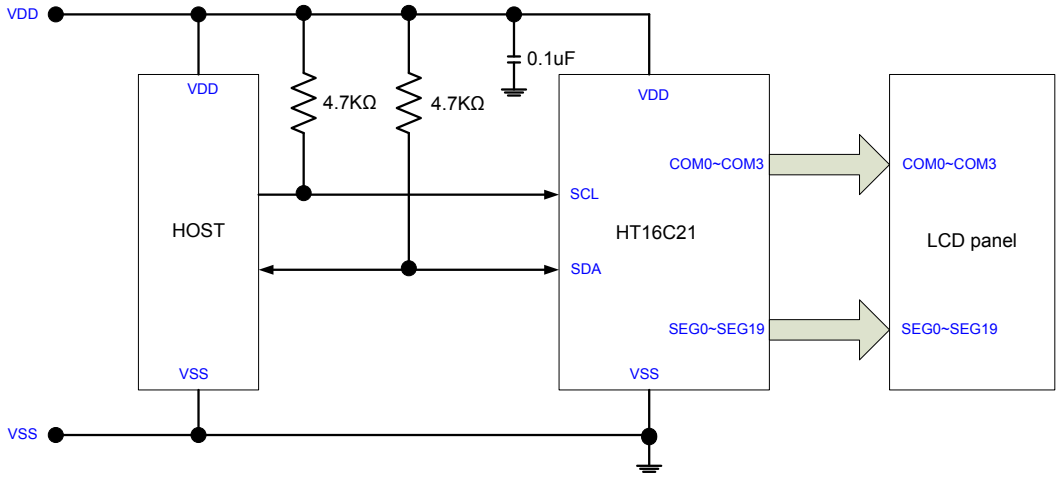
- When the V_{LCD} voltage is smaller than or is equal to V_{DD} voltage application



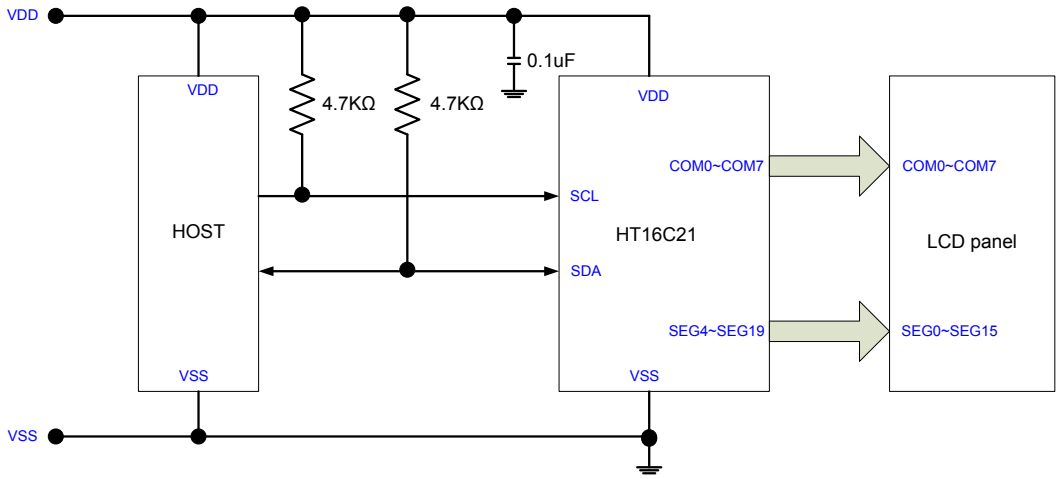
Application Circuit

Set as Segment pin

- **1/4 Duty**



- **1/8 duty**



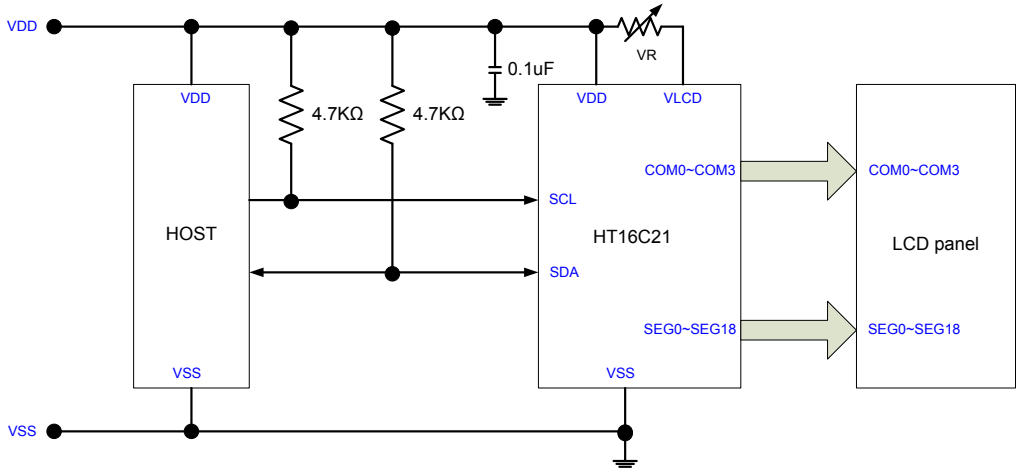
Note: 1. If the internal V_{LCD} voltage adjustment function is disabled, the bias voltage is supplied by internal VDD power.

2. If the internal V_{LCD} voltage adjustment function is enabled, the bias voltage is supplied by the internal adjusted voltage selected by the DA3~DA0 bits.

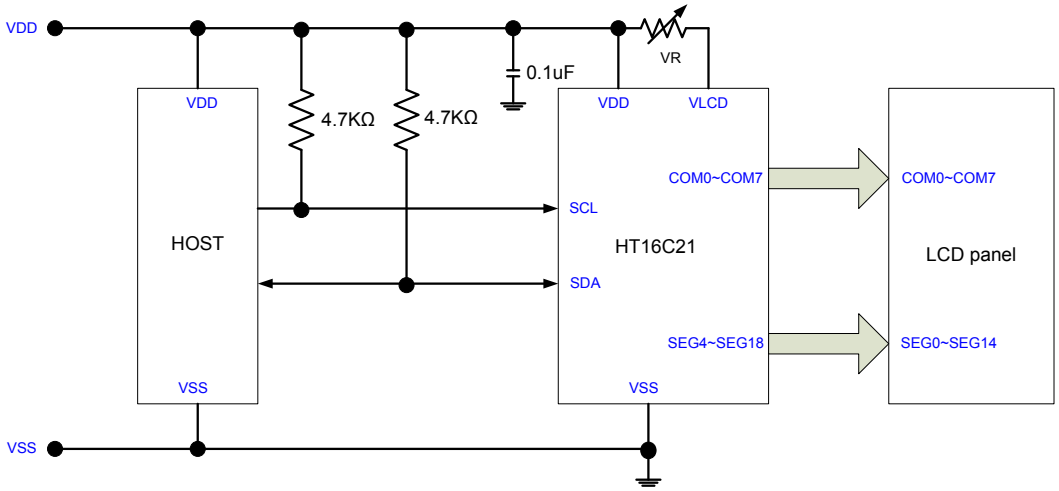
Set as VLCD pin

When the internal V_{LCD} voltage adjustment function is disabled, an external resistor must be connected between the VLCD and VDD pins to determine the supplied bias voltage.

- **1/4 duty**

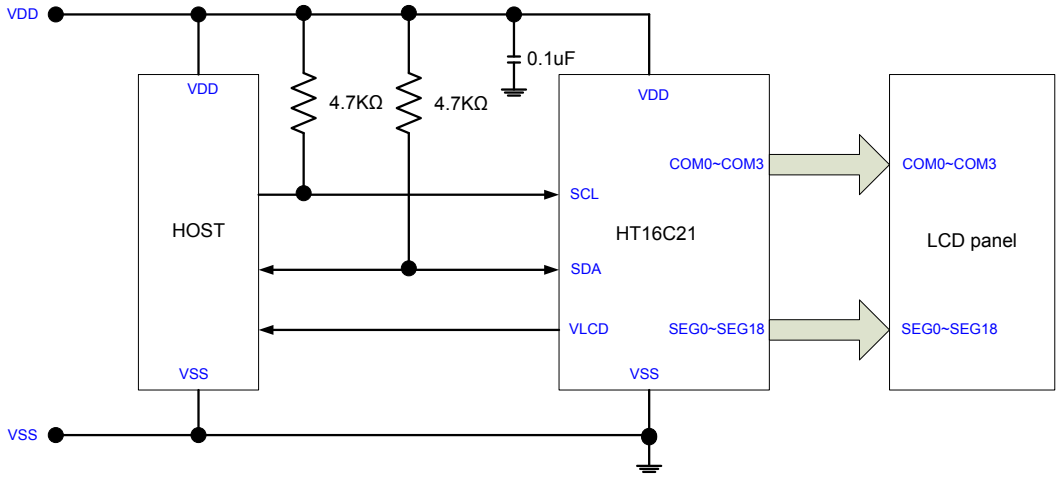


- **1/8 duty**

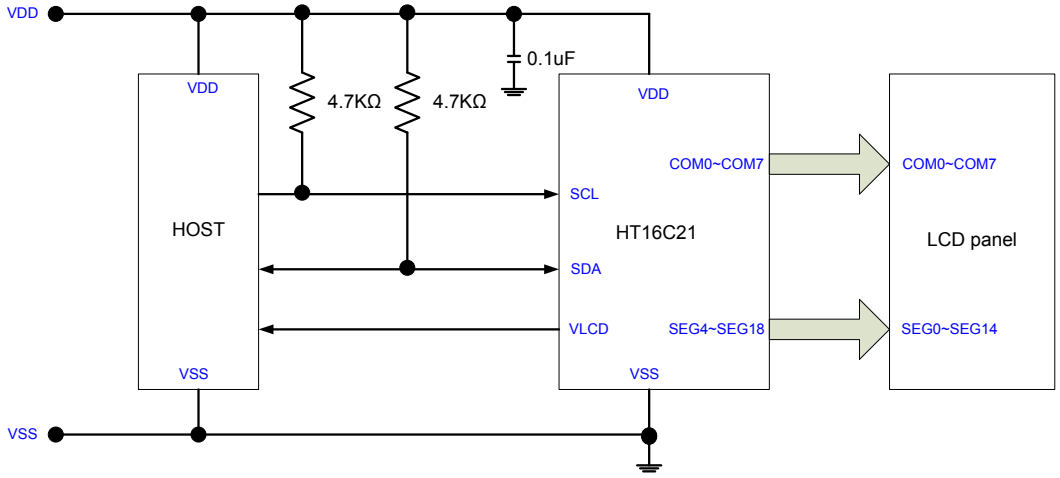


When the internal VLCD voltage adjustment function is enabled and the Segment/VLCD shared pin is set as VLCD pin, the bias voltage is supplied by the internal adjusted voltage, derived from the VDD voltage, determined by the DA3~DA0 bits and the VLCD pin is used as an output pin of which the voltage is detected by the external MCU host.

- **1/4 duty**



- **1/8 duty**



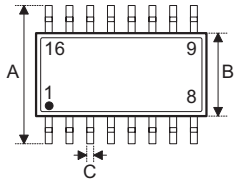
Package Information

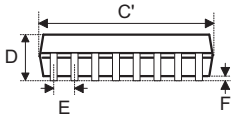
Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

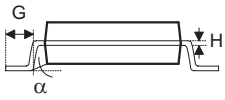
Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

16-pin NSOP (150mil) Outline Dimensions



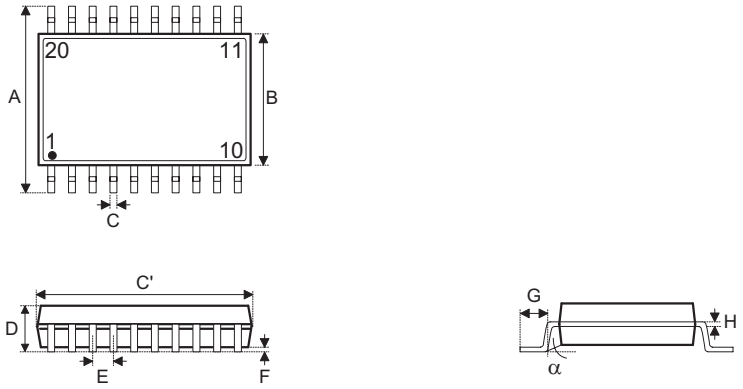




Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.390 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.000 BSC	—
B	—	3.900 BSC	—
C	0.31	—	0.51
C'	—	9.900 BSC	—
D	—	—	1.75
E	—	1.270 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

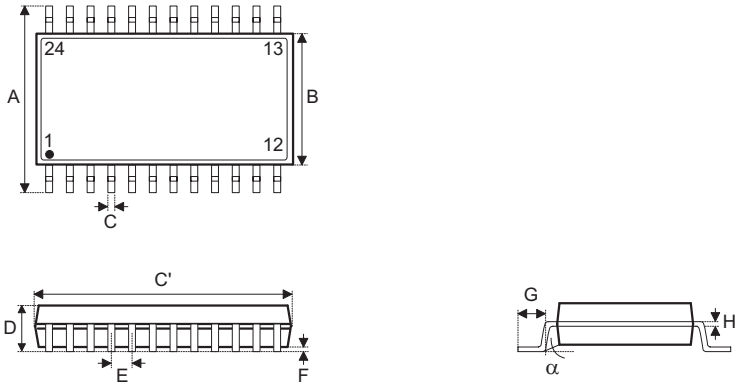
20-pin SOP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.406 BSC	—
B	—	0.295 BSC	—
C	0.012	—	0.020
C’	—	0.504 BSC	—
D	—	—	0.104
E	—	0.050 BSC	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	10.30 BSC	—
B	—	7.50 BSC	—
C	0.31	—	0.51
C’	—	12.80 BSC	—
D	—	—	2.65
E	—	1.27 BSC	—
F	0.10	—	0.30
G	0.40	—	1.27
H	0.20	—	0.33
α	0°	—	8°

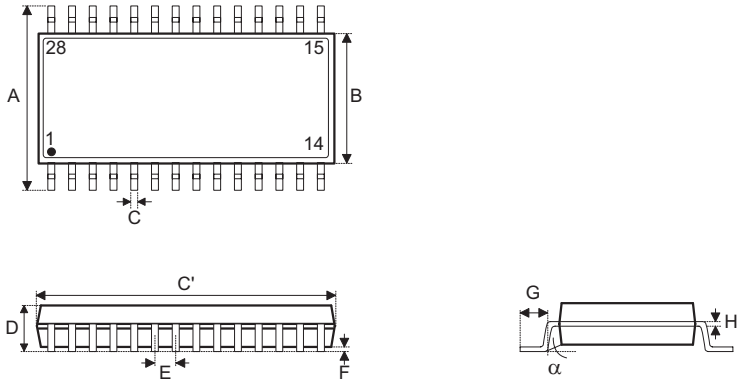
24-pin SOP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.406 BSC	—
B	—	0.295 BSC	—
C	0.012	—	0.020
C’	—	0.606 BSC	—
D	—	—	0.104
E	—	0.050 BSC	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	10.30 BSC	—
B	—	7.50 BSC	—
C	0.31	—	0.51
C’	—	15.40 BSC	—
D	—	—	2.65
E	—	1.27 BSC	—
F	0.10	—	0.30
G	0.40	—	1.27
H	0.20	—	0.33
α	0°	—	8°

28-pin SOP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.406 BSC	—
B	—	0.295 BSC	—
C	0.012	—	0.020
C’	—	0.705 BSC	—
D	—	—	0.104
E	—	0.050 BSC	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	10.30 BSC	—
B	—	7.5 BSC	—
C	0.31	—	0.51
C’	—	17.9 BSC	—
D	—	—	2.65
E	—	1.27 BSC	—
F	0.10	—	0.30
G	0.40	—	1.27
H	0.20	—	0.33
α	0°	—	8°