FUJITSU
MICROELECTRONICS, INC.

MB8168-55
MB8168-70

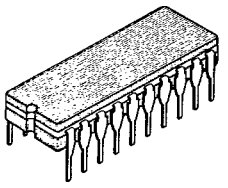
NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

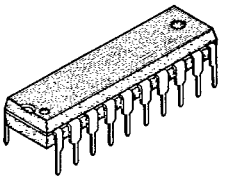
The Fujitsu MB8168 is a 4096 word by 4-bit static random access memory fabricated using N-channel silicon gate MOS technology. The memory is fully static and requires no clock or timing strobe. All pins are TTL compatible and a single 5V power supply is required.

A separate chip select $\overline{E}$ pin simplifies multipackage system design. It permits the selection of an individual package when outputs are OR-tied. Furthermore, when selecting a single package by $\overline{E}$, the other deselected packages automatically power down.

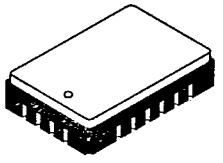
All Fujitsu devices offer the advantages of low power dissipation, low cost and high performance.



CERDIP PACKAGE
DIP-20C-C03



PLASTIC PACKAGE
DIP-20P-M01

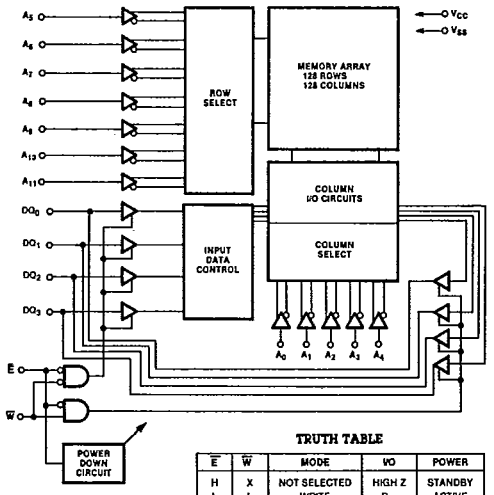


LCC PACKAGE
LCC-20C-F01

FEATURES

- **Organized as 4096 words x 4-bits**
- **Fully Static Operation, no clocks or timing strobe required**
- **Fast Access Time:**
  MB8168-55 55 ns Max.
  MB8168-70 70 ns Max.
- **Low Power Consumption:**
  I_{CC} = 150mA Max. (Active)
  I_{SB} = 40mA Max.(Standby)
- **Single +5V DC Supply Voltage, ±10% tolerance**
- **Common data input and output**
- **Three-state outputs with OR-tie capability**
- **Chip select for simplified memory expansion, automatic power-down**
- **Standard 20-pin DIP package**
- **Pin compatible with Intel 2168**

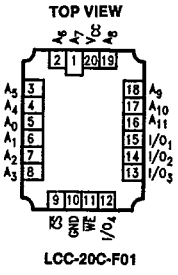
MB8168 BLOCK DIAGRAM

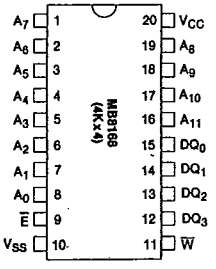


TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

PIN ASSIGNMENTS





ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7.0	V
Short Circuit Output Current	I_{SO}	20	mA
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	Tstg Ceramic Plastic	−65 to +150 −40 to +125	°C
Power Dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0[2]	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

Note: 1. The operating ambient temperature range is guaranteed with transverse airflow exceeding 2 linear meters/second.
2. −3.0 V Min. for Pulse width less than 20 ns. (V_{IL} Min. = −0.5 V at DC level)

CAPACITANCE (T_A = 25° C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance Address, $\overline{W}$: V_{IN} = 0V	C_{IN}	—	7	pF
Input Capacitance $\overline{E}$: V_{IN} = 0V	$C_{\overline{E}}$	—	8	pF
Output Capacitance Data I/O, V_{OUT} = 0V	$C_{I/O}$	—	8	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{OUT} = V_{SS} to 4.5V, V_{CC} = Max)	I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{E}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC}	—	150	mA
Output Low Voltage (I_{OL} = 8mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)	V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{E}$ = V_{IH}, I_{OUT} = 0mA)	I_{SB}	—	40	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{E}$ = Lower of V_{CC} or V_{IH} Min)*	I_{PO}	—	50	mA

Note: *A pull-up resistor to V_{CC} or the $\overline{CS}$ input is required to keep the device deselected. Otherwise, power-on current approaches I_{CC} active.

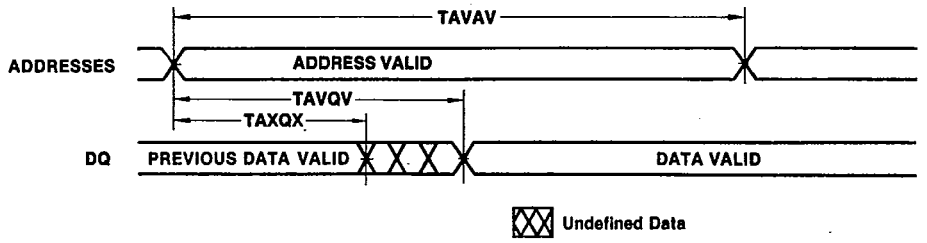
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

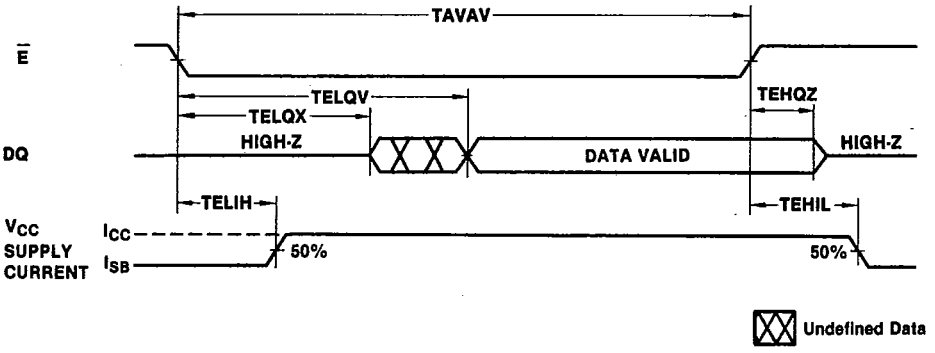
READ CYCLE

Parameter	NOTES	Symbol	MB8168-55			MB8168-70			Unit
			Min	Typ	Max	Min	Typ	Max	
Read Cycle Time		TAVAV	55	—	—	70	—	—	ns
Address Access Time		TAVQV	—	—	55	—	—	70	ns
Chip Enable Access Time		TELQV	—	—	55	—	—	70	ns
Output Hold from Address Change		TAXQX	5	—	—	5	—	—	ns
Chip Enable to Output Active	1 2	TELQX	10	—	—	10	—	—	ns
Chip Enable to Output in High Z	1 2	TEHQZ	—	—	30	—	—	40	ns
Chip Enable to Power Up Time	3	TELIH	0	—	—	0	—	—	ns
Chip Enable to Power Down Time	3	TEHIL	—	—	55	—	—	70	ns

READ CYCLE: ADDRESS CHANGING 4,5



READ CYCLE: $\overline{CS}$ CHANGING 4,6

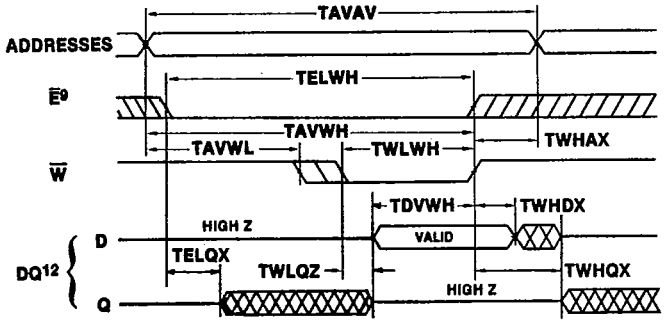


Notes: 1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig. 2.
3. $I_H = I_{CC\,(Max)}$, $I_L = I_{SB\,(Max)}$
4. $\overline{W}$ is high for Read Cycle.
5. Device is continuously selected. $\overline{E} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{E}$ transition low.

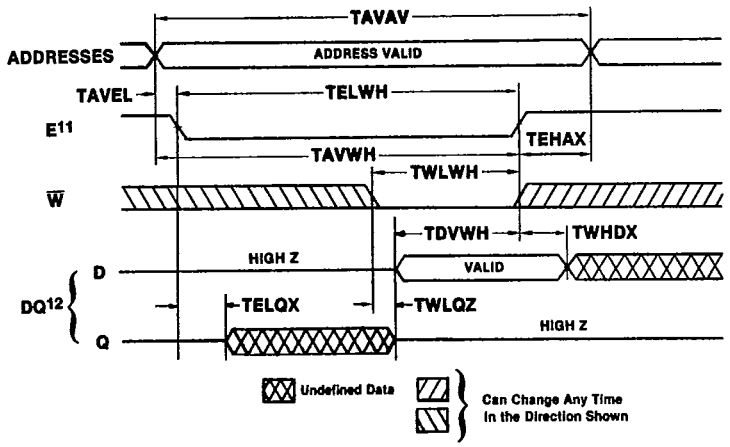
WRITE CYCLE

Parameter	NOTES	Symbol	MB8168-55 Min	MB8168-55 Typ	MB8168-55 Max	MB8168-70 Min	MB8168-70 Typ	MB8168-70 Max	Unit
Write Cycle Time		TAVAV	55	—	—	70	—	—	ns
Address Valid to End of Write		TAVWH	50	—	—	60	—	—	ns
Chip Enable to End of Write		TELWH	50	—	—	60	—	—	ns
Data Valid to End of Write		TDVWH	25	—	—	30	—	—	ns
Data Hold Time		TWHDX	0	—	—	0	—	—	ns
Write Pulse Width		TWLWH	50	—	—	60	—	—	ns
Write Recovery Time		TWHAX, TEHAX	0	—	—	0	—	—	ns
Address Setup Time		TAVWL, TAVEL	0	—	—	0	—	—	ns
Output Active From End of Write	7 8	TWHQX	0	—	—	0	—	—	ns
Write Enable to Output in High Z	7 8	TWLQZ	0	—	30	0	—	40	ns
Chip Enable to Output Active		TELQX	10	—	—	10	—	—	ns

WRITE CYCLE: $\overline{W}$ CONTROLLED[10]



WRITE CYCLE: $\overline{E}$ CONTROLLED[10]



Notes: 7. Transition is measureed at the point of ±500 mV from steady state voltage.
8. This parameter is measured with specified loading in Fig. 2.
9. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.
10. $\overline{E}$ or $\overline{W}$ must be high during address transitions.
11. If $\overline{W}$ is low for the entire cycle Data Out remains High Z throughout the cycle.
12. Q shows when the DQ pin is driven by the memory chip. D shows when the DQ pin is externally driven.

AC TEST CONDITIONS

Input Conditions:

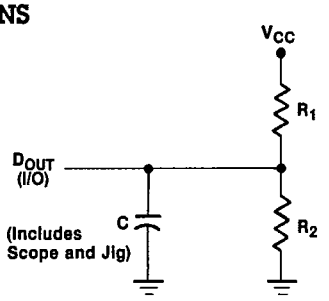
Input Pulse Levels:	**0V to 3.0V**
Input Pulse Rise/Fall Times:	**5 ns**
Input Timing Reference Level:	**1.5V**

Output Conditions:

Output Timing Reference Level:	**0.8V to 2.0V**

Output Load:

	R_1	R_2	C	Parameters Measured
Load I	480Ω	255Ω	30pF	except TELQX, TEHQZ, TWLQZ, and TWHQX
Load II	480Ω	255Ω	5pF	TELQX, TEHQZ, TWLQZ, and TWHQX



OUTPUT LOAD

DEVICE OPERATION

Controls

The MB8168 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When $\overline{E} \geq V_{IH}$, the device is deselected and automatically controlled to the standby mode, reducing the power requirements to less than one-sixth of the selected state. When $\overline{E} \leq V_{IL}$, the device is selected (active) and read or write cycles may be performed. $\overline{E}$ should be controlled to track V_{CC} during the initial system power-on to prevent all of the MB8168's in a system from drawing active I_{CC} during power-up.

When $\overline{W} \geq V_{IH}$ and the chip is selected, a read cycle may be performed. When $\overline{W} \leq V_{IL}$ and the chip is selected a write cycle may be performed.

Read Cycle

A read cycle is selected when $\overline{E} \leq V_{IL}$ and $\overline{W} \geq V_{IH}$. Read access time is measured from either the $\overline{E}$ high to low transition or from valid address as shown in the read cycle timing diagrams.

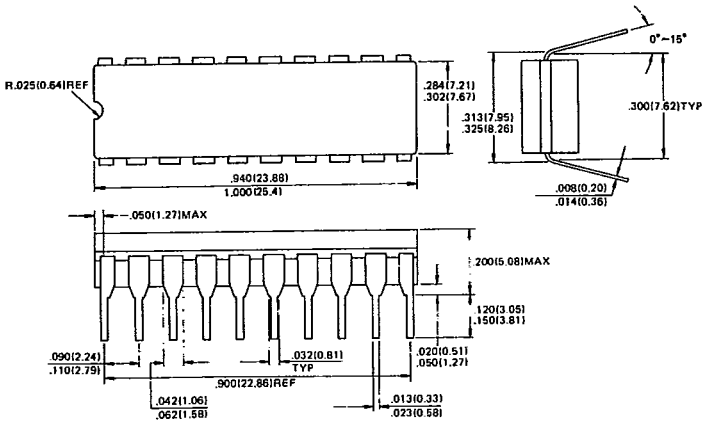
Write Cycle

A write cycle is seleted when $\overline{E} \leq V_{IL}$ and $\overline{W} \leq V_{IH}$. The actual beginning of the write cycle is initiated by the latter of $\overline{E}$ or $\overline{W}$ going low as shown in the write cycle timing diagrams. The address setup times shown in the timing diagrams must be met and the addresses must remain stable for the entire write cycle. The write cycle is terminated by either $\overline{E}$ or $\overline{W}$ going high. If the timing specifications are not met, data may be altered or lost.

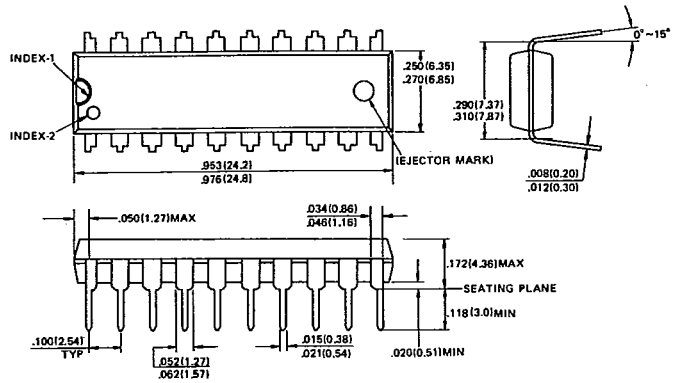
In summary, the write cycle may be initiated by the latter of $\overline{E}$ or $\overline{W}$ going low and may be terminated by $\overline{E}$ or $\overline{W}$ going high, whichever occurs first, and the setup and hold times must be referenced to the controlling signal transitions. Either $\overline{E}$ or $\overline{W}$ must be high (greater than V_{IH}), during an address transition.

PACKAGE DIMENSIONS Dimensions in Inches (millimeters)

20-LEAD CERDIP DUAL IN-LINE PACKAGE
DIP-20C-C03



20-LEAD PLASTIC DUAL IN-LINE PACKAGE
DIP-20P-M01



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
LCC-20C-F01