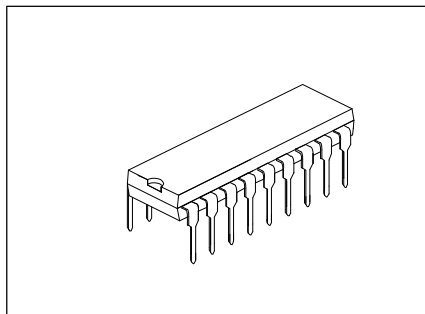


1517

**LINEAR INTEGRATED CIRCUIT**
**2 × 6 W stereo power amplifier**
**DESCRIPTION**

The CD1517 is an integrated class B dual output amplifier in a plastic single in-line medium power package with fin and a plastic heat-dissipating dual in-line package. The device is primarily developed for multi-media applications.


**FEATURES**

- \* Requires very few external components
- \* High output power
- \* Fixed gain
- \* Good ripple rejection
- \* Mute/standby switch
- \* AC and DC short-circuit safe to ground and VP
- \* Thermally protected
- \* Reverse polarity safe
- \* Capability to handle high energy on outputs ( $V_P = 0\text{ V}$ )
- \* No switch-on/switch-off pop
- \* Electrostatic discharge protection.

**QUICK REFERENCE DATA**

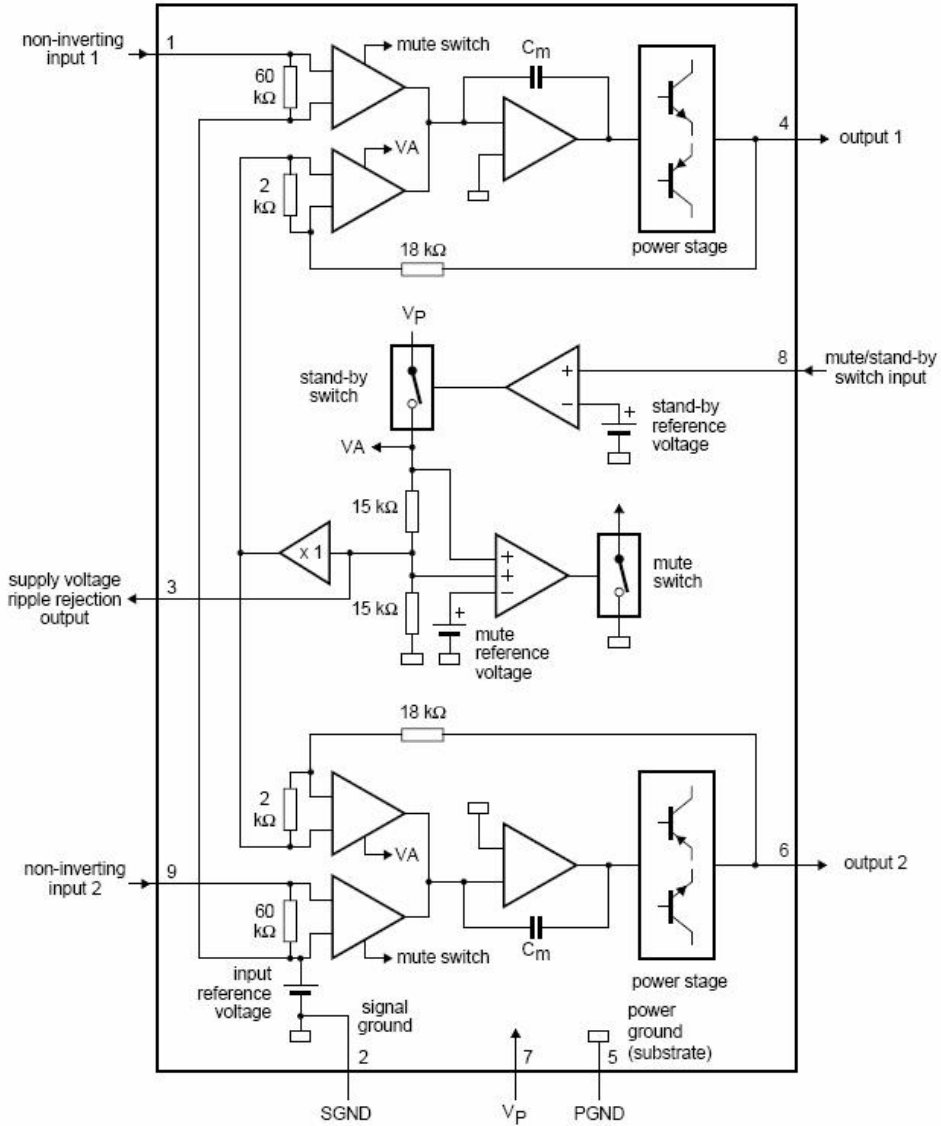
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage		6.0	14.4	18.0	V
$I_{ORH}$	repetitive peak output current		-	-	2.5	A
$I_{q(tot)}$	total quiescent current		-	40	80	mA
$I_{sb}$	standby current		-	0.1	100	$\mu\text{A}$
$I_{sw}$	switch-on current		-	-	40	$\mu\text{A}$
$ Z_I $	input impedance		50	-	-	$\text{k}\Omega$
$P_o$	output power	$R_L = 4\Omega$ ; THD = 0.5%	-	5	-	W
		$R_L = 4\Omega$ ; THD = 10%	-	6	-	W
SVRR	supply voltage ripple rejection	$f_1 = 100\text{ Hz to }10\text{ kHz}$	48	-	-	dB
$\alpha_{cs}$	channel separation		40	-	-	dB
$G_v$	closed loop voltage gain		19	20	21	dB
$V_{no(rms)}$	noise output voltage (RMS value)		-	50	-	$\mu\text{V}$
$T_c$	crystal temperature		-	-	150	$^{\circ}\text{C}$

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BLOCK DIAGRAM



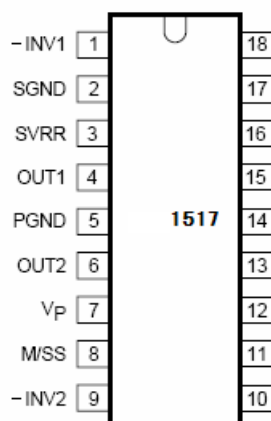
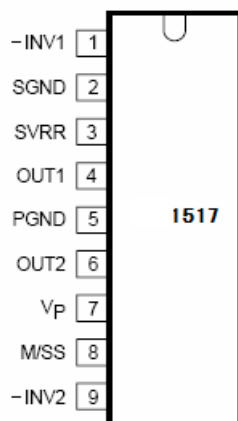
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## PINNING

SYMBOL	PIN	DESCRIPTION
-INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
VP	7	supply voltage
M/SS	8	mute/standby switch input
-INV2	9	non-inverting input 2



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# LINEAR INTEGRATED CIRCUIT

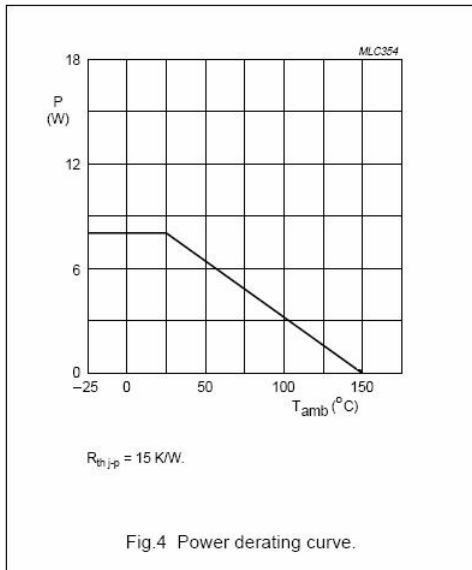
## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_p$	supply voltage		-	18	V
$V_{P(SC)}$	AC and DC short-circuit safe voltage		-	18	V
$V_{P(r)}$	reverse polarity		-	6	V
$ERG_0$	energy handling capability at outputs	$V_p = 0V$	-	200	mJ
$I_{OSM}$	non-repetitive peak output current		-	4	A
$I_{ORM}$	repetitive peak output current		-	2.5	A
$P_{tot}$	total power dissipation	see Fig. 4	-	15	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	operating ambient temperature		-40	+85	°C
$T_c$	crystal temperature		-	150	°C

## THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-p}$	thermal resistance from junction to pins	15	K/W
$R_{th\ j-a}$	thermal resistance from junction to ambient	50	K/W



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# 1517 LINEAR INTEGRATED CIRCUIT

## DC CHARACTERISTICS

$V_P = 14.4\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; measured in Fig. 6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_P$	supply voltage	note 1	6.0	14.4	18.0	V
$I_{q(\text{tot})}$	total quiescent current		-	40	80	mA
$V_O$	DC output voltage		-	6.95	-	V
Mute/standby switch						
$V_B$	switch-on voltage level	see Fig. 5	8.5	-	-	V
Mute condition						
$V_O$	output signal in mute position	$V_{i(\text{max})} = 1\text{V}$ ; $f_i = 20\text{Hz to } 15\text{kHz}$	-	-	2	mV
Standby condition						
$I_{sb}$	DC current in standby condition		-	-	100	$\mu\text{A}$
$V_{SR}$	switch-on current		-	12	40	$\mu\text{A}$

Note: 1. The circuit is DC adjusted at  $V_P = 6$  to  $18\text{ V}$  and AC operating at  $V_P = 8.5$  to  $18\text{ V}$ .

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# LINEAR INTEGRATED CIRCUIT

## AC CHARACTERISTICS

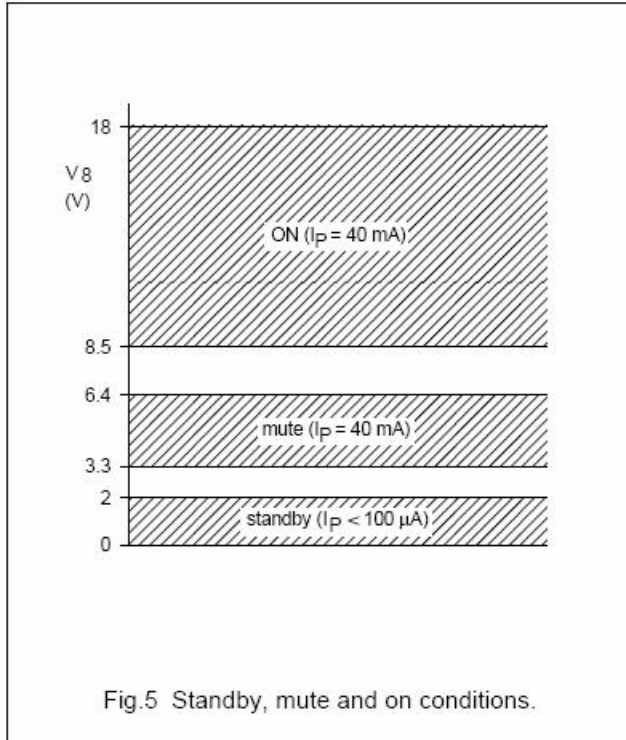
$V_P = 14.4\text{ V}$ ;  $R_L = 4\text{ W}$ ;  $f = 1\text{ kHz}$ ;  $T_{amb} = 25^\circ\text{C}$ ; measured in Fig. 6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_o$	output power	THD = 0.5%; note 1	4	5	-	W
		THD = 10%; note 1	5.5	6.0	-	W
THD	total harmonic distortion	$P_o = 1\text{W}$	-	0.1	-	%
$f_{lr}$	low frequency roll-off	at -3 dB; note 2	-	45	-	Hz
$f_{hr}$	high frequency roll-off	at -1dB	20	-	-	kHz
$G_v$	closed loop voltage gain		19	20	21	dB
SVRR	supply voltage ripple rejection on	note 3	48	-	-	dB
	mute		48	-	-	dB
	standby		80	-	-	dB
$ Z_i $	input impedance		50	60	75	k $\Omega$
$V_{no}$	noise output voltage on	$R_s = 0\Omega$ ; note 4	-	50	-	$\mu\text{V}$
	on	$R_s = 10\Omega$ ; note 4	-	70	100	$\mu\text{V}$
	mute	note 5	-	50	-	$\mu\text{V}$
$\alpha_{cs}$	channel separation	$R_s = 10\text{ W}$	40	-	-	dB
$ \Delta G_v $	channel unbalance		-	0.1	1	dB

### Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of  $0\Omega$ , maximum ripple amplitude of 2 V (p-p) and a frequency between 100 Hz and 10 kHz.
4. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage independent of  $R_s$  ( $V_i = 0\text{ V}$ ).

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APPLICATION INFORMATION

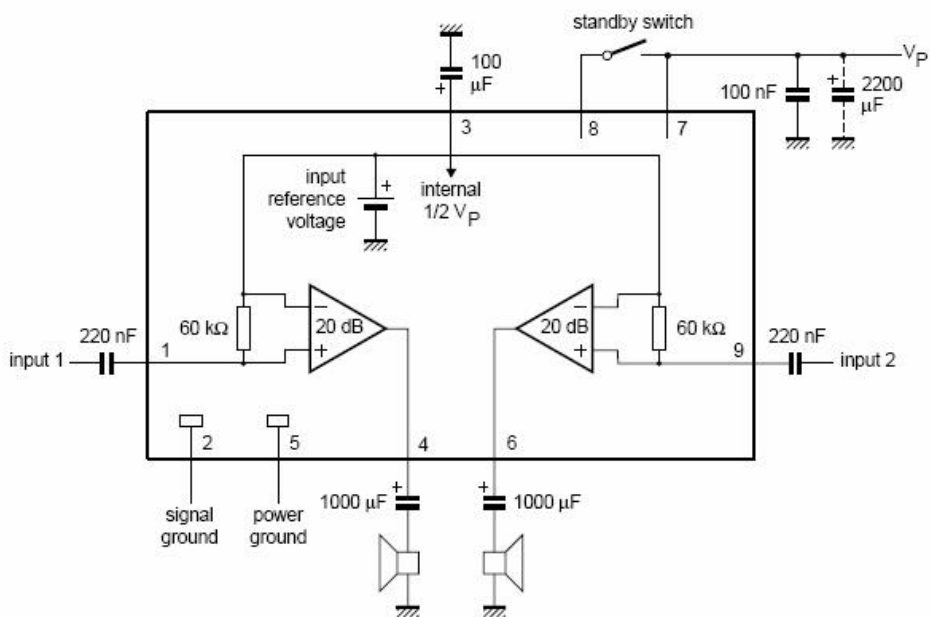


Fig.6 Application circuit diagram.

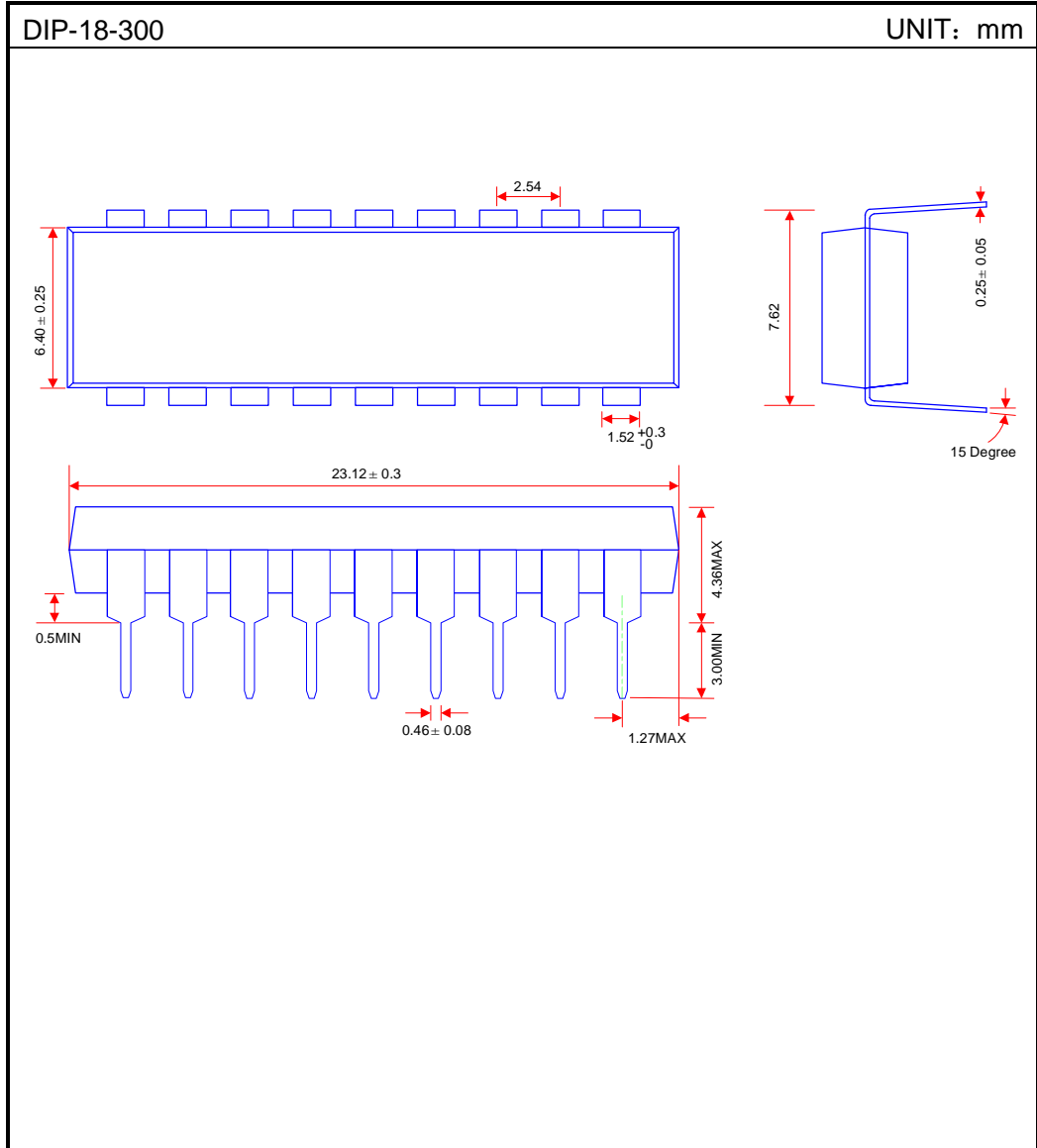
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PACKAGE OUTLINE



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