3.5W/CH STEREO CLASS-D AUDIO POWER AMPLIFIER WITH GAIN CONTROL,HOPPING FREQUENCY AND SPREAD SPECTRUM

GENERAL DESCRIPTION

The TMPA268DS is a stereo class-D audio power amplifier IC with digital volume control. With BTL (Bridge-Tied-Load) configuration, it delivers up to 3.5W/ch (7W in all) into a 3 ohm load. Up and down volume control signals provide -57dB attenuation form maximum voltage gain. No external heat-sink is required.

For multiple-input applications, independent gain control and corner frequency can be implemented by summing the input sources through resistor ratio and input capacitor values. Automatic output power control makes the best use of battery.

Analog input signal is converted into digital output which drives directly to the speaker. High power efficiency is achieved due to digital output at the load. The audio information is embedded in PWM(Pulse Width Modulation). The function of hopping frequency allows the users to change switching frequency to avoid interfere to nearby receiver. Spread spectrum reduces or spread the interference energy to reduce EMI.

APPLICATIONS

TMPA268DS is designed for portable devices including Cellular phones, PDAs, GPSs, MP3 players, iPOD docking or speaker systems, It also can be used for TFT LCD TVs/Monitors.

FEATURES

- 2.5V to 6V Single Supply
- Up to 3.5W / Ch at 5.5V, 3 ohms
- Up to 91% Power Efficiency
- 9mA Quiescent Current/7.8mA standby current at 5V
- Less Than 0.2uA / Ch Shutdown Current
- 0dB to -57dB attenuation from max. voltage gain
- Automatic output power control (APC)
- Memory of voltage gain at shutdown
- Pop-less Power-Up, Shutdown and Recovery
- Differential 380 KHz PWM Allows Bridge-Tied Load to increase Output Power and Eliminates LC Output Filter
- Thermal Shutoff and Automatic Recovery
- Output Pin Short-Circuit Protection (Short to Other Outputs, Short to VCC, Short to Ground) and Automatic Recovery
- AM2 Mode/FM Mode to Hop Frequency and to Spread PWM Spectrum in case of Radio Interference
- Differential Signal Processing Improves CMRR

Package

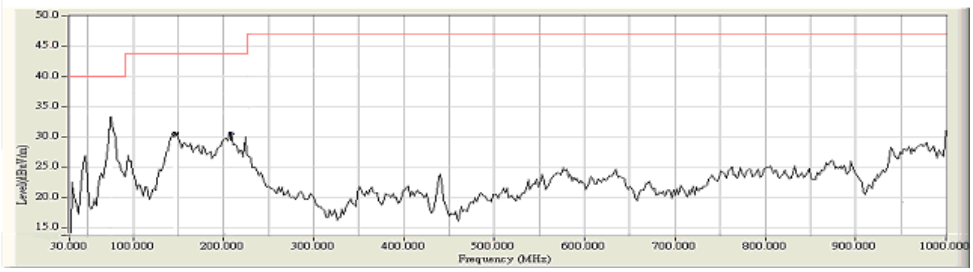
TSSOP24 Available, pb free【RoHS】

PART NO.

TMPA2680DSGCT【Tube】

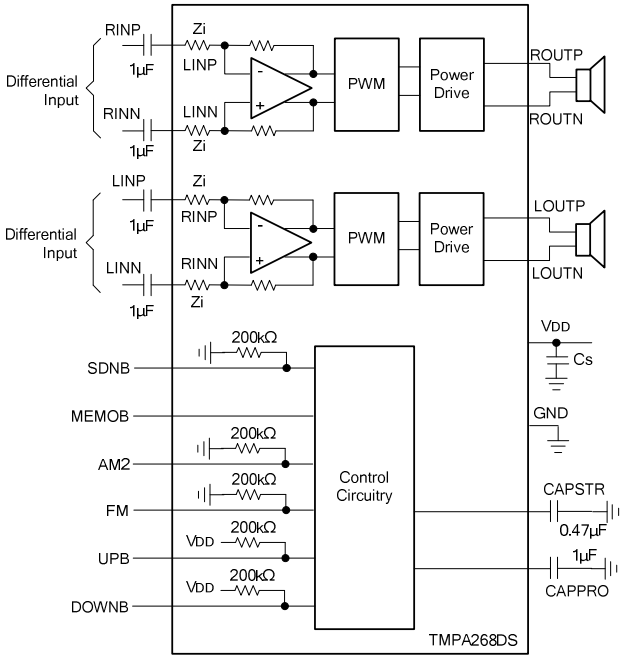
TMPA2680DSGCR【Tape & Reel】

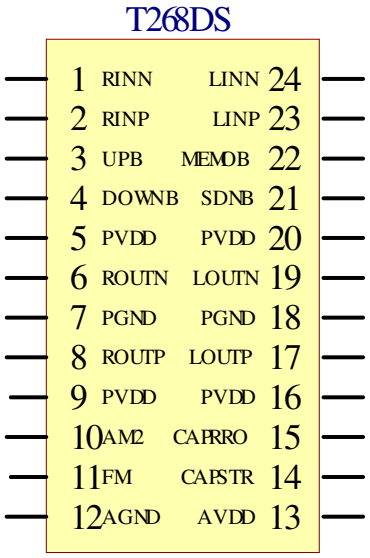
For best performance, please refer to
http://www.taimec.com.tw/English/EVM.htm
http://www.class-d.com.tw/English/EVM.htm
for PCB layout.



TMPA268DS EMI (No LC filter)- 300mm Speaker Wire

REFERENCE CIRCUIT（Please refer to TMPA002.APP for application）





（Please email david@taimec.com.tw for complete datasheet.）

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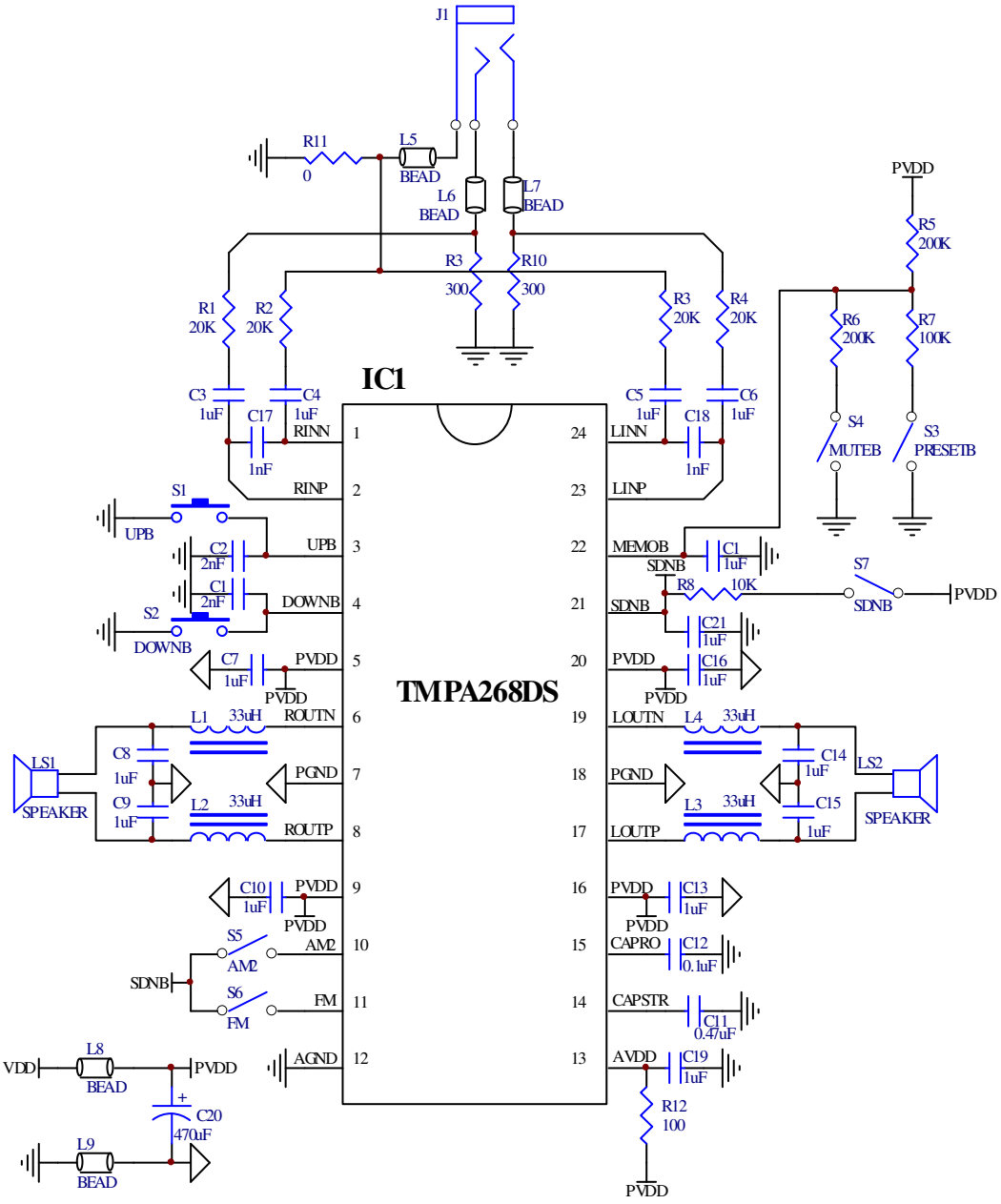
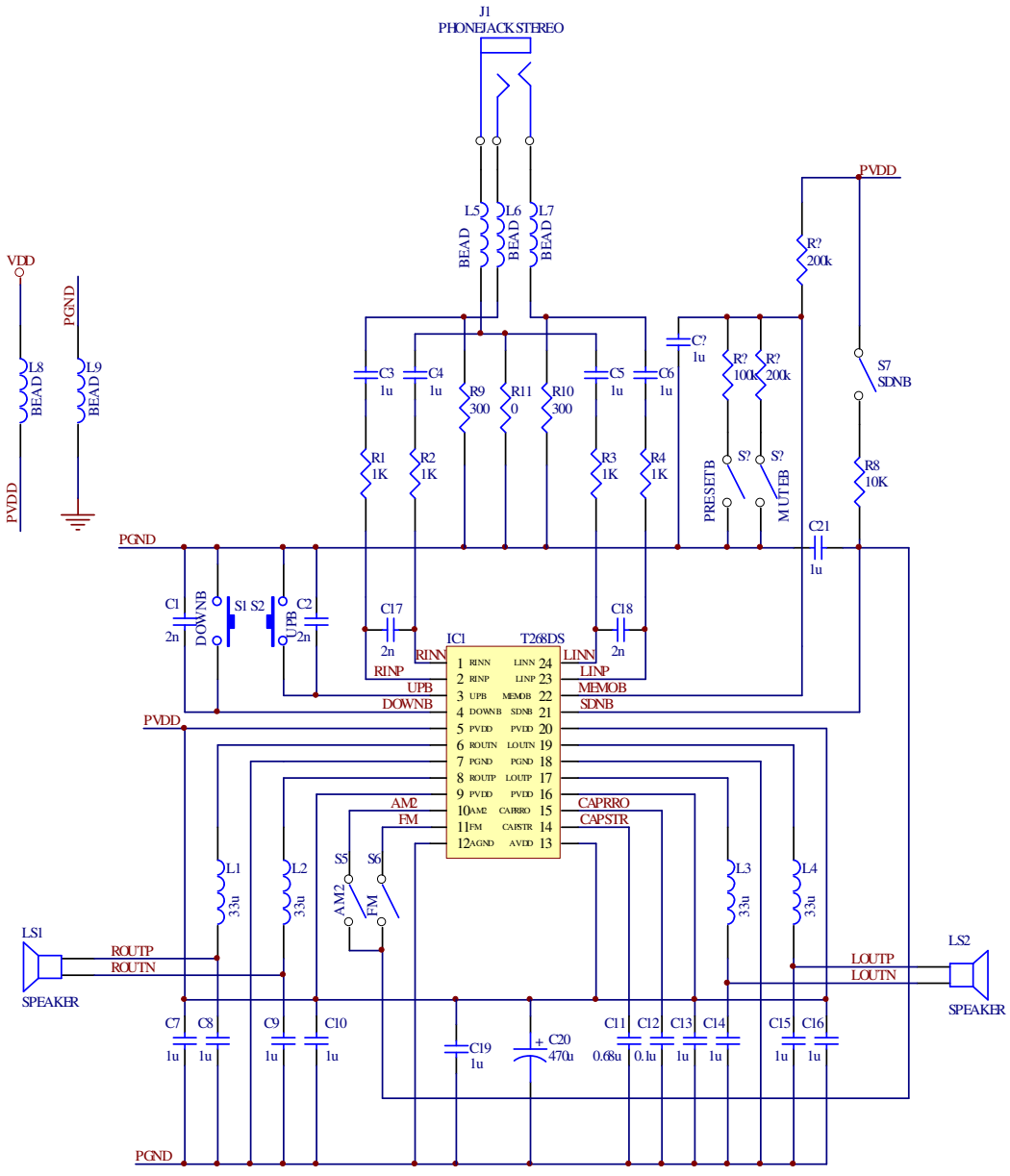
Note that the external components or PCB layout should be designed not to generate abnormal voltages to the chip to prevent from latch up which may cause damage to the device.

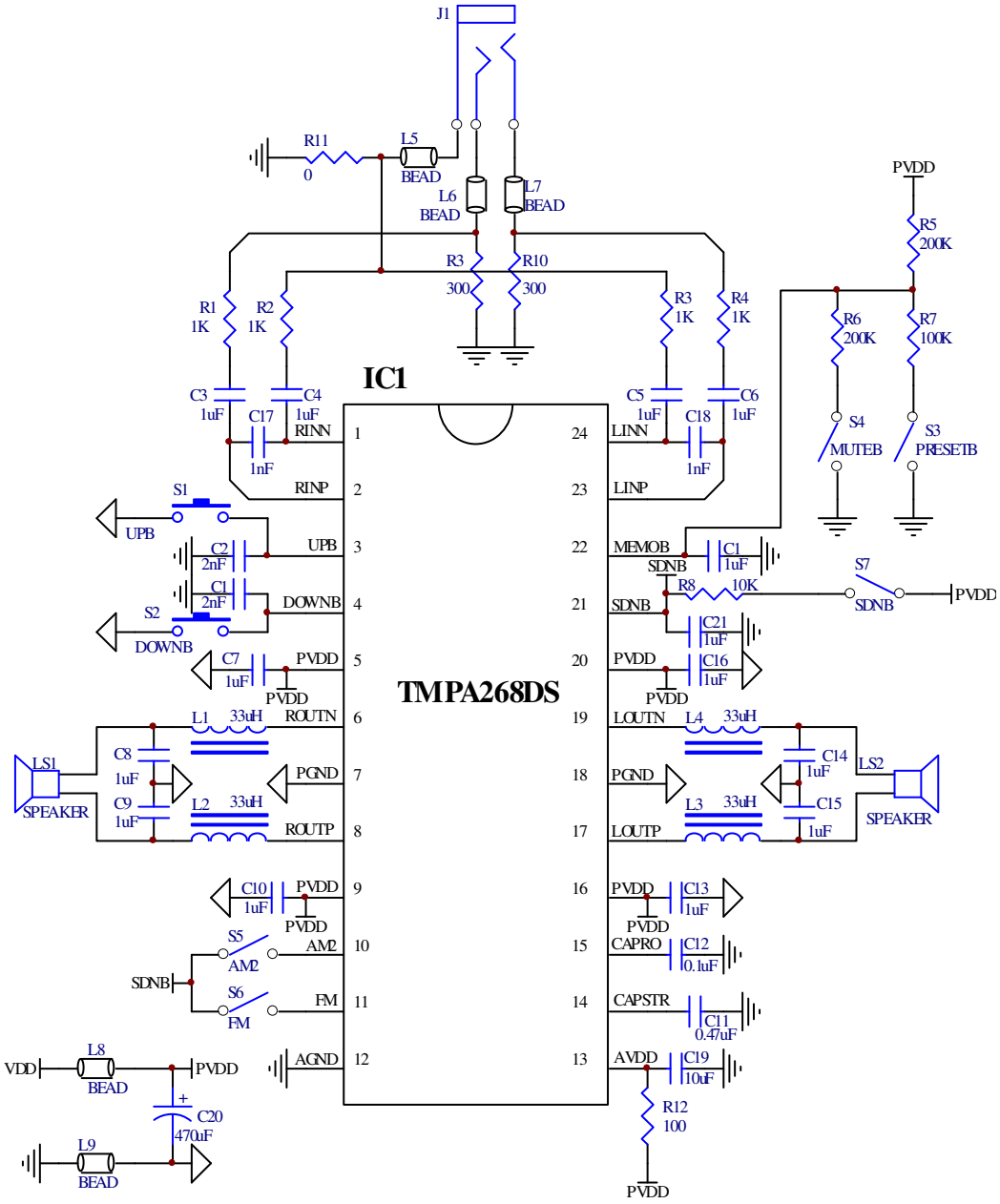
Typical Application 1. With bead only



Typical Application 2. With LC Filter



Typical Application 3. Simplified Application



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted(1)

Supply voltage, V_{DD}, AV_{DD}	In normal mode	-0.3V to 6V	V
	In shutdown mode	-0.3V to 7V	V
Input voltage, V_I		-0.3V to V_{DD}+0.3V	V
Continuous total power dissipation		See package dissipation ratings	
Operating free-air temperature, T_A		-40 to 85	℃
Operating junction temperature, T_J		-40 to 150	℃
Storage temperature, T_{stg}		-40 to 150	℃

(1) Stresses beyond those listed under"absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions "is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITONS

PARAMETER		TEST ONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage	V_{DD}, AV_{DD}		2.5		6	V
High-level input voltage, $V_{IH}1$	VIH for SDNB, AM2,FM	V_{DD}= AV_{DD} = 5V	2		V_{DD}	
Low-level input voltage, $V_{IL}1$	VIL for SDNB,AM2,FM		0		0.8	
High-level input voltage, $V_{IH}21$	VIH for MEMOB(to mute)		90%xV_{DD}		V_{DD}	
Low-level input voltage, $V_{IL}21$	VIL for MEMOB(to mute)		58%xV_{DD}		70%xV_{DD}	
High-level input voltage, $V_{IH}22$	VIH for MEMOB(to preset)		58%xV_{DD}		V_{DD}	
Low-level input voltage, $V_{IL}22$	VIL for MEMOB(to preset)		0		38%xV_{DD}	
High-level input voltage, $V_{IH}3$	VIH for UPB, DOWNB		3.5		V_{DD}	
Low-level input voltage, $V_{IL}3$	VIL for UPB, DOWNB		0		1.0	
Operating free-air temperature T_A			-40		85	℃

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR	$T_A \leq 25$ ℃ POWER RATING	T_A = 70 ℃ POWER RATING	T_A = 85 ℃ POWER RATING
TSSOP24	21.8 mW/ ℃	2.18W	1.2W	0.87W

ELECTRICAL CHARACTERISTICS

T_A=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	V_I=0V,Av=2, V_{DD}=AV_{DD}=2.5V to 5.5V		25		mV
PSRR	Power supply rejection ratio	V_{DD}=AV_{DD}=2.5V to 5.5V		-75	-55	dB
CMRR	Common mode rejection ratio	V_{DD}=AV_{DD}=2.5V to 5.5V, V_{IC}=1Vpp, RL=8Ω		-55	-50	dB
$\lvert I_{IH1} \rvert$	High-level input current	V_{DD}=AV_{DD}=5.5V, V_I= AV_{DD} (SDNB)		30		μA
$\lvert I_{IL1} \rvert$	Low-level input current	V_{DD}=AV_{DD}=5.5V, V_I=0V (SDNB)			0.1	μA
$\lvert I_{IH21} \rvert$ $\lvert I_{IH22} \rvert$	High-level input current	V_{DD}=AV_{DD}=5.5V, SDNB=High V_I= AV_{DD} (MEMOB)			±0.1	μA

		V_{DD}=AV_{DD}=5.5V, SDNB=Low V_I= AV_{DD} (MEMOB)		±0.1	
| I_{IL21} | | I_{IL22} |	Low-level input current	V_{DD}=AV_{DD}=5.5V, SDNB=High V_I=-0V (MEMOB)		±0.1	µA
		V_{DD}=AV_{DD}=5.5V, SDNB=Low V_I=-0V (MEMOB)		±0.1	
| I_{IH3} |	High-level input current	V_{DD}=AV_{DD}=5.5V, SDNB=High V_I= AV_{DD} (UPB, DOWNB)		±0.1	µA
		V_{DD}=AV_{DD}=5.5V, SDNB= Low V_I= AV_{DD} (UPB, DOWNB)		±0.1	
| I_{IL3} |	Low-level input current	V_{DD}=AV_{DD}=5.5V, SDNB=High V_I=0V (UPB, DOWNB)	30		µA
		V_{DD}=AV_{DD}=5.5V, SDNB= Low V_I=0V (UPB, DOWNB)		±0.1	
$I_{Q\ (OP)}$	Operating current / Ch (No Load)	V(SDNB)=5V, V_{DD}=AV_{DD}=5V	4.5		mA
$I_{Q\ (MU)}$	Mute current / Ch	V(SDNB)=5V, V_{DD}=AV_{DD}=5V	3.9		mA
$I_{Q\ (SD)}$	Shutdown current / Ch	V(SDNB)=0.8V, V_{DD}=AV_{DD}=2.5V to 5.5V	0.2	0.5	µA
$r_{DS(on)}$	Static output resistance	V_{DD}=AV_{DD}=5.5V	720		mΩ
f(sw)	Switching frequency	V_{DD}=AV_{DD}=5V, AM2=Low/FM=Low	380		kHz
		V_{DD}=AV_{DD}=5V,AM2/FM="other conditions"	*		
Avmax	Max. BTL Gain	V_{DD}=AV_{DD}=2.5V to 5.5V, RL=8Ω	23		db
R_{SDN}	Resistance from SDNB to GND	V(SDNB)= 5V	200		kΩ
Rud	Resistance from UpB / DownB to VDD	V(UPB)= V(DOWNB)=5V	200		kΩ
$Z_{I(min)}$	Input impedance	RINP, RINN, LINP, LINN	28		kΩ

＊Please refer to Hopping Frequency and Spread Spectrum

OPERATING CHARACTERISTICS

T_A=25 °C, L=33u, C=1u, R_L=8Ω speaker (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN TYP MAX	UNIT
P_O	Output power / Ch THD+N=10%,f=1kHz. (Limited by thermal condition)	R_L=8Ω	V_{DD}=AV_{DD}=5.5V.	1.9	W
		R_L=4Ω		3	
		R_L=3Ω		3.5	
		R_L=3Ω	V_{DD}=AV_{DD}=6V.	4.1	
THD+N	Total harmonic distortion plus noise	V_{DD}=AV_{DD}=5.5V, P_O=1W, R_L=8Ω, f=1kHz		0.29	%
		V_{DD}=AV_{DD}=5.5V, P_O=1.5W, R_L=4Ω, f=1kHz		0.25	
		V_{DD}=AV_{DD}=5.5V, P_O=2W, R_L=3Ω, f=1kHz		0.27	
SNR	Signal-to-noise ratio	V_{DD}=AV_{DD}=5.5V, P_O=1W, R_L=8Ω		95	dB
Crosstalk	Crosstalk between outputs	V_{DD}=AV_{DD}=5.5V, P_O=1W R_L=8Ω		-62	dB

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO		
AGND	12	-	Analog ground
AM2	10	I	AM2 mode to hop frequency in case of radio interference
AV_{DD}	13	-	Analog power supply
CAPRRO	15	O	Capacitance for delay after protection
CAPSTR	14	O	Capacitance for power up delay and UPB/DOWNB reaction time
DOWNB	4	I	Volume down (active low logic)
FM	11	I	FM mode to spread PWM spectrum to reduce EMI
PGND	7,18	-	Digital ground
LINN	24	I	Negative input of left channel
LINP	23	I	Positive input of left channel
LOUTN	19	O	Negative output of left channel
LOUTP	17	O	Positive output of left channel
RINN	1	I	Negative input of right channel
RINP	2	I	Positive input of right channel
MEMOB	22	I	Memory of volume after power removal (active low logic)
ROUTN	6	O	Negative output of right channel
ROUTP	8	O	Positive output of right channel
SDNB	21	I	Shutdown control (active low logic)
UPB	3	I	Volume up (active low logic)
PV_{DD}	5,9,16,20	-	Digital Power supply

TYPICAL CHARACTERISTICS

Note 1. Input coupling 1µF capacitors are used for all measurements.

2. Differential inputs are applied and BTL outputs are measured.

3. Balanced LC filter is used for THD+N measurement and power efficiency measurement.

4. Characteristic frequency of the LC filter is set 41 KHz unless otherwise specified.

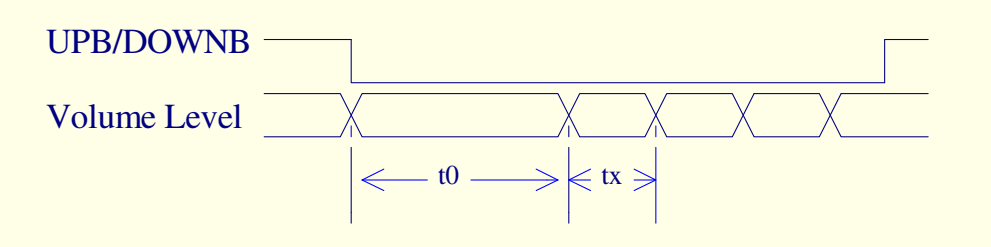
Volume Step and Attenuation at Vdd=5v (set by design, not measured)

Step	Attenuation(dB)	Overall AV(dB)	Step	Attenuation(dB)	Overall AV(dB)	Step	Attenuation(dB)	Overall AV(dB)
0	0	23	11	12	11	22	36	-13
1	1	22	12	14	9	23	39	-16
2	2	21	13	16	7	24	42	-19
3	3	20	14	18	5	25	45	-22
4	4	19	15	20	3	26	48	-25
5	5	18	16	22	1	27	51	-28
6	6	17	※17	24	-1	28	54	-31
7	7	16	18	26	-3	29	∞	-∞
8	8	15	19	28	-5			
9	9	14	20	30	-7			
10	10	13	21	33	-10			

※ Overall gain is preset at -1db after a low at MEMOB. Power up does not necessary preset voltage gain to -1 db. Please refer to **Memory of voltage gain/Mute** for details.

Volume UP/DOWN Control

- Volume up and down control are executed by UPB and DOWNB digital input signals.
- UPB and DOWNB are “low” active.
- Continuous “low” at UPB or DOWNB will make volume to change continuously.
- A “low” at DOWNB overwrites a “low” at UPB.
- Timing diagram(capacitance at CAPSTR pin is 1uF for following timing relationship)



1. First volume change is set at ~0.5s(t0) delay after falling edge of UPB/DOWNB input. If UPB/DOWNB low time is less than 0.5s, there will be no volume change.

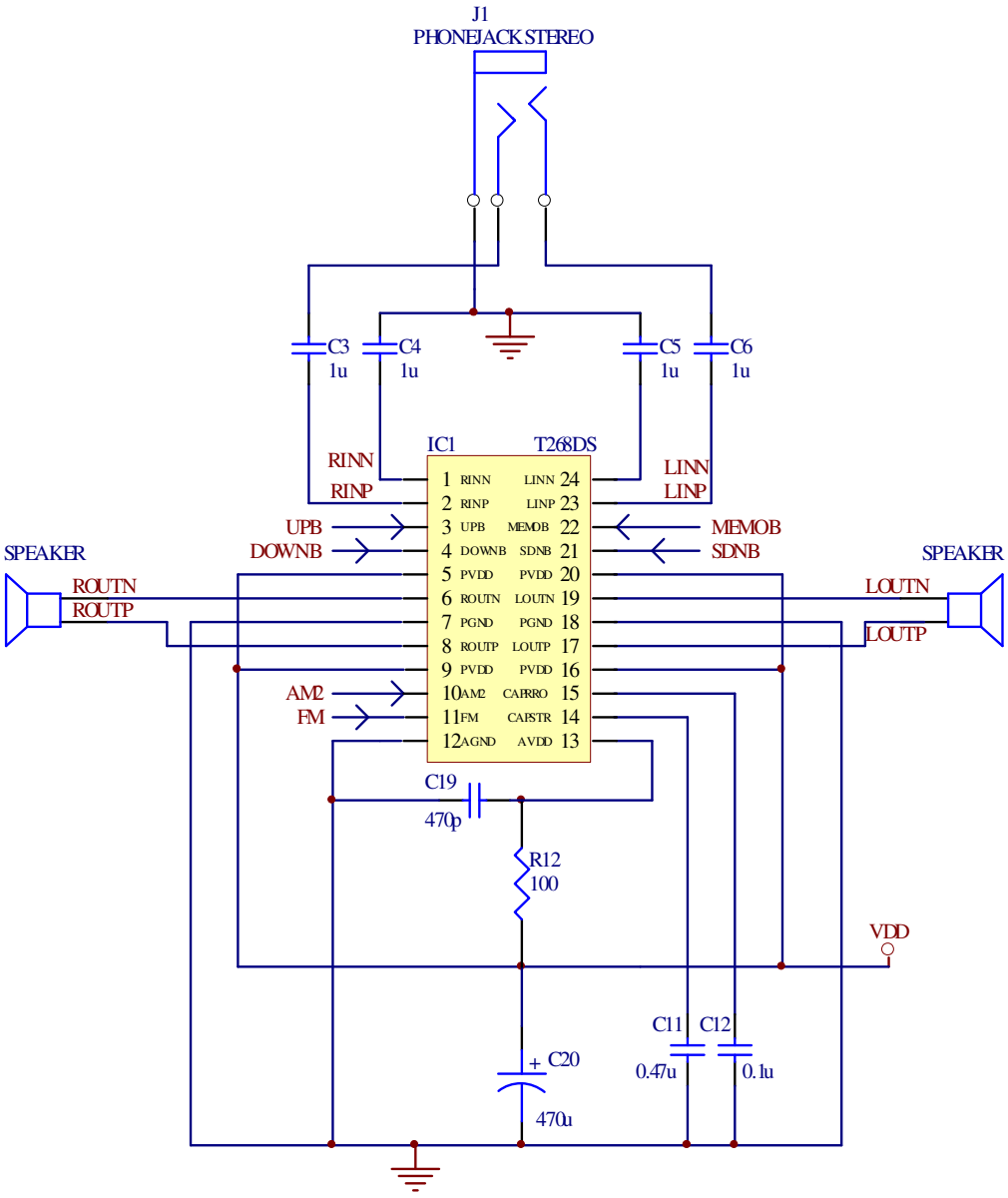
2. Following volume changes are set at ~0.1s(tx) from previous change.

Note that the capacitance at pin CAPSTR=0.47uF is for t0=0.45s & t1=0.09s. The delay time t0 & t1 change linearly with capacitance at CAPSTR pin, i.e. t0=0.21s & t1=0.04s if CAPSTR=0.22uF.

Hopping Frequency and Spread Spectrum

AM2/FM		Switching Frequency (typical) at 5V
0	0	380 KHz
0	1	360 KHz ± 15 KHz
1	0	330 KHz ± 15 KHz
1	1	360 KHz ± 30 KHz

APPLICATION INFORMATION



DETAILED DESCRIPTION

Efficiency

The output transistors of the device behave like switches. The power loss is mainly due to the turn on resistance of the output transistors when driving current to the load. As the turn on resistance is so small that the power loss is small and the power efficiency is high. With 8 ohm load the power efficiency can be up to 91%.

Automatic output Power Control (APC)

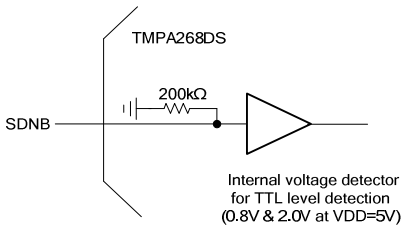
The voltage gain is self adjusted in the chip over voltage range. This means that, regardless the change of supply voltage, the output power keeps about the same for a given input level from V_{DD}=6v to 2.5v. It allows the best use of the battery.

Low voltage detection

A low voltage detector is integrated in the device to detect the V_{DD} voltage. When the V_{DD} voltage is below 1.8 volts the detector will mute the device. The device resumes to normal operation when the V_{DD} voltage goes above 2.15 volts.

Shutdown

The shutdown mode reduces power consumption to sub-micro watt. A LOW at SDNB pin forces the device to shutdown mode and a HIGH forces the device to normal operating mode. Floating at SDNB is also defined as a LOW. Internal circuit for shutdown pin is shown below.

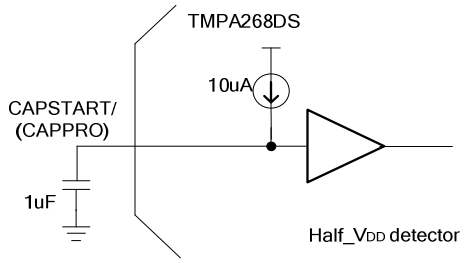


CAPSTR for Pop-less and Volume Change

A soft start capacitor can be added to the CAPSTR pin. This capacitor introduces a delay for the amplifier to be stable before driving the load. Thus the pop or click noise when power up/down or switching to/from shutdown mode can be eliminated. CAPSTR capacitor is also used to control how fast the UPB or DOWNB changes the volume. The update speed of the volume change by UPB/DOWNB is illustrated in the timing diagram.

CAPSTR provides a way of soft startup delay. A 10uA current source and a half_ V_{DD} detector are integrated in the chip. The charge capacitor is externally hooked up. For C=1uF the half_ V_{DD} delay is

T = CV / I = （1uF × 2.5V）/ 10uA = 0.25 seconds



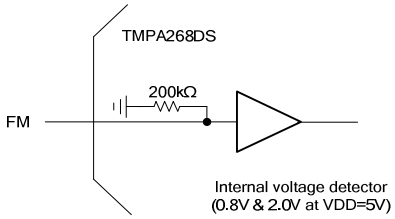
The delay time is proportional to the value of the capacitance. By changing the capacitance the delay time can be changed accordingly. This is true for both start-up delay and volume change intervals.

CAPPRO for mute and protection

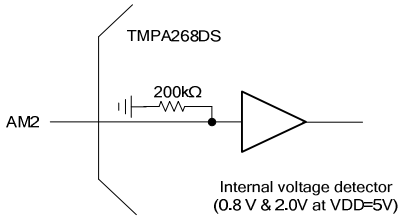
A capacitor at CAPPRO is used to add delay time after mute release and protection release. The delay time is proportional to the CAPPRO capacitance and the structure of CAPPRO pin is the same as CAPSTR pin. A 1uF capacitance introduces 0.25 seconds delay after mute release. It introduces 100ms~500ms delay after protection recover and the delay time depends on how protection is generated. For protection delay, please refer to Over Temperature Protection and Over Current Protection.

FM Mode and AM2 Mode

To decrease interference to FM receiver or to reduce EMI, FM pin can be connected to V_{DD} to spread the PWM switching frequencies. The FM pin can be left floating or connected to ground if spread spectrum is not necessary.



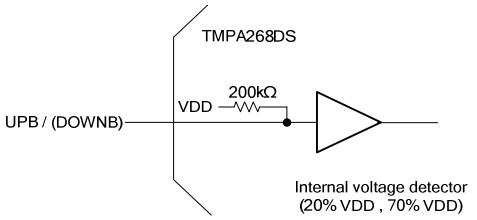
AM2 pin can be left floating or grounded. But when TMPA268DS is incorporated with AM receiver and if interference happens, AM2 can be connected to V_{DD} to change PWM switching frequency when FM is low. This may avoid the interference to AM receiver. Thus a control signal to AM2 input is suggested to switch between V_{DD} and ground as need. A push button can be used to switch PWM frequencies back and forth manually when AM/SW receiver is incorporated.



Please refer to Hopping Frequency and Spread Spectrum for details.

Voltage gain(UPB/DOWNB)

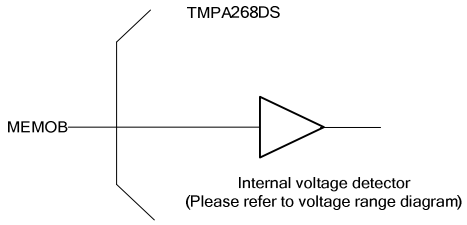
The voltage gain is preset, at power up, to -1db typical with 8 ohms load. The voltage gain can be increased by applying a LOW at UPB or decreased by applying a LOW at DOWNB. The maximum gain it can reach is 23db and the minimum gain is -31db. Beyond -31db is a MUTE. The threshold voltage for UPB/DOWNB input pins is 1 volt to reduce interference caused by unwanted glitches at UPB or DOWNB inputs. Please refer to Volume Step and Attenuation table for voltage gain.



Memory of voltage gain/Mute

Memory of voltage gain:

The voltage gain is preset to -1db at power up. The voltage gain can be changed to higher or lower value by applying a LOW at UPB or DOWNB. The changed voltage gain can be memorized during shutdown. In other words the voltage gain is the same before and after shutdown operation. A voltage below 38% V_{DD} at MEMOB resets the voltage gain to preset value or -1db. Note that a RC delay is necessary between V_{DD} & MEMOB at power up to ensure proper operation of the memory.



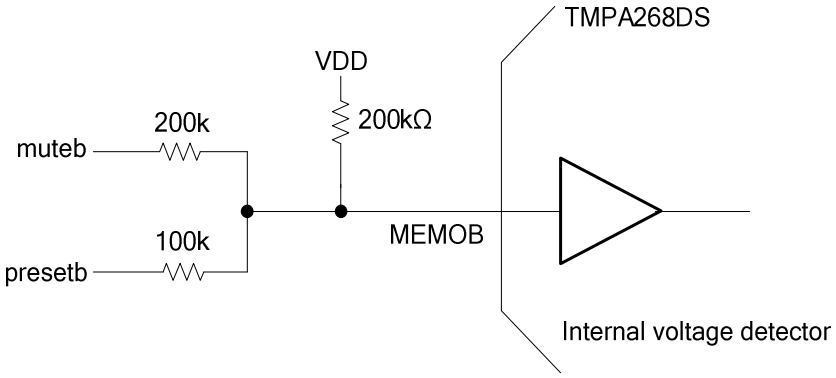
During shutdown mode, memory of voltage gain is still in effect even battery is removed for some time if a decoupling capacitor is applied between V_{DD} and ground. The time period in which the voltage gain is still memorized during battery removal depends on the V_{DD} -GND capacitance and V_{DD} voltage.

Example 1. Two-battery power supply with V_{DD} -GND capacitance equals 1000uF.
If the voltage of each exhausted battery to be replaced is 1.0v on average then the voltage on the 1000uF capacitor is 2.0v. The voltage allowed to drop is 2.0v-1.3v=0.7v. With typical leakage current of 0.2uA the time to survive is

$$CV/I = 1000uF \times 0.7v / 0.2uA = 3500 \text{ sec} \fallingdotseq 1 \text{ hrs}$$

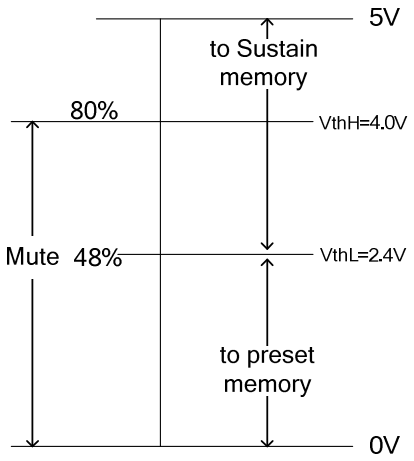
Mute:
Mute of output signals is enabled by applying a voltage between 70% V_{DD} and 58% V_{DD} at MEMOB. A voltage below 38% V_{DD} applied at MEMOB may preset the volume to -1db after mute as described before.

The input voltage at MEMOB to
1. preset memory of voltage gain is below 38% V_{DD}.
2. mute output signals is between 58% V_{DD} and 70% V_{DD}.



(Please refer to voltage range diagram)

A diagram below is to show the control voltage range. Note that to ensure proper operation, a margin of 10% V_{DD} is required to compensate for process variation and V_{DD} fluctuation.



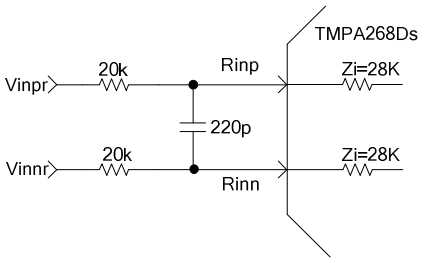
As shown above the threshold voltages to mute and preset memory are 80% V_{DD} and 48% V_{DD} respectively at 5V.

Input filter

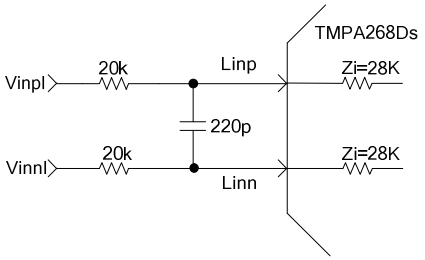
Input filter is not required for most of the applications. However in some designs if it is necessary to reduce overall voltage gain, one can add an external input resistor as a voltage divider. It is advantageous to add a capacitor in between positive input and negative input to form an input filter.

An example to reduce voltage gain to 58% at maximum gain, as shown in the schematic on

page 3 and page 4, is also shown below. Note that the layout of input traces has to be symmetric.

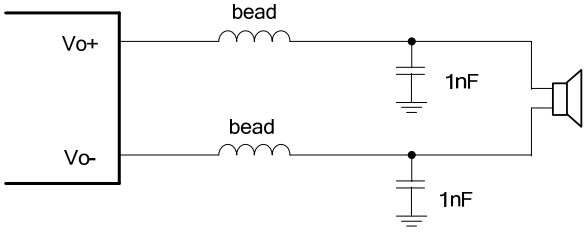


voltage gain = 28k / (20k + 28k) = 58%



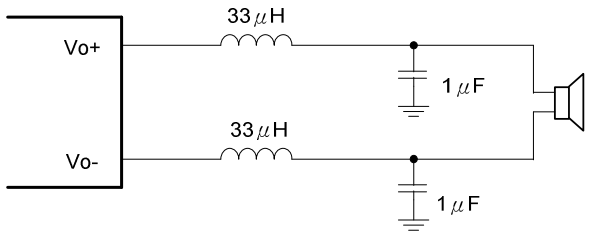
Output filter

With spread spectrum technique, output LC filter is not necessary, instead ferrite bead is used for EMI reduction. The ferrite filter reduces EMI around 1 MHz and higher（FCC and CE only test radiated emissions greater than 30 MHz）. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies. Under some special operating condition LC output filter may be necessary if there are low frequency（＜1 MHz）EMI sensitive circuits and/or there are long wires from the amplifier to the speaker. EMI is also affected by PCB layout and the placement of the surrounding components.

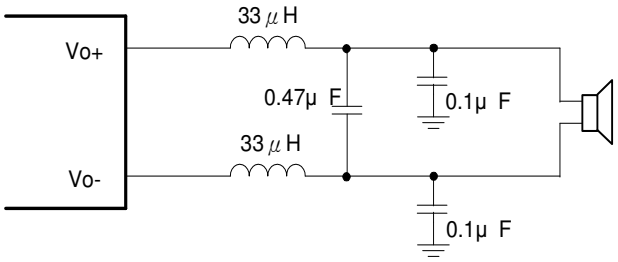


With bead (No LC Filter)

The suggested LC values for different speaker impendence are showed in following figures for reference.



Typical LC Output Filter (1)



Typical LC Output Filter (2)

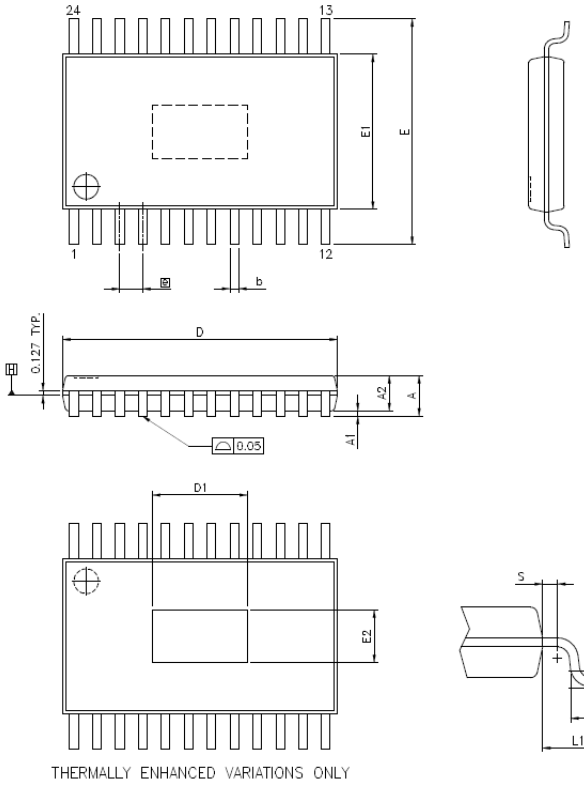
Over temperature protection

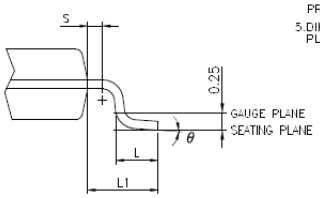
A temperature sensor is built in the device to detect the temperature inside the device. When a high temperature around 145°C and above is detected the switching output signals are disabled to protect the device from over temperature. Automatic recovery circuit enables the device to come back to normal operation when the internal temperature of the device is below around 120 °C. However there is a delay between protection release and output signal enable. The delay time is explained in CAPPRO for mute and protection. Note that the delay time is proportional to the capacitance connected to CAPPRO pin.

Over current protection

A current detection circuit is built in the device to detect the switching current of the output stages of the device. It disables the device when the current is beyond about 3.5amps. It protects the device when there is an accident short between outputs or between output and power/ground pins. It also protects the device when an abnormal low impedance is tied to the output. Automatic recovery circuit enables the device to come back to normal operation after ~100ms delay. If short circuit condition is not removed it will be detected and the protection circuit is activated again. The protection circuit will switch on and off until the short circuit condition removed. The speaker, if connected, will give cracking noise to warn such a short circuit condition. Note that the delay time is proportional to the capacitance connected to CAPPRO pin.

Physical Dimensions (IN MILLIMETERS)





VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

5 THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
74X18E	1.50	1.88	3.70	4.62
112X18E	2.28	2.85	3.70	4.62

NOTES:
1. JEDEC OUTLINE : MO-153 AD/MO-153 ADT(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

TSSOP24

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