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1. Feature/显示特性

Display resolution/点阵数 : 16(列)*2(行)个字符

Display mode/显示模式 : STN ,Positive, Transmissive（黄绿膜，正显，全透明）

Driving method/驱动方式 : 1/16 Duty , 1/4 Bias

Viewing direction/视角 : 12:00 o'clock

Backlight/背光 : LED , White(or Other)

Built-in controller/控制器 : ST7032

Operation temp/工作温度 : 0℃~50℃

Storage temp/储存温度 : -10℃~60℃

2. Mechanical Specifications/外形尺寸说明

2.1 尺寸描述

Dimensional outline (W*H*T)/外形尺寸 : 68.6.0mm*26.0mm*2.8mm（+BL5.0）

Viewing area (W*H)/视域尺寸 : 64.6mm*16.0mm

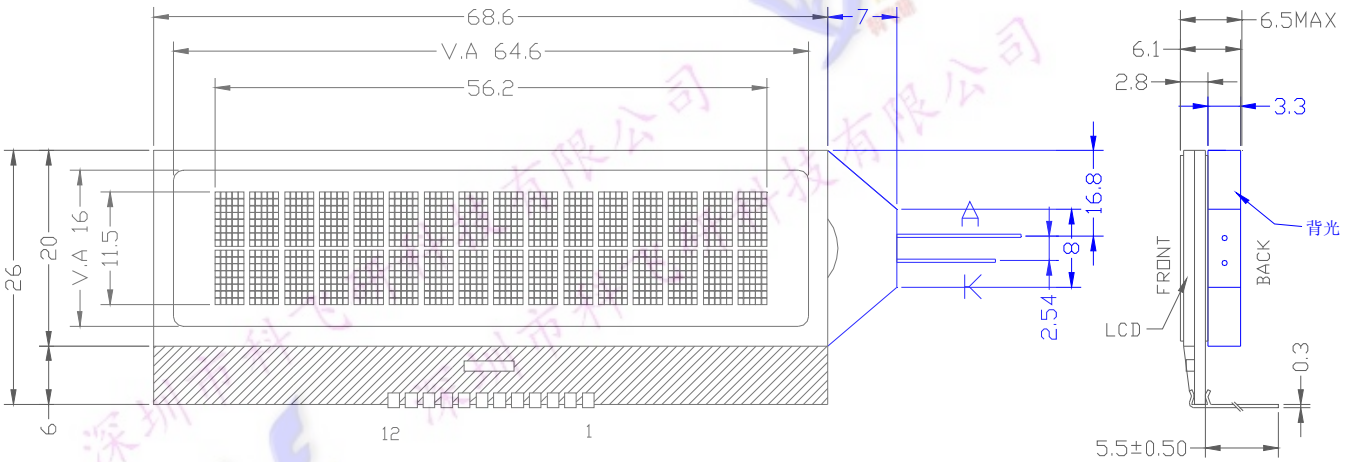
Active area(W*H)/显示尺寸 : 56.25mm*11.5mm

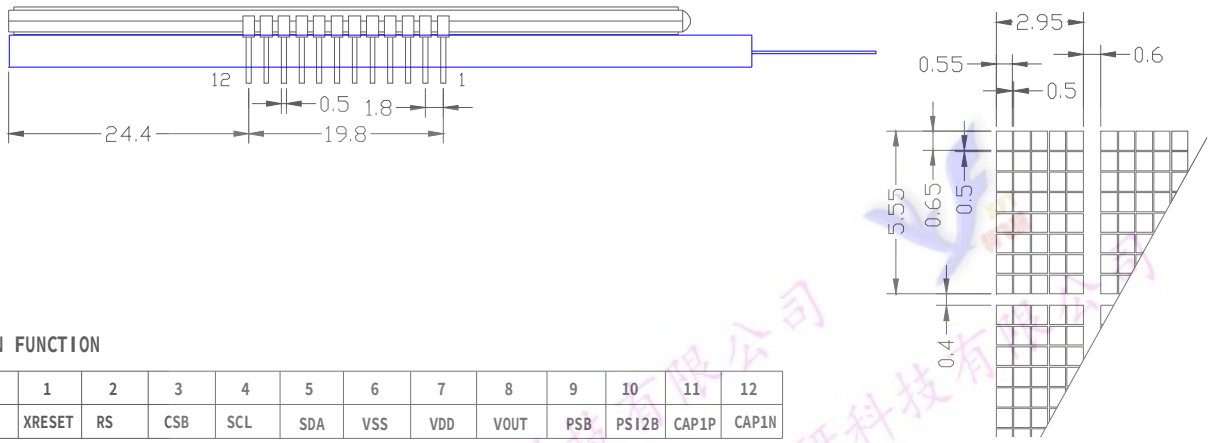
Dot pitch (W*H)/点距 : 0.6mm*0.7mm

Dot size (W*H)/点大小 : 0.55mm*0.65mm

Weigh/重量 t : Approx

2.2 Outline Dimension 外形尺寸图



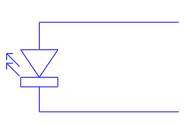


LCD PIN FUNCTION

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12
SYMBOL	XRESET	RS	CSB	SCL	SDA	VSS	VDD	VOUT	PSB	PSI2B	CAP1P	CAP1N

Specifications:
1> LCD Display Type : STN,Positive,
2> Polarizer : Transmissive
3> Viewing Direction : 12 O'CLOCK
4> Drive Method : 1/16Duty; 1/4Bias
5> Operating Voltage : VDD: 3.3V or 5.0'
VOP: 5.6V
6> Operating Temperature : 0°C~50°C
7> Storage Temperature : -10°C~60°C
8> Driver IC: ST7032
9> Connector: PIN

Backlight Circuit



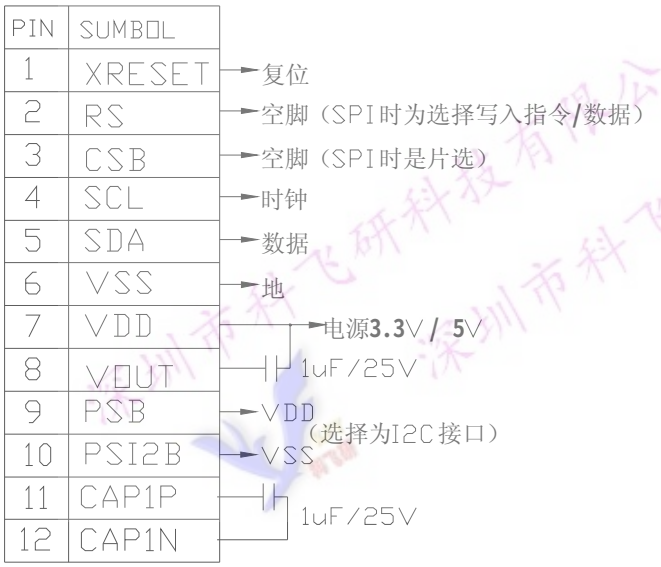
(If=10~15mA;Vf=3.0V±0.2)

注:此款可以3.3V\5V,但请注意对比度需要通过程序进行调整,另配套背光时也需注意背光的限流,
需要根据供电参数及LED背光参数进行限流处理(加限流电阻)。

3.Block Diagram & Power supply/电路原理图

COG1602-7532

I2C 电路参考图



SPI 电路参考图

4. Pin description/PIN 脚描述

Pin No.	Pin Name	Function
1	XRESET	External reset pin. Only if the power on reset used, the XRESET pin must be fixed to VDD. Low active. 复位
2	RS	Select registers. 0: Instruction register (for write) Busy flag & address counter (for read) 1: Data register (for write and read) 选择写入指令或是数据
3	CSB	Chip select input pin. 片选
4	SCL	Clock input pin. 时钟
5	SDA	Input Data pin. 数据
6	VSS	GND. 0V 地
7	VDD	Power Supply. 3.3V or 5.0V 电源
8	VOUT	Connect capacitors Ground 倍压输出（与VDD接一电容）
9	PSB	Interface selection 0:serial mode ("E" must connect to "VDD" when serial mode is selected.) 1:parallel mode(4/8 bit) In I^2C interface PSB must connect to VDD
10	PSI2B	SI4:PSB=0,PSI2B=1 ; SI2(IIC):PSB=1,PSI2B=0
11	CAP1P	Conntet capacitors between CAP1P and CAP1N 接电容
12	CAP1N	Pin11与Pin12之间接电容

5. Absolute Maximum Ratings/限定参数

Items	Symbol	MIN.	MAX.	Unit	Condition
Supply Voltage/供电电压	VDD	-0.3	+5.5	V	Vss = 0V
	Vlcd	-0.3	+7.0	V	Vss = 0V
Input Voltage/输入电压	VIN	-0.3	VDD+0.3	V	Vss = 0V
LED forward current/背光电流	If	0	60	mA	---
Operating Temp./工作温度	TOP	0	+50	℃	---
Storage Temp./储存温度	Tst	-10	+60	℃	---

6. Electrical Characteristics/电气特性

6.1 Typical Electrical Characteristics

■ DC Characteristics

(TA = 25℃ , VDD = 2.7 V – 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	2.7	-	4.5	V
V_{LCD}	LCD Voltage	V0-Vss	2.7	-	7.0	V
I_{CC}	Power Supply Current	VDD=3.0V (Use internal booster/follower circuit)	-	160	230	uA
V_{IH1}	Input High Voltage (Except OSC1)	-	1.9	-	VDD	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.8	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7 VDD	-	VDD	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	0.2 VDD	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -1.0mA	0.75 VDD	-	-	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 1.0mA	-	-	0.8	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8 VDD	-	VDD	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.2 VDD	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to VDD	-1	-	1	μA
I_{PUP}	Pull Up MOS Current	VDD = 3V	20	30	40	μA
fOSC	Oscillation frequency	VDD = 3V,1/17duty	350	540	1100	KHz

■ DC Characteristics

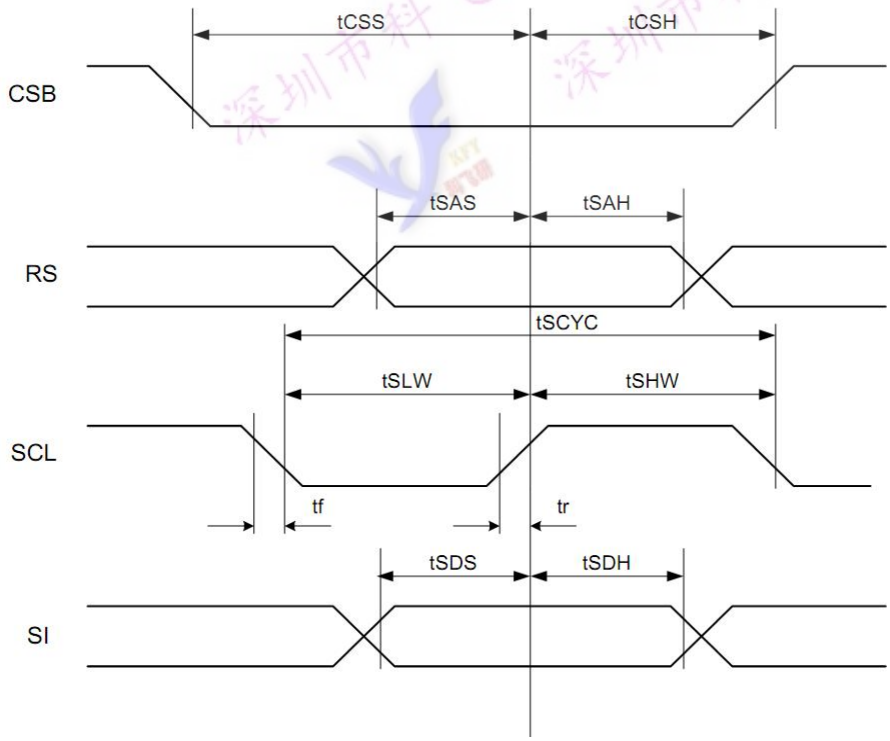
(TA = 25℃, VDD = 4.5 V - 5.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	4.5	-	5.5	V
V_{LCD}	LCD Voltage	V0-Vss	2.7	-	7.0	V
I_{CC}	Power Supply Current	VDD=5.0V (Use internal booster/follower circuit)	-	240	340	uA
V_{IH1}	Input High Voltage (Except OSC1)	-	2.7	-	VDD	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	-0.3	-	0.8	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7 VDD	-	VDD	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	1.0	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -1.0mA	3.8	-	VDD	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 1.0mA	-	-	0.8	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8 VDD	-	VDD	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.2 VDD	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to VDD	-1	-	1	μA
I_{PUP}	Pull Up MOS Current	VDD = 5V	65	95	125	μA
fOSC	Oscillation frequency	VDD = 5V,1/17duty	350	540	1100	KHz

6.2 Timing Specifications

6.2.1

- **Serial Interface**



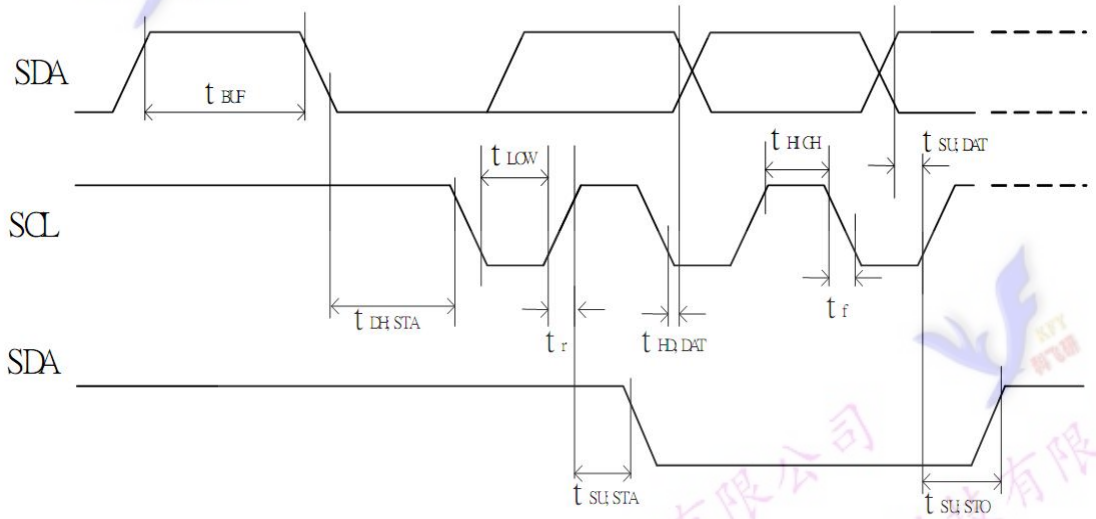
(Ta = 25°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
Serial Clock Period	SCL	tSCYC	—	200	-	100	-	ns
SCL "H" pulse width		tSHW		20	-	20	-	
SCL "L" pulse width		tSLW		160	-	120	-	
SCL Rise/Fall time	SCL	tr,tf	—	-	20	-	20	ns
Address setup time	RS	tSAS	—	10	-	10	-	ns
Address hold time		tSAH		250	-	150	-	
Data setup time	SI	tSDS	—	10	-	10	-	ns
Data hold time		tSDH		10	-	20	-	
CS-SCL time	CS	tCSS	—	20	-	20	-	ns
		tCSH		350	-	200	-	

*1 All timing is specified using 20% and 80% of VDD as the standard.

6.2.2

- **I2C interface**

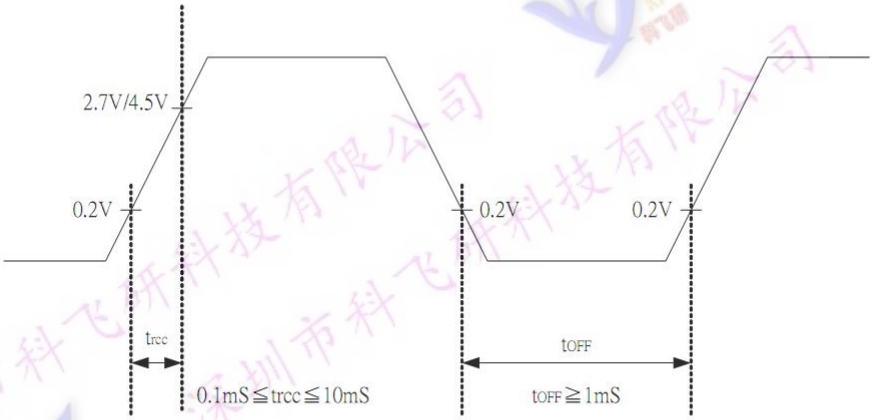


(Ta = 25°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}		0.6	–	0.6	–	
Data set-up time	SI	$t_{SU;DAT}$	—	**180**	–	100	–	ns
Data hold time		$t_{HD;DAT}$		0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCL,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	–	400	–	400	pf
Setup time for a repeated START condition	SI	$t_{SU;STA}$	—	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	–	1.3	–	us

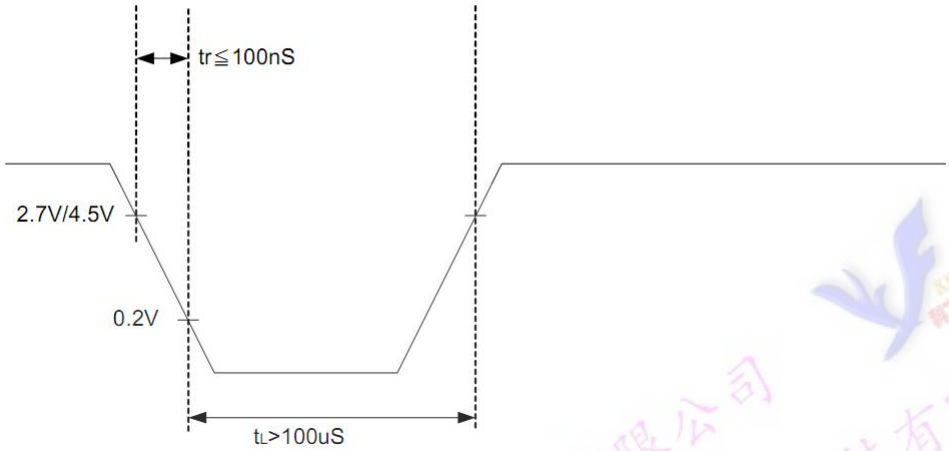
6.3 Reset timing

- **Internal Power Supply Reset**



Notes:
- tOFF compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 4.5V for 5V operation,and at 2.7V for 3V operation.
- If 2.7V/4.5V is not reached during 3V/5V operation, internal reset circuit will not operate normally.

- **Hardware reset(XRESET)**



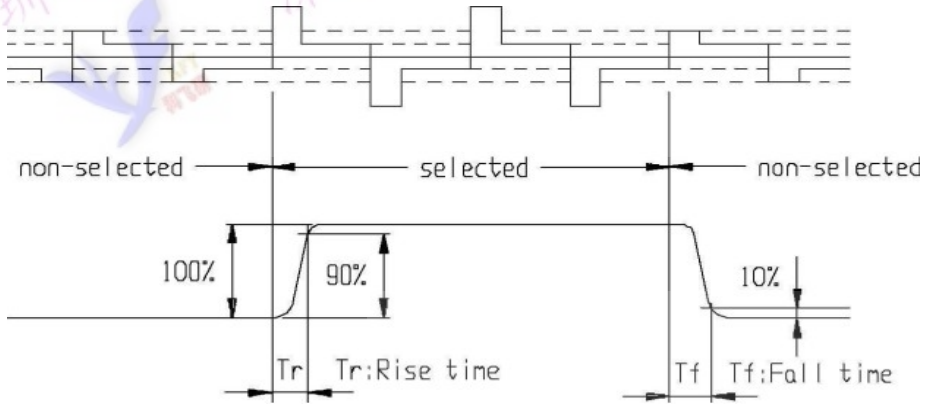
7. Backlight Characteristics/背光特性

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forward Voltage/电压	Vf	2.8	3.0	3.1	V	If=10mA
Reverse current/电流	Ir	---	10	15	mA	Vr=3V
Peak wave length/波长	λ	---	---	---	nM	If=10mA
Luminance/亮度	Lv	---	---	---	Cd/m^2	If=10mA
Color /颜色	White (白色，或者其他色)					
引脚定义	A：正极（3V）； K：负极（0V 或接 VSS）					

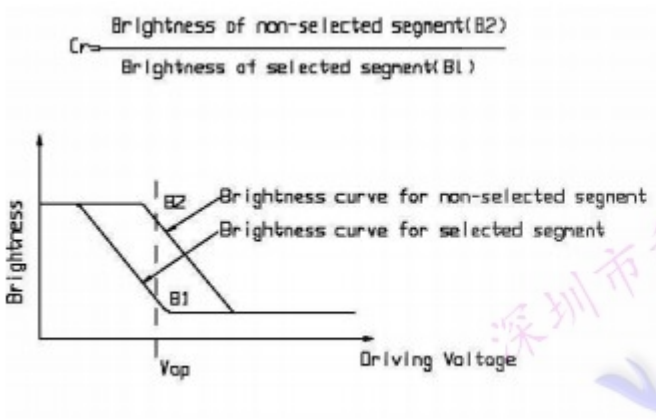
8. Electrical-Optical Characteristics/光学特性

Items	Symbol	Condition	MIN.	TYP.	MAX.	Unit	NOTE
Response time/反应时间	Tr	Ta= 25℃	---	250	---	ms	2
	Tf		---	400	---		
Contrast ratio/对比度	Cr	Ta= 25℃	---	--	---		3
Viewing angle range/视角范围	θ	Cr≥2	-40	---	40	degree	

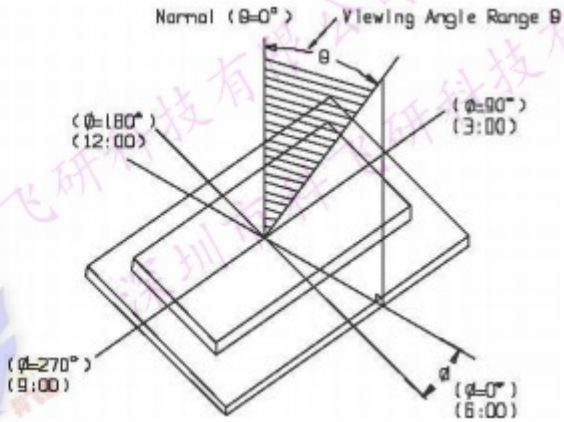
Note 1. Definition of response time



Note2 . Definition of Contrast Ratio‘Cr’



Note 3. Definition of Viewing Angle Range ‘θ’



9. Control and display commands/指令表

➢ instruction table at "Extension mode"

(when "EXT" option pin connect to Vss, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380KHz	OSC= 540kHz	OSC= 700KHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	DH	*0	IS	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS: instruction table select	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us

Note * : this bit is for test command , and must always set to "0"

Instruction table 0(IS=0)														
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us

Instruction table 1(IS=1)														
Internal OSC frequency	0	0	0	0	0	1	BS	F2	F1	F0	BS=1:1/4 bias BS=0:1/5 bias F2~0: adjust internal OSC frequency for FR frequency.	26.3 us	18.5 us	14.3 us
Set ICON address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	26.3 us	18.5 us	14.3 us
Power/ICON control/Contrast set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us
Follower control	0	0	0	1	1	0	Fon	Rab 2	Rab 1	Rab 0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	26.3 us	18.5 us	14.3 us
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us

10. DDRAM 映射表

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 7 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (A_{DD}) is set in the address counter (AC)as hexadecimal.

- **2-line display (N = 1) (Figure 10)**

Case 1: When the number of display characters is less than 40 ，2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. See Figure 10.

Display Position	1	2	3	4	5	6		38	39	40
DDRAM Address (hexadecimal)	00	01	02	03	04	05	.....	25	26	27
	40	41	42	43	44	45	.....	65	66	67

Figure 10. 2-Line Display

Case 2: For a 16-character ，2-line display See Figure 11.
When display shift operation is performed, the DDRAM address shifts. See Figure 11.

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
For Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
For Shift Right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

Figure 11. 2-Line by 16-Character Display Example

Table 3. Correspondence between Character Codes and Character Patterns

ST7032-0D (ITO option OPR1=1, OPR2=1)

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																
0010																
0011																
0100																
0101																
0110																
0111																
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

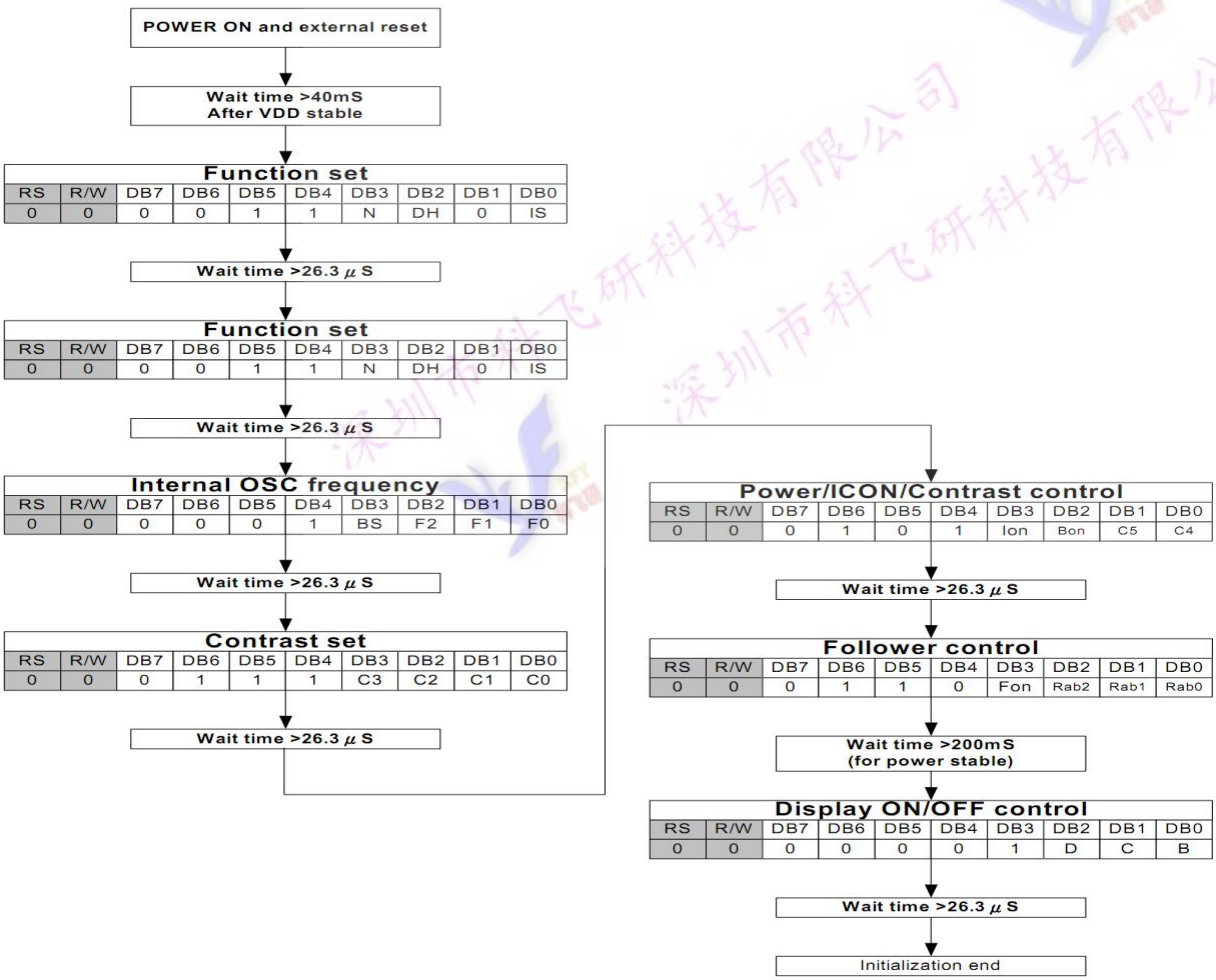
Character Code (DDRAM Data)								CGRAM Address						Character Patterns (CGRAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
					0	0	0				0	0	1				0	0	1	0	0
					0	0	0				0	1	0				0	0	1	0	0
					0	0	0				0	1	1				0	0	1	0	0
					0	0	0				1	0	0				0	0	1	0	0
					0	0	0				1	0	1				0	0	1	0	0
					0	0	0				1	1	0				0	0	1	0	0
					0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
					0	0	1				0	0	1				1	0	0	0	1
					0	0	1				0	1	0				1	0	0	0	1
					0	0	1				0	1	1				1	1	1	1	0
					0	0	1				1	0	0				1	0	1	0	0
					0	0	1				1	0	1				1	0	0	1	0
					0	0	1				1	1	0				1	0	0	0	1
					0	0	1				1	1	1				0	0	0	0	0

Table 4. Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

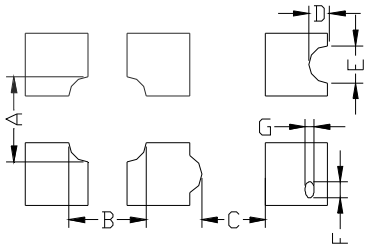
Notes:
1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 4, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. "1" for CGRAM data corresponds to display selection and "0" to non-selection,"-" Indicates no effect.
6. Different OPR1/2 ITO option can select different CGRAM size.

11. Initializing by Instruction 初始化流程

- **Serial interface & IIC interface (fosc = 380KHz)**



12. Inspection Standards/检验标准

Item	Criterion for defects	Defect type
1) Display on inspection/显示效果	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot/黑点或白点	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line/黑线或白线	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern/显示模式	 $\frac{A+B}{2}\leq 0.28$ | $0<C$ | $\frac{D+E}{2}\leq 0.25$ | $\frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity/均匀度	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer/玻璃内有气泡	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer/玻璃刮痕/凹痕	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel/玻璃上有污点	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color/杂色	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10)Viewing-area encroachment/玻璃边线出现在视域	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance/铁筐外观	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface 表面缺裂	Evident crevices that are visible are rejected.	Minor
13) Parts mounting/部件安装	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment/部件结合度	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball,solder hips)/杂质（焊接遗留物）	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw/铁筐缺裂	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)/标志	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor