LITE ARRAY OLED (BVI) CO. LTD.

MODULE NO.: LPST128064A00-AB
DOC.REVISION: 0.0

	SIGNATURE	
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PRODUCT PREVIEW

Product Part#:	**LPST128064A00-AB**
Product Name:	**128x64 Area Color OLED Module**
Revision:	**0.0**
Date:	**Feb'2005**

REVISION RECORD

Revision	Description of Revision	Revision date	Remark
0.0	Initial release	17-Feb-05	--

TABLE OF CONTENTS

1. FUNCTIONS & FEATURES

1.1. Format	: 128*64 dots
1.2. Display mode	: Passive Matrix
1.3. Display color	: Area Color (Light Blue, Yellow)
1.4. Duty	: 1/64

2. MECHANICAL SPECIFICATIONS

2.1. Module size	: 30.00mm(W)*34.66mm(H)
2.2. Panel size	: 30.00mm(W)*20.16mm(H)
2.3. Viewing area	: 25.02mm(W)*13.86mm(H)
2.4. Active area	: 23.02mm(W)*11.86mm(H)
2.5. Dot pitch	: 0.18mm(W)*0.18mm(H)
2.6. Dot size	: 0.16mm(W)*0.16mm(H)
2.7. Thickness(with polarizer)	: 1.80mm
2.8. Weight	: 2.0g

3. BLOCK DIAGRAM

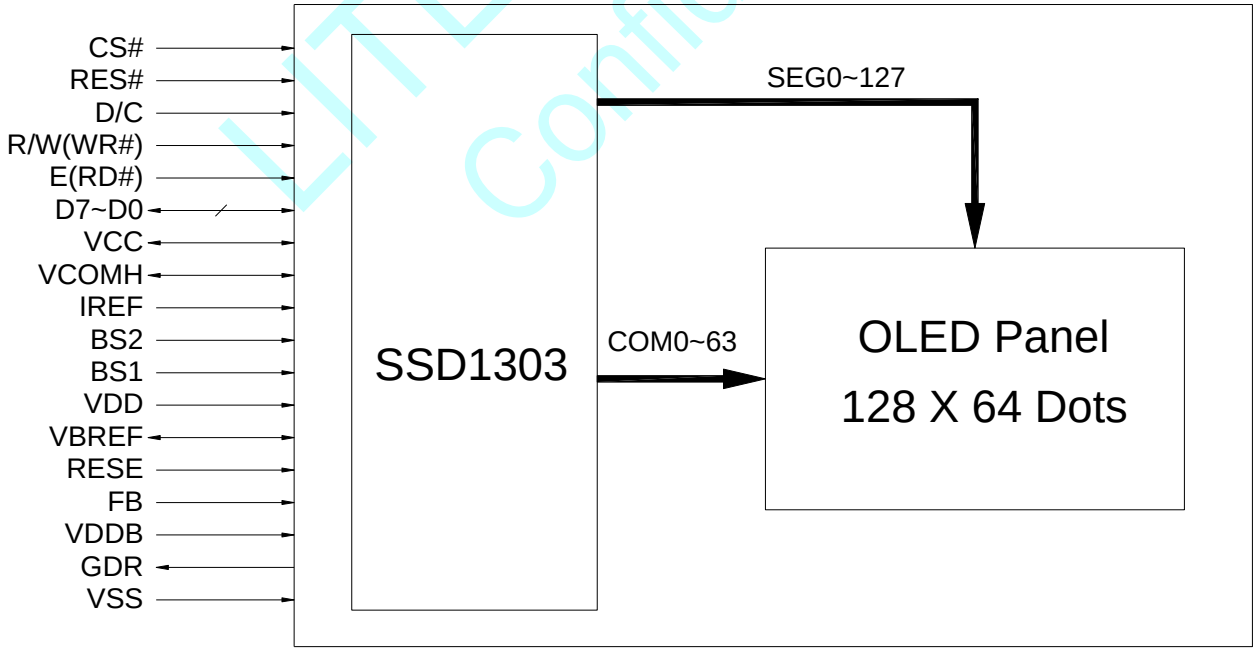


Figure 1: Block diagram

4. DIMENSIONAL OUTLINE

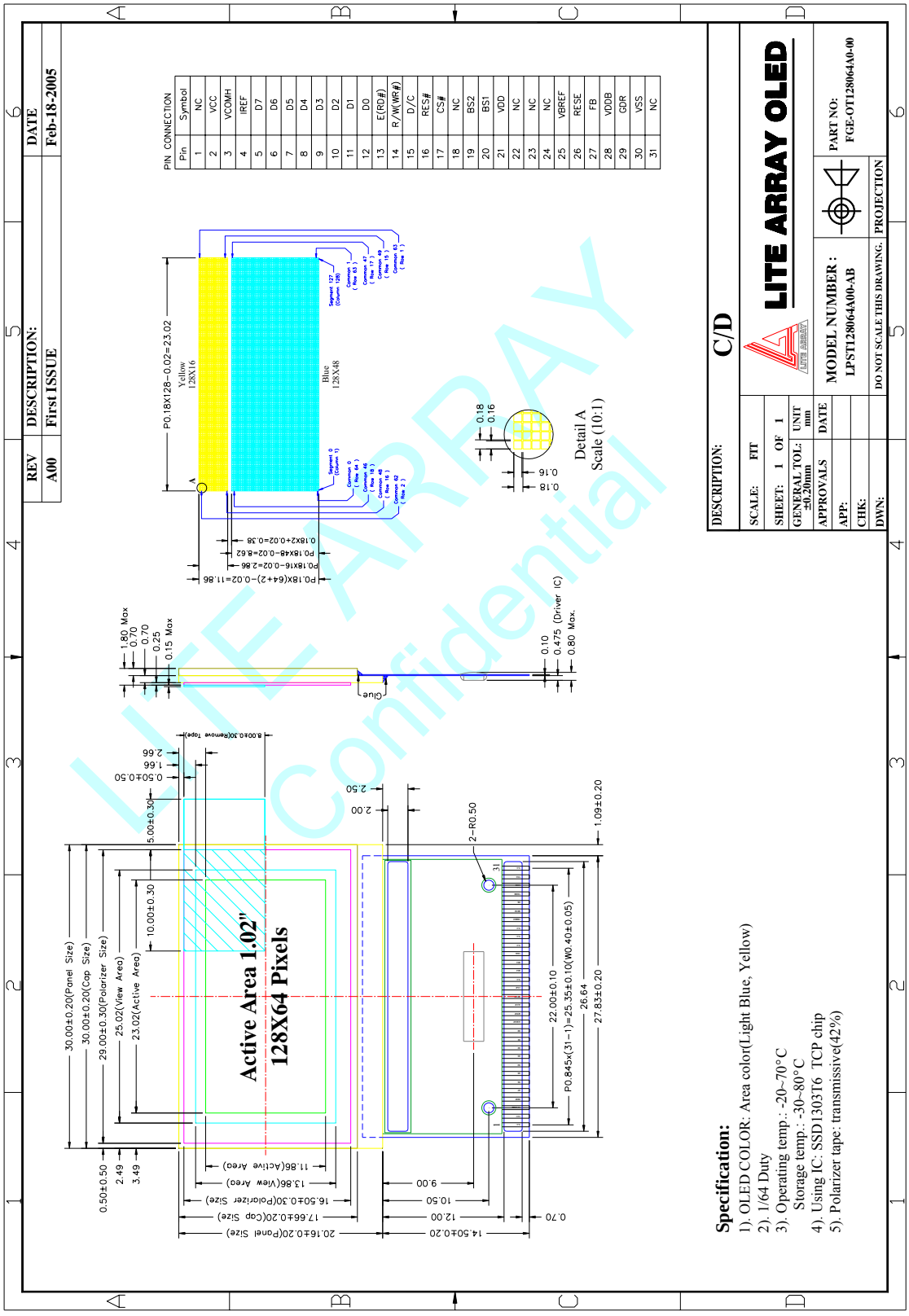


Figure 2: Dimensional outline

5. PIN DESCRIPTION

Pin no.	Symbol	Function
21	VDD	This is the supply voltage pin to logic circuit. It must be connected to the external power source.
30	VSS	This is the ground pin and is a reference for the logic pins. It must be connected to the external ground.
2	VCC	Supply voltage for OLED This is the supply voltage for OLED system and it is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC/DC voltage converter.
3	VCOMH	This is an input pin and a capacitor should be connected between VCOMH and VSS.
4	IREF	This is a segment current reference pin. A resistor should be connected between IREF and VSS
28	VDDB	This is a supply voltage pin for internal buffer DC/DC voltage converter. It must be connected to VDD when the converter is used. When use external VCC, the pin should be left open.
29	GDR	This is an output pin to drive the gate of the external NMOS of the booster circuit. When use external VCC, the pin should be left open.
27	FB	This is a feedback resistor input pin for the booster circuit. It is used to adjust the booster output voltage VCC. When use external VCC, the pin should be left open.
26	RESE	This is a source current pin of the external NMOS of the booster circuit. When use external VCC, the pin should be left open.
25	VBREF	This is an internal voltage reference pin for booster circuit. A stabilization capacitor should be connected to VSS. When use external VCC, the pin should be left open.
20, 19	BS1, BS2	These pins are for MCU selection. • BS1=0 and BS2=1 for 6800 parallel interface • BS1=1 and BS2=1 for 8080 parallel interface • BS1=0 and BS2=0 for SPI
17	CS#	This pin is the chip select input. Pull “Low” to enable the chip for MCU communication.
16	RES#	This pin is reset signal input. • Pull “Low” for the initialization of the chip.
15	D/C	This pin is used for Data/Command selection. • Pull “Low” to set the D7~D0 inputs as command to control the chip. • Pull “High” to set the D7~D0 inputs as display data.
14	R/W(WR#)	This pin is MCU interface input. - For 6800-series parallel interface, • This pin is used as Read/Write (R/W) selection input. • Pull “High” to set Read mode provided that CS# is “Low”. • Pull “Low” to set Write mode provided that CS# is “Low”. - For 8080-series parallel interface, • This pin is used for receiving the Write (WR#) signal. • Pull “Low” to initiate data write operation provided that CS# is “Low”; • Pull “High” to stop Write operation. - For Serial peripheral interface, • This pin must be connected to VSS.

Pin no.	Symbol	Function
13	E(RD#)	This pin is MCU interface input. - For 6800-series parallel interface, • This pin is used as the Enable (E) signal. • Pull "High" to enable the chip to initiate Read/Write operation provided that CS# is "Low". • Pull "Low" to disable the Read/Write operation. - For 8080-series parallel interface, • This pin is used for receiving the Read (RD#) signal. • Pull "Low" to initiate data read operation provided that CS# is "Low". • Pull "High" to stop Read operation. - For Serial peripheral interface, • This pin must be connected to VSS.
5 ~ 12	D7 ~ D0	These pins are 8-bit bi-directional data bus. They should be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input and D0 will be the serial clock input.
1, 18, 22, 23, 24 31	N.C.	Reserved pins and should not be connected together.

Table1: Pin Description

6. ABSOLUTE MAXIMUM RATINGS

6.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	V_{DD}	-0.3	4.0	V	1,2
Driver Supply Voltage	V_{CC}	0	15.0	V	1,2
Operating Temperature	T_{OP}	-20	70	°C	--
Storage Temperature	T_{STG}	-30	80	°C	--

Table2: Absolute Maximum Ratings

Note 1: All above voltages are on the basis of "VSS = 0.0V".

Note 2: When this module is used beyond above absolute maximum ratings, permanent breakage of the module may occur. For normal operations, it is desirable to use this module under the conditions according to Section "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module will occur and the reliability of the module may deteriorate.

6.2 Regarding the Gradation

Although this module possesses the gradation function, respective gradation levels will vary depending on the production conditions etc. The temperature range where the gradation function can be guaranteed is -10 °C ~ 60 °C.

7. OPTICS & ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With polarizer	35	60	--	Cd/m^2
CIE (Blue)	X	Without polarizer	0.12	0.16	0.20	--
	Y		0.24	0.28	0.32	--
CIE (Yellow)	X	Without polarizer	0.43	0.47	0.51	--
	Y		0.46	0.50	0.54	--
Dark Room Contrast	CR	--	--	>100	--	--
View Angle	A	--	>160	--	--	degree

Table 3: Optics & electrical characteristics

Note: Optical measurement is taken at 1/64 duty,100Hz Frame Rate, 0xFF Contrast setting.

8. ELECTRICAL CHARACTERISTICS

8.1 DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage for logic	--	2.6	2.8	3.5	V
V_{CC}	Operating Voltage for OLED	--	8	9	10	V
V_{IH}	High Level Input	--	$0.8*V_{DD}$	--	V_{DD}	V
V_{IL}	Low Level Input	--	0.0	--	$0.2*V_{DD}$	V
V_{OH}	High Level Output	--	$0.9*V_{DD}$	--	V_{DD}	V
V_{OL}	Low Level Output	--	0.0	--	$0.1*V_{DD}$	V
I_{DD}	Operating Current at V_{DD}	VDD = 2.8V, VCC = 9.0V, Frame rate = 100Hz, Contrast setting = 0xFF, 50% display area turn-on.	--	TBD	TBD	mA
		VDD = 2.8V, VCC = 9.0V, Frame rate = 100Hz, Contrast setting = 0xFF, 100% display area turn-on.	--	TBD	TBD	mA
I_{CC}	Operating Current at V_{CC}	VDD = 2.8V, VCC = 9.0V, Frame rate = 100Hz, Contrast setting = 0xFF, 50% display area turn-on.	--	TBD	TBD	mA
		VDD = 2.8V, VCC = 9.0V, Frame rate = 100Hz, Contrast setting = 0xFF, 100% display area turn-on.	--	TBD	TBD	mA

Table 4: DC characteristics

8.2 AC Characteristics

8.2.1 6800-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Max	Unit
t_{cycle}	Clock cycle time	300	--	ns
t_{AS}	Address Setup Time	0	--	ns
t_{AH}	Address Hold Time	0	--	ns
t_{DSW}	Write Data Setup Time	40	--	ns
t_{DHW}	Write Data Hold Time	15	--	ns
t_{DHR}	Read Data Hold Time	20	--	ns
t_{OH}	Output Disable Time	--	70	ns
t_{ACC}	Access Time	--	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-- --	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-- --	ns ns
t_R	Rise time	--	15	ns
t_F	Fall time	--	15	ns

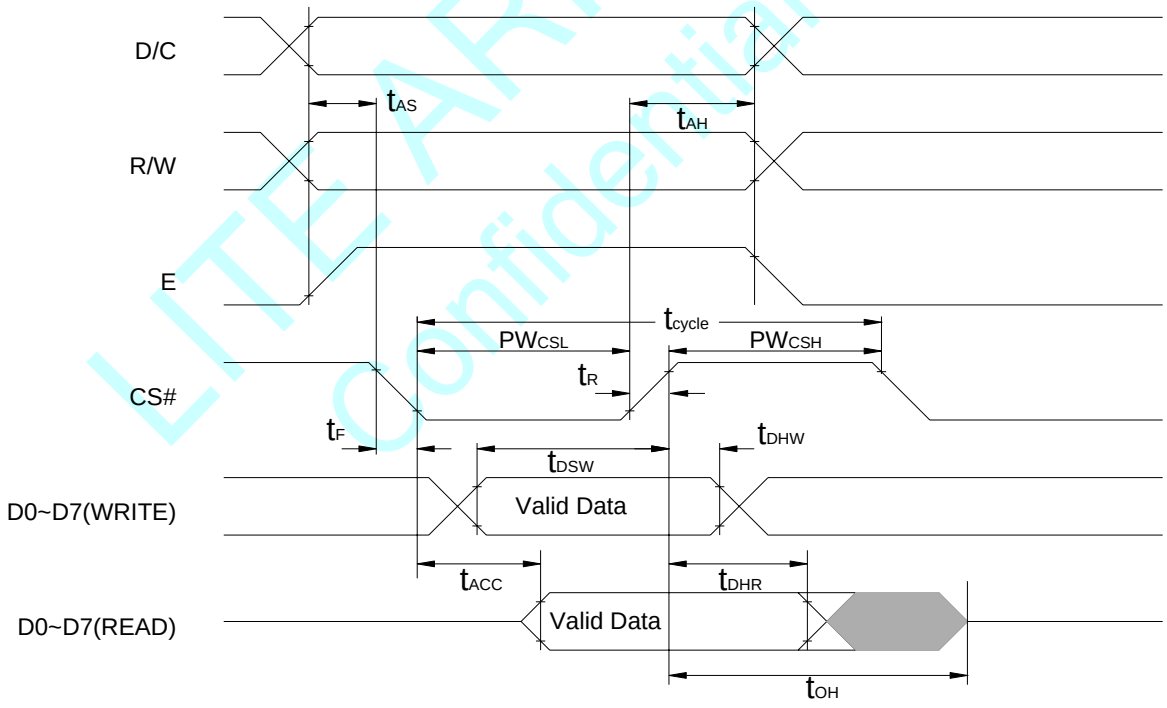


Figure 3: Timing diagram for 6800-series MPU parallel interface

8.2.2 8080-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Max	Unit
t_{cycle}	Clock cycle time	300	--	ns
t_{AS}	Address Setup Time	0	--	ns
t_{AH}	Address Hold Time	0	--	ns
t_{DSW}	Write Data Setup Time	40	--	ns
t_{DHW}	Write Data Hold Time	15	--	ns
t_{DHR}	Read Data Hold Time	20	--	ns
t_{OH}	Output Disable Time	--	70	ns
t_{ACC}	Access Time	--	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-- --	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-- --	ns ns
t_R	Rise time	--	15	ns
t_F	Fall time	--	15	ns

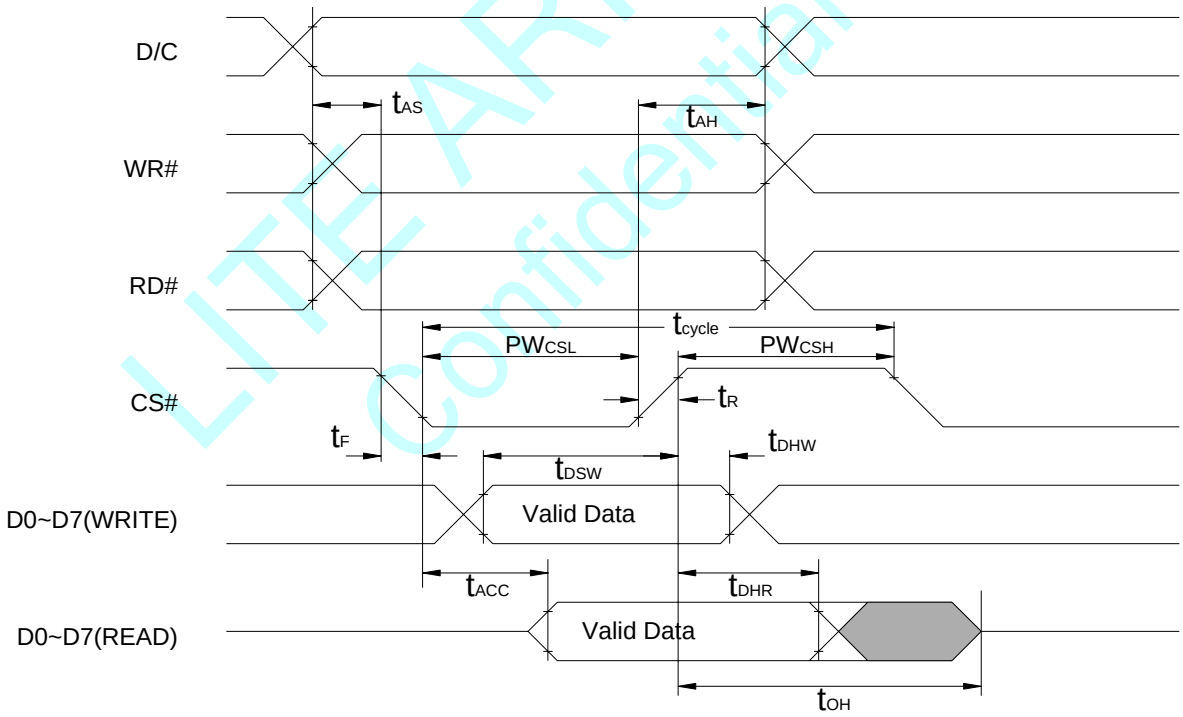


Figure 4: Timing diagram for 8080-series MPU parallel interface

8.2.3 Serial Interface Timing Characteristics

Symbol	Parameter	Min	Max	Unit
t_{cycle}	Clock cycle time	200	--	ns
t_{AS}	Address Setup Time	150	--	ns
t_{AH}	Address Hold Time	150	--	ns
t_{CSS}	Chip Select Setup Time	120	--	ns
t_{CSH}	Chip Select Hold Time	60	--	ns
t_{DSW}	Write Data Setup Time	100	--	ns
t_{DHW}	Write Data Hold Time	100	--	ns
t_{CLKL}	Clock Low Time	100	--	ns
t_{CLKH}	Clock High Time	100	--	ns
t_R	Rise time	--	15	ns
t_F	Fall time	--	15	ns

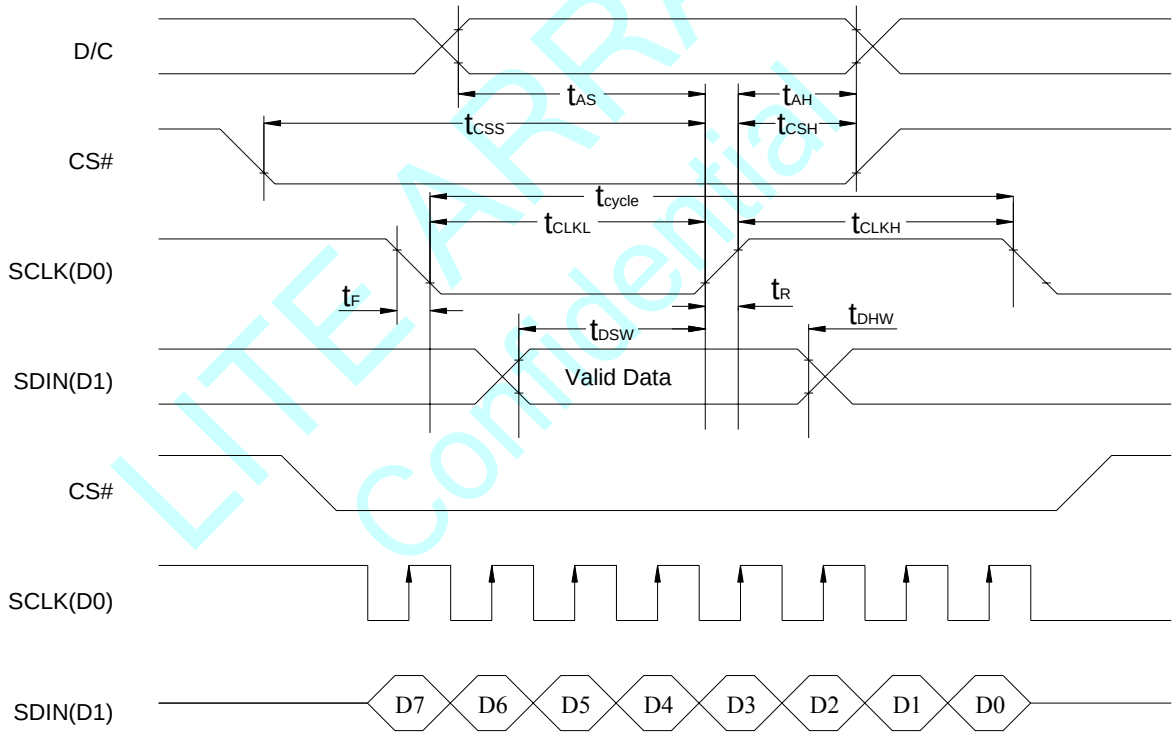


Figure 5: Timing diagram for serial interface

9. CONTROL AND DISPLAY COMMAND

9.1 Command table

(D/C = 0, R/W (WR#) = 0, E(RD#) = 1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Address	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Address	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
0	26	0	0	1	0	0	1	1	0	Horizontal scroll setup	A[2:0] Set the number of column scroll per step
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		Valid value: 001b, 010b, 011b, 100b
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		B[2:0] Define start page address
0	C[1:0]	*	*	*	*	*	*	C_1	C_0		C[1:0] Set time interval between each scroll step in terms of frame frequency
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		00b – 12 frame 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	40-7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display TAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000 during POR
0	81	1	0	0	0	0	0	0	1	Set Contrast Control Register	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 80h)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT) for area colour	Set current drive pulse width of Bank 0, Colour A, B and C.
0	X[5:0]	*	*	X_5	X_4	X_3	X_2	X_1	X_0		Bank 0: X[5:0] = 0… 63; for pulse width set to 1 ~ 64 clocks
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		Colour A: A[5:0] same as above
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		Colour B: B[5:0] same as above
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		Colour C: C[5:0] same as above Note: colour D pulse width is fixed at 64 clocks pulse .

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank colour of for bank 1-16 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 1
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 2
0	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		:
0	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		:
0	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[7:6]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 16
0	93	1	0	0	1	0	0	1	1	Set bank colour of for bank 17-32 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 17
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 18
0	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		:
0	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		:
0	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[7:6]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 32
0	A0~ A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	X_0=0: column address 0 is mapped to SEG0 (POR) X_0=1: column address 131 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X_0	Set Entire Display ON/OFF	X_0=0: normal display (POR) X_0=1: entire display ON
0	A6~A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	The next command, A[5:0] determines multiplex ratio N from 16MUX-64MUX, POR= 64MUX
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0 0	AD	1 1	0 0	1 0	0 0	1 1	1 0	0 1	1 X_0	Set DC-DC on/off	X_0 : 1 DC-DC will be turned on when display on (POR) 0 DC-DC is disable
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	X_0=0: turns OFF OLED panel (POR) X_0=1: turns ON OLED panel
0	B0~BF	1	0	1	1	X_3	X_2	X_1	X_0	Set Page Address	Set GDDRAM Page Address (0~7) for read/write using $X_3X_2X_1X_0$
0	C0/C8	1	1	0	0	X_3	*	*	*	Set COM Output Scan Direction	X_3=0: normal mode (POR) Scan from COM 0 to COM [N –1] X_3=1: remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.
0	D0-D1	1	1	0	1	0	0	0	X_0	Reserved	Reserved, do not use

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D3	1	1	0	1	0	0	1	1	Set Display Offset	Set vertical scroll by COM from 0-63.
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		The value is reset to 00H after POR.
0	D5	1	1	0	1	0	1	0	1	Set Display Clock Divide Ratio/Oscillator Frequency	The lower nibble of the next command define the divide ratio of the display clocks (DCLK):
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Divide ratio= A[3:0] + 1, POR is 0000b (divide ratio = 1) The higher nibble of the next command sets the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa.
0	D8	1	1	0	1	1	0	0	0	Set area colour mode on/off & low power display mode	X_5X_4= 00 (POR) : mono mode
0		0	0	X_5	X_4	0	X_2	0	X_0		X_5X_4= 11 Area Colour enable X_2=0 and X_0=0: Normal (POR) power mode X_2=1 and X_0=1: Set low power save mode
0	D9	1	1	0	1	1	0	0	1	Set Pre-charge period	A[3:0] Phase 1 period of up to 15 dclk clocks [POR=2h]
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] Phase 2 period of up to 15 dclk clocks [POR=2h]
0	DA	1	1	0	1	1	0	1	0	Set COM pins hardware configuration	X_4=0, Sequential COM pin configuration
0		0	0	0	X_4	0	0	1	0		(i.e. COM31, 30, 29….0 ; SEG0-132; COM31,32….62,63) X_4=1(POR), Alternative COM pin configuration (i.e. COM62,60,58,…2,0; SEG0-132; COM1,3,5…61,63)
0	DB	1	1	0	1	1	0	1	1	Set VCOM Deselect Level	A[6:0] 0000000 low VCOM deselect level (~ 0.43 Vref)
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		0110101 noraml VCOM deselect level (~ 0.77*Vref (POR)) 1111111 high VCOM deselect level (equal Vref)
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation
0	F*	1	1	1	1	*	*	*	*	Reserved	Reserved, do not use

Note: Remark "*" stands for "Don't Care"

Table 5: Command Table

9.2 Read command table

(D/C = 0, R/W(WR#) = 1, E(RD#) = 1 for 6800 or E(RD#) = 0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read *	D_7 : "1" for Command lock D_6 : "1" for display OFF / "0" for display ON D_5 : Reserve D_4 : Reserve D_3 : Reserve D_2 : Reserve D_1 : Reserve D_0 : Reserve

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

Table 6: Read Command Table

10. REFERENCE APPLICATION CIRCUIT

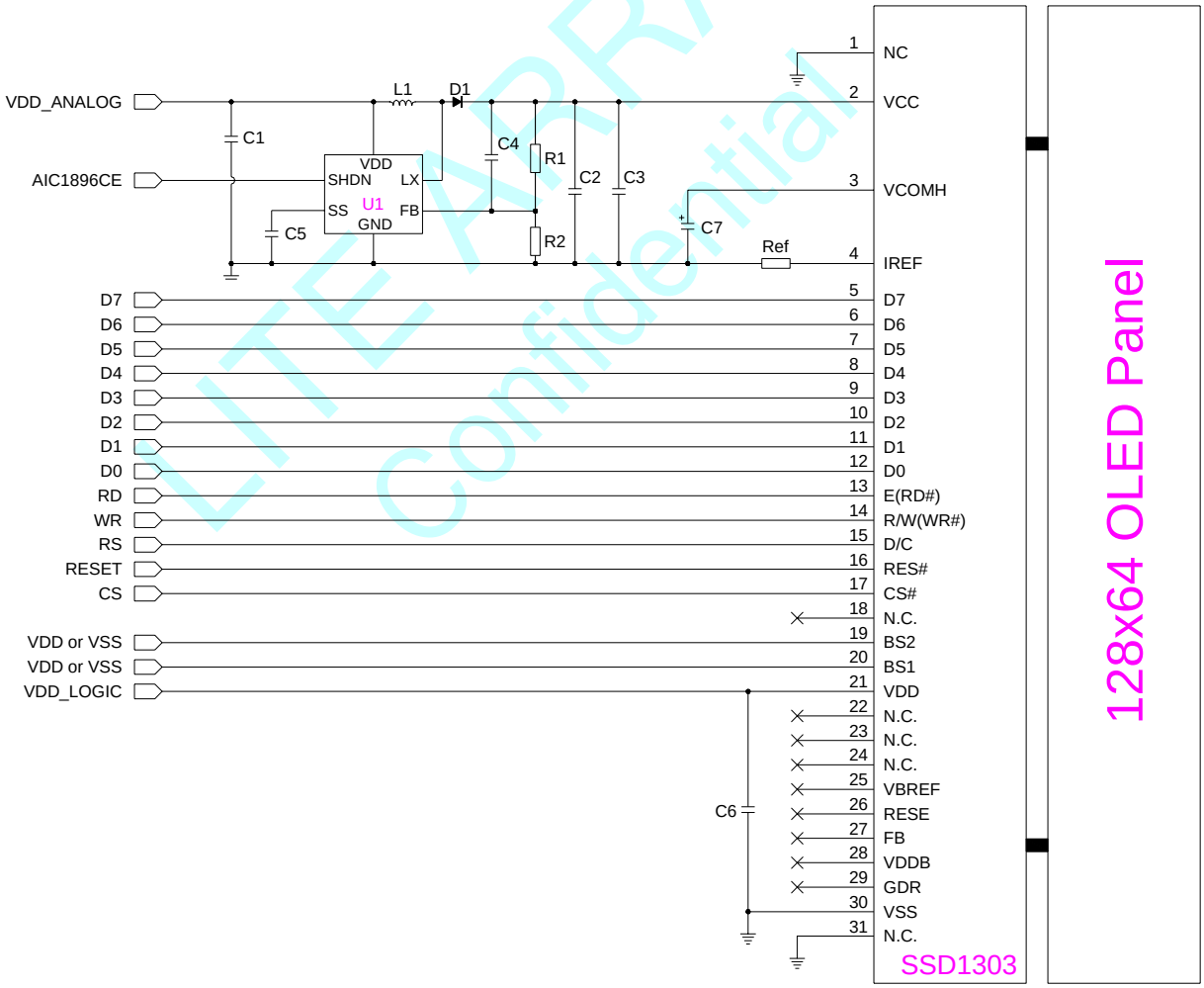


Figure 6: Reference Application Circuit (using external DC/DC voltage converter)

Notes:

- MPU interface: 8-bit 6800-series/8080-series parallel interface or Serial interface. It is pin selectable by BS1 and BS2.

	6800-series parallel interface	8080-series parallel interface	Serial interface
BS1	0	1	0
BS2	1	1	0

- U1: AIC1896 DC/DC Converter
- AIC1896CE can be connected to MCU or VDD for alternative solution.
- VCC = 1.23 x (R1 + R2)/R2

Below table is the component list for the application circuit.

Item	Description
SSD1303	OLED Driver IC (*Solomon*)
U1	DC/DC Converter – AIC1896 Step-up(*AIC*)
L1	Inductor – 15µH, 2A
D1	Schottky Diode – 20V, 1A
R1	Resistor – 820kΩ , 1%, 1/4W
R2	Resistor – 130kΩ , 1%, 1/4W
Ref	Resistor – 910kΩ , 1% (see remark)
C1	Capacitor – 10µF, 6.3V, Low ESR
C2	Capacitor – 10µF, 16V, Low ESR
C3	Capacitor – 1µF, 16V, Low ESR
C4	Capacitor – 15nF, 16V, Low ESR
C5	Capacitor – 0.033µF, 6.3V, Low ESR
C6	Capacitor – 4.7µF, 6.3V, Low ESR
C7	Tantalum Capacitor – 1.0µF~2.2µF, 16V

Table 7: Component list for the external DC-DC voltage converter application circuit

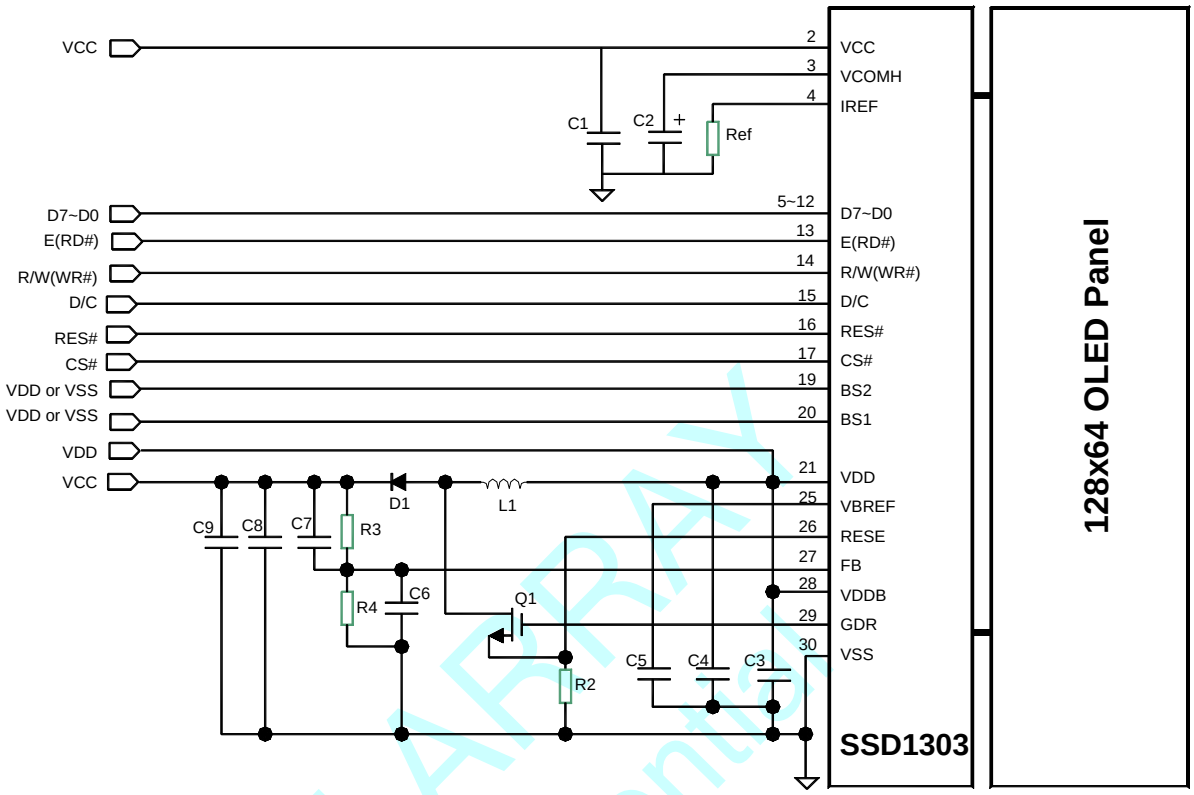


Figure 7: Reference Application Circuit (using internal DC/DC voltage converter)

Notes:

- MPU interface: 8-bit 6800-series/8080-series parallel interface or Serial interface. It is pin selectable by BS1 and BS2.

	6800-series parallel interface	8080-series parallel interface	Serial interface
BS1	0	1	0
BS2	1	1	0

- L1, D1, Q1 and C4 should be grouped closed together on PCB layout
- R2, R3, C5 and C6 should be grouped closed together on PCB layout
- The VCC output voltage level is adjusted by R2 and R3, the formula is:

  VCC = 1.2 x (R2+R3)/R3

  The value of (R2+R3) should be between 500k to 1M ohm.

Below table is the component list for the application circuit.

Item	Description
SSD1303	OLED Driver IC (*Solomon*)
Q1	MOSFET – N-FET with low R_{DS}(on) and low Vth voltage, eg, MGSF1N02Lt1 (*On Semi*)
L1	Inductor – 10µH, 1A
D1	Schottky diode – 1A, 25V, eg, 1N5822, BAT54 (*Philips Semi*)
Ref	Resistor – 1%, 1/2W (see remark)
R1	Resistor – 1.2Ω , 1%, 1/2W
R2, R3	Resistor – 1%, 1/10W
C1	Capacitor – 4.7µF, 16V
C2	Tantalum Capacitor – 1.0µF~2.2µF, 16V
C3	Capacitor – 0.1 ~ 1µF, 16V
C4	Capacitor – 1 ~ 10µF, 16V
C5	Capacitor – 1µF, 16V
C6	Capacitor – 10nF, 16V
C7	Capacitor – 15nF, 16V
C8	Capacitor – 6.8µF, 25V, Low ESR
C9	Capacitor – 1µF, 16V

Table 8: Component list for the internal DC-DC voltage converter application circuit

Remark:

Ref = (Voltage at IREF pin – VSS)/I_{REF}; Voltage at I_{REF} pin = VCC - VDD

For example, VDD = 3.0V, VCC = 12V, I_{REF} = 10µA

Ref = $(12-3)/10^{-6}$ = about 910kΩ

11. QUALITY SPECIFICATIONS

11.1 Inspection Method:

11.1.1 Applicable Standard

MIL-STD-105E, Level II, Normal Inspection, single sampling

11.1.2 AQL

Partition	AQL	Definition
Major	0.65	Defects may lead to the failure of display function or the failure of passing the reliability criteria.
Minor	1.0	Defects do not affect all of the display functions, and have no impact to the reliability.

11.1.3 Inspection Condition

Test and measurement were conducted under the following conditions:

Temperature: 23±5℃

Humidity: 55±15%RH

Distance between the panel and eyes of the inspector: ≥30cm

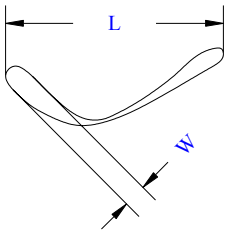
11.2 Inspection Criterion

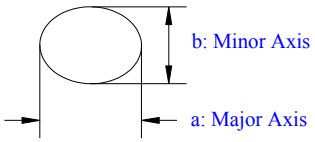
Check Item	Classification	Criteria	
Non operation/display	major	Not Allowable	
Flicker			
Miss line or pixel			
Wrong display			
Cross talk *			
Scratches, fiber **	minor	$W \le 0.05$ $W \le 0.1, L \le 2$ $2 < L$	Ignore $n \le 3$ $n = 0$
Dirt, Black spot, white spot, Greasy dirt, Foreign material, Dent, Bubbles **		$\Phi \le 0.1$ $0.1 < \Phi \le 0.2$ $0.2 < \Phi \le 0.25$ $0.25 < \Phi$	Ignore $n \le 3$ $n \le 1$ $n \le 0$
Fingerprint, Flow mark	minor	Not allowable	

* In displays which manifests itself has the other shadowing, ghosting or streaking.

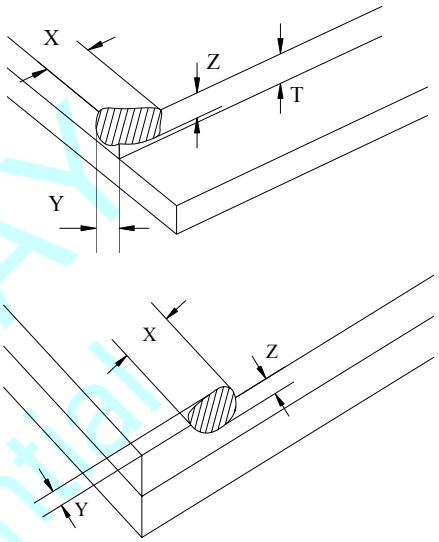
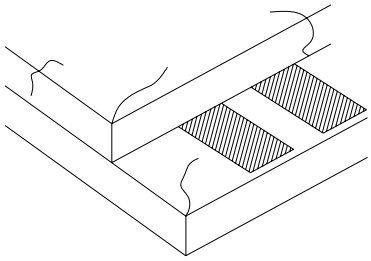
** Distance between any 2 defects should over 10mm

*** Definition of W & L & Φ (unit: mm): $\Phi=(a+b)/2$





Visual check in non-active area

Check Item	Classification	Criteria
Panel General Chipping	Major	X≤1/6 Panel Length Y≤1 Z≤T 
Panel Crack	minor	Any crack is not allowable 
Terminal cable: twist, Scar, Split, Scratch	Minor	Not Allowable

11.3 Reliability

11.3.1 Contents of Reliability Tests

Item	Condition	Criteria
High Temperature Operation	70°C, 240 hrs	No such changes as to obstruct image & function
Low Temperature Operation	-20°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-30°C, 240 hrs	
High Temperature /Humidity Storage	60°C, 90%RH, 240 hrs	
Thermal Shock	-30°C⇔ 80°C, 10 cycles 30 mins dwell	

* The samples used for above tests do not include polarizer.
* No moisture condensation is observed during tests.

11.3.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

An average operating lifetime of more than 10,000 hrs at room temperature is approached by 240 hrs @ 70°C operating.

11.3.3 Failure Check Standard

After the completion of the described reliability test, the samples were left room temperature for 2 hrs prior to conducting the failure teat at 23±5℃; 55±15% RH.