LGDP4216 is a controller & driver on-chip IC for PMOLED (passive matrix OLED) display, which supports 260K colors and 160x128 format. The IC includes 480-channel data driver and scan driver and RC oscillator (RC-OSC). And it also includes SRAM memory for 1-frame display contents, MPU interface block, and display control circuits.

Features

Power Supply

- Data driver supply voltage DVCC=10-21V
- Scan regulator supply voltage SVCC=10-21V
- Interface I/O supply voltage IOVDD=2.2V~3.3V
- Logic supply voltage VDD=2.2V~2.9V
- Analog supply voltage AVDD=2.2V~2.9V
- Make sure IOVDD≥VDD=AVDD

Dot Matrix Display Area

- Variable display size : Max 160(RGB) X 128 Lines.

Graphics RAM(GRAM)

- Dot Matrix : 128 x 18bit x 160 = 368,640 bits

Dot Matrix Data Driver

- Max 480 outputs (160 x RGB)
- Data format:

  RGB 6:6:6 ➔ 64 Gray scales (260K colors)

  RGB 5:6:5 ➔ 64 Gray (G), 32 Gray(R, B) scale (65K colors)
- Maximum output current ➔ R : 10 ~ 153uA (Step : 0.6 uA)

  Maximum output current => G/B : 10uA ~ 102uA (Step : 0.4 uA)
- Pin-to-Pin current deviation ➔ TBD
- Current deviation at 1Chip ➔ TBD

Dot Matrix Scan Driver

- Max 128 outputs
- Maximum on resistance 20Ω

CPU Interface

- I80 and M68 parallel interface
- 18-/16-/9-/8-Bit write and read with address RS
- Address RS is used to select command and parameters

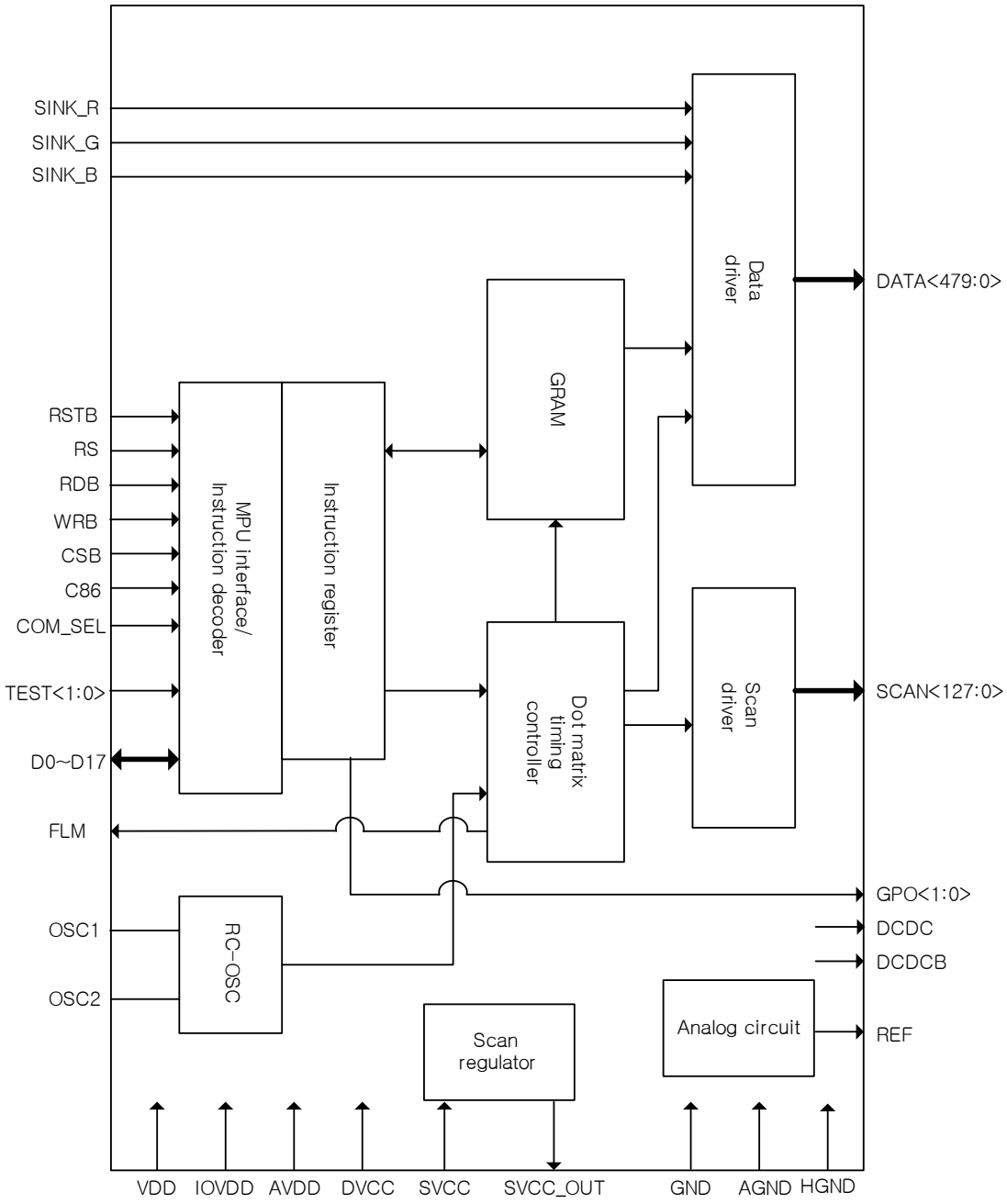
RC-OSC

- Frequency (3 ~ 5MHz,Typ.= 4.0MHz, ±12%)

Frame Rate

- Variable frame rate 60, 75, 90,105,120,135,150 Hz (default: 90Hz)

Block Diagram



Chip Pin Function

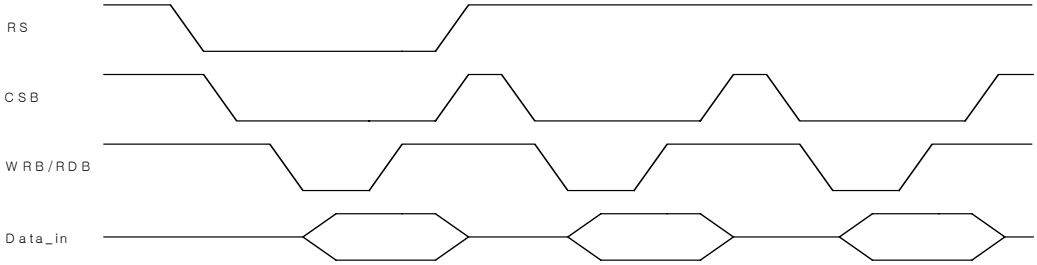
Signals	No. of pins	Pad type	Functions
DVCC	15	-	A supply voltage for data driver.
SVCC	4	-	A supply voltage for scan regulator
SVCC_OUT	6	-	A power supply for the scan driver.
IOVDD	2	-	A supply voltage for the interface pins.
VDD	2	-	A supply voltage for the logic.
AVDD	2	-	A supply voltage for the analog circuit.
HGND	22	-	Ground for the data driver and scan driver and scan regulator.
VSS	4	-	Ground for the logic and GRAM and I/O unit.
AGND	2	-	Ground for the analog circuit.
OSC1	1	I/O	Connect an external resistor for RC oscillation.
OSC2	1	I/O	
SINK_R	8	I/O	Discharge Voltage for Red
SINK_G	8	I/O	Discharge Voltage for Green
SING_B	8	I/O	Discharge Voltage for Blue
REF	1	O	A reference voltage output for the analog circuit.
C86	1	I	H: M68 series L: I80 series
DCDC	1	I/O	This pins control the external DC-DC converter on off.
DCDCB	1	I/O	This pins control the external DC-DC converter on off.
GPO [1:0]	2	O	General-purpose output pin.
TEST [1:0]	2	I/O	A test pins. The pin must be fixed at the VSS.
CSB	1	I	Chip Select (Active low)
RDB	1	I	Read (Active low, 80 interface), Enable (68 interface)
WRB	1	I	Write (Active low, 80 interface), H: Read, L: Write (68 interface)
RSTB	1	I	Reset (Active low)
RS	1	I	Address (L: index, H: parameter or data)
DUMMY_EN	1	O	Dummy scan status output (H : dummy scan, L : normal scan)
D0~D17	18	I/O	An 18bit bus for RGB data.
COM_SEL	1	I	Data Bit Selection Signal Input
FLM	1	O	Frame Start Signal Output
DATA [479:0]	480	O	Data driver output.
SCAN [127:0]	128	O	Scan driver output.

Access to GRAM and Internal Register

I80 Series CPU

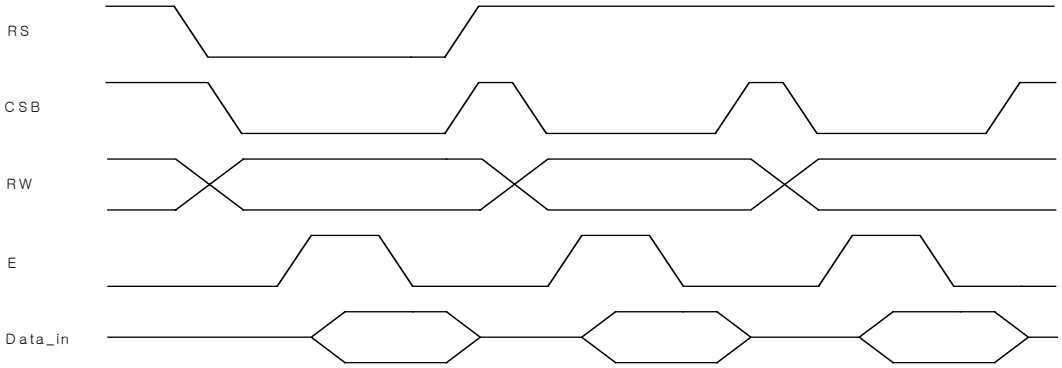
(Maximum input frequency: 10MHz)

Function	CSB	WRB	RDB	RS	D
Write Command	L	↑	H	L	Index
Write Parameter Or Data	L	↑	H	H	Parameter or Data
Read Parameter Or Data	L	H	↑	H	Parameter or Data



M68 Series CPU

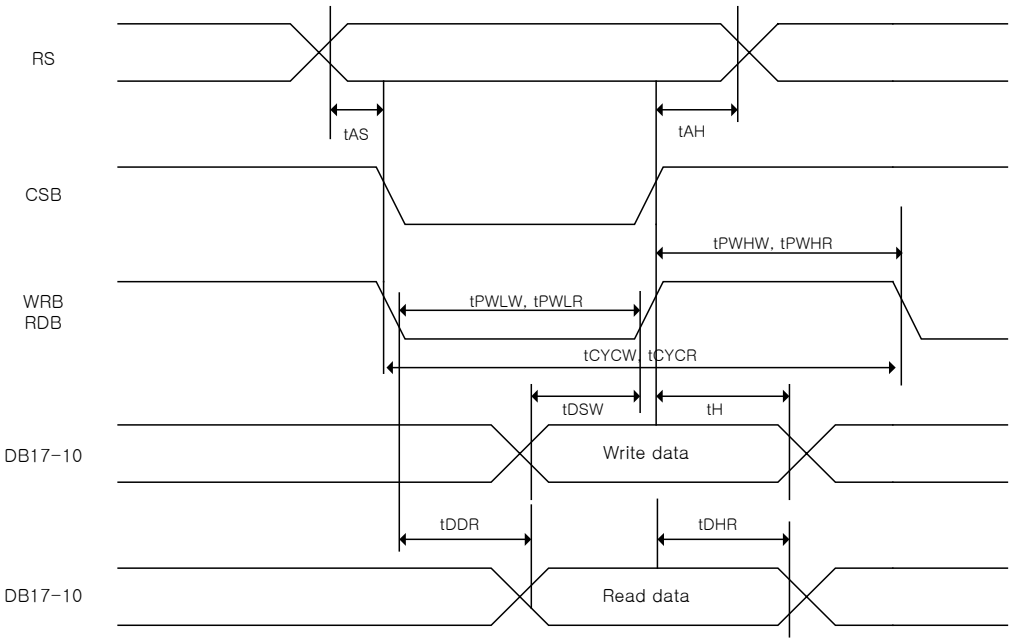
Function	CSB	RW	E	RS	D
Write Command	L	L	↓	L	Index
Write Parameter Or Data	L	L	↓	H	Parameter or Data
Read Parameter Or Data	L	H	↓	H	Parameter or Data



M68 Series Parallel Interface

When M68 series parallel data transfer has been selected, data is written to the controller at the falling edge of the E signal when the RW signal is low. During the data read operation, the data bus enters the output status when the RW signal is high, output valid data at the rising edge of the E signal, and enters the high-impedance state at the falling edge of the RW signal.

I80 Series Interface Timing Characteristics



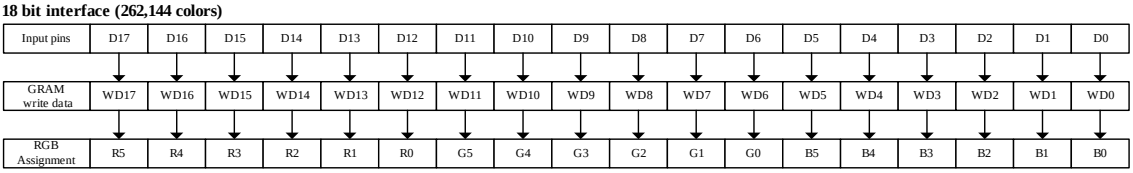
Item		Symbol	Unit	Min	Typ	Max
Bus cycle	Write	tCYCW	ns	100		
	Read	tCYCR	ns	100		
Write “Low” level pulse width	Write	tPWLW	ns	40		
Read “Low” level pulse width	Read	tPWLR	ns	40		
Write “High” level pulse width	Write	tPWHW	ns	40		
Read “High” level pulse width	Read	tPWHR	ns	40		
Setup time	Write (RS~CSB, WRB)	tAS	ns	0		
	Read (RS~CSB, RDB)		ns	0		
Address hold time		tAH	ns			
Write data setup time		tDSW	ns			
Write data hold time		tH	ns			
Read data delay time		tDDR	ns	10		
Read data hold time		tDHR	ns	10		

Interface Selection

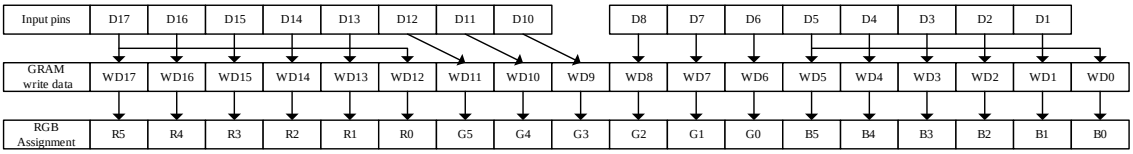
C86 (interface selection Pin)	CSB	RS	RW	WRB	D
H (M68 series MPU)	CSB	RS	E	R/W	D [17:0]
L (I80 series MPU)	CSB	RS	RDB	WRB	D [17:0]

Input Data Format

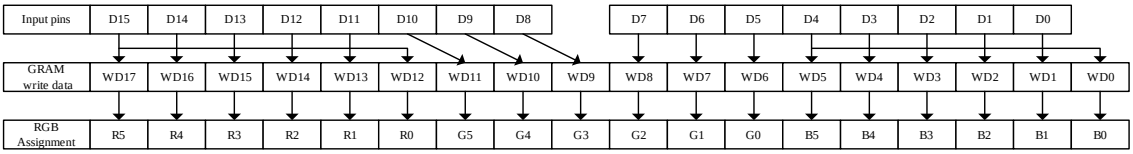
18 bit interface (262,144 colors)



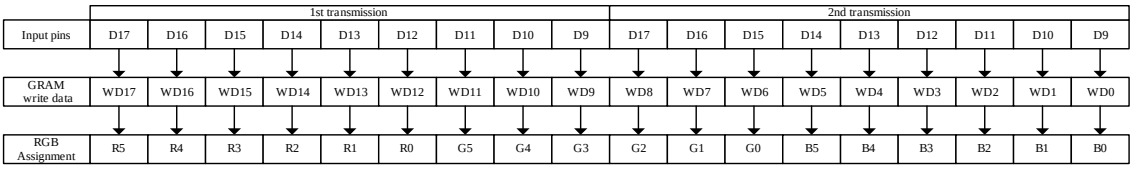
16 bit interface (65,536 colors, COM_SEL='1')



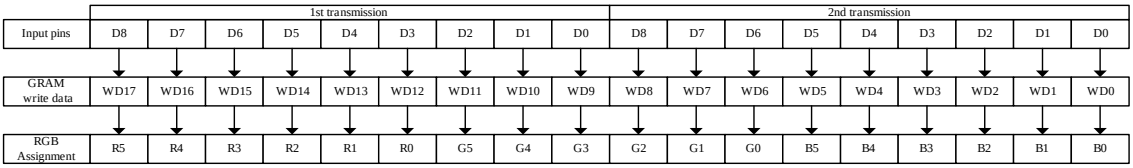
16 bit interface (65,536 colors, COM_SEL='0')



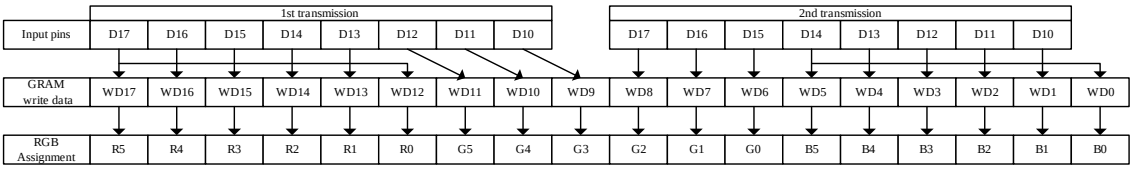
9 bit interface (262,144 colors, 2 transmission, COM_SEL='1')



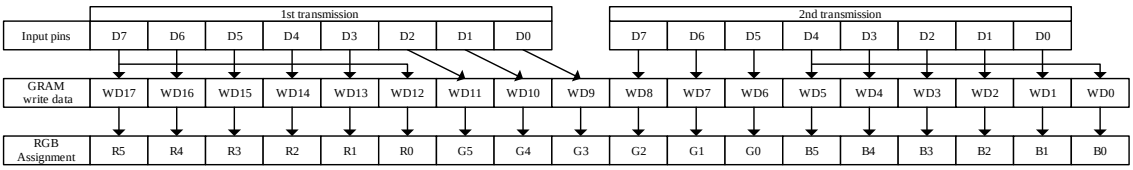
9 bit interface (262,144 colors, 2 transmission, COM_SEL='0')



8 bit interface (65,536 colors, 2 transmission, COM_SEL='1')



8 bit interface (65,536 colors, 2 transmission, COM_SEL='0')



8 bit interface (262,144 colors, 3 transmission, COM_SEL='1')

	1st transmission								2nd transmission								3rd transmission	
Input pins	D17	D16	D15	D14	D13	D12	D11	D10	D17	D16	D15	D14	D13	D12	D11	D10	D17	D16
GRAM write data	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

8 bit interface (262,144 colors, 3 transmission, COM_SEL='0')

	1st transmission								2nd transmission								3rd transmission	
Input pins	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6
GRAM write data	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

6 bit interface (262,144 colors, 3 transmission, COM_SEL='1')

	1st transmission						2nd transmission						3rd transmission					
Input pins	D17	D16	D15	D14	D13	D12	D17	D16	D15	D14	D13	D12	D17	D16	D15	D14	D13	D12
GRAM write data	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

6 bit interface (262,144 colors, 3 transmission, COM_SEL='0')

	1st transmission						2nd transmission						3rd transmission					
Input pins	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
GRAM write data	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Instruction

COM_SEL='1'

Input pins	D17	D16	D15	D14	D13	D12	D11	D10
ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

COM_SEL='0'

Input pins	D7	D6	D5	D4	D3	D2	D1	D0
ID	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Register Table

	D7	D6	D5	D4	D3	D2	D1	D0
0x00	DISP(0)	-	-	DIR(0)	BGR(0)	-	-	RESET(0)
0x01	-	WR_DIR(101)			-	IF_MODE(000)		
0x02	-	-	-	DIS_SZ(0)	-	DIS_FRAME(010)		
0x03	-	-	-	-	-	-	SCAN_DIR(0)	SCAN_SEQ(0)
0x04	-	-	-	-	-	-	-	DIS_ROT
0x05	WR_DATA							
0x06	AD_X(10011111)							
0x07	-	AD_Y(0000000)						
0x08	MXSTART(00000000)							
0x09	MXEND(10011111)							
0x0a	-	MYSTART(0000000)						
0x0b	-	MYEND(1111111)						
0x0c	SETTING DISABLE							
0x0d	-	-	-	-	-	-	-	PCDR(0)
0x0e-0f	SETTING DISABLE							
0x10	-	SAVE_TIME_SS(000)			-	DISP_TIME_SS(000)		
0x11	STEP_TIME_SS0(0000)				-	IMAGE_STOP_TIME0(000)		
0x12	STEP_TIME_SS1(0000)				-	IMAGE_STOP_TIME1(000)		
0x13	STEP_TIME_SS2(0000)				-	IMAGE_STOP_TIME2(000)		
0x14	-	SSMP0(000)			-	SSM(000)		
0x15	-	SSMP2(000)			-	SSMP1(000)		
0x16	PV_SEL0(00)		COL_FADE_STEP0(00)		SCRL_DIR0(00)		FADE_MODE0(11)	
0x17	PV_SEL1(00)		COL_FADE_STEP1(00)		SCRL_DRI1(00)		FADE_MODE1(11)	
0x18	PV_SEL2(00)		COL_FADE_STEP2(00)		SCRL_DRI2(00)		FADE_MODE2(11)	
0x19	-	-	FADE_STOP_LEVEL0(000000)					
0x1a	-	-	FADE_STOP_LEVEL1(000000)					
0x1b	-	-	FADE_STOP_LEVEL2(000000)					
0x1c	X_LIMIT0(00000000)							
0x1d	X_LIMIT1(10011111)							
0x1e	-	Y_LIMIT0(0000000)						
0x1f	-	Y_LIMIT1(1111111)						
0x20	DIS_CHARGE_TIME_R(00000000)							
0x21	DIS_CHARGE_TIME_G(00000000)							
0x22	DIS_CHARGE_TIME_B(00000000)							

0x23	R_PEAK_TIME(00000100)							
0x24	G_PEAK_TIME(00000110)							
0x25	B_PEAK_TIME(00001000)							
0x26	-	-	SCAN_TIME(000000)					
0x27	-	-	-	BP_EN(0)	-	-	-	BP_MODE(0)
0x28	FLM_LINE(01111111)							
0x29-0x3f	SETTING DISABLE							
0x40	-	R_LUT(0000000)						
0x41	-	G_LUT(0000000)						
0x42	-	B_LUT(0000000)						
0x43								LUT_BP(0)
0x44-0x4f	SETTING DISABLE							
0x50	R_CURRENT(01010000)							
0x51	G_CURRENT(01010000)							
0x52	B_CURRENT(01010000)							
0x53	R_PEAK_DC_CURRENT(000)			R_PEAK_CURRENT(00011)				
0x54	G_PEAK_DC_CURRENT(000)			G_PEAK_CURRENT(00011)				
0x55	B_PEAK_DC_CURRENT(000)			B_PEAK_CURRENT(00011)				
0x56						BP2_CURRENT(010)		
0x57	SETTING DISABLE -							
0x58	SETTING DISABLE							
0x59	SETTING DISABLE							
0x5a								GRAY_LEVEL(0)
0x5a-0x5f	SETTING DISABLE							
0x60						SCAN_VOLTAGE(000)		
0x61			SCAN_DRV(00)			SCAN_BIAS(100)		
0x62-0x9f	SETTING DISABLE							
0xa0								STBY(0)
0xa1							GPO(00)	
0xa2				TEST(0)		TEST_PAT(000)		
0xa3								FOSC_TEST(0)
0xa4		OFF_STEP_TIME(000)						OFF_SET(0)
0xa5			OFF_GRAY(000000)					
0xa6-0xaf	SETTING DISABLE							

Display Register 1 (0x00)

	D7	D6	D5	D4	D3	D2	D1	D0
	DISP	-	-	DIR	BGR	-	-	RESET
INIT	0	-	-	0	0	-	-	0

DISP Dot matrix display on/off controls.

Display off means

1) All data output become SINK_R/G/B pin level.

2) Scan output become SVCC_OUT

3) Stop transferring data from memory to data driver

Also, Display on/off controls DCDC, DCDCB (hardware pin) at the same time.

0 : display off, DCDC = 0, DCDCB = 1(default)

1 : display on, DCDC = 1, DCDCB = 0

1ms or more RC-OSC & scan regulator stabilizing time is needed

DIR This bit sets direction of output data.

0 : normal direction

1 : reverse direction

BGR This bit sets direction of RGB or BGR.

0 : normal direction.

1 : reverse direction

Display data		0 [17:0]			1 [17:0]			158 [17:0]			159 [17:0]		
Column Output	DIR='0' BGR='0'	D0	D1	D2	D3	D4	D5	D474	D475	D476	D477	D478	D479
	DIR='0' BGR='1'	D2	D1	D0	D5	D4	D3	D476	D475	D474	D479	D478	D477
	DIR='1' BGR='0'	D477	D478	D479	D474	D475	D476	D3	D4	D5	D0	D1	D2
	DIR='1' BGR='1'	D479	D478	D477	D476	D475	D474	D5	D4	D3	D2	D1	D0

RESET This bit specifies whither all the command register is reset or not.

0 : normal (default)

1 : all command registers reset

* All register are reset state after RESET = 1. You must set RESET = 0 to do normal operation

.

Display Register 2 (0x01)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	WR_DIR			-	IF_MODE		
INIT	-	1	0	1	-	0	0	0

WR_DIR [2:0] This bit sets increment direction of address

WR_DIR [0]: x address increment direction set

0: from 0 to 159.

1: from 159 to 0

WR_DIR [1]: y address increment direction set

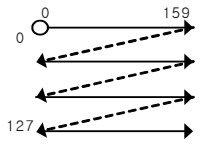
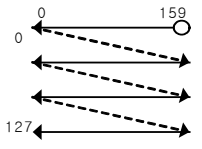
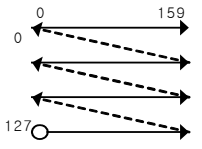
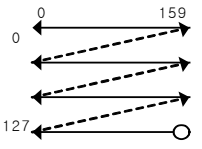
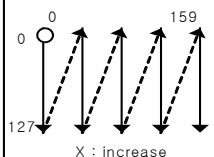
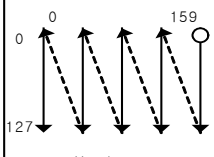
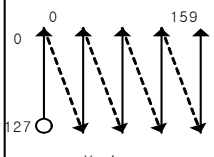
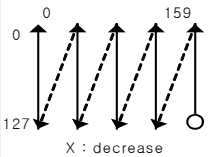
0: from 0 to 127

1: from 127 to 0

WR_DIR[2]: address that increase first of x address or y address

0: y address increase after x address increase

1: x address increase after y address increase

	WR_DIR[1:0]="00"	WR_DIR[1:0]="01"	WR_DIR[1:0]="10"	WR_DIR[1:0]="11"
WR_DIR[2]='0'	 X : increase Y: increase (default)	 X : decrease Y: increase (Y 축 mirror)	 X : increase Y: decrease (X축 mirror)	 X : decrease Y: decrease (X,Y 축mirror)
WR_DIR[2]='1'	 X : increase Y: increase (clockwise 90 rotate and Y 축 mirror)	 X : decrease Y: increase (clockwise 90 rotate)	 X : increase Y: decrease (clockwise 270 rotate)	 X : decrease Y: decrease (clockwise 90 rotate and X축 mirror)

○ Start address (AD_X, AD_Y)

IF_MODE [2:0] This bit sets MPU interface mode

000: 18bit interface, 1 transmission (260k colors)

001: 16bit interface, 1 transmission (65k colors)

010: 9bit interface, 2 transmissions (260k colors)

011: 8bit interface, 2 transmissions (65k colors)

100: 8bit interface, 3 transmissions (260k colors)

101: 6bit interface, 3 transmissions (260k colors)

110-111 : setting disabled

Display Register 3 (0x02)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	DIS_SZ	-	DIS_FRAME		
INIT	-	-	-	0	-	0	1	0

DIS_SZ Display size set

0: 160x128(default)

1: 128x128

Note) **You must change display frame and size in display off mode.**

Data0, scan0 pin is start point of display size that is driver active range.

DIS_FRAME [2:0]

000: 60 Hz

001: 75 Hz

010: 90 Hz

011: 105 Hz

100: 120 Hz

101: 135 Hz

11x : 150 Hz

Panel Typeset Register 1 (0x03)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	-	SCAN_DIR	SCAN_SEQ
INIT	-	-	-	-	-	-	0	0

SCAN_DIR Scan direction set

When scan direction set is '1', first scan line is last line that is setting display size.

SCAN_SEQ Scan time sequence set

0: alternate scan mode (default)

1: sequential scan mode

SCAN_SEQ	SCAN_DIR	128 Line Scan Pin
0	0	S0, S2, … S124, S126, S1, S3, S125, S127
	1	S127, S125, … S3, S1, S126, S124, … S2, S0
1	0	S0, S1, … S126, S127
	1	S127, S126, … S1, S0

Panel Typeset Register 2 (0x04)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	-	-	DIS_ROT
INIT	-	-	-	-	-	-	-	0

DIS_ROT Set the display rotate

0 : not rotate(160x128)

1 : rotate(128x160)

Display Data Register (0x05)

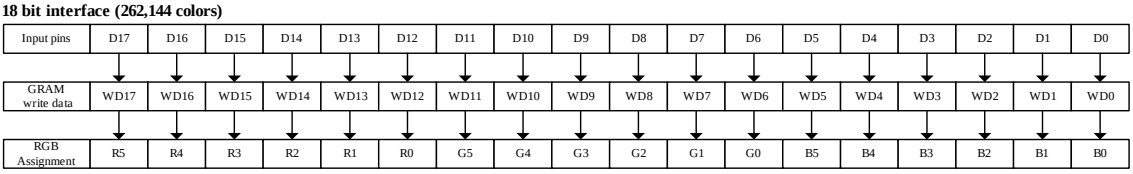
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WD [17:0]																	

WD [17:0] This register is not a real register.

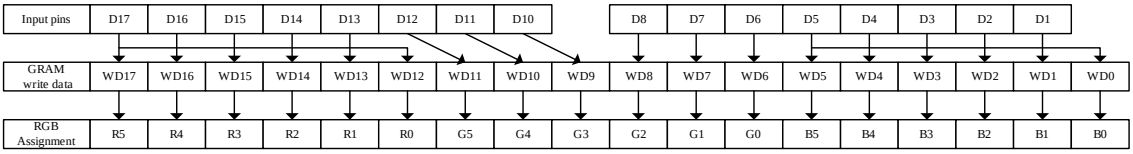
When memory address increment is reached at the end of reading/writing box,

Memory writes finish. If you read or write again, re-enter data read or write command.

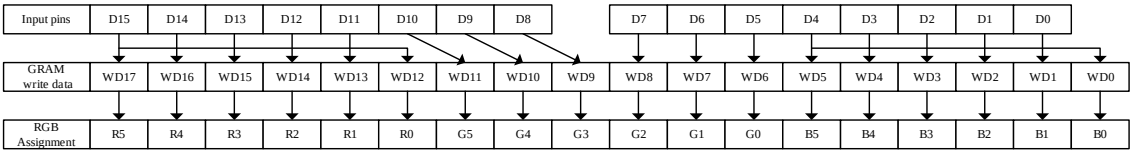
18 bit interface (262,144 colors)



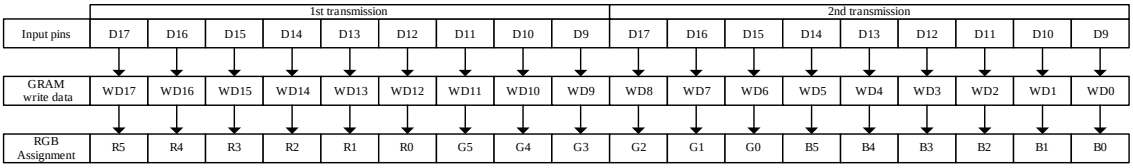
16 bit interface (65,536 colors, COM_SEL='1')



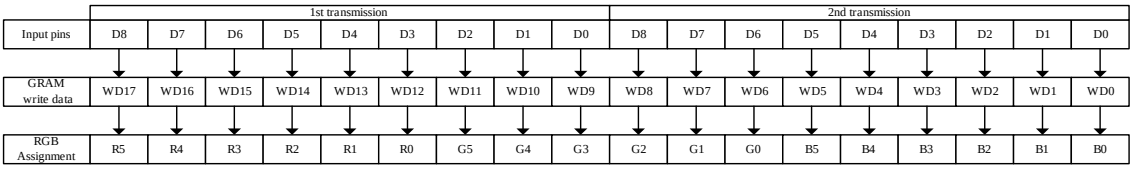
16 bit interface (65,536 colors, COM_SEL='0')



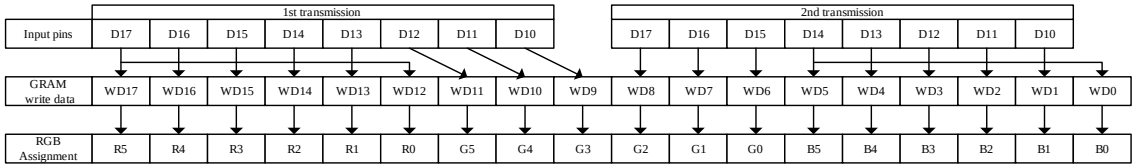
9 bit interface (262,144 colors, 2 transmission, COM_SEL='1')



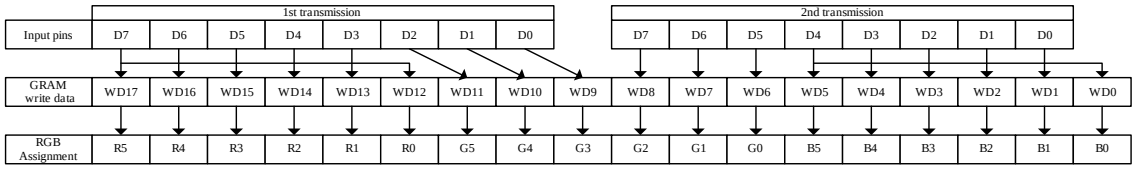
9 bit interface (262,144 colors, 2 transmission, COM_SEL='0')



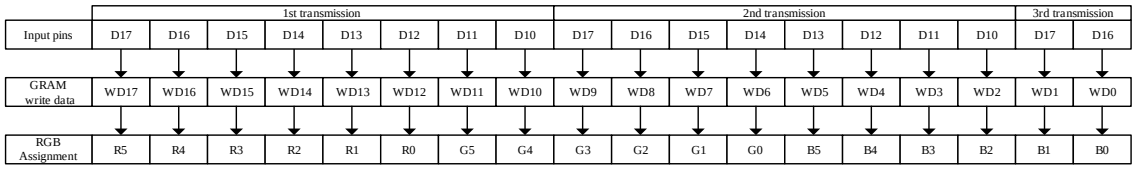
8 bit interface (65,536 colors, 2 transmission, COM_SEL='1')



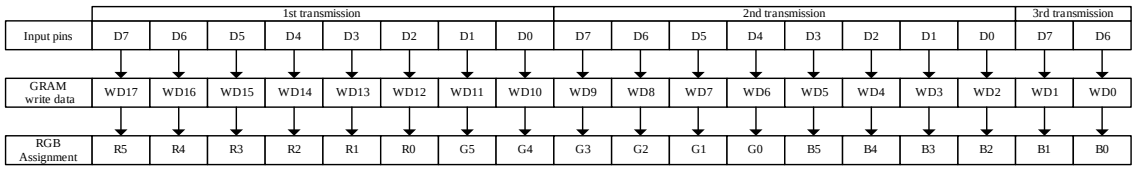
8 bit interface (65,536 colors, 2 transmission, COM_SEL='0')



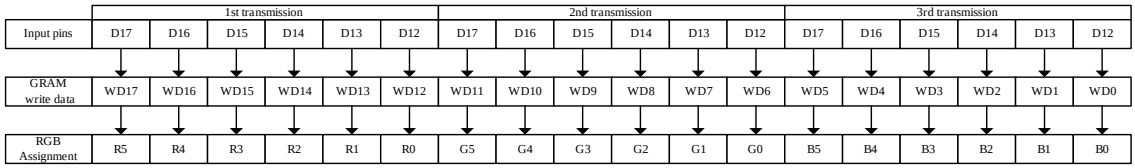
8 bit interface (262,144 colors, 3 transmission, COM_SEL='1')



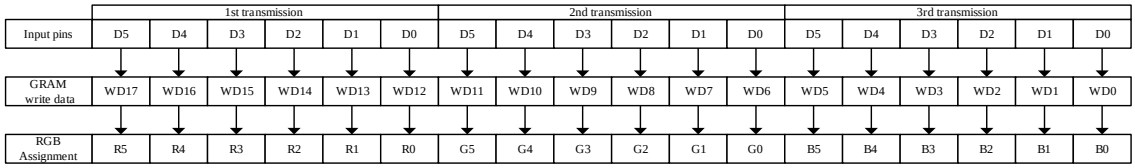
8 bit interface (262,144 colors, 3 transmission, COM_SEL='0')



6 bit interface (262,144 colors, 3 transmission, COM_SEL='1')



6 bit interface (262,144 colors, 3 transmission, COM_SEL='0')



Memory Write Start X Register (0x06)

	D7	D6	D5	D4	D3	D2	D1	D0
	AD_X							
INIT	1	0	0	1	1	1	1	1

AD_X [7:0] Write memory X address value. If want to change X address manually, change this value.

Note) All x direction that described in this spec is a data line.

Memory Write Start Y Register (0x07)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	AD_Y						
INIT	-	0	0	0	0	0	0	0

AD_Y [6:0] Write memory Y address value. If want to change Y address manually, change this value.

Memory X Stat Position Register (0x08)

	D7	D6	D5	D4	D3	D2	D1	D0
	MXSTART							
INIT	0	0	0	0	0	0	0	0

MXSTART [7:0] This registers set the position of start X address of rectangle window.

Memory X End Position Register (0x09)

	D7	D6	D5	D4	D3	D2	D1	D0
	MXEND							
INIT	1	0	0	1	1	1	1	1

MXEND [7:0] This register sets the position of end X address of rectangle window.

Memory Y Starts Position Register (0x0a)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	MYSTART						
INIT	-	0	0	0	0	0	0	0

MYSTART [6:0] This register sets the position of start Y address of rectangle window.

Memory Y End Position Register (0x0b)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	MYEND						
INIT	-	1	1	1	1	1	1	1

MYEND [6:0] This register sets the position of end Y address of rectangle window.

Clock Configuration Register (0x0d)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	-	-	PCDR
INIT	-	-	-	-	-	-	-	0

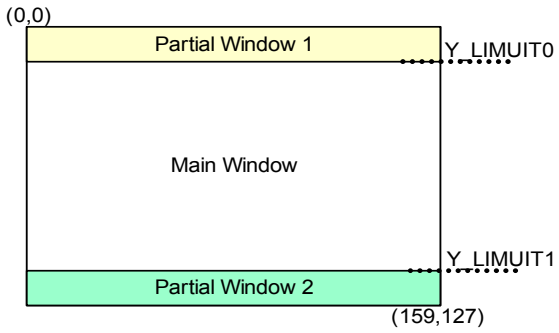
PCDR This register sets unit of Pixel clock

The MCLK is master clock. The PCLK is divided clock.

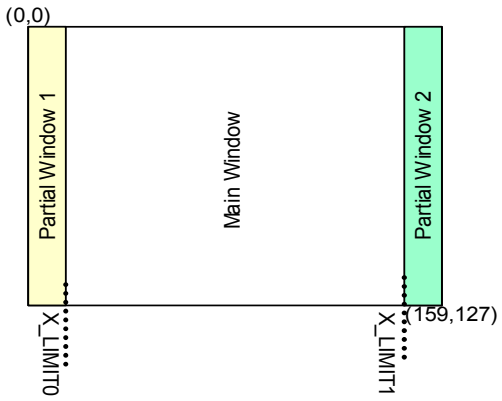
0: PCLK = 1/2*MCLK

1: PCLK = 1/4*MCLK

R_DIS_ROT='0'



R_DIS_ROT='1'



Example)

Y_LIMIT0 = 0, Y_LIMIT1 = 78
Partial Window 1 = Zero Scan line
Main Window = SCAN 0 line ~ SCAN 78 line
Partial Window 2 = SCAN 79 line ~ SCAN 127 line

Screen Save Time Register 1 (0x10)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	SAVE_TIME_SS			-	DISP_TIME_SS		
INIT	-	0	0	0	-	0	0	0

SAVE_TIME_SS [2:0] These bits sets screen save mode time.

000: 480 frames

001: 960 frames

010: 2880 frames

011: 5760 frames

100: 11520 frames

101, 11X : all the time

DISP_TIME_SS [2:0] These bits set how long the current display endure before starting screen save mode.

000: 60 frames

001: 120 frames

010: 180 frames

011: 240 frames

100: 300 frames

101: 360 frames

110: 600 frames

111: 960 frames

Screen Save Time Register 2 (0x11)

	D7	D6	D5	D4	D3	D2	D1	D0
	STEP_TIME_SS0				-	IMAGE_STOP_TIME0		
INIT	0	0	0	0	-	0	0	0

STEP_TIME_SS0 [2:0] These bits set how long one image endures during screen save mode in the Partial window1

0000: 1 frame 0001: 2 frames

0010: 3 frames 0011: 4 frames

0100: 5 frames 0101: 10 frames

0110: 15 frames 0111: 30 frames

1000: 240 frames 1001: 360 frames

1010: 480 frames 1011: 960 frames

1100: 1920 frames 1101: 3840 frames

1110: 5760 frames 1111: setting disabled

IMAGE_STOP_TIME0 [2:0] These bits set how long the screen save mode stops its pattern repetition in the Partial window1.

000: 0 frame

001: 60 frames

010: 120 frames

011: 180 frames

100: 240 frames

101: 360 frames

110-111: Setting disabled

Screen Save Time Register 3 (0x12)

	D7	D6	D5	D4	D3	D2	D1	D0
	STEP_TIME_SS1				-	IMAGE_STOP_TIME1		
INIT	0	0	0	0	-	0	0	0

STEP_TIME_SS1 [2:0] These bits set how long one image endures during screen save mode in the Main window

0000: 1 frame 0001: 2 frames

0010: 3 frames 0011: 4 frames

0100: 5 frames 0101: 10 frames

0110: 15 frames 0111: 30 frames

1000: 240 frames 1001: 360 frames

1010: 480 frames 1011: 960 frames

1100: 1920 frames 1101: 3840 frames

1110: 5760 frames 1111: setting disabled

IMAGE_STOP_TIME1 [2:0] These bits set how long the screen save mode stops its pattern repetition in the Main window.

000: 0 frame

001: 60 frames

010: 120 frames

011: 180 frames

100: 240 frames

101: 360 frames

110-111: Setting disabled

Screen Save Time Register 4 (0x13)

	D7	D6	D5	D4	D3	D2	D1	D0
	STEP_TIME_SS2				-	IMAGE_STOP_TIME2		
INIT	0	0	0	0	-	0	0	0

STEP_TIME_SS2 [2:0] These bits set how long one image endures during screen save mode in the Partial window2

0000: 1 frame 0001: 2 frames

0010: 3 frames 0011: 4 frames

0100: 5 frames 0101: 10 frames

0110: 15 frames 0111: 30 frames

1000: 240 frames 1001: 360 frames

1010: 480 frames 1011: 960 frames

1100: 1920 frames 1101: 3840 frames

1110: 5760 frames 1111: setting disabled

IMAGE_STOP_TIME2 [2:0] These bits set how long the screen save mode stops its pattern repetition in the Partial window2.

000: 0 frame

001: 60 frames

010: 120 frames

011: 180 frames

100: 240 frames

101: 360 frames

110-111: Setting disabled

Screen Save Pattern Register 1 (0x14)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	SSMP0			-	SSM		
INIT	-	0	0	0	-	0	0	0

SSMP0 [2:0] These bits set the pattern during screen save mode in the Partial window 1

000 : multi scroll

001 : color fade

010 : color inversion

011 : fade in/out stop

100 : Pixel vibration

SSM[2:0] These bits set on or Off of screen save mode

SSM[0]:Partial window 1

SSM[1]:Main window

SSM[2]:Partial window 2

0 : off

1 : on

Screen Save Pattern Register 2 (0x15)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	SSMP2			-	SSMP1		
INIT	-	0	0	0	-	0	0	0

SSMP2 [2:0] These bits set the pattern during screen save mode in the Partial window 2

000 : multi scroll

001 : color fade

010 : color inversion

011 : fade in/out stop

100 : Pixel vibration

SSMP1 [2:0] These bits set the pattern during screen save mode in the Main window

000 : multi scroll

001 : color fade

010 : color inversion

011 : fade in/out stop

100 : Pixel vibration

Screen Save Pattern Register 3 (0x16)

	D7	D6	D5	D4	D3	D2	D1	D0
	PV_SEL0		COL_FADE_STEP0		SCRL_DIR0		FADE_MODE0	
INIT	0	0	0	0	0	0	1	1

PV_SEL0[1:0] These bits set the dummy data pattern of pixel vibration mode in the Partial window 1.

00 : black

01: white

10: moving data

11: moving data inversion

COL_FADE_STEP0[1:0] These bits set color fade steps of color fade screen save mode in the Partial window 1.

00 : 1 gray fade out

01: 2 gray fade out

10: 4 gray fade out

11: 8 gray fade out

SCRL_DIR0[1:0] These bits set the direction of multi-scroll screen save mode in the Partial window 1.

00: left scrolling

01: right scrolling

10: down scrolling

11: up scrolling

FADE_MODE0 [1:0] These bits set the face in/out mode in the Main window.

01: Fade In

10: Fade Out

11: Fade In/Out

Screen Save Pattern Register 4 (0x17)

	D7	D6	D5	D4	D3	D2	D1	D0
	PV_SEL1		COL_FADE_STEP1		SCRL_DIR1		FADE_MODE1	
INIT	0	0	0	0	0	0	1	1

PV_SEL1[1:0] These bits set the dummy data pattern of pixel vibration mode in the Main window.

00 : black

01: white

10: moving data

11: moving data inversion

COL_FADE_STEP1[1:0] These bits set color fade steps of color fade screen save mode in the Main window

00 : 1 gray fade out

01: 2 gray fade out

10: 4 gray fade out

11: 8 gray fade out

SCRL_DIR1[1:0] These bits set the direction of multi-scroll screen save mode in the Main window

00: left scrolling

01: right scrolling

10: down scrolling

11: up scrolling

FADE_MODE1 [1:0] These bits set the face in/out mode in the Main window.

01: Fade In

10: Fade Out

11: Fade In/Out

Screen Save Pattern Register 5 (0x18)

	D7	D6	D5	D4	D3	D2	D1	D0
	PV_SEL2		COL_FADE_STEP2		SCRL_DIR2		FADE_MODE2	
INIT	0	0	0	0	0	0	1	1

PV_SEL2[1:0] These bits set the dummy data pattern of pixel vibration mode in the Partial window 2.

00 : black

01: white

10: moving data

11: moving data inversion

COL_FADE_STEP2[1:0] These bits set color fade steps of color fade screen save mode in the Partial window 2

00 : 1 gray fade out

01: 2 gray fade out

10: 4 gray fade out

11: 8 gray fade out

SCRL_DIR2[1:0] These bits set the direction of multi-scroll screen save mode in the Partial window 2

00: left scrolling

01: right scrolling

10: down scrolling

11: up scrolling

FADE_MODE2 [1:0] These bits set the face in/out mode in the Partial window 2.

01: Fade In

10: Fade Out

11: Fade In/Out

Screen Save Pattern Register 6 (0x19)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	FADE_STOP_LEVEL0					
INIT	-	-	0	0	0	0	0	0

FADE_STOP_LEVEL0[5:0] These bits set the lowest gray level of fade in/out stop screen save mode in the Partial window 1

Fade in/out screen save pattern level

FADE_STOP_LEVEL0 has 63 steps of Gray in/out

Set is available set to “000000”~”111110”

Screen Save Pattern Register 7 (0x1a)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	FADE_STOP_LEVEL1					
INIT	-	-	0	0	0	0	0	0

FADE_STOP_LEVEL1[5:0] These bits set the lowest gray level of fade in/out stop screen save mode in the Main window

Fade in/out screen save pattern level

FADE_STOP_LEVEL0 has 63 steps of Gray in/out

Set is available set to “000000”~”111110”

Screen Save Pattern Register 8 (0x1b)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	FADE_STOP_LEVEL2					
INIT	-	-	0	0	0	0	0	0

FADE_STOP_LEVEL2[5:0] These bits set the lowest gray level of fade in/out stop screen save mode in the Partial window 2

Fade in/out screen save pattern level

FADE_STOP_LEVEL0 has 63 steps of Gray in/out

Set is available set to “000000”~”111110”

Limited Screen Save X Position Register 1 (0x1c)

	D7	D6	D5	D4	D3	D2	D1	D0
	X_LIMIT0							
INIT	0	0	0	0	0	0	0	0

X_LIMIT0 [7:0] This register sets the position of X address of limited screen save window.

Limited Screen Save X Position Register 2 (0x1d)

	D7	D6	D5	D4	D3	D2	D1	D0
	X_LIMIT1							
INIT	1	0	0	1	1	1	1	1

X_LIMIT1 [7:0] This register sets the position of X address of limited screen save window.

Limited Screen Save Y Position Register 1 (0x1e)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	Y_LIMIT0						
INIT	-	0	0	0	0	0	0	0

Y_LIMIT0 [6:0] This register sets the position of Y address of limited screen save window.

Limited Screen Save Y Position Register 2 (0x1f)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	Y_LIMIT1						
INIT	-	1	1	1	1	1	1	1

Y_LIMIT0 [6:0] This register sets the position of Y address of limited screen save window.

Screen Save Pattern	Control registers	
Multi Scroll	SCRL_DIR	SAVE_TIME, DISP_TIME, STEP_TIME, IMAGE_STOP_TIME
Color Fade	COL_FADE_STEP	
Fade in/out	FADE_MODE	
Fade in/out Stop	FADE_MODE, FADE_STOP_LEVEL	
Pixel Vibration	-	SAVE_TIME, DISP_TIME, STEP_TIME

Display Timing Register 1 (0x20)

	D7	D6	D5	D4	D3	D2	D1	D0
	DISCHARGE_TIME_R							
INIT	0	0	0	0	0	0	0	0

DIS_CHARGE_TIME_R[7:0] Set the red discharge time of scan line

Discharge time is available set to 0-155 UNIT.

Display Timing Register 2 (0x21)

	D7	D6	D5	D4	D3	D2	D1	D0
	DISCHARGE_TIME_G							
INIT	0	0	0	0	0	0	0	0

DIS_CHARGE_TIME[7:0] Set the green discharge time of scan line

Discharge time is available set to 0-155 UNIT

Display Timing Register 3 (0x22)

	D7	D6	D5	D4	D3	D2	D1	D0
	DISCHARGE_TIME_B							
INIT	0	0	0	0	0	0	0	0

DIS_CHARGE_TIME[7:0] Set the blue discharge time of scan line

Discharge time is available set to 0-155 UNIT

Display Timing Register 4 (0x23)

	D7	D6	D5	D4	D3	D2	D1	D0
	R_PEAK_TIME							
INIT	0	0	0	0	0	1	0	0

R_PEAK_TIME[7:0] Set red peak time of scan line

Red peak time is available set to 0-255 UNIT

Display Timing Register 5 (0x24)

	D7	D6	D5	D4	D3	D2	D1	D0
	G_PEAK_TIME							
INIT	0	0	0	0	0	1	1	0

G_PEAK_TIME[7:0] Set green peak time of scan line

Green peak time is available set to 0-255 UNIT

Display Timing Register 6 (0x25)

	D7	D6	D5	D4	D3	D2	D1	D0
	B_PEAK_TIME							
INIT	0	0	0	0	1	0	0	0

G_PEAK_TIME[7:0] Set blue peak time of scan line

Blue peak time is available set to 0-255 UNIT

Display Timing Register 7 (0x26)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	SCAN_TIME					
INIT	-	0	0	0	0	0	0	0

SCAN_TIME[5:0] Period in scan-to-scan is available 0-63 UNIT

Display Timing Register 8 (0x27)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	BP_EN	-	-	-	BP_MODE
INIT	-	-	-	0	-	-	-	0

BP_EN Dummy 2 line on/off select

0 : Total 1frame time = 128 scan line time

1: Total 1 frame time = 128+2 scan line time

BP_MODE Set display state in Dummy 2 line

0: All SCAN high, all DATA low (zener level)

1: All DATA floating(discharge time section does discharge while is each line)

Even SCAN(SCAN0, SCAN2, …, SCAN126) low → high

Odd SCAN(SCAN1, SCAN3, …, SCAN127) high → low

Display Timing Register 9 (0x28)

	D7	D6	D5	D4	D3	D2	D1	D0
	FLM_LINE							
INIT	0	1	1	1	1	1	1	1

FLM_LINE[7:0] Sets the SCAN Line that FLM output is displayed by high appointment

Red Gamma correction loop-up table set Register (0x40)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	R_LUT						
INIT	-	0	0	0	0	0	0	0

R_LUT [7:0] Set the Red data Gamma correction Look-up table

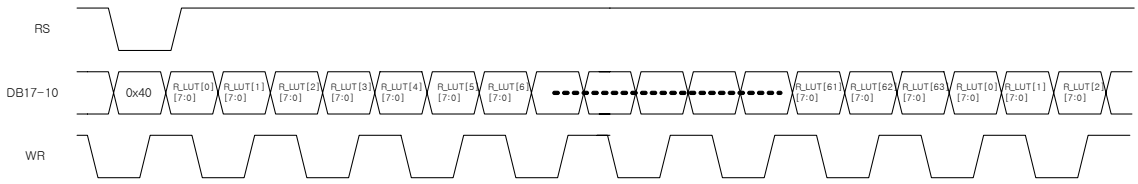
Set the R_LUT[0]~R_LUT[63] register value consecutively

Substitute 6bit gray scale original data by display data that have 7bit gray scale

NOTE) If enter more than 64, value is set from R_LUT[0] again

Substitute 6bit original data by 7bit data

Substitute 6bit gray scale original data by display data that have 7bit gray scale



Green Gamma correction loop-up table set Register (0x41)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	G_LUT						
INIT	-	0	0	0	0	0	0	0

G_LUT [7:0] Set the Green data Gamma correction Look-up table

Set the G_LUT[0]~G_LUT[63] register value consecutively

Substitute 6bit gray scale original data by display data that have 7bit gray scale

NOTE) If enter more than 64, value is set from G_LUT[0] again

Blue Gamma correction loop-up table set Register (0x42)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	B_LUT						
INIT	-	0	0	0	0	0	0	0

B_LUT [7:0] Set the Blue data Gamma correction Look-up table

Set the B_LUT[0]~B_LUT[63] register value consecutively

Substitute 6bit gray scale original data by display data that have 7bit gray scale

NOTE) If enter more than 64, value is set from B_LUT[0] again

Red Dot Current Set Register (0x50)

	D7	D6	D5	D4	D3	D2	D1	D0
	R_CURRENT							
INIT	0	1	0	1	0	0	0	0

R_CURRENT[7:0] Set Maximum current of Red dot

Set 10~153uA in unit of 0.6uA

Green Dot Current Set Register (0x51)

	D7	D6	D5	D4	D3	D2	D1	D0
	G_CURRENT							
INIT	0	1	0	1	0	0	0	0

G_CURRENT[7:0] Set maximum current of Green dot

Set 10~102uA by unit of 0.4uA

Blue Dot Current Set Register (0x52)

	D7	D6	D5	D4	D3	D2	D1	D0
	B_CURRENT							
INIT	0	1	0	1	0	0	0	0

B_CURRENT[7:0 maximum current of Blue dot

Set 10~102uA by unit of 0.4uA

Red Peak Current Set Register (0x53)

	D7	D6	D5	D4	D3	D2	D1	D0
	R_PEAK_DC_CURRENT			R_PEAK_CURRENT				
INIT	0	0-	0	0	0	0	1	1

R_PEAK_CURRENT [4:0] Data channel peak current level set by Red Dot Current

“00000” : 1 time

“00001” : 2 times

“00011” : 4 times

“00111” : 6 times

“01111” : 8 times

“11111” : 10 times

BIAS(DOT) CURRENT SET	PEAK CURRENT SET
RED BIAS(DOT) CURRENT≤102uA	available to 11111(10 times)
102uA <RED BIAS(DOT) CURRENT ≤153uA	available to 00111(6 times)

R_PEAK_DC_CURRENT [2:0] Red data channel peak constant current level set by Red data 1 Gray Current.

“000” : 0

“001” : 1Gray X 16 times

“010” : 1Gray X 32 times

“011” : 1Gray X 48 times

“100” : 1Gray x 64 times

“101” : 1Gray X 80 times

“110” : 1Gray X 96 times

“111” : 1Gray x 112 times

Green Peak Current Set Register (0x54)

	D7	D6	D5	D4	D3	D2	D1	D0
	G_PEAK_DC_CURRENT			G_PEAK_CURRENT				
INIT	0	0	0	0	0	0	1	1

G_PEAK_CURRENT [4:0] Data channel peak current level G set by Green dot current.

"00000" : 1 time

"00001" : 2 times

"00011" : 4 times

"00111" : 6 times

"01111" : 8 times

"11111" : 10 times

G_PEAK_DC_CURRENT [2:0] Green data channel peak constant current level set by Green data 1 Gray current.

"000" : 0

"001" : 1Gray X 16 times

"010" : 1Gray X 32 times

"011" : 1Gray X 48 times

"100" : 1Gray x 64 times

"101" : 1Gray X 80 times

"110" : 1Gray X 96 times

"111" : 1Gray x 112 times

Blue Peak Current Set Register (0x55)

	D7	D6	D5	D4	D3	D2	D1	D0
	B_PEAK_DC_CURRENT			B_PEAK_CURRENT				
INIT	0	0	0	0	0	0	1	1

B_PEAK_CURRENT[4:0] Data channel peak current level B set by blue dot current

"00000" : 1 time

"00001" : 2 times

"00011" : 4 times

"00111" : 6 times

"01111" : 8 times

"11111" : 10 times

B_PEAK_DC_CURRENT [2:0] Blue data channel peak constant current level set by Blue data 1 Gray current.

"000" : 0

"001" : 1Gray X 16 times

"010" : 1Gray X 32 times

"011" : 1Gray X 48 times

"100" : 1Gray x 64 times

"101" : 1Gray X 80 times

"110" : 1Gray X 96 times

"111" : 1Gray x 112 times

BP2 Bias Current Set Register (0x56)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	BP2_CURRENT		
INIT	-	-	-	-	-	0	1	0

BP2_CURRENT[2:0] BP2 Bias Current Set

"000" : 48uA

"001": 60uA

"010": 72uA

"011": 84uA

"100": 96uA

"101":108uA

"110": 120A

'111": 132uA

Data Gray Level Control Register (0x5a)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	-	-	GRAY_LEVEL
INIT	-	-	-	-	-	-	-	0

GRAY_LEVEL 0 gray data level control signal

0 : Floating

1 : Zener level

Scan Voltage Setting Register (0x60)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	SCAN_VOLTAGE		
INIT	-	-	-	-	-	0	0	0

SCAN_VOLTAGE[2:0] Scan voltage set.

"000" : SVCC_OUT = SVCC

"001" : SVCC_OUT = SVCC-(SVCC*0.06)

"010" : SVCC_OUT = SVCC-(SVCC*0.1)

"011" : SVCC_OUT = SVCC-(SVCC*0.14)

"100" : SVCC_OUT = SVCC-(SVCC*0.18)

"101" : SVCC_OUT = SVCC-(SVCC*0.22)

"110" : SVCC_OUT = SVCC-(SVCC*0.26)

"111" : SVCC_OUT = SVCC-(SVCC*0.30)

Scan Driver Control Register (0x61)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	SCAN_DRV		-	SCAN_BIAS		
INIT	-	-	0	0	-	1	0	0

SCAN_BIAS[2:0] Scan Regulator Bias Current Set. Setting larger bias current will stabilizes the scan regulator.

"000" : Halt

"001" : 6uA

"010" : 12uA

"011" : 18uA

"100" : 24uA

"101" : 30uA

"110" : 36uA

"111" : 42uA

SCAN_DRV[1:0] Scan regulator drive capacity set.

"00" : x1

"01" : x10

"10": Setting disabled

"11" : x20

Power Save Set Register (0xa0)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	-	-	STBY
INIT	-	-	-	-	-	-	-	0

STBY This register sets on or Off of blocking clock. If STBY is on, the master clock is stop.

0: not blocking (go)

1: blocking (stop)

GPO Register (0xa1)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	-	GPO	
INIT	-	-	-	-	-	-	0	0

GPO [1:0] This register specifies the value GPO output pin.

Test Mode Register (0xa2)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	TEST	-	TEST_PAT		
INIT	-	-	-	0	-	0	0	0

TEST This bit sets on or Off of test pattern mode.

0: off

1: on

TEST_PAT [2:0] These bits set test patterns.

000: black pattern

001: red pattern

010: green pattern

100: blue pattern

111: white pattern

RC–OSC Test Register (0xa3)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	-	-	-	FOSC_TEST
INIT	-	-	-	-	-	-	-	0

FOSC_TEST This register sets on or off of fosc test.

0 : normal operation

1 : fosc test mode

Display OFF Mode Register 1 (0xa4)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	OFF_STEP_TIME			-	-	-	OFF_SET
INIT	-	-	-	-	-	-	-	0

OFF_STEP_TIME [2:0] These bits set fade out display off step.

000: 1 frame

001: 2 frames

010: 3 frames

011: 4 frames

100: 5 frames

101: 10 frames

110: 15 frames

111: 30 frames

OFF_SET This register sets display off mode.

0 : normal display off

1 : fade out display off

Display OFF Mode Register 2 (0xa5)

	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	OFF_GRAY					
INIT	-	-	0	0	0	0	0	0

OFF_GRAY[5:0] These bits set gray level of fade out display off

After fade out as 64-OFF_GRAY step, become display off

Display Timing

Data channel waveform is consisted of Hold time, Discharge time, Peak time and display time.

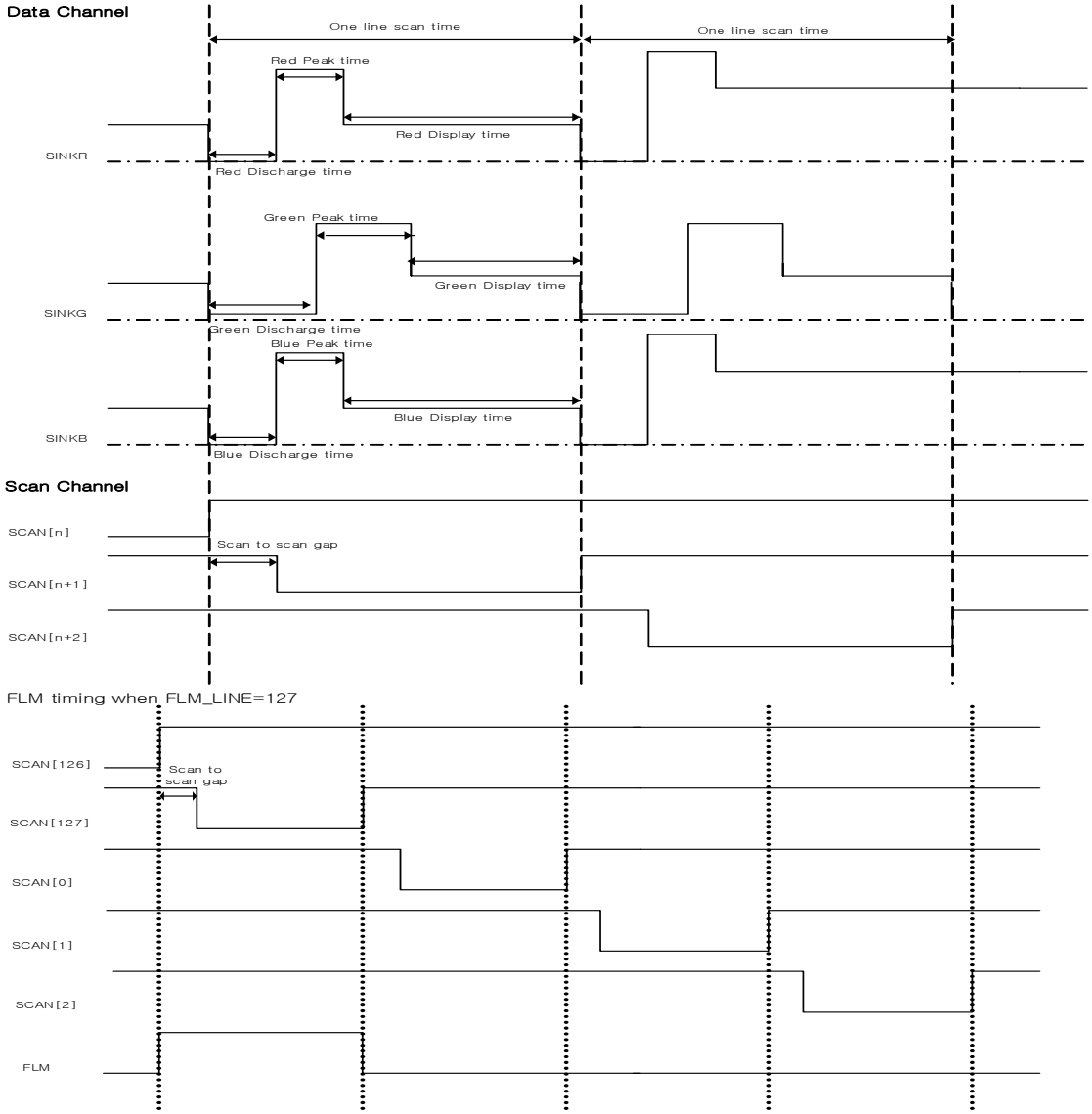
Hold time is that N line data is valid from rising edge of N line scan channel. Set the Discharge time is data output by SINK_R/G/B zener level set

Peak time is

That if N+1 line data output is zero, data output becomes SINK_R/G/B zener level.

That if N+1 line data output is not zero, data output becomes Peak current ((N+1 line data) x (5~40))

Display tine is that data output becomes gray current level corresponding to gray scale of GRAM.



Scan Time and Frame Frequency

Scan time is sum of holding time, discharge time, step time, display time. Unit time (UNIT) to decide Scan time is division / RC-OSC frequency

➔ Scan time = hold time + discharge time + peak time + display time

➔ UNIT = division ratio / RC-OSC freq.

RC-OSC freq. = 4MHz, UNIT = 2 x 250ns = 500ns (default)

RC-OSC freq. = 5MHz, UNIT = 2 x 200ns = 400ns

Frame frequency can be selected in 60, 75, 90, 105, 120, 135, 150Hz. Scan time is decided by each Frame frequency and Display Time is automatically decided by holding time, discharge time and peak time

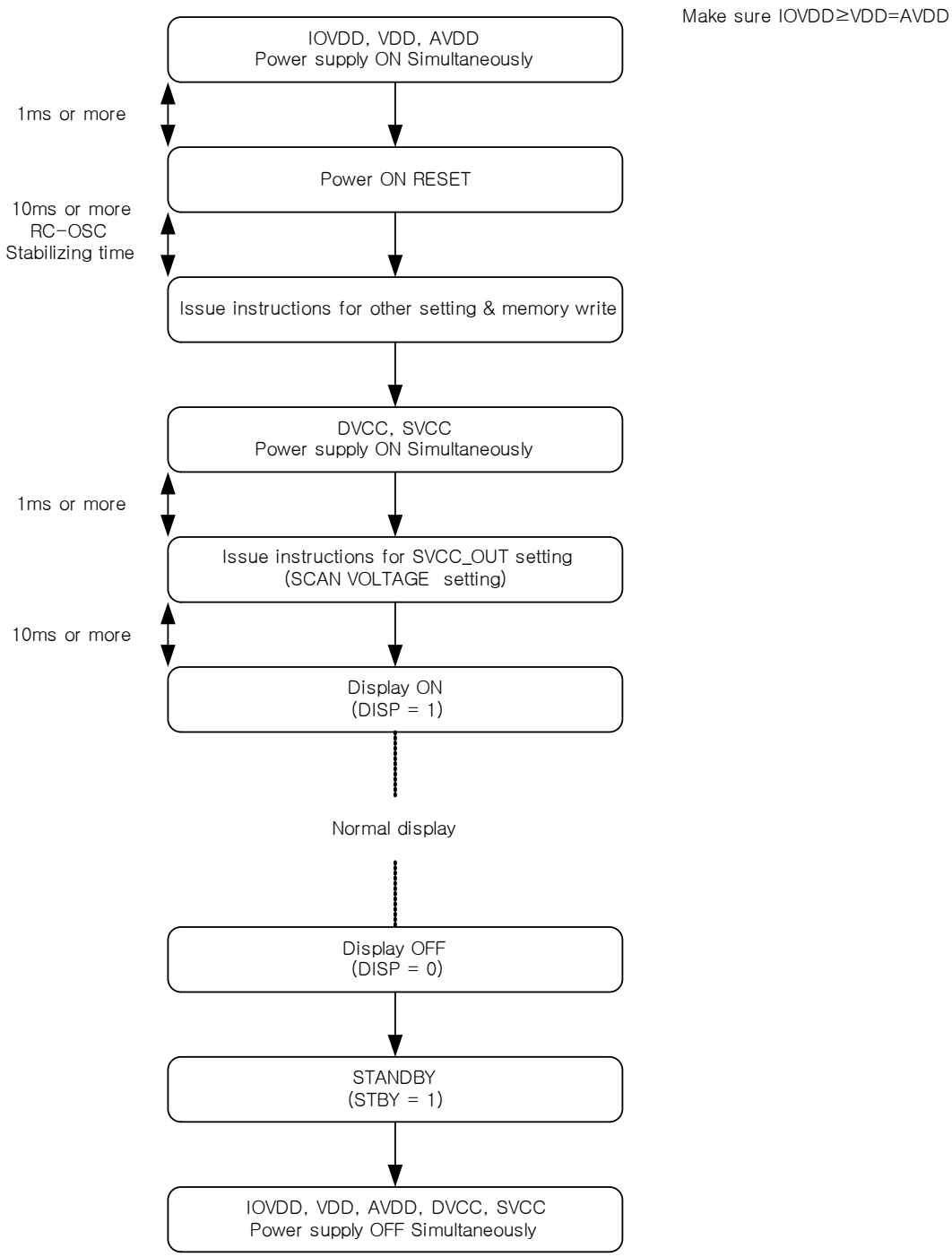
➔ Display time = scan time – (hold time + discharge time + peak time)

Display size supports 160x128, 128x128.

Display size	Frame freq. (Hz)	Scan Time (UNIT)	Discharge Time (UNIT)	Peak Time (UNIT)	Display Time (UNIT)
160x128	60	256			
	75	205			
	90(default)	170			
	105	146			
	120	128			
	135	114			
	150	102			
128x128	60	256			
	75	205			
	90(default)	170			
	105	146			
	120	128			
	135	114			
	150	102			

Power Supply ON/OFF Sequence

When supplying and cutting off power, follow the sequence below.



Reference Current Resistor Values

AVDD	2.2V	2.5V	2.7V	2.8V	2.9V
RREF	13kOhm	16kOhm	16kOhm	18kOhm	18kOhm

The RREF should be fixed according to the AVDD. For example, the RREF should be 18kOhm, if AVDD is 2.8V. Other RREF value is not allowed.

RC-OSC Resistor Values

ROSC[kΩ]	RC-OSC frequency : fosc[MHz]		
	2.2V	2.8V	2.9V
11[kΩ]	5.03	5.3	5.34
15[kΩ]	3.85	4.02	4.03
20[kΩ]	2.96	3.08	3.1

The ROSC should be fixed according to the VDD. For example, the ROSC should be 15kOhm, if VDD is 2.8V. Other ROSC value is not allowed. The oscillation frequency is changeable with the value of external resistor. Clock pulses can be supplied externally. During stand-by mode, the RC oscillation is halted to reduce power consumption.

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes
Power supply voltage(1)	DVCC, SVCC	V	TBD	
Power supply voltage(2)	IOVDD	V	TBD	
Power supply voltage(3)	VDD, AVDD	V	TBD	
Input voltage	Vin	V	TBD	
Operating temperature	Topr	°C	TBD	

Recommended Operating Conditions

Item	Symbol	Unit	Min	Typ	Max	Notes
Power supply voltage(1)	DVCC, SVCC	V	10		21	
Power supply voltage(2)	IOVDD	V	2.2		3.3	
Power supply voltage(3)	VDD, AVDD	V	2.2		2.9	
Input voltage	Vin	V			TBD	
Operating temperature	Topr	°C			TBD	

Electrical Characteristics (DC Characteristics)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Logic input high level		0.7VDD		VDD	V
VIL	Logic input low level		0		0.3VDD	V
VOH	Logic output high level		0.8VDD		VDD	V
VOL	Logic output low level		0		0.2VDD	V
Iol	Output leakage current				TBD	uA
Iil	Logic input leakage current				TBD	uA
Ip2p	Data current pin to pin mismatch				TBD	%
Icin	Data output current chip in mismatch				TBD	%
Ic2c	Data current chip to chip mismatch				TBD	%
Ron	Scan on resistance				20	Ω
Roff	Scan off resistance				3	kΩ
Rdis	Data discharge on resistance				500	Ω
Ist_high	High voltage standby current	DVCC=SVCC=21V			TBD	uA
Ist_low	Low voltage standby current	IOVDD=3.3V			TBD	uA
Ist_low	Low voltage standby current	VDD=AVDD=2.9V			TBD	uA
Iop_high	High voltage operating current	DVCC=SVCC=21V			TBD	uA
Iop_low	Low voltage operating current	IOVDD=3.3V			TBD	uA
Iop_low	Low voltage operating current	VDD=AVDD=2.9V			TBD	uA

Electrical Characteristics of RC-OSC

Item	Symbol	Unit	Conditions	Min	Typ	Max	Notes
Power supply	VDD	V		2.2	2.8	2.9	
R-C oscillation clock	fosc	MHz	ROSC= 15kΩ, VDD = 2.8V	3.52	4	4.48	
Clock fluctuation	∆fosc	%		-12		+12	