DS12864-6

Presented by: _____

Date: _____

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1 MECHANICAL SPECIFICATIONS & FEATURES

1.1 Mechanical Specifications

※ Module Size: 93.0(W)×70.0(H)×13.5(T) (mm)

※ Viewing Area: 70.6(W)×38.8 (H)(mm)

※ Dot Size: 0.48W)×0.48(H)(mm)

※ Dot Pitch: 0.52(W) ×0.52(H)(mm)

1.2 Features

※ Dot Matrix: 128×64 Dots

※ LCD Mode: STN

※ Controller IC: S6B0107/S6B0108

※ Data Display RAM: 4096 Bits

※ Driving Method: 1/64 Duty; 1/9 Bias

※ Viewing Angie: 6 O'clock direction

※ 4-Bit or 8-Bit MPU Interface

※ Backlight: LED

※ Backlight Color: White

※ Operating Temperature Range: -20 to 70℃;

※ Storage Temperature Range : -30 to 80℃;

　　Note: Color tone is slightly changed by temperature and driving voltage.

2 PINS CONNECTION

Pin NO.	Symbol	Function
1	VSS	Ground
2	VDD	Power Supply Voltage for Logic (DC+5V)
3	V0	Supply Voltage for LCD
4	RS	Data/Instruction Select (1: Data; 0: Instruction)
5	R/W	Read/Write Select. 1: Read; 0: Write
6	E	Enable Signal
7~14	DB0~DB7	Data Bus
15	CSA	SEG Driver A Select
16	CSB	SEG Driver B Select
17	RES	Reset System
18	VEE	Negative Voltage for LCD Driving(-10V)
19	VLBA	Power Supply for LED Backlight (5.0V)
20	VLBK	LED Backlight Power Ground

3 EXTERNAL DIMENSION
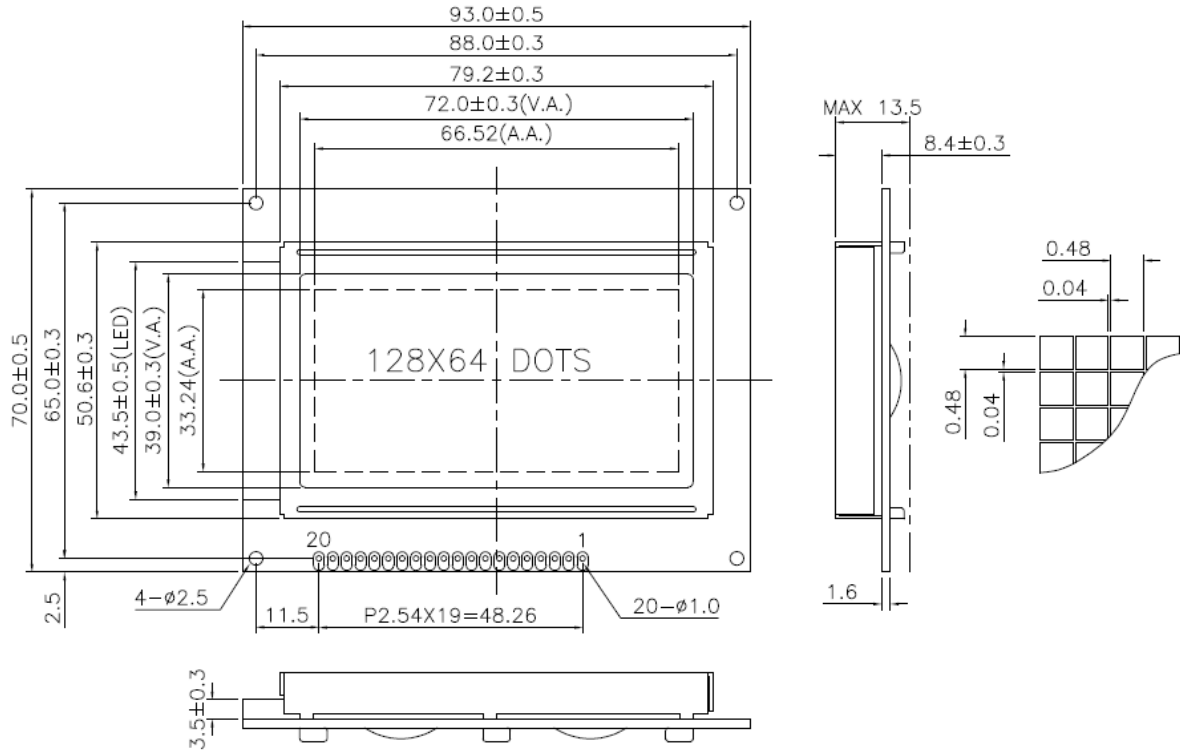
4 ABS0LUTE MAXIMUM RATINGS

4.1 Electrical Absolute Ratings

Item	Symbol	Standard Value		Unit
		Min.	Max.	
Power supply Voltage	VDD-VSS	0	7	V
LCD Driving Voltage	VDD-VEE	VDD-19.0V	VDD+0.3V	V
Input Voltage	VIN	VEE-0.3	VDD+0.3V	V
Static Electricity	-	-	100	V
Operating Temperature Range	TOP	-20	+70	$^{\circ}$C
Storage Temperature Range	TST	-30	+80	$^{\circ}$C

4.2 Environmental Absolute Ratings

Item	TST		TOP		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-30°C	+80°C	-20°C	+70°C	Note 1)
Humidity	Note 2)		Note 2)		No Condensation
Vibration	-	4.9m/s²	-	20m/s²	3 Directions (X/Y/Z)
Shock	-	30m/s²	-	490m/s²	6 Directions (±X±Y±Z)

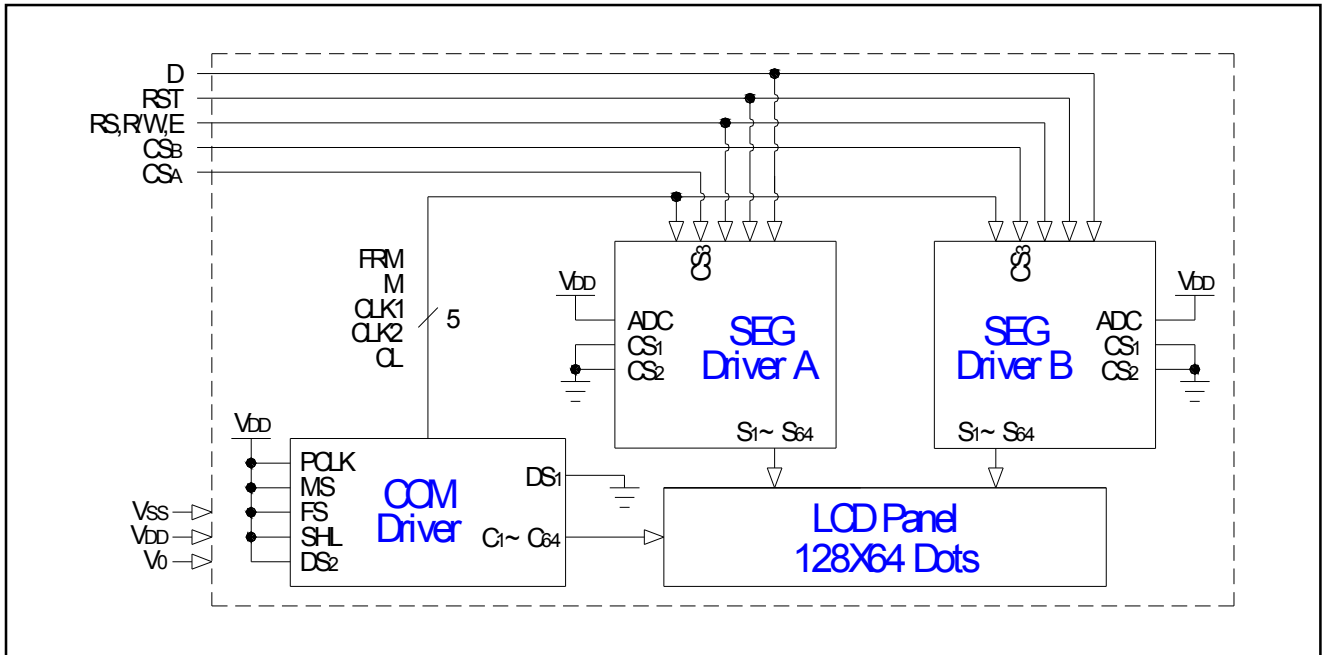Note 1) Care should be taken so that the LCD module may not be subjected to the temperature out of this specification.

Note 2) Ta≤40°C: 90% RH Max

Ta＞40°C: Absolute humidity shall be less than Ta=40°C/90% RH.

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5 BLOCK DIAGRAM

Module internal set description:

※ *Data shift direction : C1→C64;*
※ *Relation between Y address of display RAM and LCD segment: Y0/S1→Y63/S64*
※ *Data shift at the rising edge of CL2;*
※ *The oscillation frequency: fOSC=430KHz;*
※ *Set CS1=0, CS2=O, and CS3 be connecting to module interface, CS3=1: chip selection.*
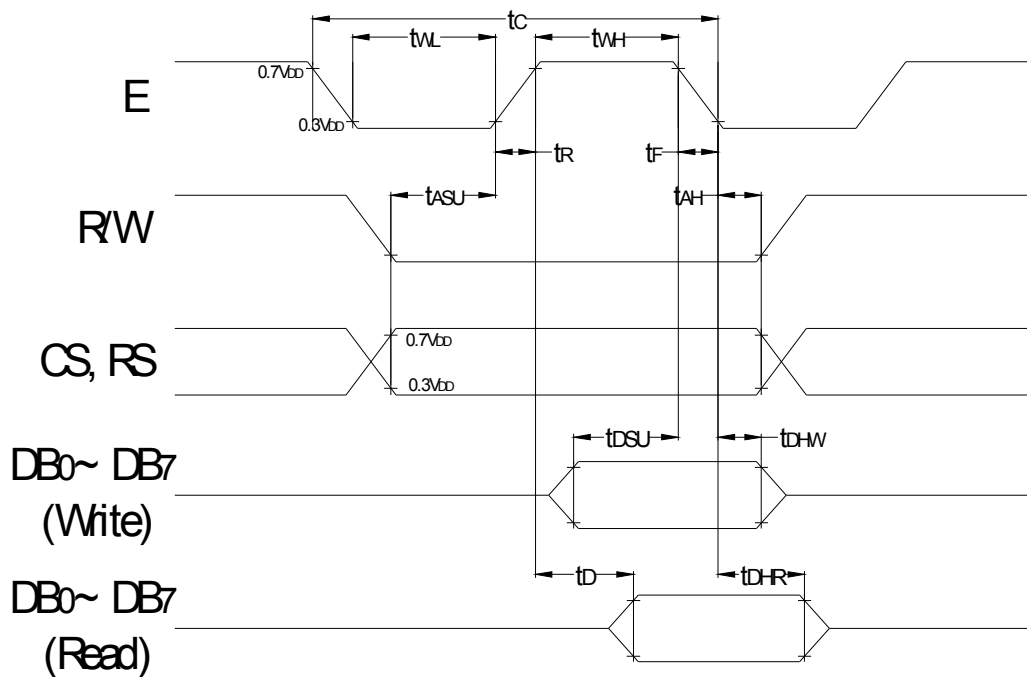
6 ELECTRICAL CHARACTERISTICS

6.1 DC Characteristics

Ta=25℃, VDD=5V±10%, VSS=OV

Item	Symbol	Standard Value			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	VDD	4.5	5.0	5.5	V
LCD Driving Voltage	VEE	-	-10.0	-	V
Input high Voltage	VIH	0.7*VDD	-	VDD	V
Input Low Voltage	VIL	0	-	0.3*VDD	V
Power Supply Current	IDD	-	-	10	mA
LCD Power Supply Current	I0	-	-	1	mA
LED Backlight Power Supply Voltage	Vf	-	3.1V	-	V
LED Backlight Power Supply Current	If	-	90	-	mA

6.2 AC Characteristics

Item	Signal	Symbol	Min	Max	Unit
E Cycle		tC	1000	-	
E High Level Width		tWH	450	-	
E Low Level Width	E	tWL	450	-	
E Rise Time		tR	-	25	
E Fall Time		tF	-	25	ns
Address Setup Time	R/W, CS, RS	tAS	140	-	
Address Hold Time		tAH	10	-	
Data Setup Time		tDS	200	-	
Data Delay Time	DB0~DB7	tDD	-	320	
Data Hold Time (Write)		tDHW	10	-	
Data Hold Time (Read)		tDHR	20	-	

7 OPTICAL CHARACTERISTICS

Item	Symbol	Min	Typ	Max	Unit	Condition	Note
Viewing Angle	θ2-θ1	70	90	120	Deg.	Cr=2.0	1,2
	Φ	-45	0	+45			
Contrast Ratio	Cr	-	4	-	-	θ＝２０°；Φ＝０°	3
Response Time (rise)	Tr	-	250	-	ms	θ＝２０°；Φ＝０°	4
Response Time (fall)	Tf	-	350	-	ms	θ＝２０°；Φ＝０°	4

Above data are measured under 1/64 duty FSTN-Grey mode

Φ= 0° means viewing direction

Note 1: Definition of viewing angle θ & Φ	*Note 2: Definition of viewing angle θ2*

Note 3: Definition of contrast Cr

$Cr = (A/B)^P$
Negative: P= -1
Positive: p= + 1

Note 4: Definition of optical response
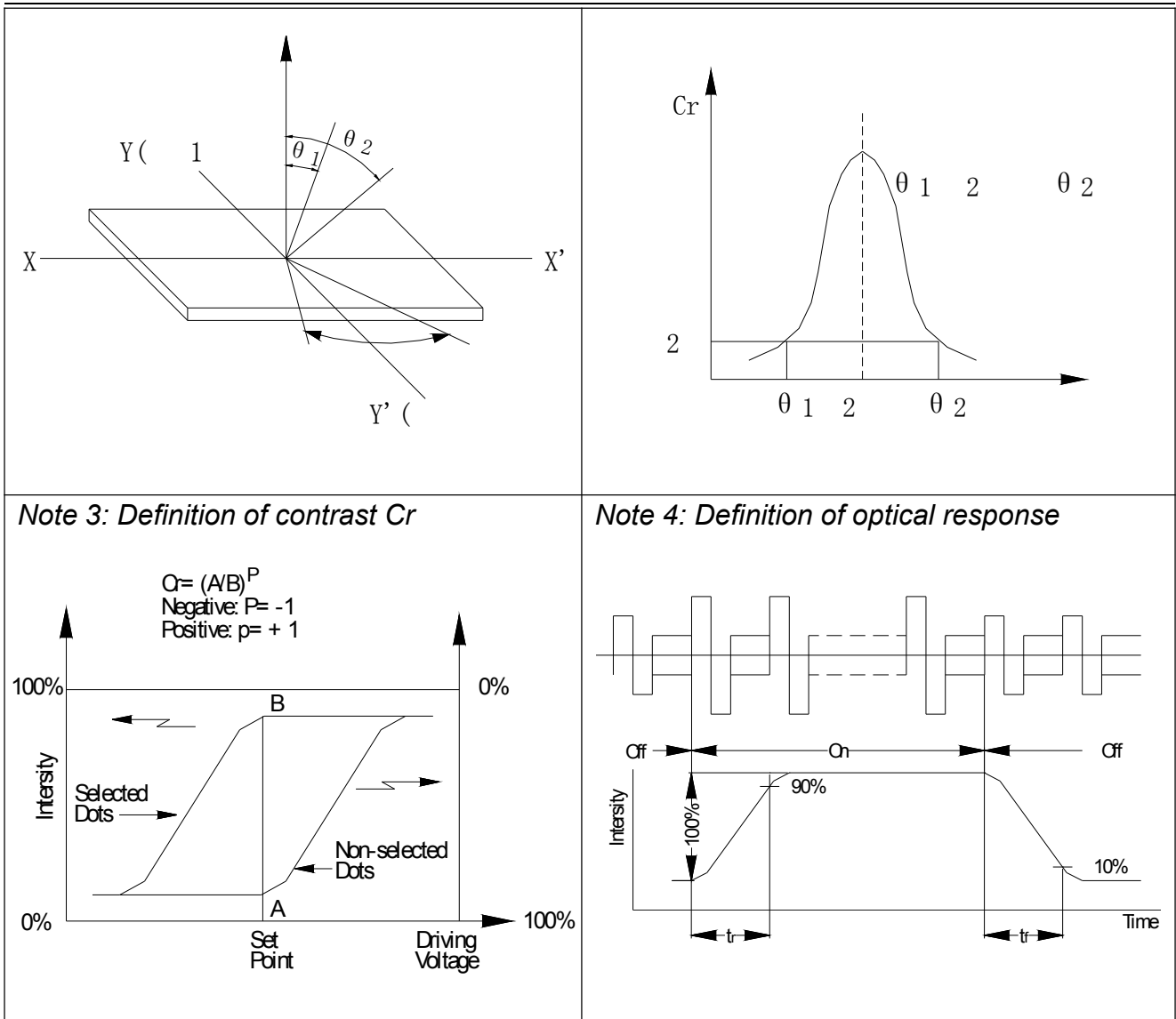
8 FUNCTIONAL DESCRIPTION

8.1 Interface Control

8.1.1 I/O Buffer

Data is transferred through 8 data bus lines (DB0~DB7).

DB7: MSB (Most significant bit); DB0: LSM (Least significant bit)

Data can neither be input nor output unless CS1 to CS3 are in the active mode. When

CS1 to CS3 are not active mode the internal state is maintained and no instructions executes. Besides, pay attention to RST and ADC which operate irrespectively of CS1 to CS3.

8.1.2 Register

△ Input register

The input register is used to store data temporarily before writing it into display data RAM (automatically by internal operation). When CS1to CS3 are in the active mode and RS and R/W select the input register as shown in table, data is latched at the fall of the E signal.

△ Out register

The output register is used to store data temporarily that is read from display data RAM. To read out the data from output register, CS1 to CS3 should be in the active mode and both RS and R/W should be 1as shown in table.

Register Selection Table

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation(DD RAM→Output register)
1	0	Writes data into input register as internal operation(Input register→DD RAM)
0	1	Busy check. Read of status data
0	0	Instruction

8.2 Busy Flag

Busy Flag = 1 indicates the IC is operating and no instructions except status read instruction can be accepted. The value of the busy flag is read out on DB7 by the status read instruction.

8.3 Display ON/OFF Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments S1 to S64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments is disappeared in off state independent of the data in RAM.

RST=0 sets the segment in 0ff state. The status of the flip/flop is output to DB5 by status read instruction. To control display data latch by this flip/flop, CL signal should be input.

Display on/off instruction does not influence data in RAM.

8.4 Display Start Line Register

The display start line register specifies the line in RAM, which corresponds to the top line of LCD panel, when displaying contests in display data RAM on the LCD panel.

6-bit display start line information is written into this by the display start line set instruction. When high level of the FRM signal starts the display, the information in this in this register is transferred to the Z address counter, which controls the display address, presetting the Z address counter.

8.5 X, Y Address Counter

A 9-bit counter which designates address of the internal display data RAM. X address counter(upper 3 bit) and Y address counter (lower 6 bit) should be set to each address by the respective instruction.

X address counter

Ordinary register with no count functions. An address is set by instruction.

Y address counter

An address is set by instruction and is increased by 1 automatically by R/W operations of

display data. The Y address counter loops the values of to 63 to count.

8.6 Display Data RAM

Stores dot data for display. 1-bit data of this RAM corresponds to light on(data=1)and light off(data=0)of 1 dot in the LCD display panel. The correspondence between Y addresses of RAM and segment pins can be reversed by ADC signal.

Note: ADC=1(ADC connect VDD) of the module internal circuit set.

Figure: Relation between RAM Data and Display

Relation between RAM Data and Display
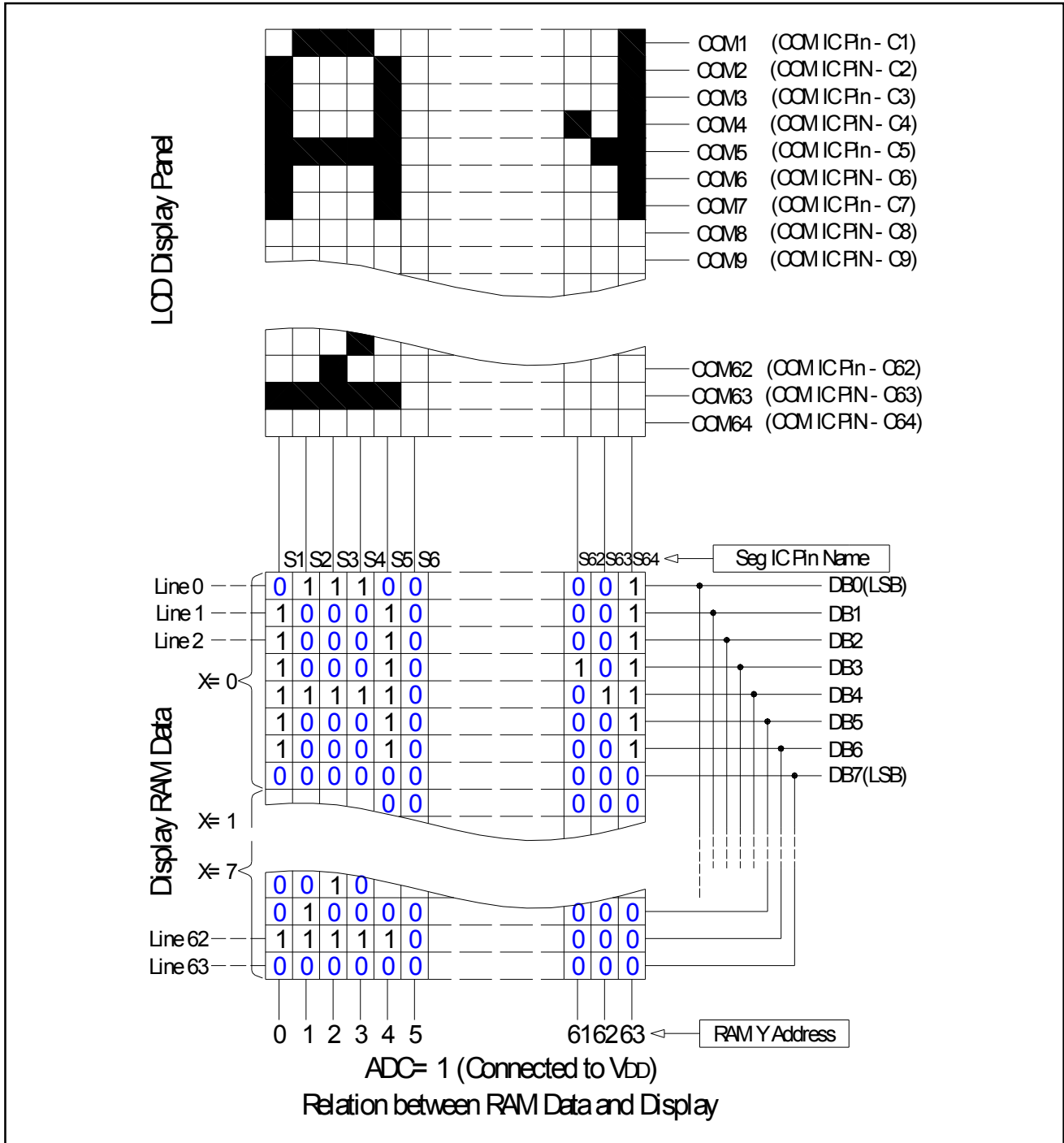
8.7 Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At the high level of FRM, the contents of the display start line register is preset at the Z

counter.

8.8 Bi-directional Shift Register

A 64-bit bi-directional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bi-directional shift register, which is on the DL side, corresponds to C1, and the highest order bit on the DR side corresponds to C64.

Note: SHL=1(SHL connect VDD) of the module internal circuit set.

8.9 Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit. Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

8.10 Timing generator Circuit

The timing generator circuit generates display timing and operating clock.

8.11 Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to he output terminals

Data of latched (columns) / Data from the shift register (lines)	M	Output Level	
		Segment	Common
1	1	V1	V2
0	1	V3	V6
1	0	V2	V1
0	0	V4	V5

8.12 Reset

The system can be initialized by setting RST terminal at low level when turning power on.

While RST is low level, no instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0(clear RESET) and DB7=0(Ready) by status read instruction. The conditions of power supply at initial power up are shown in table.

9 INSTRUCTIONS

9.1 Instructions table

Instruction	Code										Function
	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	0	0	1	1	1	1	1	0 / 1	Controls the Display ON or OFF. Internal Status and Display RAM Data are not Affected. L:OFF; H:ON
Set Address (Y-Address)	0	0	0	1	Y-Address (1~64)						Set the Y-Address in the Y counter
Set Page (X-Address)	0	0	1	0	1	1	1	Page (0~3)			Set the X-Address in the X-Address Register
Display Start Line (Z-Address)	0	0	1	1	Display Start Line (1~64)						Determines the Display Data RAM Displayed at the top of the Screen
Statue Read	0	1	BUSY	0	ON/OFF	RESET	0	0	0	0	Read the Status BUSY=0: Ready; BUSY=1: In Operation; ON/OFF=1: Display Off; ON/OFF=0: Display On; RESET=1: Reset; RESET =0: Normal
Write Display Data	1	0	Write Data								Write Data (DB0~DB7) to the Display Data RAM. After Writing Instruction, Y-Address Automatically Incremented by 1.
Read Display Data	1	1	Read Data								Read Data (DB0~DB7) from Display Data RAM to the Data Bus.

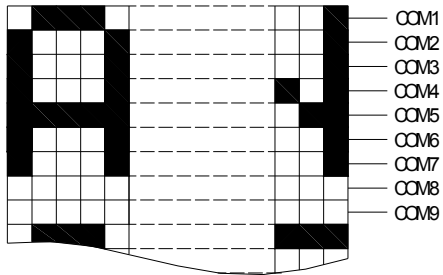## 9.2 Explanation of Instruction Code
9.2.1 Display On/Off

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	1	1	1	1	D

This command turns the display on and off.

D=0: Display On;   D=1: Display Off

9.2.2 Display Start Line

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	1	A	A	A	A	A	A

Start Line= 0
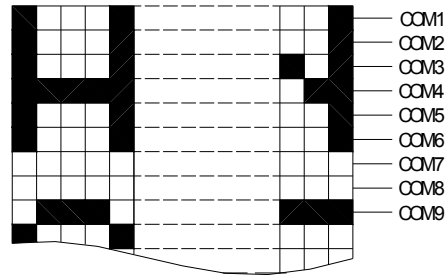
Start Line= 1
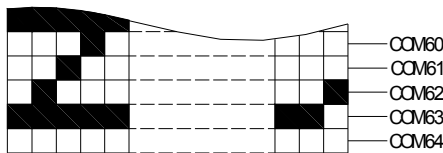
Start Line= 2

Start Line= 3
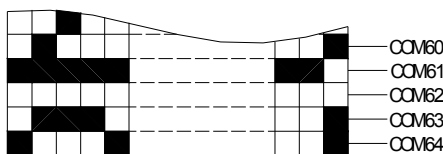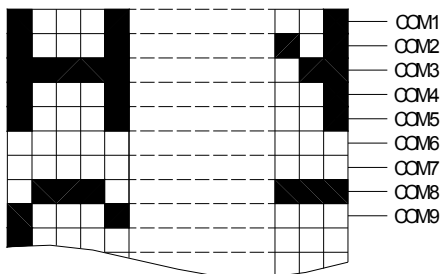
9.2.3 Set Address (Y-Address)

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

This command loads the display start line register.

9.2.4 Set Page (X- Address)

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	1	1	1	AC2	AC1	AC0

This command loads the page address register.

9.2.5 Read Status

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BUSY	0	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

BUSY: BUSY=1 indicate the operating or Reset cycle.

he instruction can be input after the BUSY status change to "0".

ON/OFF: Indicate the whole display ON/OFF status.

0: Whole Display "ON"; 1: Whole Display "OFF"

RESET: Indicate the initialization period by RST signal or reset instruction.

0: Currently executing reset command; 1: Initialization Period

9.2.6 Write Display Data

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

9.2.7 Read Display Data

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	Read data							

Reads 8-bits of data from the I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.

After loading a new address into the column address register one dummy read is required before valid data is obtained.

10 PRECAUTIONS IN USE OF LCM
10.1 Handing of LCM

LCM may be broken because it is made of glass. In case the liquid crystal touches human hand, skin, eye and cloth, must use water to wash it out thoroughly and immediately.

Leave the module in its package bag before use it.

Keep the module operated or storage within specified temperature and humidity range.

Polarize is a soft material and can easily be scratched.

Please avoid static electricity.

Do not touch the connection rubber or heat seal, nor modify the location.

Do not move the tab of the metal holder nor make any rearrangement to it.

10.2 Storage

Store in an ambient temperature of 5 to 35°C and in a relative humidity of 40 to 60%.

If you store as unpacked, put in anti-static bag, seal its opening and store where it is not subjected to direct sunlight and fluorescent lamp.

10.3 Installing

Do not take off the protective firm attached on display surface.

Leave enough height to avoid stressing to the surface. A measurement tolerance ±0.1mm is necessary.

Do not directly mark on the PCB while soldering the connector or cable.

Soldering iron, no higher than 260°C and less than 3-4 second during soldering.

Connector rework soldering, no more than 3 times.