R61580

262,144-color, 240RGB x 320-dot Graphics Liquid Crystal Controller Driver for Amorphous-Silicon TFT Panel

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Description

The R61580 is a liquid crystal controller driver LSI with internal frame memory for amorphous silicon TFT panel sized 240RGB x 320-dot at the maximum.

The driver supports high-speed 8-/, 9-/, 16-/ and 18- bit interfaces as system interface to microcomputer enabling an efficient data transfer.

The R61580 is also supports RGB-I/F (VSYNC, HSYNC, DOTCLK, ENABLE and DB[17:0]) for video data display.

The R61580 incorporates step-up and voltage follower circuits to generate drive voltage required for α-Si TFT panel and dynamic backlight control (BLC) function to control backlight brightness depending on image data reducing power consumption at the backlight with slightest influence on the image quality.

Other features include 8-color display and power management functions, making the driver best suitable for small or mid sized portable devices such as digital mobile phones and small PDAs where a long battery life is a major concern.

Features

- Single chip driver for 262,144-color TFT 240RGB x 320-dot graphics (with internal source, gate and power supply circuits)
- System interface
  - 16-/, 18- bit RGB I/F (VSYNC, HSYNC, DOTCLK, ENABLE and DB[17:0])
  - VSYNC I/F (System interface + VSYNC)
  - FMARK I/F (System interface + FMARK Synchronization signal)
- Window address function to specify a rectangular area in the internal frame memory to write data
- Write data within a rectangular area in the internal frame memory via moving picture interface
  - Reduce data transfer by specifying the area in the frame memory to rewrite data
  - Enable displaying the data in the still picture frame memory area with a moving picture simultaneously
- Abundant color display
  - 262,144-color display
  - Partial display function
- Low-power consumption architecture (allowing direct input of interface I/O power supply)
  - Deep standby mode
  - 8-color mode
  - Input power supply voltage:
    Interface I/O power supply: IOVCC
    Logic power supply: VCC
    Liquid crystal analog circuit power supply: VCI
- Dynamic Backlight Control Function
- Internal liquid crystal drive power supply circuit
  - Liquid crystal drive (source driver/VCOM): DDVDH, VREG1OUT, VCL, VCI
  - Gate driver power supply: VGH, VGL

  - VCOM drive (common VCOM): VCOMH, VCOML
- Liquid crystal power supply start up sequencer
- TFT storage capacitance: Cst only (common VCOM)
- Internal frame memory: 172,800 bytes
- Liquid crystal display drive circuits: 720 source signal lines, 320 gate signal lines
- Single chip, gate output arranged on both sides of the chip for COG mounting
- Internal Non-Volatile Memory (NVM)
  - 8 bits for user identification code,
  - 7x2 bits for VCOM adjustment): Rewriting is possible up to 5 times.
  - Write/Erase sequencer
  - Power supply circuit for write/erase
- Internal reference voltage to generate VREG1OUT

Note:1. The moving picture interface has been patented.
United States Patent No. 7,176,870
Japanese Patent No.3,826,159
Korean Patent No.747,636

Power Supply Specification

Table 1 R61580 Power Supply Specification

No.	Item		R61580
1	TFT data lines drive circuit		720 outputs
2	TFT gate line drive circuit		320 outputs
3	TFT display storage capacitance		Cst only (common VCOM method)
4	Liquid crystal drive output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH-VGL
		VCOM	VCOMH=3.0～(DDVDH-0.5)V VCOML=(VCL+0.5)～0V Amplitude between VCOMH and VCOML=6V (max) Change VCOMH with electronic volume or from VCOMR Change amplitude between VCOMH and VCOML using electronic volume
5	Input voltages	IOVCC (interface voltage)	1.65V ~ 3.3V Power supply to IM3-0, RESETX, DB17-0, RDX, SDI, SDO, WRX/SCL, RS, CSX, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK and LEDPWM. Connect to VCC and VCI on the FPC when the electrical potentials are the same.
		VCC (power supply to for logic regulator)	VCC=2.5V ~ 3.3V Connect to IOVCC and VCI on the FPC when the electrical potentials are the same.
		VCI (LCD drive power supply)	VCI=2.5V ~ 3.3V Connect to IOVCC and VCC on the FPC when the electrical potentials are the same.
6	LCD drive supply voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 18.0V
		VGL	-4.5V ~ -13.0V
		VGH-VGL	Max. 28V
		VCL	-1.9V ~ -3.0V
		VCI-VCL	Max. 6V
7	Internal step-up circuits	DDVDH	VCI1 x 2
		VGH	VCI1 x 5, x 6
		VGL	VCI1 x –3, -4, -5
		VCL	VCI1 x –1

Block Diagram

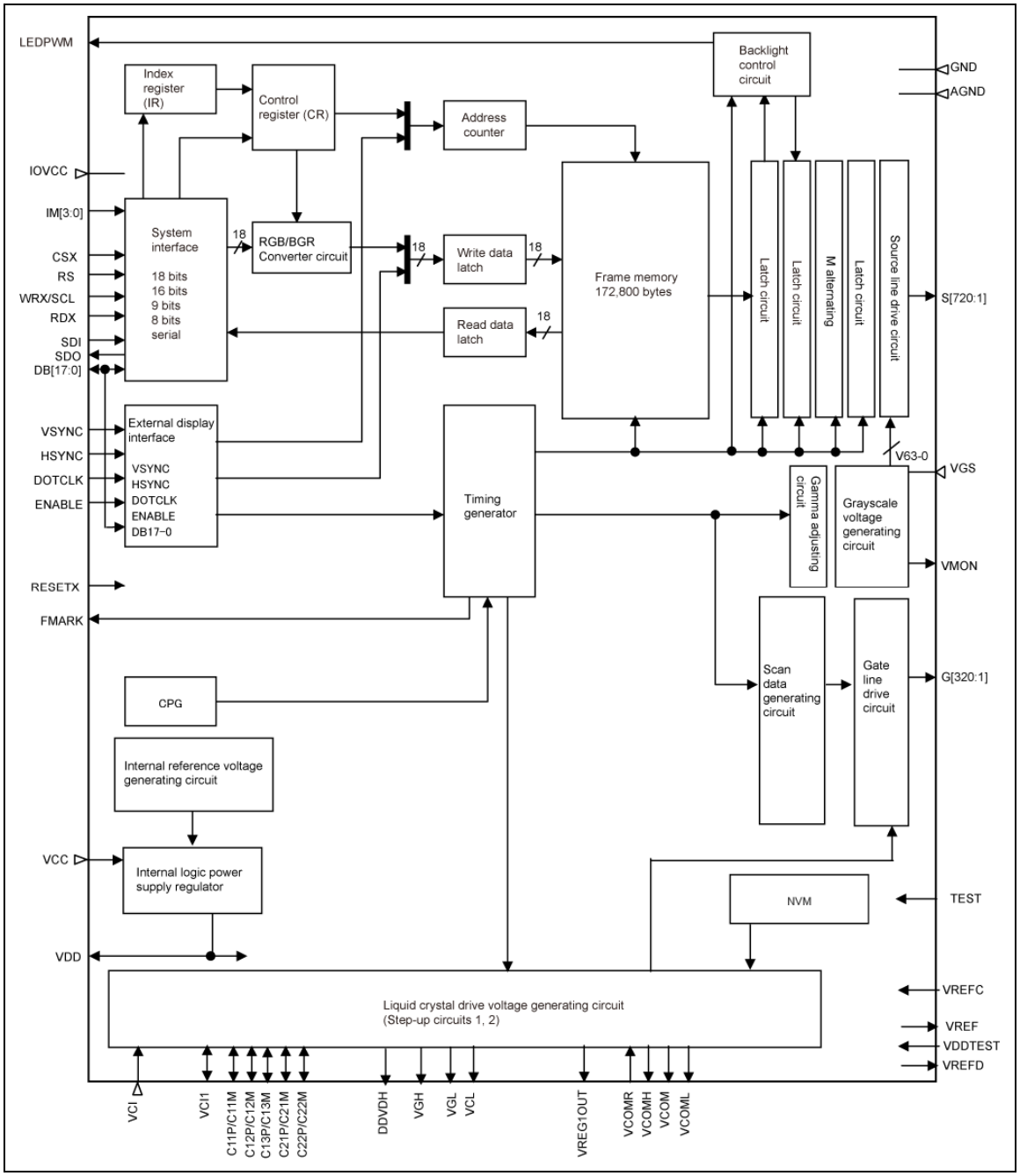


Figure 1

Block Function

1. System Interface

The R61580 supports 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The R61580 has an index register (IR), a 16-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control register and internal frame memory. The WDR is the register to temporarily store data to be written to control register and internal frame memory. The RDR is the register to temporarily store the data read from the frame memory. The data from the host processor to be written to the internal frame memory is first written to the WDR and then automatically written to the internal frame memory by an internal operation. The data is read via RDR from the internal frame memory. Therefore, invalid data is sent to the data bus when the R61580 performs the first read operation from the internal frame memory. Valid data is read out when the R61580 performs the second and subsequent read operation.

The instruction execution time except that of starting oscillation takes 0 clock cycle to allow writing instructions consecutively.

Table 2 Register setting when 8-/, 9-/, 16-/ or 18- parallel interface is selected

80-system bus			Operation
WRX	RDX	RS	
0	1	0	Index is written to IR
1	0	0	Setting inhibited
0	1	1	Control register and frame memory are written via WDR
1	0	1	Frame memory and register are read via RDR

Table 3 Register setting when clock synchronous serial interface is selected

Start byte		Operation
RW bit	RS bit	
0	0	Index is written to IR
1	0	Setting inhibited
0	1	Control register and frame memory are written via WDR
1	1	Frame memory and register are read via RDR

Table 4

IM[3:0]				System interface	DB pin	Frame memory write transfer	Instruction write transfer
3	2	1	0				
0	0	0	0	Setting inhibited	—	—	—
0	0	0	1	Setting inhibited	—	—	—
0	0	1	0	80-system 16 bit interface	DB17-10,8-1	One-transfer (16bit) Two-transfer (1^{st}:2bit, 2^{nd}:16bit) Two-transfer (1^{st}:16bit, 2^{nd}:2bit)	One-transfer (16bit)
0	0	1	1	80-system 8 bit interface	DB17-10	Two-transfer (1^{st}:8bit, 2^{nd}:8bit) Three-transfer (1^{st}:6bit, 2^{nd}:6bit, 3^{rd}:6bit)	Two-transfer (1^{st}: 8bit, 2^{nd}:8bit)
0	1	0	0	Clock synchronous serial interface	— (SDI,SDO)	Two-transfer (1^{st}:8bit, 2^{nd}:8bit)	Two-transfer (1^{st}:8bit, 2^{nd}:8bit)
0	1	0	1	Setting inhibited	—	—	—
0	1	1	0	Setting inhibited	—	—	—
0	1	1	1	Setting inhibited	—	—	—
1	0	0	0	Setting inhibited	—	—	—
1	0	0	1	Setting inhibited	—	—	—
1	0	1	0	80-system 18 bit interface	DB17-0	One-transfer (18bit)	One-transfer (16bit)
1	0	1	1	80-system 9 bit interface	DB17-9	Two-transfer (1^{st}:9bit, 2^{nd}:9bit)	Two-transfer (1^{st}:8bit, 2^{nd}:8bit)
1	1	0	0	Setting inhibited	—	—	—
1	1	0	1	Setting inhibited	—	—	—
1	1	1	0	Setting inhibited	—	—	—
1	1	1	1	Setting inhibited	—	—	—

2. External Display Interface (RGB and VSYNC Interfaces)

The R61580 supports RGB and VSYNC interfaces as external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK.

In RGB interface operation, data (DB17-0) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is

written to the internal frame memory via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal frame memory. For details, see the "VSYNC interface" section.

It is allowed to switch interface by instruction according to the image type, i.e. still and/or moving picture(s) in order to transfer data only when the data is updated and thereby reduce the data transfer and power consumption for moving picture display.

3. Address Counter (AC)

The address counter (AC) gives an address to the internal frame memory. When the index of the register to set a frame memory address in the AC is written to the IR, the address information is sent from the IR to the AC. As the R61580 writes data to the internal frame memory, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only within the rectangular area specified in the frame memory.

4. Frame Memory

Frame memory can store bit-pattern data of 172,800 (240RGB x 320 (dots) x 18(bits)) bytes at maximum, using 18 bits per pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltages according to the grayscale data in the γ-correction registers to enable 262,144-color display.

6. Liquid Crystal Drive Power Supply Circuit

The liquid crystal drive power supply circuit generates DDVDH, VGH, VGL and VCOM levels to drive liquid crystal.

7. Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal frame memory. The timing signal for display operation such as frame memory read operation and the timing signal for internal operation such as frame memory access from the host processor are generated separately in order to avoid mutual interference.

8. Oscillator (OSC)

Internal oscillator generates clock signal used to operate the R61580.

The R61580 generates the internal oscillation clock using internal oscillator. Adjusting the frequency by external resistance is impossible. Adjust the oscillation frequency and line numbers by Frame-Frequency Adjustment Function. During the deep standby mode, internal oscillation halts to reduce power consumption. See "Oscillator" for details.

9. Liquid Crystal Driver Circuit

The liquid crystal driver circuit of the R61580 consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). The display pattern data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

10. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates internal logic power supply VDD.

11. Backlight Control Circuit

Backlight control circuit adjusts backlight brightness according to histogram of the image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

Pin Function

Table 5 Interface Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM3-0</td><td>I</td><td>GND or IOVCC</td><td>Select a mode to interface to host processor. (Amplitude: IOVCC ~ GND)
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode
2. 65,536 colors in two transfer mode</td><td>-</td></tr>
<tr><td>CSX</td><td>I</td><td>Host processor</td><td>Chip selection signal. Amplitude: IOVCC-GND
Low: the R61580 is selected and accessible
High: the R61580 is not selected and not accessible.</td><td>IOVCC</td></tr>
<tr><td>RS</td><td>I</td><td>Host processor</td><td>Register selection signal. Amplitude: IOVCC-GND
Low: Index register is selected
High: Control register is selected</td><td>IOVCC</td></tr>
<tr><td>WRX/SCL</td><td>I</td><td>Host processor</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when WRX is low. Synchronous clock signal (SCL) in serial interface operation. Amplitude: IOVCC-GND</td><td>IOVCC</td></tr>
<tr><td>RDX</td><td>I</td><td>Host processor</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when RDX is low. Amplitude: IOVCC-GND</td><td>IOVCC</td></tr>
<tr><td>SDI</td><td>I</td><td>Host processor</td><td>Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal. Amplitude: IOVCC-GND</td><td>GND or IOVCC</td></tr>
<tr><td>SDO</td><td>O</td><td>Host processor</td><td>Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal.
Amplitude: IOVCC-GND</td><td>Open</td></tr>
</table>

Signal	I/O	Connect to	Function	When not in use
DB0-DB17	I/O	Host processor	18-bit parallel bi-directional data bus for 80-system interface operation. 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation. 16-bit I/F: DB17-DB13 and DB11-1 are used. 18-bit I/F: DB17-DB0 are used.	GND or IOVCC
ENABLE	I	Host processor	Data enable signal for RGB interface operation. (Amplitude: IOVCC-GND). Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit. (Amplitude: IOVCC-GND).	GND or IOVCC
VSYNC	I	Host processor	Frame synchronous signal. Low active. (Amplitude: IOVCC-GND).	GND or IOVCC
HSYNC	I	Host processor	Line synchronous signal. Low active. (Amplitude: IOVCC-GND).	GND or IOVCC
DOTCLK	I	Host processor	Dot clock signal. The data input timing is on the rising edge of DOTCLK. (Amplitude: IOVCC-GND).	GND or IOVCC
FMARK	O	Host processor	Frame head pulse signal, which is used when writing data to the internal frame memory. (Amplitude: IOVCC-GND).	Open

Table 6 LED Driver Control Pin

Signal	I/O	Connect to	Function	When not in use
LEDPWM	O	LED driver	Control signal for brightness of LED backlight. PWM signal's width is selected from 256 values between 0% (Low) and 100% (High). (Amplitude: IOVCC~GND)	Open

Table 7 Reset and Internal Oscillation Pins

Signal	I/O	Connect to	Function	When not in use
RESETX	I	Host processor or external circuit	Reset signal. The R61580 is initialized when this signal is low. Make sure to execute a power-on reset when turning on power supply (Amplitude: IOVCC-GND).	-

Table 8 Power Supply Pins

Signal	I/O	Connect to	Function	When not in use
VCC	-	Power supply	Power supply to internal logic regulator circuit.	-
GND	-	Power supply	Internal logic GND.	-
VDD	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.	-
IOVCC	-	Power supply	Power supply to the interface pins: RESETX, CSX, WRX, RDX, RS, DB17-0, VSYNC, HSYNC, DOTCLK, and ENABLE. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.	-
AGND	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit). In case of COG, connect to GND on the FPC to prevent noise.	-
VCI	I	Power supply	Power supply to the liquid crystal power supply analog circuit.	-

Table 9 Step-up Circuit Pins

Signal	I/O	Connect to	Function	When not in use
VCI1	I/O	Stabilizing capacitor	Reference voltage of step-up circuit 1. Define the voltage so that DDVDH, VGH and VGL do not exceed the ratings.	-
DDVDH	O	Stabilizing capacitor	Power supply for the source driver liquid crystal drive unit and VCOM drive which is generated from VCI1 and output from internal step-up circuit 1. The step-up factor is 2. Make sure to connect to stabilizing capacitor.	-
VGH	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from VCI1 and DDVDH and output from internal step-up circuit 2. The step-up factor is set by BT bit. Make cure to connect to stabilizing capacitor.	-
VGL	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from VCI1 and DDVDH and output from internal step-up circuit 2. The step-up factor is set by BT bit. Make sure to connect to a stabilizing capacitor.	-
VCL	O	Stabilizing capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor.	-
C11P, C11M C12P, C12M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C13P, C13M, C21P, C21M, C22P, C22M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.	-

Table 10 LCD Drive Pins

Signal	I/O	Connect to	Function	When not in use
VREG1OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used as (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Make sure to connect to a stabilizing capacitor when in use.	-
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.	-
VCOMH	O	-	The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or internal electronic volume (VCM1).	-
VCOML	O	-	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits).	-
VCOMR	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.	Open
VGS	I	GND	Reference level for the grayscale voltage generating circuit.	-
S1-S720	O	LCD	Liquid crystal application voltages. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the frame memory address h00000 is output from S1. When SS = 1, the data in the frame memory address h00000 is output from S720.	Open
G1-G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level	Open

Table 11 Others (Test and Dummy Pins)

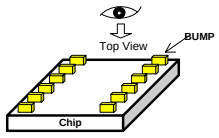
Signal	I/O	Connect to	Function	When not in use
VREFC	I	GND	Test pin. Make sure to fix to the GND level or leave open.	-
VREFD	O	Open	Test pin. Leave open.	Open
VREF	O	Open	Test pin. Leave open.	Open
VDDTEST	I	GND	Test pin. Make sure to fix to the GND level or leave open.	-
VMON	O	Open	Test pin. Leave open.	Open
VCIR	O	Open	Test pin. Leave open.	Open
IOGNDDUM AGNDDUM*	O	-	Connect unused interface and test pins to fix voltage levels on the glass. Leave open when not used.	Open
TEST	I	GND	Test pin. Connect to GND or leave open.	-
VPP1	I	GND	Test pin. Connect to GND or leave open.	-

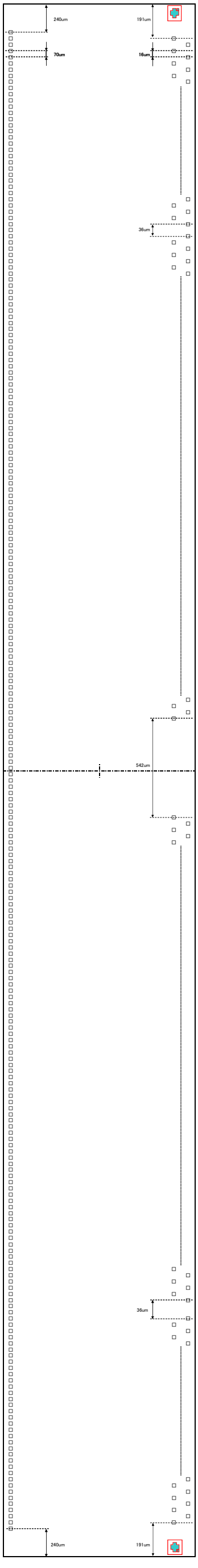
Patents of dummy pins used to fix pin to VCC or GND are granted as below:

PATENT ISSUED: Japanese Patent No. 3,980,066
United States Patent No. 6,323,930
Korean Patent No. 401,270
Taiwan Patent No. 175,413
Japanese Patent No. 4,226,627
United States Patent No. 6,924,868

R61580 PAD Arrangement Rev.1.00 2009.03.31

Rev	Date	Change History
1.00	2009/3/31	





No	Pin Name
1	AGNDDUM1
2	AGNDDUM2
3	IOGNDDUM
4	AGNDDUM3
5	AGNDDUM4
6	AGNDDUM5
7	IM0/ID
8	IM1
9	IM2
10	IM3
11	TEST
12	AGNDDUM6
13	AGNDDUM7
14	AGNDDUM8
15	AGNDDUM9
16	AGNDDUM10
17	AGNDDUM11
18	AGNDDUM12
19	RESETX
20	RESETX
21	VSYNC
22	HSYNC
23	DOTCLK
24	DE
25	DB17
26	DB16
27	DB15
28	DB14
29	DB13
30	AGNDDUM13
31	DB12
32	DB11
33	DB10
34	DB9
35	DB8
36	AGNDDUM14
37	AGNDDUM15
38	DB7
39	DB6
40	DB5
41	DB4
42	DB3
43	DB2
44	DB1
45	DB0
46	AGNDDUM16
47	SDO
48	SDI
49	RDX
50	WRX/SCL
51	RS
52	CSX
53	AGNDDUM17
54	AGNDDUM18
55	FMARK
56	AGNDDUM19
57	AGNDDUM20
58	AGNDDUM21
59	AGNDDUM22
60	AGNDDUM23
61	AGNDDUM24
62	VREF
63	VREFD
64	VREFC
65	VDDTEST
66	AGNDDUM25
67	IOVCC
68	IOVCC
69	IOVCC
70	IOVCC
71	IOVCC
72	IOVCC
73	VDD
74	VDD
75	VDD
76	VDD
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78	VDD
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123	VCOML
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134	VCL
135	VCL
136	DDVDH
137	DDVDH
138	DDVDH
139	DDVDH
140	DDVDH
141	DDVDH
142	VCI1
143	VCI1
144	VCI1
145	VCI
146	VCI
147	VCI
148	VCI
149	VCI
150	VCI
151	VCI
152	VCI
153	VCI
154	VCI
155	VCI
156	VCI
157	VCC
158	VCC
159	VCC
160	VCC
161	VCC
162	VCC
163	LEDPWM
164	LEDPWM
165	C12M
166	C12M
167	C12M
168	C12M
169	C12M
170	C12P
171	C12P
172	C12P
173	C12P
174	C12P
175	C11M
176	C11M
177	C11M
178	C11M
179	C11M
180	C11P
181	C11P
182	C11P
183	C11P
184	C11P
185	VGL
186	VGL
187	VGL
188	VGL
189	VGL
190	VGL
191	VGL
192	VGL
193	VGL
194	VGL
195	AGND
196	AGND
197	AGND
198	VGH
199	VGH
200	VGH
201	VGH
202	VGH
203	VGH
204	AGNDDUM27
205	AGNDDUM28
206	C13M
207	C13M
208	C13M
209	C13M
210	C13P
211	C13P
212	C13P
213	C13P
214	C21M
215	C21M
216	C21M
217	C21M
218	C21M
219	C21M
220	C21M
221	C21P
222	C21P
223	C21P
224	C21P
225	C21P
226	C21P
227	C21P
228	C22M
229	C22M
230	C22M
231	C22M
232	C22M
233	C22M
234	C22M
235	C22P
236	C22P
237	C22P
238	C22P
239	C22P
240	C22P
241	C22P
242	AGNDDUM29
243	AGNDDUM30

Pin Name	No
TESTO8	1291
G<319>	1290
G<317>	1289
G<315>	1288
G<313>	1287
G<311>	1286
G<309>	1285
G<307>	1284
G<7>	1134
G<5>	1133
G<3>	1132
G<1>	1131
TESTO7	1130
TESTO6	1129
S<1>	1128
S<2>	1127
S<3>	1126
S<4>	1125
S<5>	1124
S<358>	771
S<359>	770
S<360>	769
TESTO5	768
TESTO4	767
S<361>	766
S<362>	765
S<363>	764
S<364>	763
S<716>	411
S<717>	410
S<718>	409
S<719>	408
S<720>	407
TESTO3	406
TESTO2	405
G<2>	404
G<4>	403
G<6>	402
G<8>	401
G<308>	251
G<310>	250
G<312>	249
G<314>	248
G<316>	247
G<318>	246
G<320>	245
TESTO1	244

●Chip size: 17.70mm x 0.67mm

●Chip thickness: 280μm (typ.)

●Pad coordinates: Pad center

●Pad coordinates: Chip center

●Au bump size:

1. 50μm x 50μm (I/O)
2. 16μm x 90μm (Output to liquid crystal)

●Au bump pitch: See “Bump Arrangement”

●Au bump height: 12 μm

Table 12 Alignment Mark

Alignment Mark shape	X	Y
(1-a)	-8751.00	194.50
(1-b)	8751.00	194.50

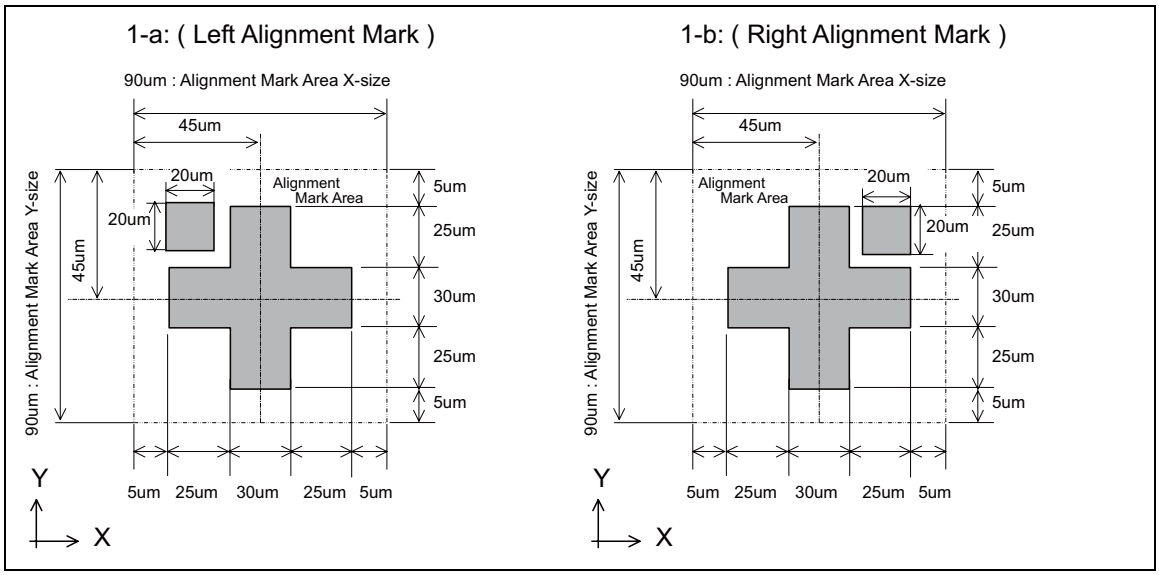


Figure 2 Alignment Mark

R61580 Pad Coordinate(No.1)

(unit: μm)

Pad No.	Pin Name	X	Y
1	DUMMY1	-8610	-241.2
2	DUMMY2	-8540	-241.2
3	IOGNDDUM	-8470	-241.2
4	DUMMY3	-8400	-241.2
5	DUMMY4	-8330	-241.2
6	DUMMY5	-8260	-241.2
7	IM0/ID	-8190	-241.2
8	IM1	-8120	-241.2
9	IM2	-8050	-241.2
10	IM3	-7980	-241.2
11	TEST	-7910	-241.2
12	DUMMY6	-7840	-241.2
13	DUMMY7	-7770	-241.2
14	DUMMY8	-7700	-241.2
15	DUMMY9	-7630	-241.2
16	DUMMY10	-7560	-241.2
17	DUMMY11	-7490	-241.2
18	DUMMY12	-7420	-241.2
19	RESETX	-7350	-241.2
20	RESETX	-7280	-241.2
21	VSYNC	-7210	-241.2
22	HSYNC	-7140	-241.2
23	DOTCLK	-7070	-241.2
24	DE	-7000	-241.2
25	DB17	-6905	-241.2
26	DB16	-6825	-241.2
27	DB15	-6745	-241.2
28	DB14	-6665	-241.2
29	DB13	-6585	-241.2
30	DUMMY13	-6495	-241.2
31	DB12	-6405	-241.2
32	DB11	-6325	-241.2
33	DB10	-6245	-241.2
34	DB9	-6165	-241.2
35	DB8	-6085	-241.2
36	DUMMY14	-5990	-241.2
37	DUMMY15	-5920	-241.2
38	DB7	-5825	-241.2
39	DB6	-5745	-241.2
40	DB5	-5665	-241.2
41	DB4	-5585	-241.2
42	DB3	-5505	-241.2
43	DB2	-5425	-241.2
44	DB1	-5345	-241.2
45	DB0	-5265	-241.2
46	DUMMY16	-5180	-241.2
47	SDO	-5110	-241.2
48	SDI	-5040	-241.2
49	RDX	-4970	-241.2
50	WRX/SCL	-4900	-241.2
51	RS	-4830	-241.2
52	CSX	-4760	-241.2
53	DUMMY17	-4690	-241.2
54	DUMMY18	-4620	-241.2
55	FMARK	-4550	-241.2
56	DUMMY19	-4480	-241.2
57	DUMMY20	-4410	-241.2
58	DUMMY21	-4340	-241.2
59	DUMMY22	-4270	-241.2
60	DUMMY23	-4200	-241.2
61	DUMMY24	-4130	-241.2
62	VREF	-4060	-241.2
63	VREFD	-3990	-241.2
64	VREFC	-3920	-241.2
65	VDDTEST	-3850	-241.2
66	DUMMY25	-3780	-241.2
67	IOVCC	-3710	-241.2
68	IOVCC	-3640	-241.2
69	IOVCC	-3570	-241.2
70	IOVCC	-3500	-241.2
71	IOVCC	-3430	-241.2
72	IOVCC	-3360	-241.2
73	VDD	-3290	-241.2
74	VDD	-3220	-241.2
75	VDD	-3150	-241.2
76	VDD	-3080	-241.2
77	VDD	-3010	-241.2
78	VDD	-2940	-241.2
79	VDD	-2870	-241.2
80	VDD	-2800	-241.2
81	VDD	-2730	-241.2
82	VDD	-2660	-241.2
83	VDD	-2590	-241.2
84	DUMMY26	-2520	-241.2
85	GND	-2450	-241.2
86	GND	-2380	-241.2
87	GND	-2310	-241.2
88	GND	-2240	-241.2
89	GND	-2170	-241.2
90	GND	-2100	-241.2
91	GND	-2030	-241.2
92	GND	-1960	-241.2
93	VGS	-1890	-241.2
94	VGS	-1820	-241.2
95	AGND	-1750	-241.2
96	AGND	-1680	-241.2
97	AGND	-1610	-241.2
98	AGND	-1540	-241.2
99	AGND	-1470	-241.2
100	AGND	-1400	-241.2

R61580 Pad Coordinate(No.2)

(unit: μm)

Pad No.	Pin Name	X	Y
101	AGND	−1330	−241.2
102	AGND	−1260	−241.2
103	AGND	−1190	−241.2
104	AGND	−1120	−241.2
105	VCIR	−1050	−241.2
106	VCOMR	−980	−241.2
107	VMON	−910	−241.2
108	VCOM	−840	−241.2
109	VCOM	−770	−241.2
110	VCOM	−700	−241.2
111	VCOM	−630	−241.2
112	VCOM	−560	−241.2
113	VCOM	−490	−241.2
114	VCOM	−420	−241.2
115	VCOMH	−350	−241.2
116	VCOMH	−280	−241.2
117	VCOMH	−210	−241.2
118	VCOMH	−140	−241.2
119	VCOMH	−70	−241.2
120	VCOMH	0	−241.2
121	VCOML	70	−241.2
122	VCOML	140	−241.2
123	VCOML	210	−241.2
124	VCOML	280	−241.2
125	VREG1OUT	350	−241.2
126	VREG1OUT	420	−241.2
127	VREG1OUT	490	−241.2
128	VPP1	560	−241.2
129	VPP1	630	−241.2
130	VPP1	700	−241.2
131	VCL	770	−241.2
132	VCL	840	−241.2
133	VCL	910	−241.2
134	VCL	980	−241.2
135	VCL	1050	−241.2
136	DDVDH	1120	−241.2
137	DDVDH	1190	−241.2
138	DDVDH	1260	−241.2
139	DDVDH	1330	−241.2
140	DDVDH	1400	−241.2
141	DDVDH	1470	−241.2
142	VCI1	1540	−241.2
143	VCI1	1610	−241.2
144	VCI1	1680	−241.2
145	VCI	1750	−241.2
146	VCI	1820	−241.2
147	VCI	1890	−241.2
148	VCI	1960	−241.2
149	VCI	2030	−241.2
150	VCI	2100	−241.2

Pad No.	Pin Name	X	Y
151	VCI	2170	−241.2
152	VCI	2240	−241.2
153	VCI	2310	−241.2
154	VCI	2380	−241.2
155	VCI	2450	−241.2
156	VCI	2520	−241.2
157	VCC	2590	−241.2
158	VCC	2660	−241.2
159	VCC	2730	−241.2
160	VCC	2800	−241.2
161	VCC	2870	−241.2
162	VCC	2940	−241.2
163	LEDPWM	3010	−241.2
164	LEDPWM	3080	−241.2
165	C12M	3150	−241.2
166	C12M	3220	−241.2
167	C12M	3290	−241.2
168	C12M	3360	−241.2
169	C12M	3430	−241.2
170	C12P	3500	−241.2
171	C12P	3570	−241.2
172	C12P	3640	−241.2
173	C12P	3710	−241.2
174	C12P	3780	−241.2
175	C11M	3850	−241.2
176	C11M	3920	−241.2
177	C11M	3990	−241.2
178	C11M	4060	−241.2
179	C11M	4130	−241.2
180	C11P	4200	−241.2
181	C11P	4270	−241.2
182	C11P	4340	−241.2
183	C11P	4410	−241.2
184	C11P	4480	−241.2
185	VGL	4550	−241.2
186	VGL	4620	−241.2
187	VGL	4690	−241.2
188	VGL	4760	−241.2
189	VGL	4830	−241.2
190	VGL	4900	−241.2
191	VGL	4970	−241.2
192	VGL	5040	−241.2
193	VGL	5110	−241.2
194	VGL	5180	−241.2
195	AGND	5250	−241.2
196	AGND	5320	−241.2
197	AGND	5390	−241.2
198	VGH	5460	−241.2
199	VGH	5530	−241.2
200	VGH	5600	−241.2

R61580 Pad Coordinate(No.3)

(unit: μm)

Pad No.	Pin Name	X	Y
201	VGH	5670	-241.2
202	VGH	5740	-241.2
203	VGH	5810	-241.2
204	DUMMY27	5880	-241.2
205	DUMMY28	5950	-241.2
206	C13M	6020	-241.2
207	C13M	6090	-241.2
208	C13M	6160	-241.2
209	C13M	6230	-241.2
210	C13P	6300	-241.2
211	C13P	6370	-241.2
212	C13P	6440	-241.2
213	C13P	6510	-241.2
214	C21M	6580	-241.2
215	C21M	6650	-241.2
216	C21M	6720	-241.2
217	C21M	6790	-241.2
218	C21M	6860	-241.2
219	C21M	6930	-241.2
220	C21M	7000	-241.2
221	C21P	7070	-241.2
222	C21P	7140	-241.2
223	C21P	7210	-241.2
224	C21P	7280	-241.2
225	C21P	7350	-241.2
226	C21P	7420	-241.2
227	C21P	7490	-241.2
228	C22M	7560	-241.2
229	C22M	7630	-241.2
230	C22M	7700	-241.2
231	C22M	7770	-241.2
232	C22M	7840	-241.2
233	C22M	7910	-241.2
234	C22M	7980	-241.2
235	C22P	8050	-241.2
236	C22P	8120	-241.2
237	C22P	8190	-241.2
238	C22P	8260	-241.2
239	C22P	8330	-241.2
240	C22P	8400	-241.2
241	C22P	8470	-241.2
242	DUMMY29	8540	-241.2
243	DUMMY30	8610	-241.2
244	TESTO1	8659	132
245	G<320>	8643	241
246	G<318>	8627	132
247	G<316>	8611	241
248	G<314>	8595	132
249	G<312>	8579	241
250	G<310>	8563	132

Pad No.	Pin Name	X	Y
251	G<308>	8547	241
252	G<306>	8531	132
253	G<304>	8515	241
254	G<302>	8499	132
255	G<300>	8483	241
256	G<298>	8467	132
257	G<296>	8451	241
258	G<294>	8435	132
259	G<292>	8419	241
260	G<290>	8403	132
261	G<288>	8387	241
262	G<286>	8371	132
263	G<284>	8355	241
264	G<282>	8339	132
265	G<280>	8323	241
266	G<278>	8307	132
267	G<276>	8291	241
268	G<274>	8275	132
269	G<272>	8259	241
270	G<270>	8243	132
271	G<268>	8227	241
272	G<266>	8211	132
273	G<264>	8195	241
274	G<262>	8179	132
275	G<260>	8163	241
276	G<258>	8147	132
277	G<256>	8131	241
278	G<254>	8115	132
279	G<252>	8099	241
280	G<250>	8083	132
281	G<248>	8067	241
282	G<246>	8051	132
283	G<244>	8035	241
284	G<242>	8019	132
285	G<240>	8003	241
286	G<238>	7987	132
287	G<236>	7971	241
288	G<234>	7955	132
289	G<232>	7939	241
290	G<230>	7923	132
291	G<228>	7907	241
292	G<226>	7891	132
293	G<224>	7875	241
294	G<222>	7859	132
295	G<220>	7843	241
296	G<218>	7827	132
297	G<216>	7811	241
298	G<214>	7795	132
299	G<212>	7779	241
300	G<210>	7763	132

R61580 Pad Coordinate(No.4)

(unit: μm)

Pad No.	Pin Name	X	Y
301	G<208>	7747	241
302	G<206>	7731	132
303	G<204>	7715	241
304	G<202>	7699	132
305	G<200>	7683	241
306	G<198>	7667	132
307	G<196>	7651	241
308	G<194>	7635	132
309	G<192>	7619	241
310	G<190>	7603	132
311	G<188>	7587	241
312	G<186>	7571	132
313	G<184>	7555	241
314	G<182>	7539	132
315	G<180>	7523	241
316	G<178>	7507	132
317	G<176>	7491	241
318	G<174>	7475	132
319	G<172>	7459	241
320	G<170>	7443	132
321	G<168>	7427	241
322	G<166>	7411	132
323	G<164>	7395	241
324	G<162>	7379	132
325	G<160>	7363	241
326	G<158>	7347	132
327	G<156>	7331	241
328	G<154>	7315	132
329	G<152>	7299	241
330	G<150>	7283	132
331	G<148>	7267	241
332	G<146>	7251	132
333	G<144>	7235	241
334	G<142>	7219	132
335	G<140>	7203	241
336	G<138>	7187	132
337	G<136>	7171	241
338	G<134>	7155	132
339	G<132>	7139	241
340	G<130>	7123	132
341	G<128>	7107	241
342	G<126>	7091	132
343	G<124>	7075	241
344	G<122>	7059	132
345	G<120>	7043	241
346	G<118>	7027	132
347	G<116>	7011	241
348	G<114>	6995	132
349	G<112>	6979	241
350	G<110>	6963	132
351	G<108>	6947	241
352	G<106>	6931	132
353	G<104>	6915	241
354	G<102>	6899	132
355	G<100>	6883	241
356	G<98>	6867	132
357	G<96>	6851	241
358	G<94>	6835	132
359	G<92>	6819	241
360	G<90>	6803	132
361	G<88>	6787	241
362	G<86>	6771	132
363	G<84>	6755	241
364	G<82>	6739	132
365	G<80>	6723	241
366	G<78>	6707	132
367	G<76>	6691	241
368	G<74>	6675	132
369	G<72>	6659	241
370	G<70>	6643	132
371	G<68>	6627	241
372	G<66>	6611	132
373	G<64>	6595	241
374	G<62>	6579	132
375	G<60>	6563	241
376	G<58>	6547	132
377	G<56>	6531	241
378	G<54>	6515	132
379	G<52>	6499	241
380	G<50>	6483	132
381	G<48>	6467	241
382	G<46>	6451	132
383	G<44>	6435	241
384	G<42>	6419	132
385	G<40>	6403	241
386	G<38>	6387	132
387	G<36>	6371	241
388	G<34>	6355	132
389	G<32>	6339	241
390	G<30>	6323	132
391	G<28>	6307	241
392	G<26>	6291	132
393	G<24>	6275	241
394	G<22>	6259	132
395	G<20>	6243	241
396	G<18>	6227	132
397	G<16>	6211	241
398	G<14>	6195	132
399	G<12>	6179	241
400	G<10>	6163	132

R61580 Pad Coordinate(No.5)

(unit: μm)

Pad No.	Pin Name	X	Y
401	G<8>	6147	241
402	G<6>	6131	132
403	G<4>	6115	241
404	G<2>	6099	132
405	TESTO2	6083	241
406	TESTO3	6047	241
407	S<720>	6031	132
408	S<719>	6015	241
409	S<718>	5999	132
410	S<717>	5983	241
411	S<716>	5967	132
412	S<715>	5951	241
413	S<714>	5935	132
414	S<713>	5919	241
415	S<712>	5903	132
416	S<711>	5887	241
417	S<710>	5871	132
418	S<709>	5855	241
419	S<708>	5839	132
420	S<707>	5823	241
421	S<706>	5807	132
422	S<705>	5791	241
423	S<704>	5775	132
424	S<703>	5759	241
425	S<702>	5743	132
426	S<701>	5727	241
427	S<700>	5711	132
428	S<699>	5695	241
429	S<698>	5679	132
430	S<697>	5663	241
431	S<696>	5647	132
432	S<695>	5631	241
433	S<694>	5615	132
434	S<693>	5599	241
435	S<692>	5583	132
436	S<691>	5567	241
437	S<690>	5551	132
438	S<689>	5535	241
439	S<688>	5519	132
440	S<687>	5503	241
441	S<686>	5487	132
442	S<685>	5471	241
443	S<684>	5455	132
444	S<683>	5439	241
445	S<682>	5423	132
446	S<681>	5407	241
447	S<680>	5391	132
448	S<679>	5375	241
449	S<678>	5359	132
450	S<677>	5343	241

Pad No.	Pin Name	X	Y
451	S<676>	5327	132
452	S<675>	5311	241
453	S<674>	5295	132
454	S<673>	5279	241
455	S<672>	5263	132
456	S<671>	5247	241
457	S<670>	5231	132
458	S<669>	5215	241
459	S<668>	5199	132
460	S<667>	5183	241
461	S<666>	5167	132
462	S<665>	5151	241
463	S<664>	5135	132
464	S<663>	5119	241
465	S<662>	5103	132
466	S<661>	5087	241
467	S<660>	5071	132
468	S<659>	5055	241
469	S<658>	5039	132
470	S<657>	5023	241
471	S<656>	5007	132
472	S<655>	4991	241
473	S<654>	4975	132
474	S<653>	4959	241
475	S<652>	4943	132
476	S<651>	4927	241
477	S<650>	4911	132
478	S<649>	4895	241
479	S<648>	4879	132
480	S<647>	4863	241
481	S<646>	4847	132
482	S<645>	4831	241
483	S<644>	4815	132
484	S<643>	4799	241
485	S<642>	4783	132
486	S<641>	4767	241
487	S<640>	4751	132
488	S<639>	4735	241
489	S<638>	4719	132
490	S<637>	4703	241
491	S<636>	4687	132
492	S<635>	4671	241
493	S<634>	4655	132
494	S<633>	4639	241
495	S<632>	4623	132
496	S<631>	4607	241
497	S<630>	4591	132
498	S<629>	4575	241
499	S<628>	4559	132
500	S<627>	4543	241

R61580 Pad Coordinate(No.6)

(unit: μm)

Pad No.	Pin Name	X	Y
501	S<626>	4527	132
502	S<625>	4511	241
503	S<624>	4495	132
504	S<623>	4479	241
505	S<622>	4463	132
506	S<621>	4447	241
507	S<620>	4431	132
508	S<619>	4415	241
509	S<618>	4399	132
510	S<617>	4383	241
511	S<616>	4367	132
512	S<615>	4351	241
513	S<614>	4335	132
514	S<613>	4319	241
515	S<612>	4303	132
516	S<611>	4287	241
517	S<610>	4271	132
518	S<609>	4255	241
519	S<608>	4239	132
520	S<607>	4223	241
521	S<606>	4207	132
522	S<605>	4191	241
523	S<604>	4175	132
524	S<603>	4159	241
525	S<602>	4143	132
526	S<601>	4127	241
527	S<600>	4111	132
528	S<599>	4095	241
529	S<598>	4079	132
530	S<597>	4063	241
531	S<596>	4047	132
532	S<595>	4031	241
533	S<594>	4015	132
534	S<593>	3999	241
535	S<592>	3983	132
536	S<591>	3967	241
537	S<590>	3951	132
538	S<589>	3935	241
539	S<588>	3919	132
540	S<587>	3903	241
541	S<586>	3887	132
542	S<585>	3871	241
543	S<584>	3855	132
544	S<583>	3839	241
545	S<582>	3823	132
546	S<581>	3807	241
547	S<580>	3791	132
548	S<579>	3775	241
549	S<578>	3759	132
550	S<577>	3743	241

Pad No.	Pin Name	X	Y
551	S<576>	3727	132
552	S<575>	3711	241
553	S<574>	3695	132
554	S<573>	3679	241
555	S<572>	3663	132
556	S<571>	3647	241
557	S<570>	3631	132
558	S<569>	3615	241
559	S<568>	3599	132
560	S<567>	3583	241
561	S<566>	3567	132
562	S<565>	3551	241
563	S<564>	3535	132
564	S<563>	3519	241
565	S<562>	3503	132
566	S<561>	3487	241
567	S<560>	3471	132
568	S<559>	3455	241
569	S<558>	3439	132
570	S<557>	3423	241
571	S<556>	3407	132
572	S<555>	3391	241
573	S<554>	3375	132
574	S<553>	3359	241
575	S<552>	3343	132
576	S<551>	3327	241
577	S<550>	3311	132
578	S<549>	3295	241
579	S<548>	3279	132
580	S<547>	3263	241
581	S<546>	3247	132
582	S<545>	3231	241
583	S<544>	3215	132
584	S<543>	3199	241
585	S<542>	3183	132
586	S<541>	3167	241
587	S<540>	3151	132
588	S<539>	3135	241
589	S<538>	3119	132
590	S<537>	3103	241
591	S<536>	3087	132
592	S<535>	3071	241
593	S<534>	3055	132
594	S<533>	3039	241
595	S<532>	3023	132
596	S<531>	3007	241
597	S<530>	2991	132
598	S<529>	2975	241
599	S<528>	2959	132
600	S<527>	2943	241

R61580 Pad Coordinate(No.7)

(unit: μm)

Pad No.	Pin Name	X	Y
601	S<526>	2927	132
602	S<525>	2911	241
603	S<524>	2895	132
604	S<523>	2879	241
605	S<522>	2863	132
606	S<521>	2847	241
607	S<520>	2831	132
608	S<519>	2815	241
609	S<518>	2799	132
610	S<517>	2783	241
611	S<516>	2767	132
612	S<515>	2751	241
613	S<514>	2735	132
614	S<513>	2719	241
615	S<512>	2703	132
616	S<511>	2687	241
617	S<510>	2671	132
618	S<509>	2655	241
619	S<508>	2639	132
620	S<507>	2623	241
621	S<506>	2607	132
622	S<505>	2591	241
623	S<504>	2575	132
624	S<503>	2559	241
625	S<502>	2543	132
626	S<501>	2527	241
627	S<500>	2511	132
628	S<499>	2495	241
629	S<498>	2479	132
630	S<497>	2463	241
631	S<496>	2447	132
632	S<495>	2431	241
633	S<494>	2415	132
634	S<493>	2399	241
635	S<492>	2383	132
636	S<491>	2367	241
637	S<490>	2351	132
638	S<489>	2335	241
639	S<488>	2319	132
640	S<487>	2303	241
641	S<486>	2287	132
642	S<485>	2271	241
643	S<484>	2255	132
644	S<483>	2239	241
645	S<482>	2223	132
646	S<481>	2207	241
647	S<480>	2191	132
648	S<479>	2175	241
649	S<478>	2159	132
650	S<477>	2143	241

Pad No.	Pin Name	X	Y
651	S<476>	2127	132
652	S<475>	2111	241
653	S<474>	2095	132
654	S<473>	2079	241
655	S<472>	2063	132
656	S<471>	2047	241
657	S<470>	2031	132
658	S<469>	2015	241
659	S<468>	1999	132
660	S<467>	1983	241
661	S<466>	1967	132
662	S<465>	1951	241
663	S<464>	1935	132
664	S<463>	1919	241
665	S<462>	1903	132
666	S<461>	1887	241
667	S<460>	1871	132
668	S<459>	1855	241
669	S<458>	1839	132
670	S<457>	1823	241
671	S<456>	1807	132
672	S<455>	1791	241
673	S<454>	1775	132
674	S<453>	1759	241
675	S<452>	1743	132
676	S<451>	1727	241
677	S<450>	1711	132
678	S<449>	1695	241
679	S<448>	1679	132
680	S<447>	1663	241
681	S<446>	1647	132
682	S<445>	1631	241
683	S<444>	1615	132
684	S<443>	1599	241
685	S<442>	1583	132
686	S<441>	1567	241
687	S<440>	1551	132
688	S<439>	1535	241
689	S<438>	1519	132
690	S<437>	1503	241
691	S<436>	1487	132
692	S<435>	1471	241
693	S<434>	1455	132
694	S<433>	1439	241
695	S<432>	1423	132
696	S<431>	1407	241
697	S<430>	1391	132
698	S<429>	1375	241
699	S<428>	1359	132
700	S<427>	1343	241

R61580 Pad Coordinate(No.8)

(unit: μm)

Pad No.	Pin Name	X	Y
701	S<426>	1327	132
702	S<425>	1311	241
703	S<424>	1295	132
704	S<423>	1279	241
705	S<422>	1263	132
706	S<421>	1247	241
707	S<420>	1231	132
708	S<419>	1215	241
709	S<418>	1199	132
710	S<417>	1183	241
711	S<416>	1167	132
712	S<415>	1151	241
713	S<414>	1135	132
714	S<413>	1119	241
715	S<412>	1103	132
716	S<411>	1087	241
717	S<410>	1071	132
718	S<409>	1055	241
719	S<408>	1039	132
720	S<407>	1023	241
721	S<406>	1007	132
722	S<405>	991	241
723	S<404>	975	132
724	S<403>	959	241
725	S<402>	943	132
726	S<401>	927	241
727	S<400>	911	132
728	S<399>	895	241
729	S<398>	879	132
730	S<397>	863	241
731	S<396>	847	132
732	S<395>	831	241
733	S<394>	815	132
734	S<393>	799	241
735	S<392>	783	132
736	S<391>	767	241
737	S<390>	751	132
738	S<389>	735	241
739	S<388>	719	132
740	S<387>	703	241
741	S<386>	687	132
742	S<385>	671	241
743	S<384>	655	132
744	S<383>	639	241
745	S<382>	623	132
746	S<381>	607	241
747	S<380>	591	132
748	S<379>	575	241
749	S<378>	559	132
750	S<377>	543	241

Pad No.	Pin Name	X	Y
751	S<376>	527	132
752	S<375>	511	241
753	S<374>	495	132
754	S<373>	479	241
755	S<372>	463	132
756	S<371>	447	241
757	S<370>	431	132
758	S<369>	415	241
759	S<368>	399	132
760	S<367>	383	241
761	S<366>	367	132
762	S<365>	351	241
763	S<364>	335	132
764	S<363>	319	241
765	S<362>	303	132
766	S<361>	287	241
767	TESTO4	271	132
768	TESTO5	-271	132
769	S<360>	-287	241
770	S<359>	-303	132
771	S<358>	-319	241
772	S<357>	-335	132
773	S<356>	-351	241
774	S<355>	-367	132
775	S<354>	-383	241
776	S<353>	-399	132
777	S<352>	-415	241
778	S<351>	-431	132
779	S<350>	-447	241
780	S<349>	-463	132
781	S<348>	-479	241
782	S<347>	-495	132
783	S<346>	-511	241
784	S<345>	-527	132
785	S<344>	-543	241
786	S<343>	-559	132
787	S<342>	-575	241
788	S<341>	-591	132
789	S<340>	-607	241
790	S<339>	-623	132
791	S<338>	-639	241
792	S<337>	-655	132
793	S<336>	-671	241
794	S<335>	-687	132
795	S<334>	-703	241
796	S<333>	-719	132
797	S<332>	-735	241
798	S<331>	-751	132
799	S<330>	-767	241
800	S<329>	-783	132

R61580 Pad Coordinate(No.9)

(unit: μm)

Pad No.	Pin Name	X	Y
801	S<328>	-799	241
802	S<327>	-815	132
803	S<326>	-831	241
804	S<325>	-847	132
805	S<324>	-863	241
806	S<323>	-879	132
807	S<322>	-895	241
808	S<321>	-911	132
809	S<320>	-927	241
810	S<319>	-943	132
811	S<318>	-959	241
812	S<317>	-975	132
813	S<316>	-991	241
814	S<315>	-1007	132
815	S<314>	-1023	241
816	S<313>	-1039	132
817	S<312>	-1055	241
818	S<311>	-1071	132
819	S<310>	-1087	241
820	S<309>	-1103	132
821	S<308>	-1119	241
822	S<307>	-1135	132
823	S<306>	-1151	241
824	S<305>	-1167	132
825	S<304>	-1183	241
826	S<303>	-1199	132
827	S<302>	-1215	241
828	S<301>	-1231	132
829	S<300>	-1247	241
830	S<299>	-1263	132
831	S<298>	-1279	241
832	S<297>	-1295	132
833	S<296>	-1311	241
834	S<295>	-1327	132
835	S<294>	-1343	241
836	S<293>	-1359	132
837	S<292>	-1375	241
838	S<291>	-1391	132
839	S<290>	-1407	241
840	S<289>	-1423	132
841	S<288>	-1439	241
842	S<287>	-1455	132
843	S<286>	-1471	241
844	S<285>	-1487	132
845	S<284>	-1503	241
846	S<283>	-1519	132
847	S<282>	-1535	241
848	S<281>	-1551	132
849	S<280>	-1567	241
850	S<279>	-1583	132
851	S<278>	-1599	241
852	S<277>	-1615	132
853	S<276>	-1631	241
854	S<275>	-1647	132
855	S<274>	-1663	241
856	S<273>	-1679	132
857	S<272>	-1695	241
858	S<271>	-1711	132
859	S<270>	-1727	241
860	S<269>	-1743	132
861	S<268>	-1759	241
862	S<267>	-1775	132
863	S<266>	-1791	241
864	S<265>	-1807	132
865	S<264>	-1823	241
866	S<263>	-1839	132
867	S<262>	-1855	241
868	S<261>	-1871	132
869	S<260>	-1887	241
870	S<259>	-1903	132
871	S<258>	-1919	241
872	S<257>	-1935	132
873	S<256>	-1951	241
874	S<255>	-1967	132
875	S<254>	-1983	241
876	S<253>	-1999	132
877	S<252>	-2015	241
878	S<251>	-2031	132
879	S<250>	-2047	241
880	S<249>	-2063	132
881	S<248>	-2079	241
882	S<247>	-2095	132
883	S<246>	-2111	241
884	S<245>	-2127	132
885	S<244>	-2143	241
886	S<243>	-2159	132
887	S<242>	-2175	241
888	S<241>	-2191	132
889	S<240>	-2207	241
890	S<239>	-2223	132
891	S<238>	-2239	241
892	S<237>	-2255	132
893	S<236>	-2271	241
894	S<235>	-2287	132
895	S<234>	-2303	241
896	S<233>	-2319	132
897	S<232>	-2335	241
898	S<231>	-2351	132
899	S<230>	-2367	241
900	S<229>	-2383	132

R61580 Pad Coordinate(No.10)

(unit: μm)

Pad No.	Pin Name	X	Y
901	S<228>	-2399	241
902	S<227>	-2415	132
903	S<226>	-2431	241
904	S<225>	-2447	132
905	S<224>	-2463	241
906	S<223>	-2479	132
907	S<222>	-2495	241
908	S<221>	-2511	132
909	S<220>	-2527	241
910	S<219>	-2543	132
911	S<218>	-2559	241
912	S<217>	-2575	132
913	S<216>	-2591	241
914	S<215>	-2607	132
915	S<214>	-2623	241
916	S<213>	-2639	132
917	S<212>	-2655	241
918	S<211>	-2671	132
919	S<210>	-2687	241
920	S<209>	-2703	132
921	S<208>	-2719	241
922	S<207>	-2735	132
923	S<206>	-2751	241
924	S<205>	-2767	132
925	S<204>	-2783	241
926	S<203>	-2799	132
927	S<202>	-2815	241
928	S<201>	-2831	132
929	S<200>	-2847	241
930	S<199>	-2863	132
931	S<198>	-2879	241
932	S<197>	-2895	132
933	S<196>	-2911	241
934	S<195>	-2927	132
935	S<194>	-2943	241
936	S<193>	-2959	132
937	S<192>	-2975	241
938	S<191>	-2991	132
939	S<190>	-3007	241
940	S<189>	-3023	132
941	S<188>	-3039	241
942	S<187>	-3055	132
943	S<186>	-3071	241
944	S<185>	-3087	132
945	S<184>	-3103	241
946	S<183>	-3119	132
947	S<182>	-3135	241
948	S<181>	-3151	132
949	S<180>	-3167	241
950	S<179>	-3183	132

Pad No.	Pin Name	X	Y
951	S<178>	-3199	241
952	S<177>	-3215	132
953	S<176>	-3231	241
954	S<175>	-3247	132
955	S<174>	-3263	241
956	S<173>	-3279	132
957	S<172>	-3295	241
958	S<171>	-3311	132
959	S<170>	-3327	241
960	S<169>	-3343	132
961	S<168>	-3359	241
962	S<167>	-3375	132
963	S<166>	-3391	241
964	S<165>	-3407	132
965	S<164>	-3423	241
966	S<163>	-3439	132
967	S<162>	-3455	241
968	S<161>	-3471	132
969	S<160>	-3487	241
970	S<159>	-3503	132
971	S<158>	-3519	241
972	S<157>	-3535	132
973	S<156>	-3551	241
974	S<155>	-3567	132
975	S<154>	-3583	241
976	S<153>	-3599	132
977	S<152>	-3615	241
978	S<151>	-3631	132
979	S<150>	-3647	241
980	S<149>	-3663	132
981	S<148>	-3679	241
982	S<147>	-3695	132
983	S<146>	-3711	241
984	S<145>	-3727	132
985	S<144>	-3743	241
986	S<143>	-3759	132
987	S<142>	-3775	241
988	S<141>	-3791	132
989	S<140>	-3807	241
990	S<139>	-3823	132
991	S<138>	-3839	241
992	S<137>	-3855	132
993	S<136>	-3871	241
994	S<135>	-3887	132
995	S<134>	-3903	241
996	S<133>	-3919	132
997	S<132>	-3935	241
998	S<131>	-3951	132
999	S<130>	-3967	241
1000	S<129>	-3983	132

R61580 Pad Coordinate(No.11)

(unit: μm)

Pad No.	Pin Name	X	Y
1001	S<128>	-3999	241
1002	S<127>	-4015	132
1003	S<126>	-4031	241
1004	S<125>	-4047	132
1005	S<124>	-4063	241
1006	S<123>	-4079	132
1007	S<122>	-4095	241
1008	S<121>	-4111	132
1009	S<120>	-4127	241
1010	S<119>	-4143	132
1011	S<118>	-4159	241
1012	S<117>	-4175	132
1013	S<116>	-4191	241
1014	S<115>	-4207	132
1015	S<114>	-4223	241
1016	S<113>	-4239	132
1017	S<112>	-4255	241
1018	S<111>	-4271	132
1019	S<110>	-4287	241
1020	S<109>	-4303	132
1021	S<108>	-4319	241
1022	S<107>	-4335	132
1023	S<106>	-4351	241
1024	S<105>	-4367	132
1025	S<104>	-4383	241
1026	S<103>	-4399	132
1027	S<102>	-4415	241
1028	S<101>	-4431	132
1029	S<100>	-4447	241
1030	S<99>	-4463	132
1031	S<98>	-4479	241
1032	S<97>	-4495	132
1033	S<96>	-4511	241
1034	S<95>	-4527	132
1035	S<94>	-4543	241
1036	S<93>	-4559	132
1037	S<92>	-4575	241
1038	S<91>	-4591	132
1039	S<90>	-4607	241
1040	S<89>	-4623	132
1041	S<88>	-4639	241
1042	S<87>	-4655	132
1043	S<86>	-4671	241
1044	S<85>	-4687	132
1045	S<84>	-4703	241
1046	S<83>	-4719	132
1047	S<82>	-4735	241
1048	S<81>	-4751	132
1049	S<80>	-4767	241
1050	S<79>	-4783	132
1051	S<78>	-4799	241
1052	S<77>	-4815	132
1053	S<76>	-4831	241
1054	S<75>	-4847	132
1055	S<74>	-4863	241
1056	S<73>	-4879	132
1057	S<72>	-4895	241
1058	S<71>	-4911	132
1059	S<70>	-4927	241
1060	S<69>	-4943	132
1061	S<68>	-4959	241
1062	S<67>	-4975	132
1063	S<66>	-4991	241
1064	S<65>	-5007	132
1065	S<64>	-5023	241
1066	S<63>	-5039	132
1067	S<62>	-5055	241
1068	S<61>	-5071	132
1069	S<60>	-5087	241
1070	S<59>	-5103	132
1071	S<58>	-5119	241
1072	S<57>	-5135	132
1073	S<56>	-5151	241
1074	S<55>	-5167	132
1075	S<54>	-5183	241
1076	S<53>	-5199	132
1077	S<52>	-5215	241
1078	S<51>	-5231	132
1079	S<50>	-5247	241
1080	S<49>	-5263	132
1081	S<48>	-5279	241
1082	S<47>	-5295	132
1083	S<46>	-5311	241
1084	S<45>	-5327	132
1085	S<44>	-5343	241
1086	S<43>	-5359	132
1087	S<42>	-5375	241
1088	S<41>	-5391	132
1089	S<40>	-5407	241
1090	S<39>	-5423	132
1091	S<38>	-5439	241
1092	S<37>	-5455	132
1093	S<36>	-5471	241
1094	S<35>	-5487	132
1095	S<34>	-5503	241
1096	S<33>	-5519	132
1097	S<32>	-5535	241
1098	S<31>	-5551	132
1099	S<30>	-5567	241
1100	S<29>	-5583	132

R61580 Pad Coordinate(No.12)

(unit: μm)

Pad No.	Pin Name	X	Y
1101	S<28>	-5599	241
1102	S<27>	-5615	132
1103	S<26>	-5631	241
1104	S<25>	-5647	132
1105	S<24>	-5663	241
1106	S<23>	-5679	132
1107	S<22>	-5695	241
1108	S<21>	-5711	132
1109	S<20>	-5727	241
1110	S<19>	-5743	132
1111	S<18>	-5759	241
1112	S<17>	-5775	132
1113	S<16>	-5791	241
1114	S<15>	-5807	132
1115	S<14>	-5823	241
1116	S<13>	-5839	132
1117	S<12>	-5855	241
1118	S<11>	-5871	132
1119	S<10>	-5887	241
1120	S<9>	-5903	132
1121	S<8>	-5919	241
1122	S<7>	-5935	132
1123	S<6>	-5951	241
1124	S<5>	-5967	132
1125	S<4>	-5983	241
1126	S<3>	-5999	132
1127	S<2>	-6015	241
1128	S<1>	-6031	132
1129	TESTO6	-6047	241
1130	TESTO7	-6083	241
1131	G<1>	-6099	132
1132	G<3>	-6115	241
1133	G<5>	-6131	132
1134	G<7>	-6147	241
1135	G<9>	-6163	132
1136	G<11>	-6179	241
1137	G<13>	-6195	132
1138	G<15>	-6211	241
1139	G<17>	-6227	132
1140	G<19>	-6243	241
1141	G<21>	-6259	132
1142	G<23>	-6275	241
1143	G<25>	-6291	132
1144	G<27>	-6307	241
1145	G<29>	-6323	132
1146	G<31>	-6339	241
1147	G<33>	-6355	132
1148	G<35>	-6371	241
1149	G<37>	-6387	132
1150	G<39>	-6403	241

Pad No.	Pin Name	X	Y
1151	G<41>	-6419	132
1152	G<43>	-6435	241
1153	G<45>	-6451	132
1154	G<47>	-6467	241
1155	G<49>	-6483	132
1156	G<51>	-6499	241
1157	G<53>	-6515	132
1158	G<55>	-6531	241
1159	G<57>	-6547	132
1160	G<59>	-6563	241
1161	G<61>	-6579	132
1162	G<63>	-6595	241
1163	G<65>	-6611	132
1164	G<67>	-6627	241
1165	G<69>	-6643	132
1166	G<71>	-6659	241
1167	G<73>	-6675	132
1168	G<75>	-6691	241
1169	G<77>	-6707	132
1170	G<79>	-6723	241
1171	G<81>	-6739	132
1172	G<83>	-6755	241
1173	G<85>	-6771	132
1174	G<87>	-6787	241
1175	G<89>	-6803	132
1176	G<91>	-6819	241
1177	G<93>	-6835	132
1178	G<95>	-6851	241
1179	G<97>	-6867	132
1180	G<99>	-6883	241
1181	G<101>	-6899	132
1182	G<103>	-6915	241
1183	G<105>	-6931	132
1184	G<107>	-6947	241
1185	G<109>	-6963	132
1186	G<111>	-6979	241
1187	G<113>	-6995	132
1188	G<115>	-7011	241
1189	G<117>	-7027	132
1190	G<119>	-7043	241
1191	G<121>	-7059	132
1192	G<123>	-7075	241
1193	G<125>	-7091	132
1194	G<127>	-7107	241
1195	G<129>	-7123	132
1196	G<131>	-7139	241
1197	G<133>	-7155	132
1198	G<135>	-7171	241
1199	G<137>	-7187	132
1200	G<139>	-7203	241

R61580 Pad Coordinate(No.13)

(unit: μm)

Pad No.	Pin Name	X	Y
1201	G<141>	-7219	132
1202	G<143>	-7235	241
1203	G<145>	-7251	132
1204	G<147>	-7267	241
1205	G<149>	-7283	132
1206	G<151>	-7299	241
1207	G<153>	-7315	132
1208	G<155>	-7331	241
1209	G<157>	-7347	132
1210	G<159>	-7363	241
1211	G<161>	-7379	132
1212	G<163>	-7395	241
1213	G<165>	-7411	132
1214	G<167>	-7427	241
1215	G<169>	-7443	132
1216	G<171>	-7459	241
1217	G<173>	-7475	132
1218	G<175>	-7491	241
1219	G<177>	-7507	132
1220	G<179>	-7523	241
1221	G<181>	-7539	132
1222	G<183>	-7555	241
1223	G<185>	-7571	132
1224	G<187>	-7587	241
1225	G<189>	-7603	132
1226	G<191>	-7619	241
1227	G<193>	-7635	132
1228	G<195>	-7651	241
1229	G<197>	-7667	132
1230	G<199>	-7683	241
1231	G<201>	-7699	132
1232	G<203>	-7715	241
1233	G<205>	-7731	132
1234	G<207>	-7747	241
1235	G<209>	-7763	132
1236	G<211>	-7779	241
1237	G<213>	-7795	132
1238	G<215>	-7811	241
1239	G<217>	-7827	132
1240	G<219>	-7843	241
1241	G<221>	-7859	132
1242	G<223>	-7875	241
1243	G<225>	-7891	132
1244	G<227>	-7907	241
1245	G<229>	-7923	132
1246	G<231>	-7939	241
1247	G<233>	-7955	132
1248	G<235>	-7971	241
1249	G<237>	-7987	132
1250	G<239>	-8003	241
1251	G<241>	-8019	132
1252	G<243>	-8035	241
1253	G<245>	-8051	132
1254	G<247>	-8067	241
1255	G<249>	-8083	132
1256	G<251>	-8099	241
1257	G<253>	-8115	132
1258	G<255>	-8131	241
1259	G<257>	-8147	132
1260	G<259>	-8163	241
1261	G<261>	-8179	132
1262	G<263>	-8195	241
1263	G<265>	-8211	132
1264	G<267>	-8227	241
1265	G<269>	-8243	132
1266	G<271>	-8259	241
1267	G<273>	-8275	132
1268	G<275>	-8291	241
1269	G<277>	-8307	132
1270	G<279>	-8323	241
1271	G<281>	-8339	132
1272	G<283>	-8355	241
1273	G<285>	-8371	132
1274	G<287>	-8387	241
1275	G<289>	-8403	132
1276	G<291>	-8419	241
1277	G<293>	-8435	132
1278	G<295>	-8451	241
1279	G<297>	-8467	132
1280	G<299>	-8483	241
1281	G<301>	-8499	132
1282	G<303>	-8515	241
1283	G<305>	-8531	132
1284	G<307>	-8547	241
1285	G<309>	-8563	132
1286	G<311>	-8579	241
1287	G<313>	-8595	132
1288	G<315>	-8611	241
1289	G<317>	-8627	132
1290	G<319>	-8643	241
1291	TESTO8	-8659	132

Bump Arrangement

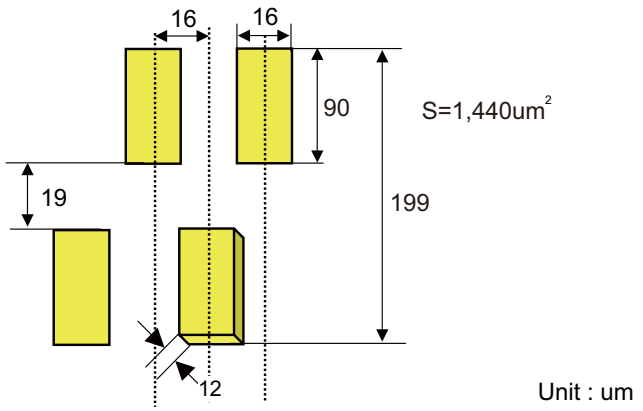
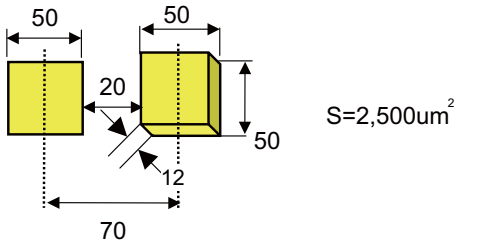
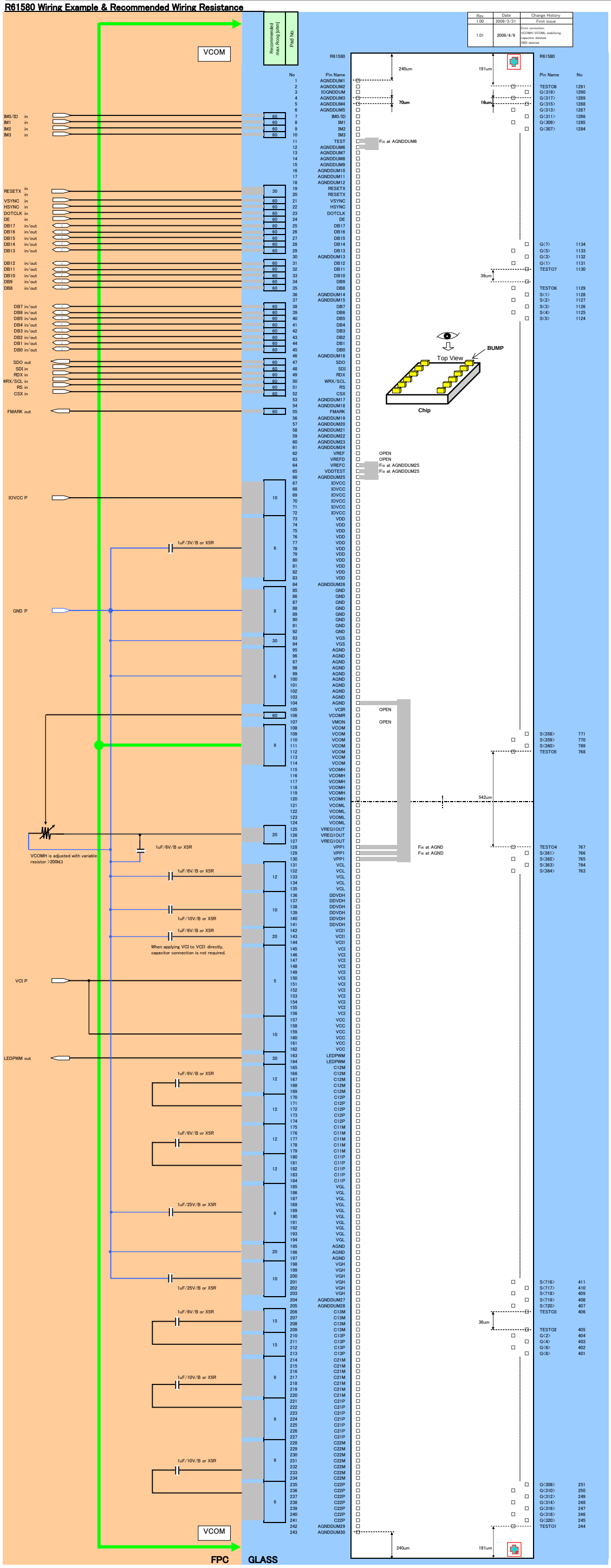
S[720:1], G[320:1], TESTO*	
I/O pins	

Figure 3

R61580 Wiring Example & Recommended Wiring Resistance



Frame memory Address Map

Table 13 Frame Memory Address and Display Position on the Panel (SS = 0, BGR = 0)

S/G pin		S[1]	S[2]	S[3]	S[4]	S[5]	S[6]	S[7]	S[8]	S[9]	S[10]	S[11]	S[12]	· · · · ·	S[709]	S[710]	S[711]	S[712]	S[713]	S[714]	S[715]	S[716]	S[717]	S[718]	S[719]	S[720]
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			· · · · ·	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G[1]	G[320]	h00000			h00001			h00002			h00003			· · · · ·	h000EC			h000ED			h000EE			h000EF		
G[2]	G[319]	h00100			h00101			h00102			h00103			· · · · ·	h001EC			h001ED			h001EE			h001EF		
G[3]	G[318]	h00200			h00201			h00202			h00203			· · · · ·	h002EC			h002ED			h002EE			h002EF		
G[4]	G[317]	h00300			h00301			h00302			h00303			· · · · ·	h003EC			h003ED			h003EE			h003EF		
G[5]	G[316]	h00400			h00401			h00402			h00403			· · · · ·	h004EC			h004ED			h004EE			h004EF		
G[6]	G[315]	h00500			h00501			h00502			h00503			· · · · ·	h005EC			h005ED			h005EE			h005EF		
G[7]	G[314]	h00600			h00601			h00602			h00603			· · · · ·	h006EC			h006ED			h006EE			h006EF		
G[8]	G[313]	h00700			h00701			h00702			h00703			· · · · ·	h007EC			h007ED			h007EE			h007EF		
G[9]	G[312]	h00800			h00801			h00802			h00803			· · · · ·	h008EC			h008ED			h008EE			h008EF		
G[10]	G[311]	h00900			h00901			h00902			h00903			· · · · ·	h009EC			h009ED			h009EE			h009EF		
G[11]	G[310]	h00A00			h00A01			h00A02			h00A03			· · · · ·	h00AEC			h00AED			h00AEE			h00AEF		
G[12]	G[309]	h00B00			h00B01			h00B02			h00B03			· · · · ·	h00BEC			h00BED			h00BEE			h00BEF		
G[13]	G[308]	h00C00			h00C01			h00C02			h00C03			· · · · ·	h00CEC			h00CED			h00CEE			h00CEF		
G[14]	G[307]	h00D00			h00D01			h00D02			h00D03			· · · · ·	h00DEC			h00DED			h00DEE			h00DEF		
G[15]	G[306]	h00E00			h00E01			h00E02			h00E03			· · · · ·	h00EEC			h00EED			h00EEE			h00EEF		
G[16]	G[305]	h00F00			h00F01			h00F02			h00F03			· · · · ·	h00FEC			h00FED			h00FEE			h00FEF		
G[17]	G[304]	h01000			h01001			h01002			h01003			· · · · ·	h010EC			h010ED			h010EE			h010EF		
G[18]	G[303]	h01100			h01101			h01102			h01103			· · · · ·	h011EC			h011ED			h011EE			h011EF		
G[19]	G[302]	h01200			h01201			h01202			h01203			· · · · ·	h012EC			h012ED			h012EE			h012EF		
G[20]	G[301]	h01300			h01301			h01302			h01303			· · · · ·	h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G[305]	G[16]	h13000			h13001			h13002			h13003			· · · · ·	h130EC			h130ED			h130EE			h130EF		
G[306]	G[15]	h13100			h13101			h13102			h13103			· · · · ·	h131EC			h131ED			h131EE			h131EF		
G[307]	G[14]	h13200			h13201			h13202			h13203			· · · · ·	h132EC			h132ED			h132EE			h132EF		
G[308]	G[13]	h13300			h13301			h13302			h13303			· · · · ·	h133EC			h133ED			h133EE			h133EF		
G[309]	G[12]	h13400			h13401			h13402			h13403			· · · · ·	h134EC			h134ED			h134EE			h134EF		
G[310]	G[11]	h13500			h13501			h13502			h13503			· · · · ·	h135EC			h135ED			h135EE			h135EF		
G[311]	G[10]	h13600			h13601			h13602			h13603			· · · · ·	h136EC			h136ED			h136EE			h136EF		
G[312]	G[9]	h13700			h13701			h13702			h13703			· · · · ·	h137EC			h137ED			h137EE			h137EF		
G[313]	G[8]	h13800			h13801			h13802			h13803			· · · · ·	h138EC			h138ED			h138EE			h138EF		
G[314]	G[7]	h13900			h13901			h13902			h13903			· · · · ·	h139EC			h139ED			h139EE			h139EF		
G[315]	G[6]	h13A00			h13A01			h13A02			h13A03			· · · · ·	h13AEC			h13AED			h13AEE			h13AEF		
G[316]	G[5]	h13B00			h13B01			h13B02			h13B03			· · · · ·	h13BEC			h13BED			h13BEE			h13BEF		
G[317]	G[4]	h13C00			h13C01			h13C02			h13C03			· · · · ·	h13CEC			h13CED			h13CEE			h13CEF		
G[318]	G[3]	h13D00			h13D01			h13D02			h13D03			· · · · ·	h13DEC			h13DED			h13DEE			h13DEF		
G[319]	G[2]	h13E00			h13E01			h13E02			h13E03			· · · · ·	h13EEC			h13EED			h13EEE			h13EEF		
G[320]	G[1]	h13F00			h13F01			h13F02			h13F03			· · · · ·	h13FEC			h13FED			h13FEE			h13FEF		

Table 14 frame memory Address and Display Position on the Panel (SS = 1, BGR = 1)

S/G pin		S[720] S[719] S[718]	S[717] S[716] S[715]	S[714] S[713] S[712]	S[711] S[710] S[709]	· · · · ·	S[12] S[11] S[10]	S[9] S[8] S[7]	S[6] S[5] S[4]	S[3] S[2] S[1]
GS=0	GS=1	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]	· · · · ·	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]
G[1]	G[320]	h00000	h00001	h00002	h00003	· · · · ·	h000EC	h000ED	h000EE	h000EF
G[2]	G[319]	h00100	h00101	h00102	h00103	· · · · ·	h001EC	h001ED	h001EE	h001EF
G[3]	G[318]	h00200	h00201	h00202	h00203	· · · · ·	h002EC	h002ED	h002EE	h002EF
G[4]	G[317]	h00300	h00301	h00302	h00303	· · · · ·	h003EC	h003ED	h003EE	h003EF
G[5]	G[316]	h00400	h00401	h00402	h00403	· · · · ·	h004EC	h004ED	h004EE	h004EF
G[6]	G[315]	h00500	h00501	h00502	h00503	· · · · ·	h005EC	h005ED	h005EE	h005EF
G[7]	G[314]	h00600	h00601	h00602	h00603	· · · · ·	h006EC	h006ED	h006EE	h006EF
G[8]	G[313]	h00700	h00701	h00702	h00703	· · · · ·	h007EC	h007ED	h007EE	h007EF
G[9]	G[312]	h00800	h00801	h00802	h00803	· · · · ·	h008EC	h008ED	h008EE	h008EF
G[10]	G[311]	h00900	h00901	h00902	h00903	· · · · ·	h009EC	h009ED	h009EE	h009EF
G[11]	G[310]	h00A00	h00A01	h00A02	h00A03	· · · · ·	h00AEC	h00AED	h00AEE	h00AEF
G[12]	G[309]	h00B00	h00B01	h00B02	h00B03	· · · · ·	h00BEC	h00BED	h00BEE	h00BEF
G[13]	G[308]	h00C00	h00C01	h00C02	h00C03	· · · · ·	h00CEC	h00CED	h00CEE	h00CEF
G[14]	G[307]	h00D00	h00D01	h00D02	h00D03	· · · · ·	h00DEC	h00DED	h00DEE	h00DEF
G[15]	G[306]	h00E00	h00E01	h00E02	h00E03	· · · · ·	h00EEC	h00EED	h00EEE	h00EEF
G[16]	G[305]	h00F00	h00F01	h00F02	h00F03	· · · · ·	h00FEC	h00FED	h00FEE	h00FEF
G[17]	G[304]	h01000	h01001	h01002	h01003	· · · · ·	h010EC	h010ED	h010EE	h010EF
G[18]	G[303]	h01100	h01101	h01102	h01103	· · · · ·	h011EC	h011ED	h011EE	h011EF
G[19]	G[302]	h01200	h01201	h01202	h01203	· · · · ·	h012EC	h012ED	h012EE	h012EF
G[20]	G[301]	h01300	h01301	h01302	h01303	· · · · ·	h013EC	h013ED	h013EE	h013EF
:	:	:	:	:	:		:	:	:	:
:	:	:	:	:	:		:	:	:	:
G[305]	G[16]	h13000	h13001	h13002	h13003	· · · · ·	h130EC	h130ED	h130EE	h130EF
G[306]	G[15]	h13100	h13101	h13102	h13103	· · · · ·	h131EC	h131ED	h131EE	h131EF
G[307]	G[14]	h13200	h13201	h13202	h13203	· · · · ·	h132EC	h132ED	h132EE	h132EF
G[308]	G[13]	h13300	h13301	h13302	h13303	· · · · ·	h133EC	h133ED	h133EE	h133EF
G[309]	G[12]	h13400	h13401	h13402	h13403	· · · · ·	h134EC	h134ED	h134EE	h134EF
G[310]	G[11]	h13500	h13501	h13502	h13503	· · · · ·	h135EC	h135ED	h135EE	h135EF
G[311]	G[10]	h13600	h13601	h13602	h13603	· · · · ·	h136EC	h136ED	h136EE	h136EF
G[312]	G[9]	h13700	h13701	h13702	h13703	· · · · ·	h137EC	h137ED	h137EE	h137EF
G[313]	G[8]	h13800	h13801	h13802	h13803	· · · · ·	h138EC	h138ED	h138EE	h138EF
G[314]	G[7]	h13900	h13901	h13902	h13903	· · · · ·	h139EC	h139ED	h139EE	h139EF
G[315]	G[6]	h13A00	h13A01	h13A02	h13A03	· · · · ·	h13AEC	h13AED	h13AEE	h13AEF
G[316]	G[5]	h13B00	h13B01	h13B02	h13B03	· · · · ·	h13BEC	h13BED	h13BEE	h13BEF
G[317]	G[4]	h13C00	h13C01	h13C02	h13C03	· · · · ·	h13CEC	h13CED	h13CEE	h13CEF
G[318]	G[3]	h13D00	h13D01	h13D02	h13D03	· · · · ·	h13DEC	h13DED	h13DEE	h13DEF
G[319]	G[2]	h13E00	h13E01	h13E02	h13E03	· · · · ·	h13EEC	h13EED	h13EEE	h13EEF
G[320]	G[1]	h13F00	h13F01	h13F02	h13F03	· · · · ·	h13FEC	h13FED	h13FEE	h13FEF

Instruction

Outline

The R61580 adopts 18-bit bus architecture in order to interface to high-performance host processor in high speed. The R61580 starts internal processing after storing 16-/8-/1-bit control information sent from the host processor, in the instruction register (IR) and the data register (DR). Since the internal operation of the R61580 is controlled by the signals sent from the host processor, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 ~ IB0) are called instruction. The instruction is categorized as below:

1. Specify index
2. Display control
3. Power management control
4. Set internal frame memory address
5. Transfer data to and from the internal frame memory
6. Adjustment
7. Window address control
8. Panel Display Control

Normally, the instruction to write data (5) is used the most frequently. The internal frame memory address is updated automatically as data is written to the internal frame memory, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the load on the host processor. The R61580 writes instructions consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycles).

Instruction Data Format

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID [7]	ID [6]	ID [5]	ID [4]	ID [3]	ID [2]	ID [1]	ID [0]

The index register specifies the index R00h to RFFh of the control register or frame memory control to be accessed using a binary number from "0000_0000" to "1111_1111". The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

Display Control

Device Code Read (R00h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0

The device code "1580"h is read out when reading out this register forcibly.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shifts from S1 to S720.
When SS = “1”, the source driver output shifts from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, color data is output in the order of R, G and then B.
When SS = “1” and BGR = “1”, color data is output in the order of B, G and then R.

When changing the SS and the BGR bit settings, frame memory data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See “Scan mode setting”.

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	BC0	0	0	0	0	0	0	0	0	NW0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NW0: When line inversion waveform is selected (BC0=1), NW0 bit sets number of line, N, as alternating cycle of line inversion. Line inversion is operated every N+1 line cycle. NW0 bit can be set to 1 or 2.

Table 15

NW[0]	Alternating cycle
0	Every line
1	Every 2 lines

BC0: Selects the liquid crystal drive waveform VCOM. See “Line Inversion AC Drive” for details.

BC0 = 0: frame inversion waveform is selected.
BC0 = 1: line inversion waveform is selected.

In either liquid crystal drive method; the polarity inversion is halted in blank period (back and front porch periods).

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRIREG	DFM	0	BGR	0	0	0	0	ORG	0	I/D [1]	I/D [0]	AM	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

The entry mode register includes instruction bits for setting how to write data from the host processor to the frame memory in the R61580.

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the R61580 writes data to the internal frame memory.

AM = "0", sets the horizontal direction.
AM = "1", sets the vertical direction.

When making a window address area, the data is written only within the area in the direction determined by I/D1-0, AM bits.

I/D[1:0]: Either increments (+1) or decrements (-1) the address counter (AC) automatically as the data is written to the frame memory. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]). The AM bit sets either horizontal or vertical direction in updating frame memory address counter automatically when writing data to the internal frame memory.

ORG: Moves the origin address according to the I/D setting when a window address area is made. This function is enabled when writing data within the window address area using high-speed frame memory write function.

ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the frame memory address map within the window address area.
ORG = 1: The origin address "h00000" is moved according to the I/D[1:0] setting.

Notes: 1. When ORG = 1, only the origin address "h00000" can be set.
2. In frame memory read operation, make sure to set ORG = 0.

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the frame memory.

BGR = 0: Write data in the order of RGB to the frame memory.
BGR = 1: Reverse the order from RGB to BGR in writing data to the frame memory.

BGR = 0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR = 1

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

DFM: In combination with the TRIREG setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM = 0 when not transferring data via 16-bit or 8-bit interface.

Write DFM=0 when using an interface other than 8-/ 16- bit interface.

TRIREG: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 80-system 8-bit interface operation,
TRIREG = 0: 16-bit frame memory data is transferred in two transfers.
TRIREG = 1: 18-bit frame memory data is transferred in three transfers.

In 80-system 16-bit bus interface operation,
TRIREG = 0: 16-bit frame memory data is transferred in one transfer.
TRIREG = 1: 18-bit frame memory data is transferred in two transfers.

Make sure TRIREG = 0 when not transferring data via 16-bit or 8-bit interface.

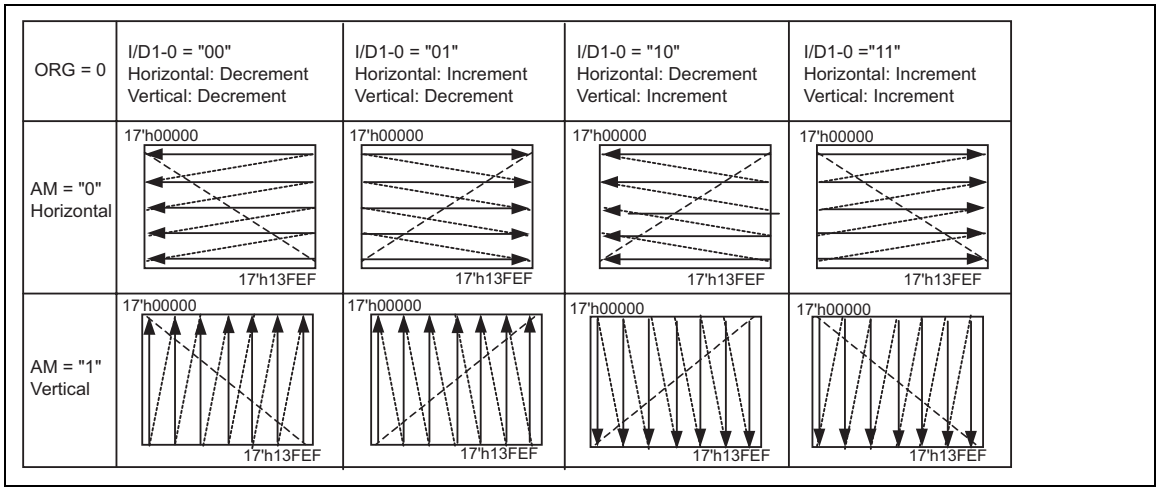


Figure 4 Automatic Address Update (ORG = 0, AM, I/D)

Note: When writing data within the window address area with ORG = 0, any address within the window address area can be designated as the starting point of frame memory write operation.

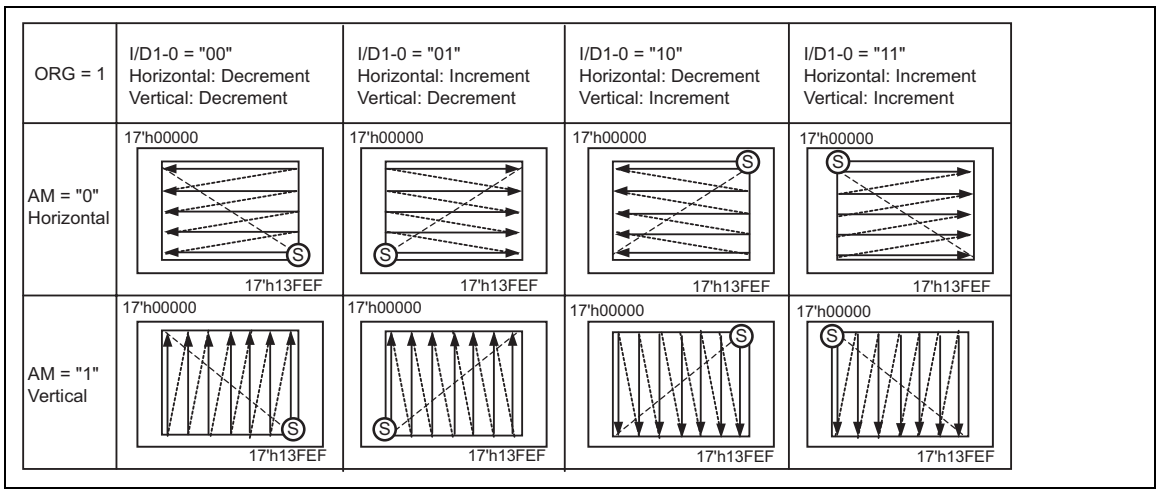


Figure 5 Automatic Address Update (ORG = 1, AM, I/D)

Notes: 1. W hen ORG = 1, the starting point of writing data within the window address area can be set at either corner of the window address area (“S” in circle in the above figure).

2. When ORG = 1, make sure to set the address “h00000” in the frame memory address set registers (R21h and R21h). Setting other addresses is inhibited.

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PTDE	0	0	0	BASEE	0	0	0	0	COL	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

COL: When COL = 1, grayscale amplifiers other than V0 and V63 halt displaying images so that power consumption is reduced. Also, only 8 colors are available. See “8-color Display Mode” in “Instruction Setting Sequence” for details.

Table 16

COL	Display color
0	262,144
1	8

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The R61580 drives liquid crystal with non-lit display level or drives only partial image display area.
BASEE = 1: A base image is displayed on the panel.

PTDE: PTDE is the display enable bit of a partial image.

PTDE=0: Partial image is not displayed. Only base image is displayed.
PTDE=1: Partial image is displayed. Write BASEE=0 to turn off a base image.

Table 17

BASEE	PTDE	VLE	COL	State
0	0	*	*	Halt display operation
1	0	0	0	262,144-color display operation
1	0	0	1	8-color display operation
1	0	1	0	262,144-color display operation with scroll function enabled
0	1	*	0	262,144-color partial display operation
0	1	*	1	8-color partial display operation

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	FP [7]	FP [6]	FP [5]	FP [4]	FP [3]	FP [2]	FP [1]	FP [0]	BP [7]	BP [6]	BP [5]	BP [4]	BP [3]	BP [2]	BP [1]	BP [0]
Default value		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP [7:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [7:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Table 18

FP[7:0] BP[7:0]	Front porch period	Back porch period
8'h00	Setting inhibited	Setting inhibited
8'h01	Setting inhibited	Setting inhibited
8'h02	Setting inhibited	2 lines
8'h03	3 lines	3 lines
8'h04	4 lines	4 lines
8'h05	5 lines	5 lines
8'h06	6 lines	6 lines
8'h07	7 lines	7 lines
8'h08	8 lines	8 lines
8'h09	9 lines	9 lines
8'h0A	10 lines	10 lines
8'h0B	11 lines	11 lines
8'h0C	12 lines	12 lines
8'h0D	13 lines	13 lines
8'h0E	14 lines	14 lines
8'h0F	15 lines	15 lines
:	:	:
8'h7F	127 lines	127 lines
8'h80	128 lines	128 lines
8'h81	Setting inhibited	Setting inhibited
:	:	:
8'hFF	Setting inhibited	Setting inhibited

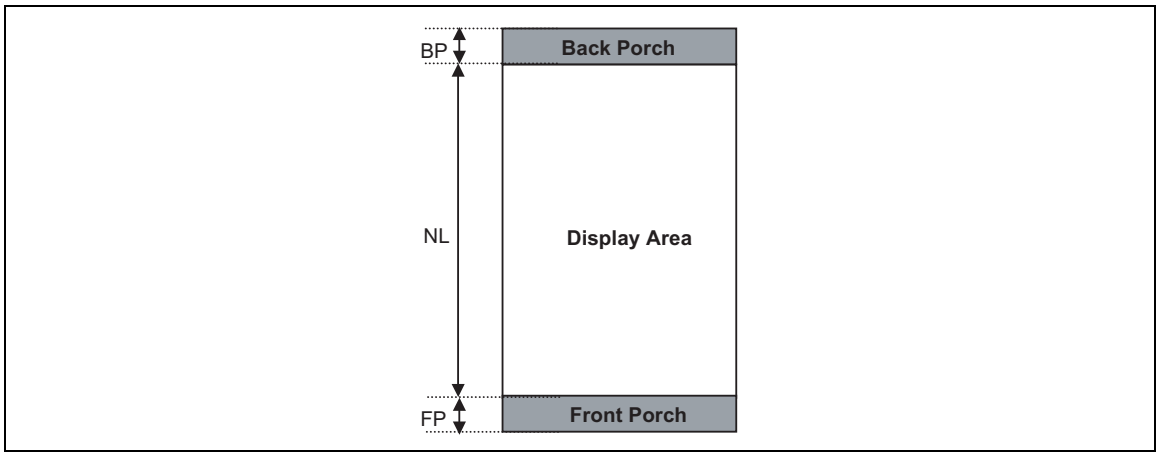


Figure 6 Front and Back Porch Periods

Note to Setting BP and FP

Set the BP and FP bits as follows:

BP ≥ 2 lines	FP ≥ 3 lines	FP + BP ≤ 256 lines

Make sure that FP+BP＝even number.

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS [2]	PTS [1]	PTS [0]	0	0	PTG	0	ISC [3]	ISC [2]	ISC [1]	ISC [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

ISC [3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 19

ISC[3:0]	Scan cycle
4'h0	Setting inhibited
4'h1	3 frames
4'h2	5 frames
4'h3	7 frames
4'h4	9 frames
4'h5	11 frames
4'h6	13 frames
4'h7	15 frames
4'h8	17 frames
4'h9	19 frames
4'hA	21 frames
4'hB	23 frames
4'hC	25 frames
4'hD	27 frames
4'hE	29 frames
4'hF	31 frames

PTG: Sets the scan mode in non-display area

Table 20

PTG	Scan mode in non-display area
0	Normal scan
1	Interval scan

Note: Select frame-inversion AC drive when interval scan is selected.

PTS[2:0]: Sets the source output level in non-display area drive period. When PTS[2] = 1, the operation of amplifiers that generate the grayscales other than V0 and V31 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 21 Source Output Level and Voltage Generating Operation in Non-display Drive Period

PTS [2]	PTS [1:0]	Source output level in non lit display area		Grayscale amplifier operation in non lit display are	Step-up clock frequency in non lit display are
		Positive polarity	Negative polarity		
0	00	V63	V0	V0 to V63	Register setting (DC0, DC1)
	01	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)
	10	GND	GND	V0 to V63	Register setting (DC0, DC1)
	11	Hi-z	Hi-z	V0 to V63	Register setting (DC0, DC1)
1	00	V63	V0	V0, V63	DC0 setting x 1/2
	01	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)
	10	GND	GND	V0, V63	DC0 setting x 1/2
	11	Hi-z	Hi-z	V0, V63	DC0 setting x 1/2

Note: Define source polarity in non-lit display area by NDL bit. Note that if PTS[2]=1, step-up operation may not be executed successfully depending on DC0 and RTN* values.

Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI [2]	FMI [1]	FMI [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE: When FMARKOE = 1, the R61580 starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits. See FMARK Interface" for details.

Table 22

FMI[2]	FMI[1]	FMI[0]	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	ENC [2]	ENC [1]	ENC [0]	0	0	0	RM	0	0	DM [1]	DM [0]	0	0	RIM [1]	RIM [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets the interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the R61580 performs display operation.

Table 23 RGB Interface Operation

RIM[1:0]	Bus width	Colors	Used pins
2'h0	18-bit RGB interface (1 transfer/pixel)	262,144	DB17-0
2'h1	16-bit RGB interface (1 transfer/pixel)	65,536	DB17-13, 11-1
2'h2	Setting inhibited	-	-
2'h3	Setting inhibited	-	-

Note: Instruction bits are set only via system interface.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

Table 24 Display Interface

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting inhibited

RM: Selects the interface for frame memory access operation. Frame memory access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 25 frame memory Access Interface

RM	Frame Memory Access Interface
0	System interface/VSYNC interface
1	RGB interface

ENC[2:0]: Sets the frame memory write cycle via RGB interface.

Table 25 Frame Memory Write Cycle

ENC[2:0]	Frame memory Write Cycle (frame periods)
3'h0	1 frame
3'h1	2 frames
3'h2	3 frames
3'h3	4 frames
3'h4	5 frames
3'h5	6 frames
3'h6	7 frames
3'h7	8 frames

Frame Marker Position (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	FMP [8]	FMP [7]	FMP [6]	FMP [5]	FMP [4]	FMP [3]	FMP [2]	FMP [1]	FMP [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is outputted at the start of back porch period for 1H period (IOVCC-GND amplitude signal). FMARK can be used as the trigger signal for frame synchronous write operation. See FMARK Interface for details.

Make sure the setting restriction 9'h000 ≤ FMP ≤ BP+NL+FP.

Table 26

FMP[8:0]	FMARK output position
9"h000	0th line
9'h001	1st line
9"h002	2nd line
:	:
9"h14E	334th line
9'h14F	335th line
9"h150~1FF	Setting disabled

VCOM Low Power Control (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	VEM [1]	VEM [0]	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

VEM [1:0]: VCOM equalize function control bit.

When VEM [0]=”1”, VCOM falls to GND level when switching to VCOMH to VCOML (VCOMH → GND → VCOML).

When VEM [1] = “1”, VCOM rises to VCI level when switching to VCOML to VCOMH (VCOML → VCI → VCOMH).

Make sure that VCI<VCOMH and GND>VCOML.

Table 27

VEM[1:0]	Description
2’h0	Setting inhibited
2’h1	Setting inhibited
2’h2	Setting inhibited
2’h3	Equalize VCOMH/VCOML

Note: Check the trade-off between the quality of display on the panel and the power efficiency before use.

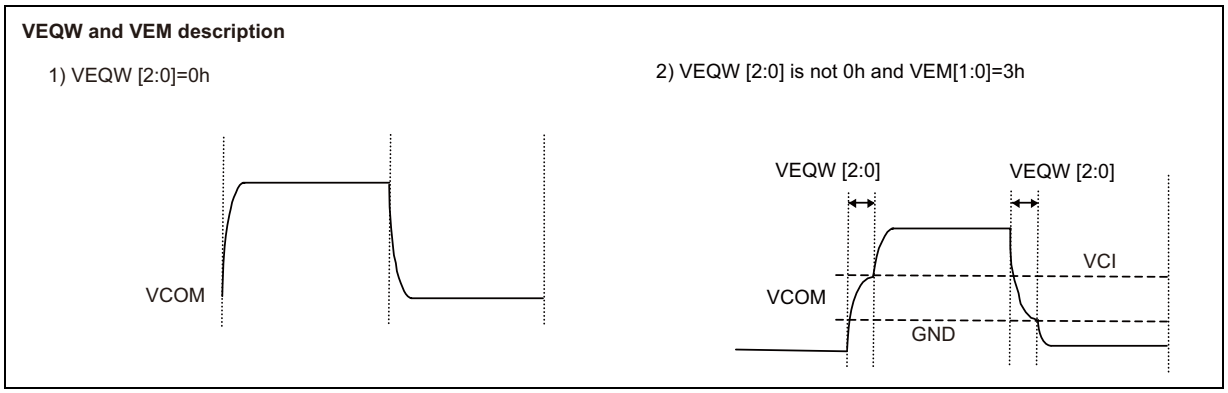


Figure 7

Note: See R93h and R98h for VEQWI and VEQWE descriptions.

External Display Interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of DOTCLK pin.

DPL = 0: input data on the rising edge of DOTCLK
DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.

EPL = 0: writes data DB17-0 when ENABLE = “0” and disables data write operation when ENABLE = “1”.
EPL = 1: writes data DB17-0 when ENABLE = “1” and disables data write operation when ENABLE = “0”.

HSPL: Sets the signal polarity of HSYNC pin.

HSPL = 0: low active
HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNC pin.

VSPL = 0: low active
VSPL = 1: high active

Power Control

Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	BT [2]	BT [1]	BT [0]	0	0	AP [1]	AP [0]	0	DSTB	0	0
Default value		0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0

DSTB: When DSTB = 1, the R61580 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The frame memory data and instruction setting are not maintained when the R61580 enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[1:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[1:0] = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

Table 28 Constant Current in Amplifier in LCD Power Supply

AP[1:0]	LCD power supply circuits
2'h0	Halt operation
2'h1	0.5
2'h2	0.75
2'h3	1

Note: In this table, the constant current in operational amplifiers is the ratio to the constant current when AP[1:0] is set to 2'h3.

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

Table 29 Step-up Factor and Output Voltage Level

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Setting inhibited			
3'h1				
3'h2				
3'h3	VCI1 x2 [x 2]	-VCI1 [x –1]	DDVDH x 3 [x 6]	-(VCI1+DDVDH x 2) [x -5]
3'h4				-(DDVDH x 2) [x –4]
3'h5 (Default)				-(VCI1+DDVDH) [x –3]
3'h6			VCI1+ DDVDH x 2 [x 5]	-(VCI1 + DDVDH x 2) [x –5]
3'h7				-(DDVDH x 2) [x -4]

Notes: 1. The step-up factor from VCI1 is shown in the brackets [ ].

2. Set the following voltages within the respective ranges:
   DDVDH = 6.0V (max.)
   VGH = 18.0V (max.)
   VGL = -13.5V (max.)
   VGH-VGL= 28.0V (max.)
   VCL=-3.0V(max.)

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC1 [2]	DC1 [1]	DC1 [0]	0	DC0 [2]	DC0 [1]	DC0 [0]	0	VC [2]	VC [1]	VC [0]
Default value		0	0	0	0	0	0	1	0	0	0	1	1	0	1	1	1

DC1[2:0]: Defines step-up clock frequency for the step-up circuit 2. The step-up clock is synchronized with internal clock.

Table 30

DC1[2:0]	**Step-up clock frequency for the step-up circuit 2** (f_{DCDC2})
3'h0	Setting inhibited
3'h1	Setting inhibited
3'h2	Line frequency / 4
3'h3	Line frequency / 8
3'h4	Line frequency / 16
3'h5	Setting inhibited
3'h6	Halt step-up circuit 2
3'h7	Setting inhibited

To calculate step-up clock frequency for the step-up circuit 2

Step-up clock frequency (f_{DCDC2}) = line frequency / $2^{(N)}$ [Hz]

= Clock frequency internal operation fosc / number of clock per line x division ratio x $2^{(N)}$ [Hz]

fosc: Clock frequency internal operation
Number of clock per line: RTNI [4:0] or RTNE [4:0]
Division ratio: DIVI [1:0] or DIVE [1:0]
N: DC1[2:0] value

DC0[2:0]: Defines step-up clock frequency for the step-up circuit 1. The step-up clock is synchronized with internal clock.

Table 31

DC0[2:0]	Step-up clock frequency for the step-up circuit 1 (f_{DCDC1})
3'h0	Setting inhibited
3'h1	Setting inhibited
3'h2	Setting inhibited
3'h3	f_{OSC} / 8
3'h4	f_{OSC} / 16
3'h5	f_{OSC} / 32
3'h6	Halt step-up circuit 1
3'h7	Setting inhibited

Note 1: Make sure that $f_{DCDC1} \geq f_{DCDC2}$.
Note 2: Make sure to set DC0 and RTN* bits so that
Step-up cycle of the Step-up circuit 1 ≤ 1 line cycle.
Otherwise the step-up operation may fail.

To calculate step-up clock frequency for the step-up circuit 1

Step-up clock frequency (f_{DCDC1}) = Reference clock frequency / 2^N [Hz]

= Clock frequency for internal operation fosc / division ratio x 2^N [Hz]

fosc: Clock frequency internal operation
Division ratio: DIVI [1:0] or DIVE [1:0]
N: DC1[2:0] value

* Step-up clock operation synchronizes with display operation. Clock division count.

VC [2:0]: Defines VCI1 level.

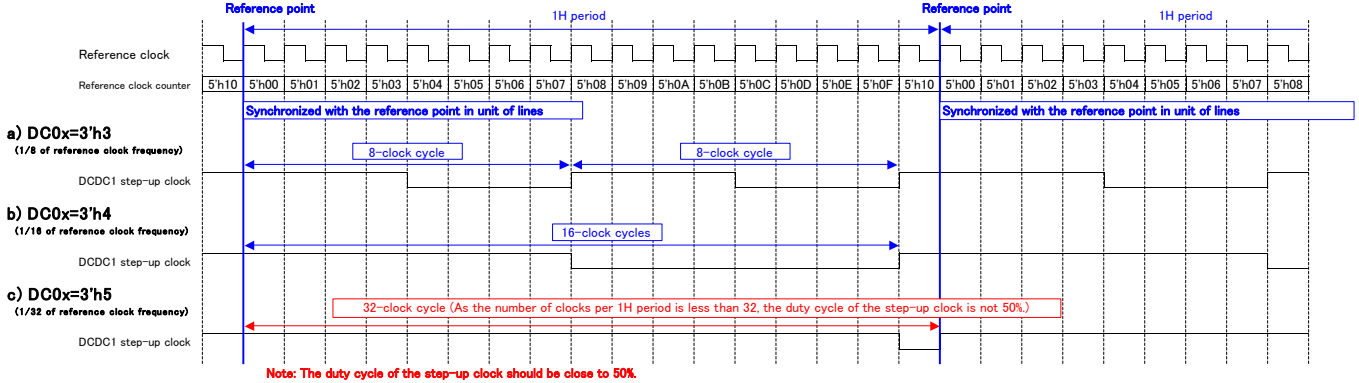
Table 32

VC[2:0]	VCI1 (Reference for step-up operation)
3'h0	Setting inhibited
3'h1	0.94 x VCI
3'h2	0.89 x VCI
3'h3	Setting inhibited
3'h4	Setting inhibited
3'h5	0.76 x VCI
3'h6	Setting inhibited
3'h7	1.00 x VCI

■DC0x Value and DCDC1 Step-up Clock Signal Waveform Example

DCDC1 performs charge operation and boost operation with the step-up clock generated from the timing generator.
The DCDC1 step-up clock frequency is adjusted by setting the division ratio of the reference clock frequency with DC0x register.
(To prevent flickering, the DCDC1 step-up clock signal is synchronized with the reference point of display operation in unit of lines.)
Note: Set DC0x and RTNI so that (DCDC1 step-up clock frequency) ≧ (line clock frequency)
If the above restriction is not followed, the duty cycle during the boost period is less than 50%. As a result, the step-up circuit may not operate normally.

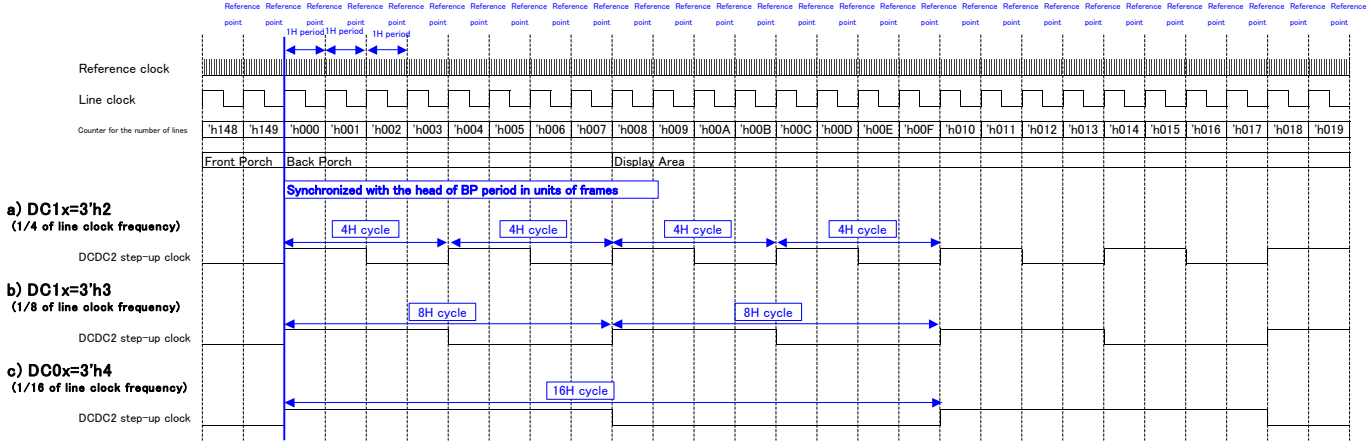
Example) DIVI=2'h1, RTNI=5'h11 (reference clock period = 1/2 of internal operation clock, 1H period = 17 clocks)



■DC1x Value and DCDC2 Step-up Clock Signal Waveform Example

DCDC2 performs charge operation and boost operation with the step-up clock generated from the timing generator.
The DCDC2 step-up clock frequency is adjusted by setting the division ratio of the reference clock frequency with DC1x register.
(To prevent flicker, the DCDC2 step-up clock signal is synchronized with the head of BP period in unit of frames.)

Example) BP=FP=8'h08, NL=7'h4F (front porch = back porch = 8 lines, the number of lines to drive the LCD = 320 lines)



Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRH [0]	0	0	0	VCM R	1	0	PSON	PON	VRH [4]	VRH [3]	VRH [2]	VRH [1]
Default value		0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1

VRH[4:0]: Sets the factor to generate VREG1OUT

Table 33

VRH[4:0]	VREG1OUT
5'h00	Halt (Hi-z)
5'h01-5'h0F	Setting inhibited
5'h10	VCIR × 1.600
5'h11	VCIR × 1.625
5'h12	VCIR × 1.650
5'h13	VCIR × 1.675
5'h14	VCIR × 1.700
5'h15	VCIR × 1.725
5'h16	VCIR × 1.750
5'h17	VCIR × 1.775
5'h18	VCIR × 1.800
5'h19	VCIR × 1.825
5'h1A	VCIR × 1.850
5'h1B	VCIR × 1.875
5'h1C	VCIR × 1.900
5'h1D	VCIR × 1.925
5'h1E	VCIR × 1.950
5'h1F	VCIR × 1.975

Note: Make sure that VREG1OUT ≤ (DDVDH-0.5)V in setting VC and VRH bits.

PON, PSON: Turns power supply on. Write PON and PSON to turn power supply on. Internal power supply operation starts. Follow the Power On sequences.

Table 34 Power supply sequences (PSON, PON)

PSON	PON	Operation
0	0	Power supply OFF sequence
0	1	Power supply OFF sequence
1	0	Power supply OFF sequence
1	1	Power supply ON sequence

VCMR: Select VCOMH voltage level from external resistance (VCOMR), internal electronic volumes VCM1 and VCM2.

Table 35

VCMR	VCOMH level
0	VCOMR
1 (Default)	Internal electronic volume

Note: Internal electronic volume is adjusted by VCM1 and VCM2 bits.

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VDV [4]	VDV [3]	VDV [2]	VDV [1]	VDV [0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0]: Set VCOM alternating amplitude in the range of VREG1OUTx0.70 to VREG1OUTx1.32.

Table 36 VDV Setting

VDV[4:0]	VCOM Amplitude
5'h0	VREG1OUT×0.70
5'h1	VREG1OUT×0.72
5'h2	VREG1OUT×0.74
5'h3	VREG1OUT×0.76
5'h4	VREG1OUT×0.78
5'h5	VREG1OUT×0.80
5'h6	VREG1OUT×0.82
5'h7	VREG1OUT×0.84
5'h8	VREG1OUT×0.86
5'h9	VREG1OUT×0.88
5'hA	VREG1OUT×0.90
5'hB	VREG1OUT×0.92
5'hC	VREG1OUT×0.94
5'hD	VREG1OUT×0.96
5'hE	VREG1OUT×0.98
5'hF	VREG1OUT×1.00

VDV[4:0]	VCOM Amplitude
5'h10	VREG1OUT×1.02
5'h11	VREG1OUT×1.04
5'h12	VREG1OUT×1.06
5'h13	VREG1OUT×1.08
5'h14	VREG1OUT×1.10
5'h15	VREG1OUT×1.12
5'h16	VREG1OUT×1.14
5'h17	VREG1OUT×1.16
5'h18	VREG1OUT×1.18
5'h19	VREG1OUT×1.20
5'h1A	VREG1OUT×1.22
5'h1B	VREG1OUT×1.24
5'h1C	VREG1OUT×1.26
5'h1D	VREG1OUT×1.28
5'h1E	VREG1OUT×1.30
5'h1F	VREG1OUT×1.32

Note: Set VDV[4:0] so that VCOM amplitude becomes 6.0V or smaller.

Frame Memory Access Control

Frame Memory Address Set (Horizontal Address) (R20h)
Frame Memory Address Set (Vertical Address) (R21h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R20	W	1	0	0	0	0	0	0	0	0	AD [7]	AD [6]	AD [5]	AD [4]	AD [3]	AD [2]	AD [1]	AD [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R21	W	1	0	0	0	0	0	0	0	AD [16]	AD [15]	AD [14]	AD [13]	AD [12]	AD [11]	AD [10]	AD [9]	AD [8]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0]: A frame memory address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the R61580 writes data to the internal frame memory so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal frame memory.

Notes: 1. In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.
2. In internal clock operation and VSYNC interface operation (RM = "0"), the address AD16-0 is set when executing the instruction.

Table 37 Frame Memory Address Setting Range

AD[16:0]	Frame Memory Data Setting
17'h00000 – 17'h000EF	Bitmap data on the 1st line
17'h00100 – 17'h001EF	Bitmap data on the 2nd line
17'h00200 – 17'h002EF	Bitmap data on the 3rd line
17'h00300 – 17'h003EF	Bitmap data on the 4th line
17'h00400 – 17'h004EF	Bitmap data on the 5th line
:	:
17'h13C00 – 17'h13CEF	Bitmap data on the 317th line
17'h13D00 – 17'h13DEF	Bitmap data on the 318th line
17'h13E00 – 17'h13EEF	Bitmap data on the 319th line
17'h13F00 – 17'h13FEF	Bitmap data on the 320th line

Frame Memory Data Write (R22h)

R/W	RS	
W	1	Frame memory write data WD[17:0] is transferred via different data bus in different interface operations.
RGB i/f operation		Frame memory write data WD[17:0] is transferred via different data bus in different interface operations.

WD[17:0]: The R61580 develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation.

The frame memory data represents the grayscale level. The R61580 automatically updates the address according to AM and I/D[1:0] settings as it writes data in the frame memory. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.

Note: When writing data in the frame memory via system interface while using the RGB interface, make sure that write operations via two interfaces do not conflict one another.

Frame Memory Data Read (R22h)

R/W	RS	
R	1	Frame memory read data RD[17:0] is transferred via different data bus in different interface operations.

RD[17:0]: 18-bit data read from the frame memory. Frame memory read data RD[17:0] is transferred via different data bus in different interface operation.

When the R61580 reads data from the frame memory to the host processor, the first word read immediately after frame memory address set is not outputted, so that it is invalid. Valid data is sent to the data bus when the R61580 reads out the second and subsequent words.

When either 8-bit or 16-bit interface is selected, the LSBs of R dot data and B dot data are not read out.

Note: This register is disabled in RGB interface operation.

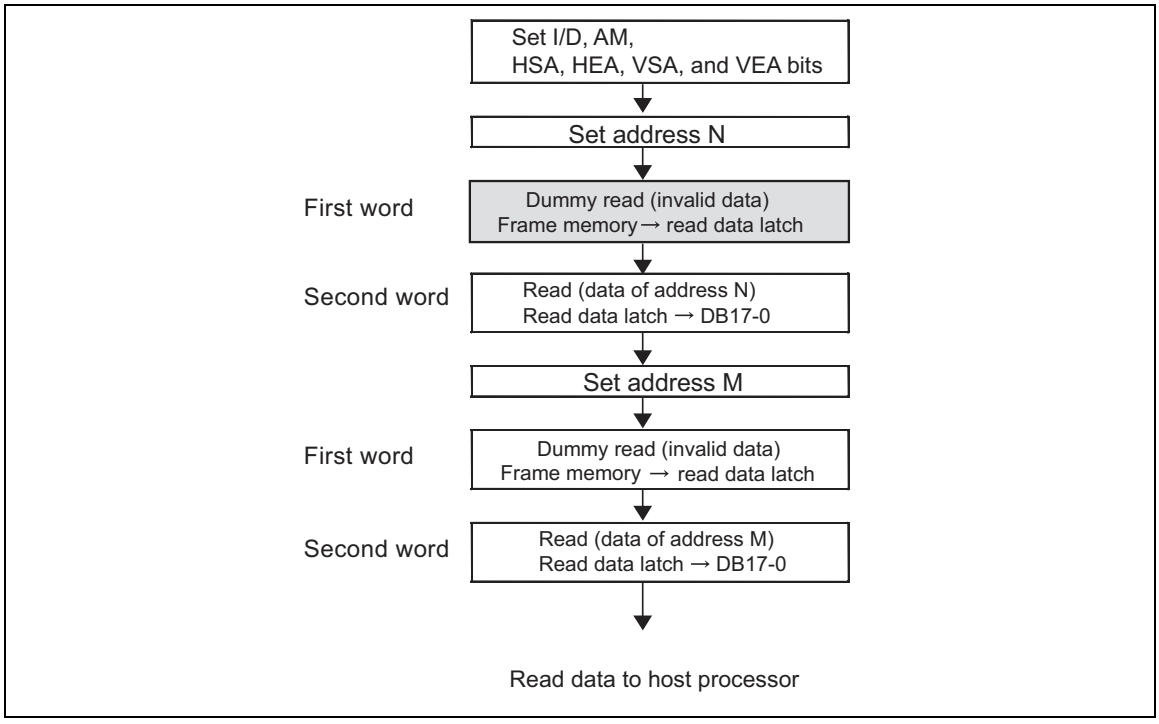


Figure 8 Frame Memory Read Sequence

NVM Control

NVM Data Read 1 (R28), NVM Data Read 2 (R29h), NVM Data Read 3 (R2Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R28	R/W	1	0	0	0	0	0	0	0	0	UID [7]	UID [6]	UID [5]	UID [4]	UID [3]	UID [2]	UID [1]	UID [0]
	Default		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R29	R/W	1	0	0	0	0	0	0	0	0	0	VCM1 [6]	VCM1 [5]	VCM1 [4]	VCM1 [3]	VCM1 [2]	VCM1 [1]	VCM1 [0]
	Default		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R2A	R/W	1	0	0	0	0	0	0	0	0	VCMSEL	VCM2 [6]	VCM2 [5]	VCM2 [4]	VCM2 [3]	VCM2 [2]	VCM2 [1]	VCM2 [0]
	Default		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

UID[7:0]: The data bits UID[7:0] are written to the designated address in NVM and the written data can be read out from NVM by instruction setting (CALB) to this register. UID[7:0] can be used to write and read user identification code in NVM.

The setting value in UID[7:0] bits is enabled when not reading out the setting value from NVM via CALB setting.

VCM1[6:0]: Selects the factor of VREG1OUT to generate VCOMH. When enabling the setting valued in VCM1[6:0], make sure to set VCMSEL = 1.

When using the data written in NVM for setting the VCOMH level, the data bits VCM1[6:0] are written to the designated address in NVM and the written data can be read out from NVM by instruction setting (CALB) to this register. When the data bits VCM2[6:0] are written in NVM before writing the data bits VCM1[6:0] to NVM, the VCM1[6:0] setting value written in NVM cannot be used for setting the VCOMH level.

VCM2[6:0]: Selects the factor of VREG1OUT to generate VCOMH. When enabling the setting valued in VCM2[6:0], make sure to set VCMSEL = 0. The function of VCM2[6:0] instruction is the same as that of VCM1[6:0].

Write the setting value in VCM2[6:0] bits and VCMSEL = 0 in the designated addresses of NVM, when reading out the setting value written in NVM for VCOMH level setting and the data is already written in the designated address of VCM1[6:0] in the NVM. The VCM2[6:0] data bits written in NVM can be read out via CALB setting for setting the VCOMH level.

Note: When R2A register is read after setting CALB=1 (RA4h), data in IB6-5, R2Ah, is not always 0 and different data may be read out from different die.

VCMSEL: When VCMSEL = 1, VCM1 is selected. When VCMSEL = 0, VCM2 is selected.

Table 38

VCM1[6:0] VCM2[6:0]	VCOMH			VCM1[6:0] VCM2[6:0]	VCOMH			VCM1[6:0] VCM2[6:0]	VCOMH		
7'h 00	VREG1OUT	X	0.492	7'h2B	VREG1OUT	X	0.664	7'h56	VREG1OUT	X	0.836
7'h 01	VREG1OUT	X	0.496	7'h2C	VREG1OUT	X	0.668	7'h57	VREG1OUT	X	0.840
7'h 02	VREG1OUT	X	0.500	7'h2D	VREG1OUT	X	0.672	7'h58	VREG1OUT	X	0.844
7'h03	VREG1OUT	X	0.504	7'h2E	VREG1OUT	X	0.676	7'h59	VREG1OUT	X	0.848
7'h04	VREG1OUT	X	0.508	7'h2F	VREG1OUT	X	0.680	7'h5A	VREG1OUT	X	0.852
7'h05	VREG1OUT	X	0.512	7'h30	VREG1OUT	X	0.684	7'h5B	VREG1OUT	X	0.856
7'h06	VREG1OUT	X	0.516	7'h31	VREG1OUT	X	0.688	7'h5C	VREG1OUT	X	0.860
7'h07	VREG1OUT	X	0.520	7'h32	VREG1OUT	X	0.692	7'h5D	VREG1OUT	X	0.864
7'h08	VREG1OUT	X	0.524	7'h33	VREG1OUT	X	0.696	7'h5E	VREG1OUT	X	0.868
7'h09	VREG1OUT	X	0.528	7'h34	VREG1OUT	X	0.700	7'h5F	VREG1OUT	X	0.872
7'h0A	VREG1OUT	X	0.532	7'h35	VREG1OUT	X	0.704	7'h60	VREG1OUT	X	0.876
7'h0B	VREG1OUT	X	0.536	7'h36	VREG1OUT	X	0.708	7'h61	VREG1OUT	X	0.880
7'h0C	VREG1OUT	X	0.540	7'h37	VREG1OUT	X	0.712	7'h62	VREG1OUT	X	0.884
7'h0D	VREG1OUT	X	0.544	7'h38	VREG1OUT	X	0.716	7'h63	VREG1OUT	X	0.888
7'h0E	VREG1OUT	X	0.548	7'h39	VREG1OUT	X	0.720	7'h64	VREG1OUT	X	0.892
7'h0F	VREG1OUT	X	0.552	7'h3A	VREG1OUT	X	0.724	7'h65	VREG1OUT	X	0.896
7'h10	VREG1OUT	X	0.556	7'h3B	VREG1OUT	X	0.728	7'h66	VREG1OUT	X	0.900
7'h11	VREG1OUT	X	0.560	7'h3C	VREG1OUT	X	0.732	7'h67	VREG1OUT	X	0.904
7'h12	VREG1OUT	X	0.564	7'h3D	VREG1OUT	X	0.736	7'h68	VREG1OUT	X	0.908
7'h13	VREG1OUT	X	0.568	7'h3E	VREG1OUT	X	0.740	7'h69	VREG1OUT	X	0.912
7'h14	VREG1OUT	X	0.572	7'h3F	VREG1OUT	X	0.744	7'h6A	VREG1OUT	X	0.916
7'h15	VREG1OUT	X	0.576	7'h40	VREG1OUT	X	0.748	7'h6B	VREG1OUT	X	0.920
7'h16	VREG1OUT	X	0.580	7'h41	VREG1OUT	X	0.752	7'h6C	VREG1OUT	X	0.924
7'h17	VREG1OUT	X	0.584	7'h42	VREG1OUT	X	0.756	7'h6D	VREG1OUT	X	0.928
7'h18	VREG1OUT	X	0.588	7'h43	VREG1OUT	X	0.760	7'h6E	VREG1OUT	X	0.932
7'h19	VREG1OUT	X	0.592	7'h44	VREG1OUT	X	0.764	7'h6F	VREG1OUT	X	0.936
7'h1A	VREG1OUT	X	0.596	7'h45	VREG1OUT	X	0.768	7'h70	VREG1OUT	X	0.940
7'h1B	VREG1OUT	X	0.600	7'h46	VREG1OUT	X	0.772	7'h71	VREG1OUT	X	0.944
7'h1C	VREG1OUT	X	0.604	7'h47	VREG1OUT	X	0.776	7'h72	VREG1OUT	X	0.948
7'h1D	VREG1OUT	X	0.608	7'h48	VREG1OUT	X	0.780	7'h73	VREG1OUT	X	0.952
7'h1E	VREG1OUT	X	0.612	7'h49	VREG1OUT	X	0.784	7'h74	VREG1OUT	X	0.956
7'h1F	VREG1OUT	X	0.616	7'h4A	VREG1OUT	X	0.788	7'h75	VREG1OUT	X	0.960
7'h20	VREG1OUT	X	0.620	7'h4B	VREG1OUT	X	0.792	7'h76	VREG1OUT	X	0.964
7'h21	VREG1OUT	X	0.624	7'h4C	VREG1OUT	X	0.796	7'h77	VREG1OUT	X	0.968
7'h22	VREG1OUT	X	0.628	7'h4D	VREG1OUT	X	0.800	7'h78	VREG1OUT	X	0.972
7'h23	VREG1OUT	X	0.632	7'h4E	VREG1OUT	X	0.804	7'h79	VREG1OUT	X	0.976
7'h24	VREG1OUT	X	0.636	7'h4F	VREG1OUT	X	0.808	7'h7A	VREG1OUT	X	0.980
7'h25	VREG1OUT	X	0.640	7'h50	VREG1OUT	X	0.812	7'h7B	VREG1OUT	X	0.984
7'h26	VREG1OUT	X	0.644	7'h51	VREG1OUT	X	0.816	7'h7C	VREG1OUT	X	0.988
7'h27	VREG1OUT	X	0.648	7'h52	VREG1OUT	X	0.820	7'h7D	VREG1OUT	X	0.992
7'h28	VREG1OUT	X	0.652	7'h53	VREG1OUT	X	0.824	7'h7E	VREG1OUT	X	0.996
7'h29	VREG1OUT	X	0.656	7'h54	VREG1OUT	X	0.828	7'h7F	VREG1OUT	X	1.000
7'h2A	VREG1OUT	X	0.660	7'h55	VREG1OUT	X	0.832				

γ Control

γ Control 1 ~ 10 (R30h ~ R39h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	PR0P01[4]	PR0P01[3]	PR0P01[2]	PR0P01[1]	PR0P01[0]	0	0	0	PR0P00[4]	PR0P00[3]	PR0P00[2]	PR0P00[1]	PR0P00[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31	W	1	PR0P04[3]	PR0P04[2]	PR0P04[1]	PR0P04[0]	PR0P03[3]	PR0P03[2]	PR0P03[1]	PR0P03[0]	0	0	0	PR0P02[4]	PR0P02[3]	PR0P02[2]	PR0P02[1]	PR0P02[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R32	W	1	0	0	0	PR0P06[4]	PR0P06[3]	PR0P06[2]	PR0P06[1]	PR0P06[0]	0	0	0	0	PR0P05[3]	PR0P05[2]	PR0P05[1]	PR0P05[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R33	W	1	0	0	0	PR0P08[4]	PR0P08[3]	PR0P08[2]	PR0P08[1]	PR0P08[0]	0	0	0	PR0P07[4]	PR0P07[3]	PR0P07[2]	PR0P07[1]	PR0P07[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R34	W	1	0	0	PI0P3[1]	PI0P3[0]	0	0	PI0P2[1]	PI0P2[0]	0	0	PI0P1[1]	PI0P1[0]	0	0	PI0P0[1]	PI0P0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R35	W	1	0	0	0	PR0N01[4]	PR0N01[3]	PR0N01[2]	PR0N01[1]	PR0N01[0]	0	0	0	PR0N00[4]	PR0N00[3]	PR0N00[2]	PR0N00[1]	PR0N00[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R36	W	1	PR0N04[3]	PR0N04[2]	PR0N04[1]	PR0N040]	PR0N03[3]	PR0N03[2]	PR0N03[1]	PR0N03[0]	0	0	0	PR0N02[4]	PR0N02[3]	PR0N02[2]	PR0N02[1]	PR0N02[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R37	W	1	0	0	0	PR0N06[4]	PR0N06[3]	PR0N06[2]	PR0N06[1]	PR0N06[0]	0	0	0	0	PR0N05[3]	PR0N05[2]	PR0N05[1]	PR0N05[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R38	W	1	0	0	0	PR0N08[4]	PR0N08[3]	PR0N08[2]	PR0N08[1]	PR0N08[0]	0	0	0	PR0N07[4]	PR0N07[3]	PR0N07[2]	PR0N07[1]	PR0N07[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R39	W	1	0	0	PI0N3[1]	PI0N3[0]	0	0	PI0N2[1]	PI0N2[0]	0	0	PI0N1[1]	PI0N1[0]	0	0	PI0N0[1]	PI0N0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PR0P00[4:0] R0 reference level adjustment register for positive polarity

PR0N00[4:0] R0 reference level adjustment register for negative polarity

PR0P01[4:0] R1 reference level adjustment register for positive polarity

PR0N01[4:0] R1 reference level adjustment register for negative polarity

PR0P02[4:0]	R2 reference level adjustment register for positive polarity
PR0N02[4:0]	R2 reference level adjustment register for negative polarity
PR0P03[3:0]	R3 reference level adjustment register for positive polarity
PR0N03[3:0]	R3 reference level adjustment register for negative polarity
PR0P04[3:0]	R4 reference level adjustment register for positive polarity
PR0N04[3:0]	R4 reference level adjustment register for negative polarity
PR0P05[3:0]	R5 reference level adjustment register for positive polarity
PR0N05[3:0]	R5 reference level adjustment register for negative polarity
PR0P06[4:0]	R6 reference level adjustment register for positive polarity
PR0N06[4:0]	R6 reference level adjustment register for negative polarity
PR0P07[4:0]	R7 reference level adjustment register for positive polarity
PR0N07[4:0]	R7 reference level adjustment register for negative polarity
PR0P08[4:0]	R8 reference level adjustment register for positive polarity
PR0N08[4:0]	R8 reference level adjustment register for negative polarity
PI0P0~1[1:0]	Interpolation adjustment register for positive polarity (V2~V7)
PI0N0~1[1:0]	Interpolation adjustment register for negative polarity (V2~V7)
PI0P2~3[1:0]	Interpolation adjustment register for positive polarity (V56~61)
PI0N2~3[1:0]	Interpolation adjustment register for negative polarity (V56~V61)

Window Address Control

Window Horizontal Frame Memory Address (Start Address) (R50h),
Window Horizontal Frame Memory Address (End Address) (R51h),
Window Vertical Frame Memory Address (Start Address) (R52h),
Window Vertical Frame Memory Address (End Address) (R53h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R50	W	1	0	0	0	0	0	0	0	0	HSA [7]	HSA [6]	HSA [5]	HSA [4]	HSA [3]	HSA [2]	HSA [1]	HSA [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51	W	1	0	0	0	0	0	0	0	0	HEA [7]	HEA [6]	HEA [5]	HEA [4]	HEA [3]	HEA [2]	HEA [1]	HEA [0]
	Default		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R52	W	1	0	0	0	0	0	0	0	VSA [8]	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53	W	1	0	0	0	0	0	0	0	VEA [8]	VEA [7]	VEA [6]	VEA [5]	VEA [4]	VEA [3]	VEA [2]	VEA [1]	VEA [0]
	Default		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting frame memory write operation.

In setting, make sure that 8'h00 ≤ HSA < HEA ≤ 8'hEF and 8'h04 ≤ HEA – HSA.

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting frame memory write operation.

In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h13F.

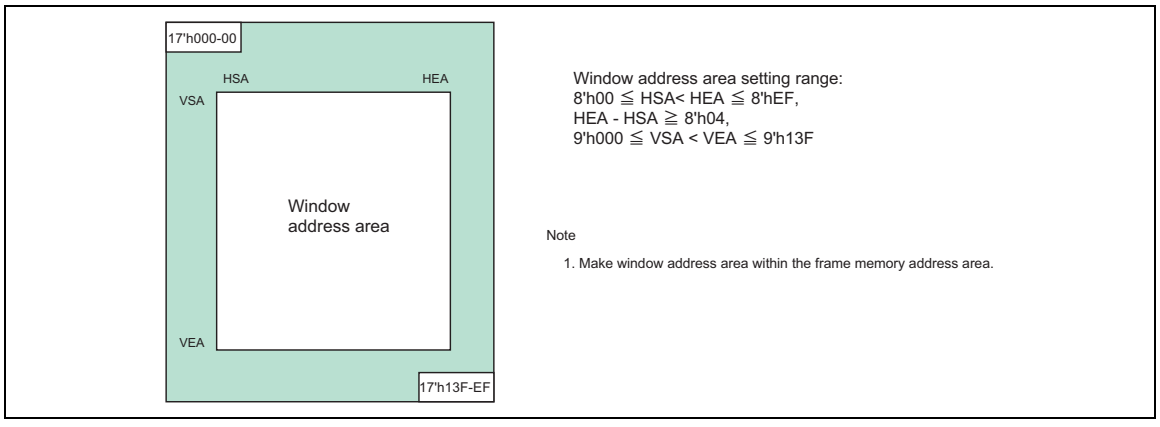


Figure 9 Frame Memory Address Map and Window Address Area

Base Image Display Control

Driver Output Control (R60h)

Base Image Display Control (R61h)

Vertical Scroll Control (R6Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R60	W	1	GS	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	0	0	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]
	Default		0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
R 61	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 6A	W	1	0	0	0	0	0	0	0	VL [8]	VL [7]	VL [6]	VL [5]	VL [4]	VL [3]	VL [2]	VL [1]	VL [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The frame memory address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 39

NL[5:0]	Number of drive lines
6'h00-6'h1C	Setting inhibited
6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 lines
6'h27	320 lines
6'h28-6'h3F	Setting inhibited

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the R61580 to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

Table 40 Frame Memory Data Grayscale Level Inversion

REV	Frame Memory Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the R61580 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

Table 41

VLE	Base image
0	Fixed
1	Enable scrolling

NDL: Sets the source output level in non-lit display area. NDL bit can keep the non-display area lit on.

Table 42

NDL	Non-display area	
	Positive	Negative
0	V63	V0
1	V0	V63

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0]. Make sure VL[8:0] ≤ 320.

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

Table 43

SCN[5:0]	Gate Line No (Scan start position)			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G1	G(N)	G1	G(2N－320)
6'h01	G9	G(N+8)	G16	G(2N－304)
6'h02	G17	G(N+16)	G33	G(2N－288)
6'h03	G25	G(N+24)	G49	G(2N－272)
6'h04	G33	G(N+32)	G65	G(2N－256)
6'h05	G41	G(N+40)	G81	G(2N－240)
6'h06	G49	G(N+48)	G97	G(2N－224)
6'h07	G57	G(N+56)	G113	G(2N－208)
6'h08	G65	G(N+64)	G129	G(2N－192)
6'h09	G73	G(N+72)	G145	G(2N－176)
6'h0A	G81	G(N+80)	G161	G(2N－160)
6'h0B-6'h2F	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

Note: N means the number of lines set by register.

When setting the SCN bit, make sure to satisfy the restriction below:

Table 44

SM	GS	Restriction
0	0	(Scan start position-1) + (Number of line (NL bit)) ≤ 320
0	1	Scan start position ≤ 320
1	0	(Scan start position -1)/2 + (Number of line (NL bit)) ≤ 320
1	1	Scan start position ≤ 320

Partial Display Control

Partial Image Display Position (R80h)

Partial Image Frame Memory Address (Start Line Address) (R81h)

Partial Image Frame Memory Address (End Line Address) (R82h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R80	W	1	0	0	0	0	0	0	0	PTDP [8]	PTDP [7]	PTDP [6]	PTDP [5]	PTDP [4]	PTDP [3]	PTDP [2]	PTDP [1]	PTDP [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R81	W	1	0	0	0	0	0	0	0	PTSA [8]	PTSA [7]	PTSA [6]	PTSA [5]	PTSA [4]	PTSA [3]	PTSA [2]	PTSA [1]	PTSA [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R82	W	1	0	0	0	0	0	0	0	PTE A[8]	PTE A[7]	PTE A[6]	PTE A[5]	PTE A[4]	PTE A[3]	PTE A[2]	PTE A[1]	PTE A[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP[8:0]: Sets the display position of partial image.

If PTDP0 = “9’h000”, the partial image is displayed from the first line of the base image.

PTSA[8:0], PTEA[8:0]: Sets the start line and end line addresses of the frame memory area, respectively for the partial image. In setting, make sure that PTSA ≤ PTEA.

Panel Interface Control

Panel Interface Control 1(R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI [1]	DIVI [0]	0	0	0	RTNI [4]	RTNI [3]	RTNI [2]	RTNI [1]	RTNI [0]
Default value		0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the R61580's display operation is synchronized with internal clock.

Table 45 Clocks per Line (Internal Clock Operation: 1 clock = 1 OSC)

RTNI[4:0]	Clocks per Line 1 clock = 1OSC
5'h00-5'h10	Setting inhibited
5'h11	17 clocks
5'h12	18 clocks
5'h13	19 clocks
5'h14	20 clocks
5'h15	21 clocks
5'h16	22 clocks
5'h17	23 clocks
5'h18	24 clocks
5'h19	25 clocks
5'h1A	26 clocks
5'h1B	27 clocks
5'h1C	28 clocks
5'h1D	29 clocks
5'h1E	30 clocks
5'h1F	31 clocks

Note: RTNI bit must be set at the "Initial instruction setting" stage when Power Supply ON and Deep Standby Exit Sequences are performed.

DIVI[1:0]: Sets the division ratio of the internal clock frequency. The R61580's internal operation is synchronized with the frequency divided internal clock. When DIVI[1:0] setting is changed, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see "Frame-Frequency Adjustment Function".

DIVI[1:0] is disabled in RGB interface operation. Setting DIVI ≠2'h0 is inhibited.

Table 46 Division Ratio of the Internal Clock

DIVI[1:0]	Division Ratio
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Note: RTNI bit must be set at the "Initial instruction setting" stage when Power Supply ON and Deep Standby Exit Sequences are performed.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{fosc}{\text{Clocks per line x division ratio x (line + BP + FP)}} \quad [Hz]$$

fosc : Internal oscillation frequency
Line: Number of lines to drive the LCD (NL bits)
Division ratio: DIVI
Clocks per line: RTNI

Panel Interface Control 1-1 (R91h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	SPCWI [3]	SPCWI [2]	SPCWI [1]	SPCWI [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SPCWI [3:0]: The bit is used to set source VCI pre-charge period. Pre-charge period is set by SPCWI[3:0] starting from the source output alternating position defined by SDTI[2:0]. This bit is disabled when RGB interface is selected.

Table 47

SPCWI [3:0]	Source VCI pre-charge period
4'h0	0 clocks
4'h1	1 clock
4'h2	2 clocks
4'h3	3 clocks
4'h4	4 clocks
4'h5	5 clocks
4'h6	6 clocks
4'h7	7 clocks
4'h8	8 clocks
4'h9	9 clocks
4'hA	10 clocks
4'hB	11 clocks
4'hC	12 clocks
4'hD	13 clocks
4'hE	14 clocks
4'hF	15 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVI (R90h).

Panel Interface Control 2(R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation synchronizing with the internal clock.

Table 48

NOWI[2:0]	Non-overlap period	NOWI[2:0]	Non-overlap period
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The internal clock is the frequency divided clock, which is set by DIVI (R90h) bits.

Panel Interface Control 3(R93h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	VEQWI [2]	VEQWI [1]	VEQWI [0]	0	0	0	0	0	MCPI[2]	MCPI[1]	MCPI[0]
Default value		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

VEQWI [2:0]: Sets VCOM equalize period. Equalizing operation continues for the period defined by VEQWI bit starting from the VCOM alternating position defined by MCPI [2:0]. VEQWI setting is enabled when VEM[1:0]=1 or larger (R0Eh) and display operation of the R61580 is synchronized with internal clock.

VEQWI is disabled when RGB interface is selected.

Table 49

VEQWI[2:0]	VCOM equalize period
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: DIVI (R90h) sets division ratio of clock frequency.

MCPI[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled display operation of the R61580 is synchronized with internal clock.

MCPI is disabled when RGN interface is selected.

Table 50

MCPI[2:0]	Source output position	MCPI[2:0]	Source output position
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: DIVI (R90h) sets division ratio of clock frequency.

Panel Interface Control 4 (R94h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI[2]	SDTI[1]	SDTI[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SDTI[2:0]: Defines source output alternating position within 1H period.

SDTI is disabled when RGB interface is selected.

Table 51

SDTI[2:0]	Source output alternating position
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: DIVI (R90h) sets division ratio of clock frequency.

Panel Interface Control 5 (R95h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE [1]	DIVE [0]	0	0	RTN E[5]	RTN E[4]	RTN E[3]	RTN E[2]	RTN E[1]	RTN E[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

RTNE[5:0]: Sets RTNE[5:0] and DIVE[1:0] bits so that the number of DOTCLK calculated from the following formula becomes the number of DOTCLK which should be inputted in 1H period. The RTNE[5:0] setting is enabled in display operation via RGB interface.

(PCDIVH + PCDIVL) x DIVE[1:0] (division ratio) x RTNE[5:0] (Number of DOTCLK) ≤ Number of DOTCLK in 1H period

DIVE[1:0]: Sets the division ratio of DOTCLK frequency. The R61580's internal operation is synchronized with the frequency divided DOTCLK. The setting in DIVE[1:0] is enabled in RGB interface operation.

Table 52 Division Ratio of DOTCLK

DIVE[1:0]	Division Ratio
2'h0	Setting disabled
2'h1	1/4
2'h2	1/8
2'h3	1/16

Internal clock frequency is calculated by below formula:

DOTCLK / (DIVE x (PCDIVL + PCDIVH))

See also R9Ch.

Table 53 DOTCLK per Line (1H Period)

RTNE[5:0]	DOTCLK per line (1H)	RTNE[5:0]	DOTCLK per line (1H)
6'h00	Setting disabled	6'h20	32 clocks
6'h01	Setting disabled	6'h21	33 clocks
6'h02	Setting disabled	6'h22	34 clocks
6'h03	Setting disabled	6'h23	35 clocks
6'h04	Setting disabled	6'h24	36 clocks
6'h05	Setting disabled	6'h25	37 clocks
6'h06	Setting disabled	6'h26	38 clocks
6'h07	Setting disabled	6'h27	39 clocks
6'h08	Setting disabled	6'h28	40 clocks
6'h09	Setting disabled	6'h29	41 clocks
6'h0A	Setting disabled	6'h2A	42 clocks
6'h0B	Setting disabled	6'h2B	43 clocks
6'h0C	Setting disabled	6'h2C	44 clocks
6'h0D	Setting disabled	6'h2D	45 clocks
6'h0E	Setting disabled	6'h2E	46 clocks
6'h0F	Setting disabled	6'h2F	47 clocks
6'h10	Setting disabled	6'h30	48 clocks
6'h11	Setting disabled	6'h31	49 clocks
6'h12	Setting disabled	6'h32	50 clocks
6'h13	Setting disabled	6'h33	51 clocks
6'h14	Setting disabled	6'h34	52 clocks
6'h15	21 clocks	6'h35	53 clocks
6'h16	22 clocks	6'h36	54 clocks
6'h17	23 clocks	6'h37	55 clocks
6'h18	24 clocks	6'h38	56 clocks
6'h19	25 clocks	6'h39	57 clocks
6'h1A	26 clocks	6'h3A	58 clocks
6'h1B	27 clocks	6'h3B	59 clocks
6'h1C	28 clocks	6'h3C	60 clocks
6'h1D	29 clocks	6'h3D	61 clocks
6'h1E	30 clocks	6'h3E	62 clocks
6'h1F	31 clocks	6'h3F	63 clocks

Panel Interface Control 5-1 (R96h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	SPCWE [3]	SPCWE [2]	SPCWE [1]	SPCWE [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SPCWE [3:0]: The bit is used to set source VCI pre-charge period. Pre-charge period is set by SPCWE[3:0] starting from the source output alternating position defined by SDTE[2:0]. This bit is enabled when RGB interface is selected.

Table 54

SPCWE [3:0]	Source VCI pre-charge period
4'h0	0 clocks
4'h1	1 clock
4'h2	2 clocks
4'h3	3 clocks
4'h4	4 clocks
4'h5	5 clocks
4'h6	6 clocks
4'h7	7 clocks
4'h8	8 clocks
4'h9	9 clocks
4'hA	10 clocks
4'hB	11 clocks
4'hC	12 clocks
4'hD	13 clocks
4'hE	14 clocks
4'hF	15 clocks

Panel Interface Control 6 (R97h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

NOWE[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

Table 55

NOWE [2:0]	Non-overlap period
3'h0	Setting disabled
3'h1	1
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK].

Panel Interface Control 7 (R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	VEQWE [2]	VEQWE [1]	VEQWE [0]	0	0	0	0	0	MCPE [2]	MCPE [1]	MCPE [0]
Default value		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

VEQWE [2:0]: VEQWE sets VCOM equalize period. Equalizing operation continues for the period defined by VEQWE bit starting from the VCOM alternating position defined by MCPE [2:0]. VEQWE setting is enabled when VEM[1:0]=1 or larger (R0Eh).

Table 56

VEQWE[2:0]	VCOM equalize period
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

MCPE[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled in display operation via RGB interface.

Table 57

MCPE[2:0]	Source output position	MCPE[2:0]	Source output position
3'h0	Setting Disabled	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK].

Panel Interface Control 8 (R99h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE[2]	SDTE[1]	SDTE[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SDTE[2:0]: Defines source output alternating position within 1H period.

SDTE is enabled when RGB interface is selected.

Table 58

SDTE[2:0]	Source output alternating position
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK]

Panel Interface Control 9 (R9Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	PCDIVH [2]	PCDIVH [1]	PCDIVH [0]	0	PCDIVL [2]	PCDIVL [1]	PCDIVL [0]
Default		0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

PCDIVH[2:0], PCDIVL[2:0]:

When DM [1:0] =2'h1 and RGB I/F is selected, internal clock used for display operation switches from internal oscillation to DOTCLKD. PCDIVH and PCDIVL bits define division ratio of DOTCLKD to DOTCLK.

PCDIVH defines number of DOTCLK during DOTCLKD is high in the units of 1 clock.

PCDIVL defines number of DOTCLK during DOTCLKD is low in the units of 1 clock.

Make sure that PCDIVL＝PCDIVH or PCDIVH-1.

Also, write PCDIVH and PCDIVL values so that DOTCLKD frequency is the closest to internal oscillation clock frequency 678KHz.

See "Setting Example of Display Control Clock in RGB Interface Operation" for details.

Table 59

PCDIVH[2:0] PCDIVL[2:0]	
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

NVM Control

NVM Control 1 (RA0h), NVM Control 2 (RA1h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R A0	R/W	1	0	0	0	0	0	0	0	0	TE	0	EOP [1]	EOP [0]	0	0	0	NV AD
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R A1	R/W	1	NV DAT [15]	NV DAT [14]	NV DAT [13]	NV DAT [12]	NV DAT [11]	NV DAT [10]	NV DAT [9]	NV DAT [8]	NV DAT [7]	NV DAT [6]	NV DAT [5]	NV DAT [4]	NV DAT [3]	NV DAT [2]	NV DAT [1]	NV DAT [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TE: Enables access to the NVM when TE=1.

EOP [1:0]: Internal NVM control bits to control write and erase operations.

Table 60

EOP[1:0]	NVM control
2'h0	Halt
2'h1	Write
2'h2	Setting disabled
2'h3	Erase

NVAD: Specifies address to access on the NVM for write and erase operation. An address consists of 16 bits. To write to the NVM, write the data that users wish to write in NVDAT (RA1h) and write EOP=2'h1 to enable the write operation. To erase, define the address users wish to erase data from and write EOP=2'h3 to enable the erase operation. See "NVM Control Sequence" for details.

Table 61

NVAD	NVDAT [15]/[7]	NVDAT [14]/[6]	NVDAT [13]/[5]	NVDAT [12]/[4]	NVDAT [11]/[3]	NVDAT [10]/[2]	NVDAT [9]/[1]	NVDAT [8]/[0]
1'h0 (MS byte)	VCMSEL	VCM2 [6]	VCM2 [5]	VCM2 [4]	VCM2 [3]	VCM2 [2]	VCM2 [1]	VCM2 [0]
1'h0 (LS byte)	1	VCM1 [6]	VCM1 [5]	VCM1 [4]	VCM1 [3]	VCM1 [2]	VCM1 [1]	VCM1 [0]
1'h1 (MS byte)	1	1	1	1	1	1	1	1
1'h1 (LS byte)	UID1 [7]	UID1 [6]	UID1 [5]	UID1 [4]	UID1 [3]	UID1 [2]	UID1 [1]	UID1 [0]

MS byte =NVDAT [15:8]. LS byte=NVDAT [7:0].

VCM1[6:0]: Defines factor to adjust VCOMH level when VCMSEL=1.

VCM2[6:0]: Defines factor to adjust VCOMH level when VCMSEL=0.

UID1[7:0]: User ID.

NVM Control 3 (RA3h)

	R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RA3	R	1	0	0	0	0	0	0	0	0	0	0	VERI FLGE R	VERI FLGW R	RTY RTL [3]	RTY RTL [2]	RTY RTL [1]	RTY RTL [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VERIFLGER: Before data is written to NVM, a verify operation is automatically performed by erasing data from the specified address. For details, see “NVM Write Sequence” and “NVM Erase Sequence”. If the verify operation after the erase operation passes, VERIFLGER is set to “1”. If it fails, VERIFLGER remains “0”.

VERIFLGWR: After data is written to NVM, a verify operation is automatically performed. For details, see “NVM Write Sequence” in “NVM Control Sequence”. If the verify operation after the write operation passes, VERIFLGWR is set to “1”. If is fails, VERIFLGWR remains “0”.

RTYRTL[3:0]: After writing data to NVM, this bit can be used to read how many times verify was executed during internal sequence. See NVM Write Sequence and NVM Erase Sequence for detail.

NVM Control 4 (RA4h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R A4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALB: When CALB=1, all data in NVM is read out and written to internal registers. When finished, CALB is set to 0.

Back Light Control

Back Light Control 1 (RC0h ~ RD3h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RC0	R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BLCM	BLCON
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RC1	R/W	1	0	0	0	0	0	0	0	0	0	0	0	THREW0[4]	THREW0[3]	THREW0[2]	THREW0[1]	THREW0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RC2	R/W	1	0	0	0	0	0	0	0	0	0	0	0	THREW1[4]	THREW1[3]	THREW1[2]	THREW1[1]	THREW1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RC3	R/W	1	0	0	0	0	0	0	0	0	0	0	ULMTW0[5]	ULMTW0[4]	ULMTW0[3]	ULMTW0[2]	ULMTW0[1]	ULMTW0[0]
	Default		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
RC4	R/W	1	0	0	0	0	0	0	0	0	0	0	ULMTW1[5]	ULMTW1[4]	ULMTW1[3]	ULMTW1[2]	ULMTW1[1]	ULMTW1[0]
	Default		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
RC5	R/W	1	0	0	0	0	0	0	0	0	0	0	LLMTW0[5]	LLMTW0[4]	LLMTW0[3]	LLMTW0[2]	LLMTW0[1]	LLMTW0[0]
	Default		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
RC6	R/W	1	0	0	0	0	0	0	0	0	0	0	LLMTW1[5]	LLMTW1[4]	LLMTW1[3]	LLMTW1[2]	LLMTW1[1]	LLMTW1[0]
	Default		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
RC7	R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	PITCHW[3]	PITCHW[2]	PITCHW[1]	PITCHW[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RC8	R/W	1	0	0	0	0	0	0	0	0	0	0	0	CGAPW[4]	CGAPW[3]	CGAPW[2]	CGAPW[1]	CGAPW[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
RC9	R/W	1	0	0	0	0	0	0	0	0	0	0	0	COEFK0[4]	COEFK0[3]	COEFK0[2]	COEFK0[1]	COEFK0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
RCA	R/W	1	0	0	0	0	0	0	0	0	0	0	0	COEFK1[4]	COEFK1[3]	COEFK1[2]	COEFK1[1]	COEFK1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
RCB	R/W	1	0	0	0	0	0	0	0	0	TBLMIN[7]	TBLMIN[6]	TBLMIN[5]	TBLMIN[4]	TBLMIN[3]	TBLMIN[2]	TBLMIN[1]	TBLMIN[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RC8	R/W	1	0	0	0	0	0	0	0	0	0	0	0	CGAPW[4]	CGAPW[3]	CGAPW[2]	CGAPW[1]	CGAPW[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
RC9	R/W	1	0	0	0	0	0	0	0	0	0	0	0	COEFK0[4]	COEFK0[3]	COEFK0[2]	COEFK0[1]	COEFK0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
RCA	R/W	1	0	0	0	0	0	0	0	0	0	0	0	COEFK1[4]	COEFK1[3]	COEFK1[2]	COEFK1[1]	COEFK1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
RCB	R/W	1	0	0	0	0	0	0	0	0	TBLMIN[7]	TBLMIN[6]	TBLMIN[5]	TBLMIN[4]	TBLMIN[3]	TBLMIN[2]	TBLMIN[1]	TBLMIN[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RCC	R/W	1	0	0	0	0	0	0	0	0	TBL0[7]	TBL0[6]	TBL0[5]	TBL0[4]	TBL0[3]	TBL0[2]	TBL0[1]	TBL0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RCD	R/W	1	0	0	0	0	0	0	0	0	TBL1[7]	TBL1[6]	TBL1[5]	TBL1[4]	TBL1[3]	TBL1[2]	TBL1[1]	TBL1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
RCE	R/W	1	0	0	0	0	0	0	0	0	TBL2[7]	TBL2[6]	TBL2[5]	TBL2[4]	TBL2[3]	TBL2[2]	TBL2[1]	TBL2[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
RCF	R/W	1	0	0	0	0	0	0	0	0	TBL3[7]	TBL3[6]	TBL3[5]	TBL3[4]	TBL3[3]	TBL3[2]	TBL3[1]	TBL3[0]
	Default		0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1
RD0	R/W	1	0	0	0	0	0	0	0	0	TBL4[7]	TBL4[6]	TBL4[5]	TBL4[4]	TBL4[3]	TBL4[2]	TBL4[1]	TBL4[0]
	Default		0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0
RD1	R/W	1	0	0	0	0	0	0	0	0	TBL5[7]	TBL5[6]	TBL5[5]	TBL5[4]	TBL5[3]	TBL5[2]	TBL5[1]	TBL5[0]
	Default		0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1
RD2	R/W	1	0	0	0	0	0	0	0	0	TBL6[7]	TBL6[6]	TBL6[5]	TBL6[4]	TBL6[3]	TBL6[2]	TBL6[1]	TBL6[0]
	Default		0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0
RD3	R/W	1	0	0	0	0	0	0	0	0	TBL7[7]	TBL7[6]	TBL7[5]	TBL7[4]	TBL7[3]	TBL7[2]	TBL7[1]	TBL7[0]
	Default		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

BLCM: The bit is used to select BLC mode. There are two sets of bits for each of THREW, ULMTW, LLMTW, COEFK and LNCOM registers, enabling different settings for different display images.

Table 62

BLCM	BLC mode	Enabled registers			
0	Mode 0	THREW0[4:0]	ULMTW0[5:0]	LLMTW0[5:0]	COEFK0[4:0]
1	Mode 1	THREW1[4:0]	ULMTW1[5:0]	LLMTW1[5:0]	COEFK1[4:0]

BLCON: The bit is used to turn the BLC function ON/OFF.

BLCON	**BLC function**
0	OFF
1	ON

The BLC function is disabled when COL=1 (8-color mode). To use BLC function (BLCON = 1), make sure that COL=0 and REV=0.

THREW0[4:0], THREW1[4:0]:

The bits are used to specify percentage from the threshold to grayscale number 63 in the total of grayscale data. This is the ratio (percentage) of the maximum number of pixels that makes display image white (= data “63”) to the total of pixels by image processing.

Percentage of pixels =

Number of pixels with the grayscale from the threshold to grayscale No. 63/ Number of all pixels

THREW0 is enabled when BLCM=0.
THREW1 is enabled when BLCM=1.

Table 63

THREW0[4:0] THREW1[4:0]	Percentage of pixels	THREW0[4:0] THREW1[4:0]	Percentage of pixels
5’h00	0%	5’h10	32%
5’h01	2%	5’h11	34%
5’h02	4%	5’h12	36%
5’h03	6%	5’h13	38%
5’h04	8%	5’h14	40%
5’h05	10%	5’h15	42%
5’h06	12%	5’h16	44%
5’h07	14%	5’h17	46%
5’h08	16%	5’h18	48%
5’h09	18%	5’h19	50%
5’h0A	20%	5’h1A	52%
5’h0B	22%	5’h1B	54%
5’h0C	24%	5’h1C	56%
5’h0D	26%	5’h1D	58%
5’h0E	28%	5’h1E	60%
5’h0F	30%	5’h1F	62%

ULMTW0[5:0], ULMTW1[5:0]:

The possible maximum value of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale.

ULMTW0 is enabled when BLCM=0.
ULMTW1 is enabled when BLCM=1.

Table 64

ULMTW0[5:0] ULMTW1[5:0]	Maximum greyscale (Frame memory Data)	ULMTW0[5:0] ULMTW1[5:0]	Maximum greyscale (Frame memory Data)
6'h00	6'h00	6'h20	6'h20
6'h01	6'h01	6'h21	6'h21
6'h02	6'h02	6'h22	6'h22
6'h03	6'h03	6'h23	6'h23
6'h04	6'h04	6'h24	6'h24
6'h05	6'h05	6'h25	6'h25
6'h06	6'h06	6'h26	6'h26
6'h07	6'h07	6'h27	6'h27
6'h08	6'h08	6'h28	6'h28
6'h09	6'h09	6'h29	6'h29
6'h0A	6'h0A	6'h2A	6'h2A
6'h0B	6'h0B	6'h2B	6'h2B
6'h0C	6'h0C	6'h2C	6'h2C
6'h0D	6'h0D	6'h2D	6'h2D
6'h0E	6'h0E	6'h2E	6'h2E
6'h0F	6'h0F	6'h2F	6'h2F
6'h10	6'h10	6'h30	6'h30
6'h11	6'h11	6'h31	6'h31
6'h12	6'h12	6'h32	6'h32
6'h13	6'h13	6'h33	6'h33
6'h14	6'h14	6'h34	6'h34
6'h15	6'h15	6'h35	6'h35
6'h16	6'h16	6'h36	6'h36
6'h17	6'h17	6'h37	6'h37
6'h18	6'h18	6'h38	6'h38
6'h19	6'h19	6'h39	6'h39
6'h1A	6'h1A	6'h3A	6'h3A
6'h1B	6'h1B	6'h3B	6'h3B
6'h1C	6'h1C	6'h3C	6'h3C
6'h1D	6'h1D	6'h3D	6'h3D
6'h1E	6'h1E	6'h3E	6'h3E
6'h1F	6'h1F	6'h3F	6'h3F

LLMTW0[4:0], LLMTW1[4:0]

The possible minimum value of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale.

LLMTW0 is enabled when BLCM=0.
LLMTW1 is enabled when BLCM=1.

Table 65

LLMTW0[5:0] LLMTW1[5:0]	**Minimum greyscale (Frame memory Data)**
6'h00	6'h00
6'h01	6'h01
6'h02	6'h02
6'h03	6'h03
6'h04	6'h04
6'h05	6'h05
6'h06	6'h06
6'h07	6'h07
6'h08	6'h08
6'h09	6'h09
6'h0A	6'h0A
6'h0B	6'h0B
6'h0C	6'h0C
6'h0D	6'h0D
6'h0E	6'h0E
6'h0F	6'h0F
6'h10	6'h10
6'h11	6'h11
6'h12	6'h12
6'h13	6'h13
6'h14	6'h14
6'h15	6'h15
6'h16	6'h16
6'h17	6'h17
6'h18	6'h18
6'h19	6'h19
6'h1A	6'h1A
6'h1B	6'h1B
6'h1C	6'h1C
6'h1D	6'h1D
6'h1E	6'h1E
6'h1F	6'h1F

LLMTW0[5:0] LLMTW1[5:0]	**Minimum greyscale (Frame memory Data)**
6'h20	6'h20
6'h21	6'h21
6'h22	6'h22
6'h23	6'h23
6'h24	6'h24
6'h25	6'h25
6'h26	6'h26
6'h27	6'h27
6'h28	6'h28
6'h29	6'h29
6'h2A	6'h2A
6'h2B	6'h2B
6'h2C	6'h2C
6'h2D	6'h2D
6'h2E	6'h2E
6'h2F	6'h2F
6'h30	6'h30
6'h31	6'h31
6'h32	6'h32
6'h33	6'h33
6'h34	6'h34
6'h35	6'h35
6'h36	6'h36
6'h37	6'h37
6'h38	6'h38
6'h39	6'h39
6'h3A	6'h3A
6'h3B	6'h3B
6'h3C	6'h3C
6'h3D	6'h3D
6'h3E	6'h3E
6'h3F	6'h3F

PITCHW[3:0]

This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one eighth of the grayscale.

Table 66

PITCHW[3:0]	Amount of change (grayscale)
4'h0	Setting inhibited
4'h1	1/8 of grayscale
4'h2	1/4 of grayscale
4'h3	3/8 of grayscale
4'h4	1/2 of grayscale
4'h5	5/8 of grayscale
4'h6	3/4 of grayscale
4'h7	7/8 of grayscale
4'h8	1 grayscale
4'h9	9/8 of grayscale
4'hA	5/4 of grayscale
4'hB	11/8 of grayscale
4'hC	3/2 of grayscale
4'hD	13/8 of grayscale
4'hE	7/4 of grayscale
4'hF	15/8 of grayscale

CGAPW[4:0]: The difference of the two grayscales counted by the threshold counter is set in units of one eighth of the grayscale.

Table 67

CGAPW[4:0]	Grayscale difference	CGAPW[4:0]	Grayscale difference
5'h00	Setting inhibited	5'h10	2 grayscales
5'h01	1/8 grayscales	5'h11	17/8 grayscales
5'h02	1/4 grayscales	5'h12	9/4 grayscales
5'h03	3/8 grayscales	5'h13	19/8 grayscales
5'h04	1/2 grayscales	5'h14	5/2 grayscales
5'h05	5/8 grayscales	5'h15	21/8 grayscales
5'h06	3/4 grayscales	5'h16	11/4 grayscales
5'h07	7/8 grayscales	5'h17	23/8 grayscales
5'h08	1 grayscale	5'h18	3 grayscales
5'h09	9/8 grayscales	5'h19	25/8 grayscales
5'h0A	5/4 grayscales	5'h1A	13/4 grayscales
5'h0B	11/8 grayscales	5'h1B	27/8 grayscales
5'h0C	3/2 grayscales	5'h1C	7/2 grayscales
5'h0D	13/8 grayscales	5'h1D	29/8 grayscales
5'h0E	7/4 grayscales	5'h1E	15/4 grayscales
5'h0F	15/8 grayscales	5'h1F	31/8 grayscales

COEFK0[4:0], COEFK1[4:0]: This register sets the range of the grayscale that prevent display image from being white, according to the ratio of the grayscale mentioned here to the grayscale number that makes data white.

Table 68

COEFK0[4:0] COEFK1[4:0]	Range of grayscale preventing image from being white	COEFK0[4:0] COEFK1[4:0]	Range of grayscale preventing image from being white
5'h00	0%	5'h10	100.00%
5'h01	6.25%	5'h11	Setting inhibited
5'h02	12.50%	5'h12	Setting inhibited
5'h03	18.75%	5'h13	Setting inhibited
5'h04	25.00%	5'h14	Setting inhibited
5'h05	31.25%	5'h15	Setting inhibited
5'h06	37.50%	5'h16	Setting inhibited
5'h07	43.75%	5'h17	Setting inhibited
5'h08	50.00%	5'h18	Setting inhibited
5'h09	56.25%	5'h19	Setting inhibited
5'h0A	62.50%	5'h1A	Setting inhibited
5'h0B	68.75%	5'h1B	Setting inhibited
5'h0C	75.00%	5'h1C	Setting inhibited
5'h0D	81.25%	5'h1D	Setting inhibited
5'h0E	87.50%	5'h1E	Setting inhibited
5'h0F	93.75%	5'h1F	Setting inhibited

TBLMIN[7:0], TBL0[7:0], TBL1[7:0], TBL2[7:0], TBL3[7:0], TBL4[7:0], TBL5[7:0], TBL6[7:0], TBL7[7:0]

The reference value used for interpolation calculation in gamma table is set by TBL*.

Table 69

TBL* [7:0]	8-bit reference value	TBL* [7:0]	8-bit reference value	TBL* [7:0]	8-bit reference value	TBL* [7:0]	8-bit reference value
8'h00	8'h00	8 'h20	8 'h20	8 'h40	8 'h40	8 'h60	8 'h60
8'h01	8'h01	8 'h21	8 'h21	8 'h41	8 'h41	8 'h61	8 'h61
8'h02	8'h02	8 'h22	8 'h22	8 'h42	8 'h42	8 'h62	8 'h62
8'h03	8'h03	8 'h23	8 'h23	8 'h43	8 'h43	8 'h63	8 'h63
8'h04	8'h04	8 'h24	8 'h24	8 'h44	8 'h44	8 'h64	8 'h64
8'h05	8'h05	8 'h25	8 'h25	8 'h45	8 'h45	8 'h65	8 'h65
8'h06	8'h06	8 'h26	8 'h26	8 'h46	8 'h46	8 'h66	8 'h66
8'h07	8'h07	8 'h27	8 'h27	8 'h47	8 'h47	8 'h67	8 'h67
8'h08	8'h08	8 'h28	8 'h28	8 'h48	8 'h48	8 'h68	8 'h68
8'h09	8'h09	8 'h29	8 'h29	8 'h49	8 'h49	8 'h69	8 'h69
8'h0A	8'h0A	8 'h2A	8 'h2A	8 'h4A	8 'h4A	8 'h6A	8 'h6A
8'h0B	8'h0B	8 'h2B	8 'h2B	8 'h4B	8 'h4B	8 'h6B	8 'h6B
8'h0C	8'h0C	8 'h2C	8 'h2C	8 'h4C	8 'h4C	8 'h6C	8 'h6C
8'h0D	8'h0D	8 'h2D	8 'h2D	8 'h4D	8 'h4D	8 'h6D	8 'h6D
8'h0E	8'h0E	8 'h2E	8 'h2E	8 'h4E	8 'h4E	8 'h6E	8 'h6E
8'h0F	8'h0F	8 'h2F	8 'h2F	8 'h4F	8 'h4F	8 'h6F	8 'h6F
8'h10	8'h10	8 'h30	8 'h30	8 'h50	8 'h50	8 'h70	8 'h70
8'h11	8'h11	8 'h31	8 'h31	8 'h51	8 'h51	8 'h71	8 'h71
8'h12	8'h12	8 'h32	8 'h32	8 'h52	8 'h52	8 'h72	8 'h72
8'h13	8'h13	8 'h33	8 'h33	8 'h53	8 'h53	8 'h73	8 'h73
8'h14	8'h14	8 'h34	8 'h34	8 'h54	8 'h54	8 'h74	8 'h74
8'h15	8'h15	8 'h35	8 'h35	8 'h55	8 'h55	8 'h75	8 'h75
8'h16	8'h16	8 'h36	8 'h36	8 'h56	8 'h56	8 'h76	8 'h76
8'h17	8'h17	8 'h37	8 'h37	8 'h57	8 'h57	8 'h77	8 'h77
8'h18	8'h18	8 'h38	8 'h38	8 'h58	8 'h58	8 'h78	8 'h78
8'h19	8'h19	8 'h39	8 'h39	8 'h59	8 'h59	8 'h79	8 'h79
8'h1A	8'h1A	8 'h3A	8 'h3A	8 'h5A	8 'h5A	8 'h7A	8 'h7A
8'h1B	8'h1B	8 'h3B	8 'h3B	8 'h5B	8 'h5B	8 'h7B	8 'h7B
8'h1C	8'h1C	8 'h3C	8 'h3C	8 'h5C	8 'h5C	8 'h7C	8 'h7C
8'h1D	8'h1D	8 'h3D	8 'h3D	8 'h5D	8 'h5D	8 'h7D	8 'h7D
8'h1E	8'h1E	8 'h3E	8 'h3E	8 'h5E	8 'h5E	8 'h7E	8 'h7E
8'h1F	8'h1F	8 'h3F	8 'h3F	8 'h5F	8 'h5F	8 'h7F	8 'h7F

(Table 69 Continued)

TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value
8'h80	8'h80	8'hA0	8'hA0	8'hC0	8'hC0	8'hE0	8'hE0
8'h81	8'h81	8'hA1	8'hA1	8'hC1	8'hC1	8'hE1	8'hE1
8'h82	8'h82	8'hA2	8'hA2	8'hC2	8'hC2	8'hE2	8'hE2
8'h83	8'h83	8'hA3	8'hA3	8'hC3	8'hC3	8'hE3	8'hE3
8'h84	8'h84	8'hA4	8'hA4	8'hC4	8'hC4	8'hE4	8'hE4
8'h85	8'h85	8'hA5	8'hA5	8'hC5	8'hC5	8'hE5	8'hE5
8'h86	8'h86	8'hA6	8'hA6	8'hC6	8'hC6	8'hE6	8'hE6
8'h87	8'h87	8'hA7	8'hA7	8'hC7	8'hC7	8'hE7	8'hE7
8'h88	8'h88	8'hA8	8'hA8	8'hC8	8'hC8	8'hE8	8'hE8
8'h89	8'h89	8'hA9	8'hA9	8'hC9	8'hC9	8'hE9	8'hE9
8'h8A	8'h8A	8'hAA	8'hAA	8'hCA	8'hCA	8'hEA	8'hEA
8'h8B	8'h8B	8'hAB	8'hAB	8'hCB	8'hCB	8'hEB	8'hEB
8'h8C	8'h8C	8'hAC	8'hAC	8'hCC	8'hCC	8'hEC	8'hEC
8'h8D	8'h8D	8'hAD	8'hAD	8'hCD	8'hCD	8'hED	8'hED
8'h8E	8'h8E	8'hAE	8'hAE	8'hCE	8'hCE	8'hEE	8'hEE
8'h8F	8'h8F	8'hAF	8'hAF	8'hCF	8'hCF	8'hEF	8'hEF
8'h90	8'h90	8'hB0	8'hB0	8'hD0	8'hD0	8'hF0	8'hF0
8'h91	8'h91	8'hB1	8'hB1	8'hD1	8'hD1	8'hF1	8'hF1
8'h92	8'h92	8'hB2	8'hB2	8'hD2	8'hD2	8'hF2	8'hF2
8'h93	8'h93	8'hB3	8'hB3	8'hD3	8'hD3	8'hF3	8'hF3
8'h94	8'h94	8'hB4	8'hB4	8'hD4	8'hD4	8'hF4	8'hF4
8'h95	8'h95	8'hB5	8'hB5	8'hD5	8'hD5	8'hF5	8'hF5
8'h96	8'h96	8'hB6	8'hB6	8'hD6	8'hD6	8'hF6	8'hF6
8'h97	8'h97	8'hB7	8'hB7	8'hD7	8'hD7	8'hF7	8'hF7
8'h98	8'h98	8'hB8	8'hB8	8'hD8	8'hD8	8'hF8	8'hF8
8'h99	8'h99	8'hB9	8'hB9	8'hD9	8'hD9	8'hF9	8'hF9
8'h9A	8'h9A	8'hBA	8'hBA	8'hDA	8'hDA	8'hFA	8'hFA
8'h9B	8'h9B	8'hBB	8'hBB	8'hDB	8'hDB	8'hFB	8'hFB
8'h9C	8'h9C	8'hBC	8'hBC	8'hDC	8'hDC	8'hFC	8'hFC
8'h9D	8'h9D	8'hBD	8'hBD	8'hDD	8'hDD	8'hFD	8'hFD
8'h9E	8'h9E	8'hBE	8'hBE	8'hDE	8'hDE	8'hFE	8'hFE
8'h9F	8'h9F	8'hBF	8'hBF	8'hDF	8'hDF	8'hFF	8'hFF

Back Light Comtrol2 (RD5h ~ RD8h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RD5	R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PWMON
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RD6	R/W	1	0	0	0	0	0	0	0	0	BDCV[7]	BDCV[6]	BDCV[5]	BDCV[4]	BDCV[3]	BDCV[2]	BDCV[1]	BDCV[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RD7	R/W	1	0	0	0	0	0	0	0	0	PWMDIV[7]	PWMDIV[6]	PWMDIV[5]	PWMDIV[4]	PWMDIV[3]	PWMDIV[2]	PWMDIV[1]	PWMDIV[0]
	Default		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
RD8	R/W	1	0	0	0	0	0	0	0	0	0	0	0	PWMWM	LEDPWME	LEDPWMPOL	0	DIMON
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PWMWM, PWMON

PWMWM = 0: Controls On/Off of the PWM output according to BASEE bit (0 or 1, defines display status).
PWMWM = 1: Controls On/Off of the PWM output according to PWMON setting.
Note that LEDPWM is always OFF when PON=0 and PSON=0 (LCD power supply is off) regardless of PWMON value.

PWMWM setting can be changed only when PON=0 and PSON=0.

LEDPWME: LEDPWM pin output enable bit.
In the system configuration using no LEDPWM pin, set LEDPWME = 0.
In the system configuration using LEDPWM pin, set LEDPWME = 1.
LEDPWME setting can be changed only when PON=0 and PSON=0.

Table 70

LEDPWME	PWMWM	PWMON	BLCON	RDPWM	LEDPWM output	
0	0	*	0	BDCV	0%	
			1	BLC*BDCV	0%	
	1	0	0	0%	0%	
			1	Setting disabled	Setting disabled	
		1	0	BDCV	0%	
			1	BLC*BDCV	0%	*2
1	0	*	0	BDCV	BDCV	*1
			1	BLC*BDCV	BLC*BDCV	*1
	1	0	0	0%	0%	
			1	Setting disabled	Setting disabled	
		1	0	BDCV	BDCV	
			1	BLC*BDCV	BLC*BDCV	*2

Note 1: If PWMWM = 0, On/Off of the PWM output is automatically controlled according to BASEE bit (0 or 1, defines display status).
Note 2: If PWMWM = 1 and BASEE=0, RDPWM and LEDPWM outputs cause BDCV value read.

BDCV[7:0]: PWM signal's width is selected from 256 values between 8'hFF and 8'h00 when LED is adjusted externally. The setting is enabled even when BLCON=0.

Table 71

BDCV[7:0]	Amount of light
8'h00	None (0%)
8'h01	1/255
8'h02	2/255
8'h03	3/255
:	:
8'hFE	254/255
8'hFF	255/255 (100%)

PWMDIV[7:0]: The bit is used to define frequency of PWM signal that is output from LEDPWM pin.

Table 72

PWMDIV[7:0]	LEDPWM frequency	PWMDIV[7:0]	LEDPWM frequency
8'h00	45.20KHz	8'h10-8'h1E	Setting disabled
8'h01	22.60KHz	8'h1F	1.46KHz
8'h02	15.07KHz	8'h20-8'h3E	Setting disabled
8'h03	11.30KHz	8'h3F	0.72KHz
8'h04-8'h06	Setting disabled	8'h40-8'h7E	Setting disabled
8'h07	6.46KHz	8'h7F	0.36KHz
8'h08-8'h0E	Setting disabled	8'h80-8'hFE	Setting disabled
8'h0F	3.01KHz	8'hFF	0.18KHz

Note: The values in the table above show the typical. There shall be variance of maximum +/-7% in the actual operation.

LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.

Table 73

LEDPWPOL	LEDPWM pin	
	Lit period	Non-lit period
0	High	Low
1	Low	High

DIMON: DIMON bit is used to enable / disable LEDPWM's DIMMING function.

The bit is used to control change in brightness (change in LEDPWM signal) when BCDV register is rewritten or LEDPWM pin is turned on. This setting is enabled only when PON=0 and PSON=0.

Table 74

DIMON	DIMMING function	Brightness
0	OFF	Changes immediately
1	ON	Changes gradually in approximately 500ms.

Note: This bit is applied to BDCV register setting and not to brightness change by the BLC function.

Back Light Control 3 (RDAh)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RDA	R	1	0	0	0	0	0	0	0	0	RDPWM[7]	RDPWM[6]	RDPWM[5]	RDPWM[4]	RDPWM[3]	RDPWM[2]	RDPWM[1]	RDPWM[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RDPWM: Used to read LED brightness data for LEDPWM signal. The read data are disabled when PON=0 and PSON=0.

Back Light Control 4 (RF9h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RF9	R	1	0	0	0	0	0	0	0	0	0	0	0	0	PBCKON	0	0	0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PBCKON: Write PBCKON=1 to use LEDPWM signal to control LED Dr., or to use BLC function. This register setting can be changed only when PON=0 and PSON=0.

●R61580 Instruction List

Major category		Minor category		Upper Code								Lower Code								Note
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
–	Index	–	Index	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID21	ID0	
0*	Display Control	00h	Device Code Read	ALMID1[7]	ALMID1[6]	ALMID1[5]	ALMID1[4]	ALMID1[3]	ALMID1[2]	ALMID1[1]	ALMID1[0]	ALMID0[7]	ALMID0[6]	ALMID0[5]	ALMID0[4]	ALMID0[3]	ALMID0[2]	ALMID0[1]	ALMID0[0]	
			(Default)	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	
		01h	Driver Output Control						SM		SS									
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		02h	LCD Driving Wave Control							BC0									NW[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		03h	Entry Mode	TRIREG	DFM		BGR					ORG		I/D[1]	I/D[0]	AM				
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	
		07h	Display Control 1				PTDE				BASEE					COL				
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		08h	Display Control 2	FP0[7]	FP0[6]	FP0[5]	FP0[4]	FP0[3]	FP0[2]	FP0[1]	FP0[0]	BP0[7]	BP0[6]	BP0[5]	BP0[4]	BP0[3]	BP0[2]	BP0[1]	BP0[0]	
			(Default)	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	
		09h	Display Control 3						PTS[2]	PTS[1]	PTS[0]			PTG		ISC[3]	ISC[2]	ISC[1]	ISC[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
		0Ah	Display Control 4													FMARKOE	FMI[2]	FMI[1]	FMI[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Ch	External Display Interface Control		ENC[2]	ENC[1]	ENC[0]				RM			DM[1]	DM[0]			RIM[1]	RIM[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Dh	Frame Marker Position								FMP[8]	FMP[7]	FMP[6]	FMP[5]	FMP[4]	FMP[3]	FMP[2]	FMP[1]	FMP[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Eh	VCOM Low Power Control											VEM[1]	VEM[0]					
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	
		0Fh	External Display Interface Control 2												VSPL	HSPL		EPL	DPL	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1*	Power Control	10h	Power Control 1						BT[2]	BT[1]	BT[0]			AP[1]	AP[0]		DSTB			
			(Default)	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	
		11h	Power Control 2						DC1[2]	DC1[1]	DC1[0]		DC0[2]	DC0[1]	DC0[0]		VC[2]	VC[1]	VC[0]	
			(Default)	0	0	0	0	0	0	1	0	0	0	1	1	0	1	1	1	
		12h	Power Control 3				VRH[0]				VCMR	1		PSON	PON	VRH[4]	VRH[3]	VRH[2]	VRH[1]	
			(Default)	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	
		13h	Power Control 4				VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]									
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
2*	Frame Memory Access Control	20h	Frame Memory Address Set (Hotizontal Address)									AD[7]	AD[6]	AD[5]	AD[4]	AD[3]	AD[2]	AD[1]	AD[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		21h	Frame Memory Address Set (Vertical Address)								AD[16]	AD[15]	AD[14]	AD[13]	AD[12]	AD[11]	AD[10]	AD[9]	AD[8]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		22h	Frame Memory Data Write/Read	Frame memory write data WD[17:0] are transferred via different data bus in different interface operations.																
	NVM Control	28h	NVM Data Read 1									ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
		29h	NVM Data Read 2										VCM1[6]	VCM1[5]	VCM1[4]	VCM1[3]	VCM1[2]	VCM1[1]	VCM1[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
		2Ah	NVM Data Read 3									VCMSEL	VCM2[6]	VCM2[5]	VCM2[4]	VCM2[3]	VCM2[2]	VCM2[1]	VCM2[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
3*	Gamma Control	30h	Gamma Control 1				PR0P01[4]	PR0P01[3]	PR0P01[2]	PR0P01[1]	PR0P01[0]				PR0P00[4]	PR0P00[3]	PR0P00[2]	PR0P00[1]	PR0P00[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		31h	Gamma Control 2	PR0P04[3]	PR0P04[2]	PR0P04[1]	PR0P04[0]	PR0P03[3]	PR0P03[2]	PR0P03[1]	PR0P03[0]				PR0P02[4]	PR0P02[3]	PR0P02[2]	PR0P02[1]	PR0P02[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		32h	Gamma Control 3				PR0P06[4]	PR0P06[3]	PR0P06[2]	PR0P06[1]	PR0P06[0]					PR0P05[3]	PR0P05[2]	PR0P05[1]	PR0P05[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		33h	Gamma Control 4				PR0P08[4]	PR0P08[3]	PR0P08[2]	PR0P08[1]	PR0P08[0]				PR0P07[4]	PR0P07[3]	PR0P07[2]	PR0P07[1]	PR0P07[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		34h	Gamma Control 5			PIR0P3[1]	PIR0P3[0]			PIR0P2[1]	PIR0P2[0]			PIR0P1[1]	PIR0P1[0]			PIR0P0[1]	PIR0P0[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		35h	Gamma Control 6				PR0N01[4]	PR0N01[3]	PR0N01[2]	PR0N01[1]	PR0N01[0]				PR0N00[4]	PR0N00[3]	PR0N00[2]	PR0N00[1]	PR0N00[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		36h	Gamma Control 7	PR0N04[3]	PR0N04[2]	PR0N04[1]	PR0N04[0]	PR0N03[3]	PR0N03[2]	PR0N03[1]	PR0N03[0]				PR0N02[4]	PR0N02[3]	PR0N02[2]	PR0N02[1]	PR0N02[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		37h	Gamma Control 8				PR0N06[4]	PR0N06[3]	PR0N06[2]	PR0N06[1]	PR0N06[0]					PR0N05[3]	PR0N05[2]	PR0N05[1]	PR0N05[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		38h	Gamma Control 9				PR0N08[4]	PR0N08[3]	PR0N08[2]	PR0N08[1]	PR0N08[0]				PR0N07[4]	PR0N07[3]	PR0N07[2]	PR0N07[1]	PR0N07[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		39h	Gamma Control 10			PIR0N3[1]	PIR0N3[0]			PIR0N2[1]	PIR0N2[0]			PIR0N1[1]	PIR0N1[0]			PIR0N0[1]	PIR0N0[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
5*	Window Address Control	50h	Window Horizontal Frame Memory Address (Start Address)									HSA[7]	HSA[6]	HSA[5]	HSA[4]	HSA[3]	HSA[2]	HSA[1]	HSA[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		51h	Window Horizontal Frame Memory Address (End Address)									HEA[7]	HEA[6]	HEA[5]	HEA[4]	HEA[3]	HEA[2]	HEA[1]	HEA[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	
		52h	Window Vertical Frame Memory Address (Start Address)								VSA[8]	VSA[7]	VSA[6]	VSA[5]	VSA[4]	VSA[3]	VSA[2]	VSA[1]	VSA[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		53h	Window Vertical Frame Memory Address (End Address)								VEA[8]	VEA[7]	VEA[6]	VEA[5]	VEA[4]	VEA[3]	VEA[2]	VEA[1]	VEA[0]	
			(Default)	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	
6*	Base Image Display Control	60h	Driver Output Control	GS		NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]			SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]	
			(Default)	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	
		61h	Base Image Display Control														NDL	VSSON	INVON	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		6Ah	Vertical Scroll Control								VL[8]	VL[7]	VL[6]	VL[5]	VL[4]	VL[3]	VL[2]	VL[1]	VL[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
8*	Partial Display Control	80h	Partial Image Display Position								PTDP[8]	PTDP[7]	PTDP[6]	PTDP[5]	PTDP[4]	PTDP[3]	PTDP[2]	PTDP[1]	PTDP[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		81h	Partial Image Frame Memory Address (Start Line Address)								PTSA[8]	PTSA[7]	PTSA[6]	PTSA[5]	PTSA[4]	PTSA[3]	PTSA[2]	PTSA[1]	PTSA[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		82h	Partial Image Frame Memory Address (End Line Address)								PTEA[8]	PTEA[7]	PTEA[6]	PTEA[5]	PTEA[4]	PTEA[3]	PTEA[2]	PTEA[1]	PTEA[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
9*	Panel Interface Control	90h	Panel Interface Control 1							DIVI[1]	DIVI[0]				RTNI[4]	RTNI[3]	RTNI[2]	RTNI[1]	RTNI[0]	
			(Default)	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	
		91h	Panel Interface Control 1-1													SPCWI[3]	SPCWI[2]	SPCWI[1]	SPCWI[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
		92h	Panel Interface Control 2						NOWI[2]	NOWI[1]	NOWI[0]									
			(Default)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
		93h	Panel Interface Control 3						VEQWI[2]	VEQWI[1]	VEQWI[0]						MCPI[2]	MCPI[1]	MCPI[0]	
			(Default)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	
		94h	Panel Interface Control 4														SDTI[2]	SDTI[1]	SDTI[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
		95h	Panel Interface Control 5							DIVE[1]	DIVE[0]			RTNE[5]	RTNE[4]	RTNE[3]	RTNE[2]	RTNE[1]	RTNE[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	
		96h	Panel Interface Control 5-1													SPCWE[3]	SPCWE[2]	SPCWE[1]	SPCWE[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
		97h	Panel Interface Control 6						NOWE[2]	NOWE[1]	NOWE[0]									
			(Default)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
		98h	Panel Interface Control 7						VEQWE[2]	VEQWE[1]	VEQWE[0]						MCPE[2]	MCPE[1]	MCPE[0]	
			(Default)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	
		99h	Panel Interface Control 8														SDTE[2]	SDTE[1]	SDTE[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
		9Ch	Panel Interface Control 9										PCDIVH[2]	PCDIVH[1]	PCDIVH[0]		PCDIVL[2]	PCDIVL[1]	PCDIVL[0]	
			(Default)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	
A*	NVM Control	A0h	NVM Control 1									FTT		OP[1]	OP[0]				NVAD	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		A1h	(Default)	ED[15]	ED[14]	ED[13]	ED[12]	ED[11]	ED[10]	ED[9]	ED[8]	ED[7]	ED[6]	ED[5]	ED[4]	ED[3]	ED[2]	ED[1]	ED[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		A3h	NVM Control 2											VERIFLGER	VERIFLGWR	RTY_RTL_[3]	RTY_RTL_[2]	RTY_RTL_[1]	RTY_RTL_[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		A4h	(Default)																CALB	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
C*	Back Light Control	C0h	Back Light Control															BLCM	BLCON	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		C1h	(Default)												THREW0[4]	THREW0[3]	THREW0[2]	THREW0[1]	THREW0[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		C2h	(Default)												THREW1[4]	THREW1[3]	THREW1[2]	THREW1[1]	THREW1[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		C3h	(Default)											ULMTW0[5]	ULMTW0[4]	ULMTW0[3]	ULMTW0[2]	ULMTW0[1]	ULMTW0[0]	
				0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
		C4h	(Default)											ULMTW1[5]	ULMTW1[4]	ULMTW1[3]	ULMTW1[2]	ULMTW1[1]	ULMTW1[0]	
				0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
		C5h	(Default)											LLMTW0[5]	LLMTW0[4]	LLMTW0[3]	LLMTW0[2]	LLMTW0[1]	LLMTW0[0]	
				0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
		C6h	(Default)											LLMTW1[5]	LLMTW1[4]	LLMTW1[3]	LLMTW1[2]	LLMTW1[1]	LLMTW1[0]	
				0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
		C7h	(Default)													PITCHW[3]	PITCHW[2]	PITCHW[1]	PITCHW[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
		C8h	(Default)												CGAPW[4]	CGAPW[3]	CGAPW[2]	CGAPW[1]	CGAPW[0]	
				0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	
		C9h	(Default)												COEFK0[4]	COEFK0[3]	COEFK0[2]	COEFK0[1]	COEFK0[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	
		CAh	(Default)												COEFK1[4]	COEFK1[3]	COEFK1[2]	COEFK1[1]	COEFK1[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	
		CBh	(Default)									TBLMIN[7]	TBLMIN[6]	TBLMIN[5]	TBLMIN[4]	TBLMIN[3]	TBLMIN[2]	TBLMIN[1]	TBLMIN[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		CCh	(Default)									TBL0[7]	TBL0[6]	TBL0[5]	TBL0[4]	TBL0[3]	TBL0[2]	TBL0[1]	TBL0[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
		CDh	(Default)									TBL1[7]	TBL1[6]	TBL1[5]	TBL1[4]	TBL1[3]	TBL1[2]	TBL1[1]	TBL1[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	
		CEh	(Default)									TBL2[7]	TBL2[6]	TBL2[5]	TBL2[4]	TBL2[3]	TBL2[2]	TBL2[1]	TBL2[0]	
				0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	
		CFh	(Default)									TBL3[7]	TBL3[6]	TBL3[5]	TBL3[4]	TBL3[3]	TBL3[2]	TBL3[1]	TBL3[0]	
				0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	
D*		D0h	(Default)									TBL4[7]	TBL4[6]	TBL4[5]	TBL4[4]	TBL4[3]	TBL4[2]	TBL4[1]	TBL4[0]	
				0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	
		D1h	(Default)									TBL5[7]	TBL5[6]	TBL5[5]	TBL5[4]	TBL5[3]	TBL5[2]	TBL5[1]	TBL5[0]	
				0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	
		D2h	(Default)									TBL6[7]	TBL6[6]	TBL6[5]	TBL6[4]	TBL6[3]	TBL6[2]	TBL6[1]	TBL6[0]	
				0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	
		D3h	(Default)									TBL7[7]	TBL7[6]	TBL7[5]	TBL7[4]	TBL7[3]	TBL7[2]	TBL7[1]	TBL7[0]	
				0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
		D5h	Back Light Control 2																PWMON	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		D6h	(Default)									BDCV[7]	BDCV[6]	BDCV[5]	BDCV[4]	BDCV[3]	BDCV[2]	BDCV[1]	BDCV[0]	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		D7h	(Default)									PWMDIV[7]	PWMDIV[6]	PWMDIV[5]	PWMDIV[4]	PWMDIV[3]	PWMDIV[2]	PWMDIV[1]	PWMDIV[0]	
				0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	
		D8h	(Default)												PWMWM	LEDPWME	LEDPWMPOL		DIMON	
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		DAh	Back Light Control 3									RDPWM[7]	RDPWM[6]	RDPWM[5]	RDPWM[4]	RDPWM[3]	RDPWM[2]	RDPWM[1]	RDPWM[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		F9h	Back Light Control 4													PBCKON				
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Reset Function

The R61580 is initialized by the RESET input. During reset period, the R61580 is in a busy state and instruction from the host processor and frame memory access are not accepted. The R61580's internal power supply circuit unit is initialized also by the RESET input.

1. Initial state of instruction bits (default)

See the instruction list. The default values are shown in the parenthesis of each instruction bit cell.

2. Frame Memory Data initialization

The frame memory data is not automatically initialized by the RESET input. It must be initialized by software in display-off period.

3. Output pin initial state

Pin name	After H/W reset
DB[17:0]	Hi-Z
SDO	Hi-Z
FMARK	GND
LEDPWM	GND
VDD	1.5V
VCI1	Hi-Z
C11P/C11M	Hi-Z/Hi-Z
C12P/C12M	Hi-Z/Hi-Z
C13P/C13M	Hi-Z/GND
C21P/C21M	VCI/GND
C22P/C22M	VCI/GND
VREG1OUT	VGS
VCOML	GND
VCOMH	VCI(DDVDH)
VCL	GND
VGL	GND
VGH	VCI
DDVDH	VCI
VCOM	GND
S[720:1]	GND
G[320:1]	GND

Basic Operation

The basic operation modes of the R61580 are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

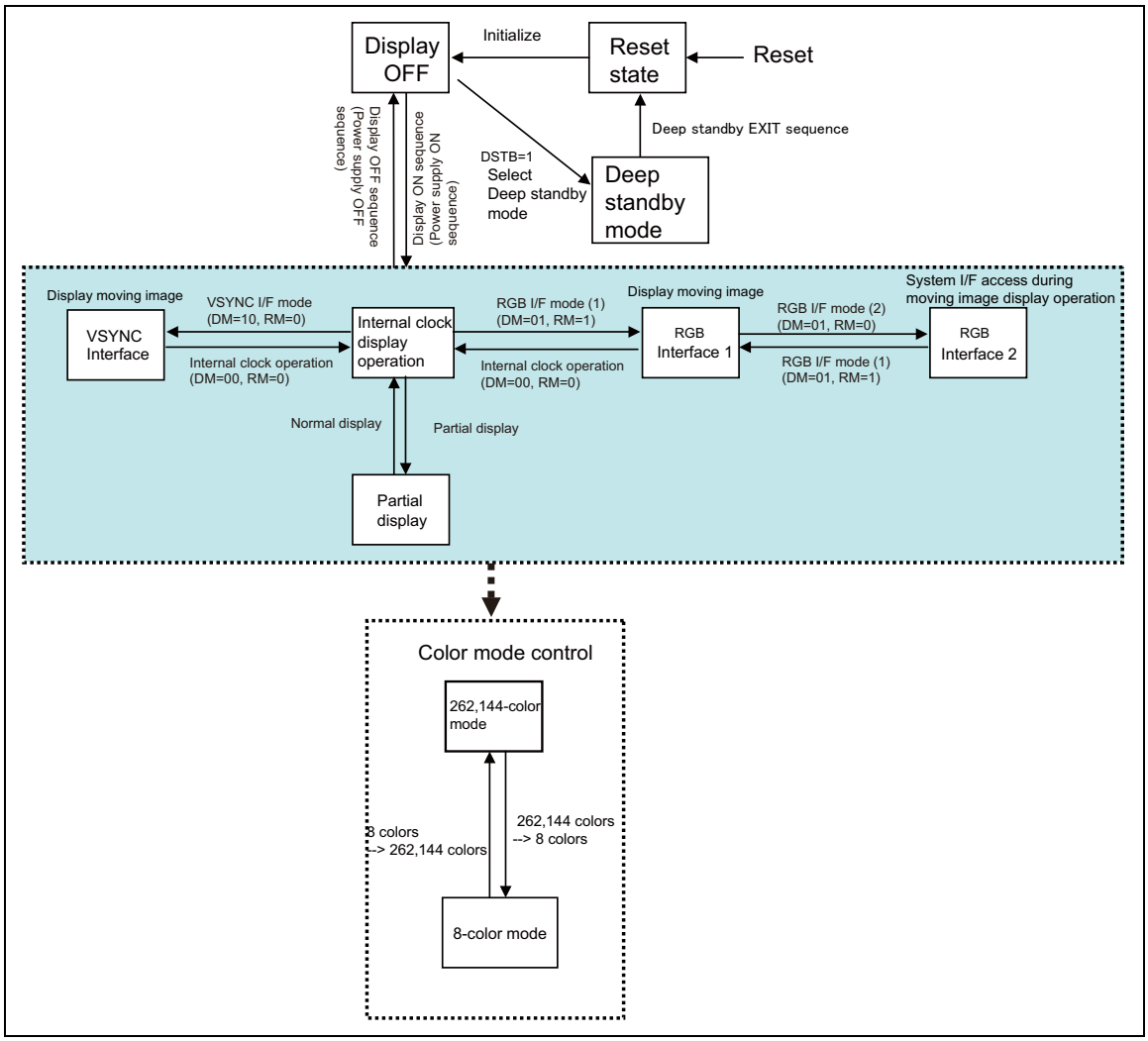


Figure 10

Interface and Data Format

The R61580 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The R61580 can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the R61580 supports RGB interface and VSYNC interface that enable data rewrite operation without flicker the moving picture on the panel.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC and DOTCLK. In synchronization with these signals, the R61580 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data are stored in the R61580's frame memory so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the frame memory area to write data for moving picture display, which enables displaying a moving picture and frame memory data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the frame memory at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal frame memory.

The R61580 operates in one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register (R0Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Table 75 Operation Modes

Operation Mode	Frame Memory Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not change RGB interface operation setting (RIM1-0) during RGB interface operation.
4. See the "External Display Interface" section for the sequences when switching from one mode to another.

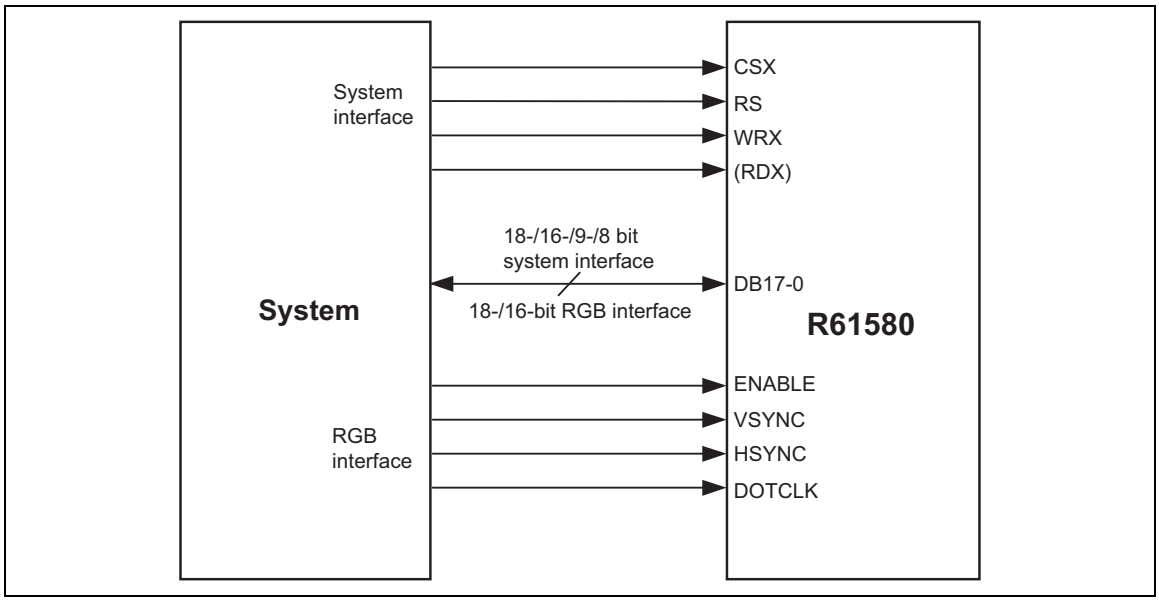


Figure 11

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. Every input via external display interface is disabled in this operation. The internal frame memory can be accessed only via system interface.

RGB interface operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61580 transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal frame memory. Window address function can minimize the total number of data transfer for moving picture display because only the moving picture data is transferred to the frame memory, enabling the R61580 to display a moving picture and another image stored in the frame memory simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61580 by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with the setting of these periods.

RGB interface operation (2)

This mode enables the R61580 to rewrite frame memory data via system interface while using RGB interface for display operation. To rewrite frame memory data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the frame memory address set register and R22h in the index register.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61580 to display a moving picture via system interface by writing data in the internal frame memory at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing frame memory data. For details, see the "VSYNC Interface" section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61580 according to the instruction settings for these periods.

FMARK interface operation

In the FMARK interface operation, data is written to internal frame memory via system interface synchronizing with the frame mark signal (FMARK), realizing tearing-less moving picture while using conventional system interface. In this case, there are restrictions in speed and method of writing frame memory data. See "FMARK Interface" for detail.

System Interface

The following are the kinds of system interfaces available with the R61580. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and frame memory access.

Table 76 IM Bit Settings and System Interface

IM3	IM2	IM1	IM0	Interfacing Mode with Host processor	DB Pins	Colors
0	0	0	0	Setting inhibited	-	-
0	0	0	1	Setting inhibited	-	-
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 *see Note1
0	0	1	1	80-system 8-bit interface	DB17-10	262,144 *see Note2
0	1	0	0	Clock synchronous serial interface	-	65,536
0	1	1	0	Setting inhibited	-	-
0	1	1	1	Setting inhibited	-	-
1	0	0	0	Setting inhibited	-	-
1	0	0	1	Setting inhibited	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	262,144
1	0	1	1	80-system 9-bit interface	DB17-9	262,144
1	1	0	0	Setting inhibited	-	-
1	1	0	1	Setting inhibited	-	-
1	1	1	0	Setting inhibited	-	-
1	1	1	1	Setting inhibited	-	-

Notes: 1. 262,144 colors in 16-bit 2-transfer mode. 65,536 colors in 16-bit 1-transfer mode.
2. 262,144 colors in 8-bit 3-transfer mode. 65,536 colors in 8-bit 2-transfer mode.

80-system 18-bit Bus Interface

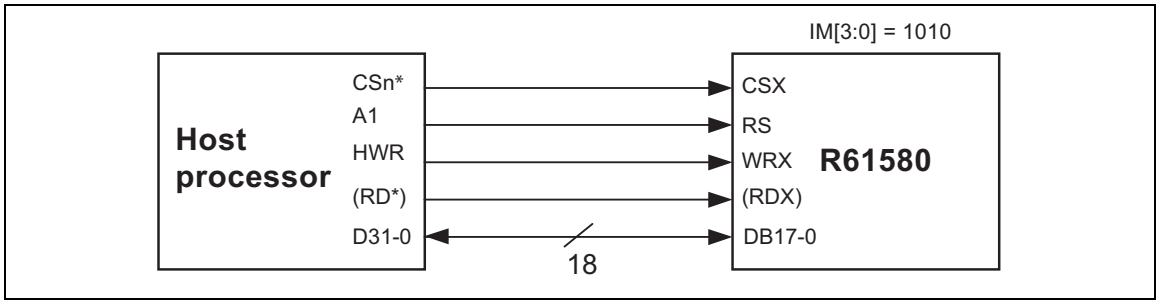


Figure 12 18-bit Interface

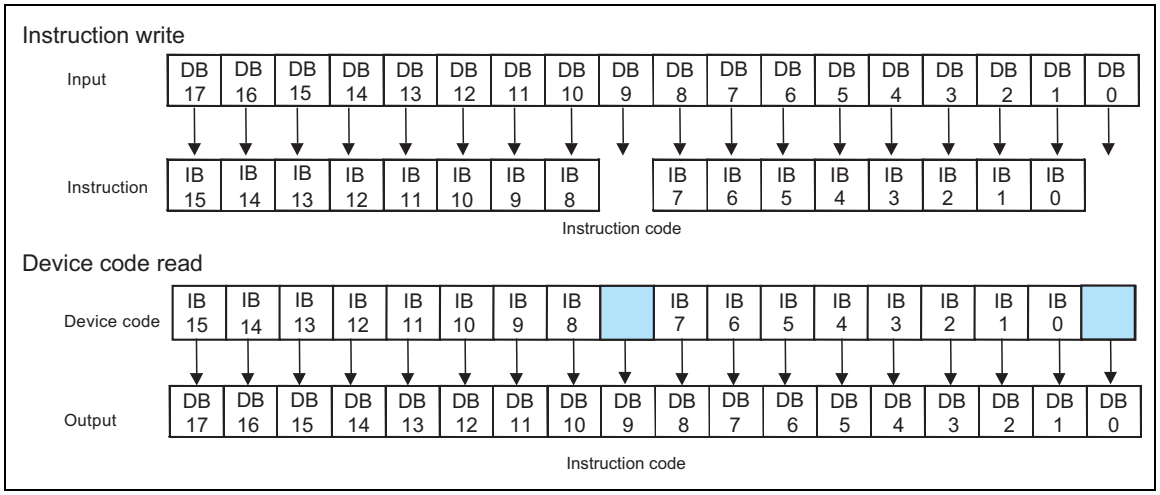


Figure 13 18-bit Interface Data Format (Instruction Write / Device Code Read) (IM[3:0]=1010)

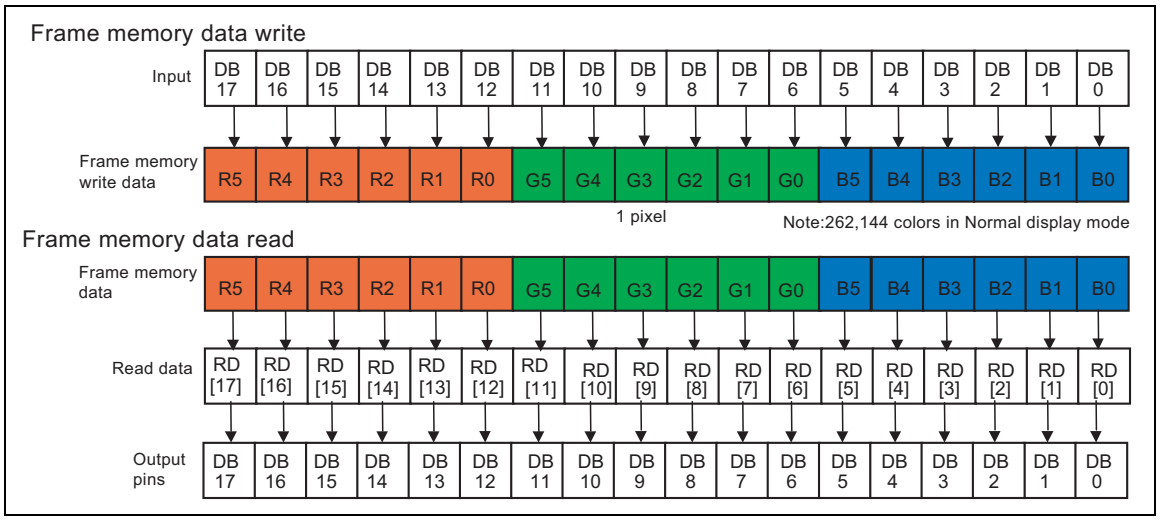


Figure 14 18-bit Interface Data Format (Frame Memory Data Write / Frame Memory Data Read)

80-system 16-bit Bus Interface

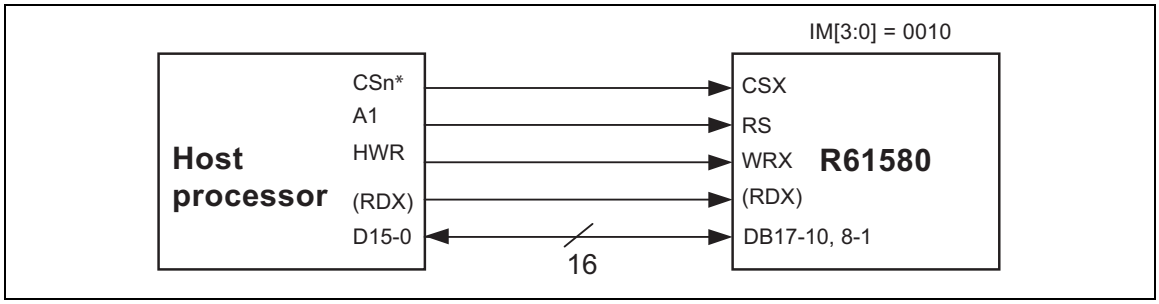


Figure 15 16-bit Interface

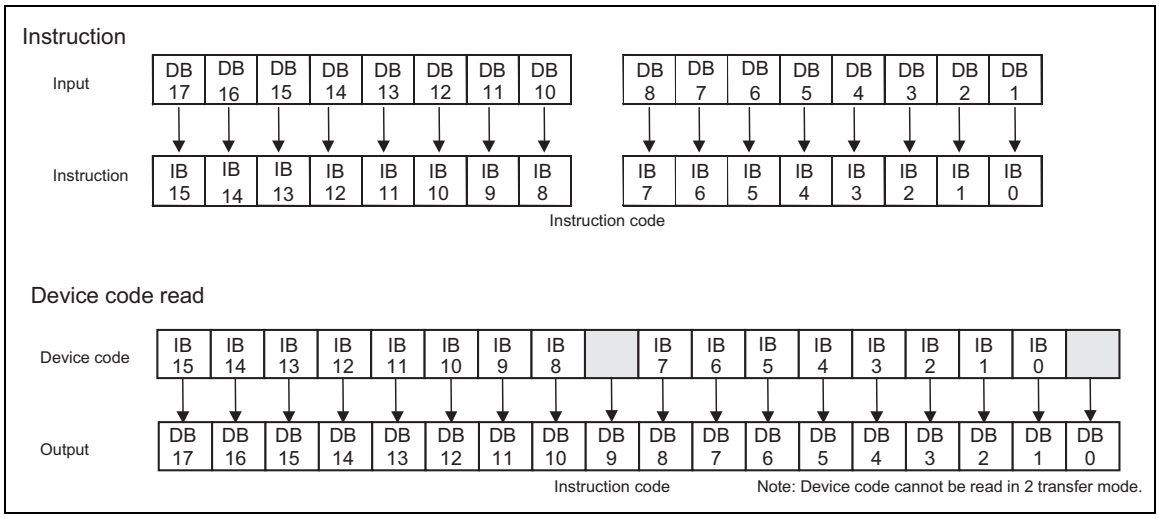


Figure 16 16-bit Interface Data Format (Instruction Write / Device Code Read)

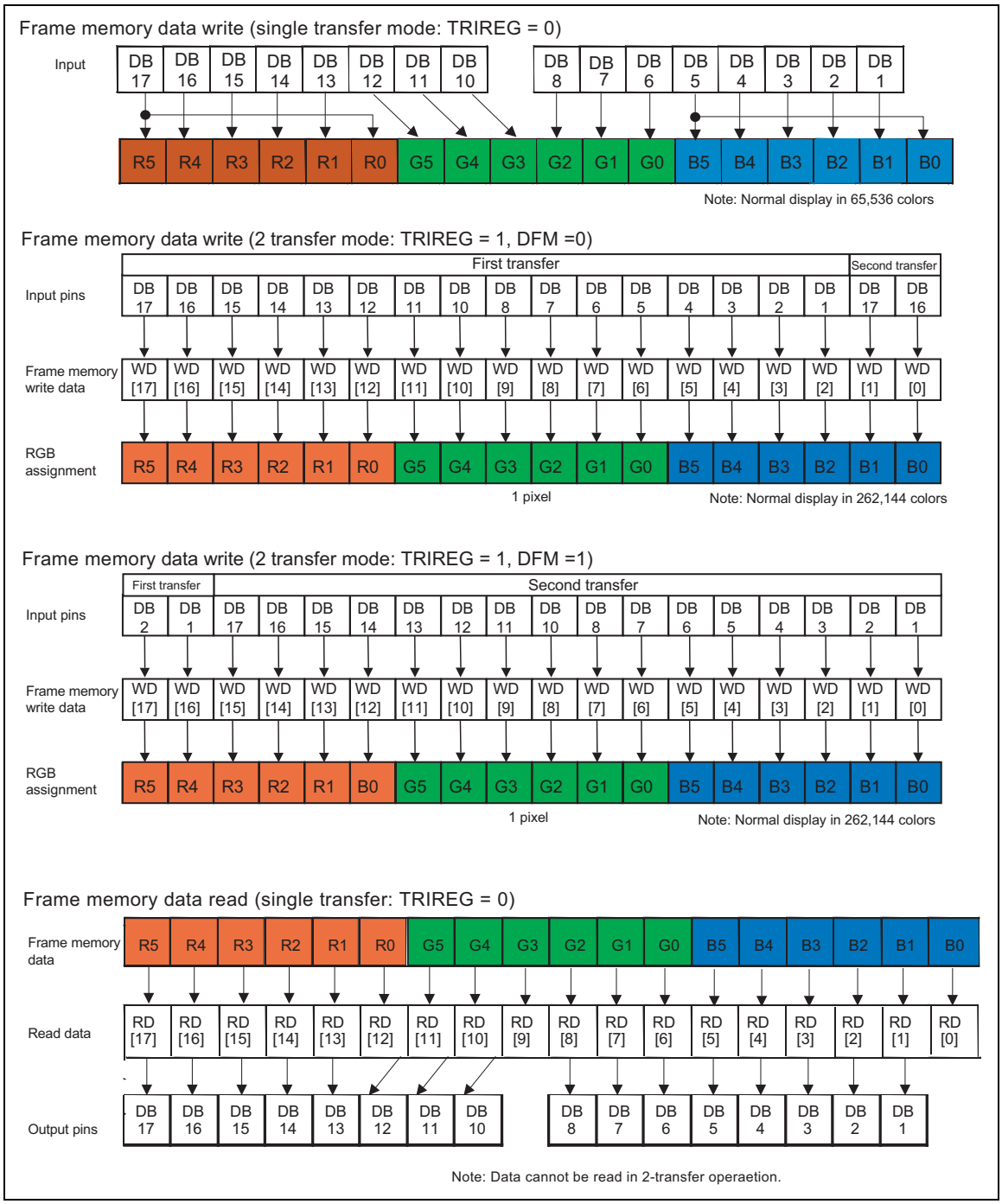


Figure 17 16-bit Interface Data Format (Frame Memory Data Write / Frame Memory Data Read)

Data Transfer Synchronization in 16-bit Bus Interface Operation

The R61580 supports data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 2/16 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

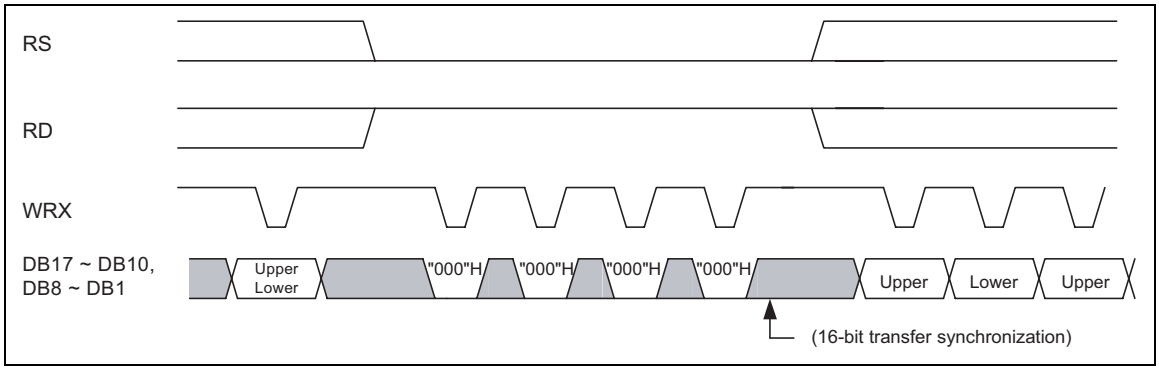


Figure 18 16-bit Data Transfer Synchronization

80-system 9-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The frame memory write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either IOVCC or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

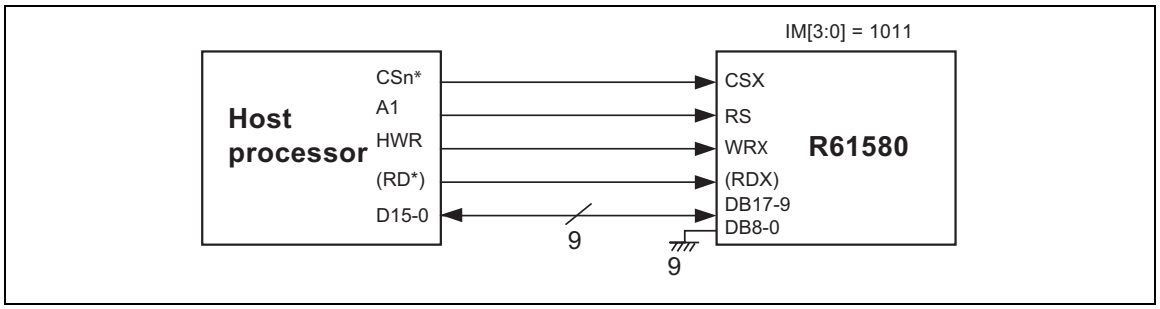


Figure 19 9-bit Interface

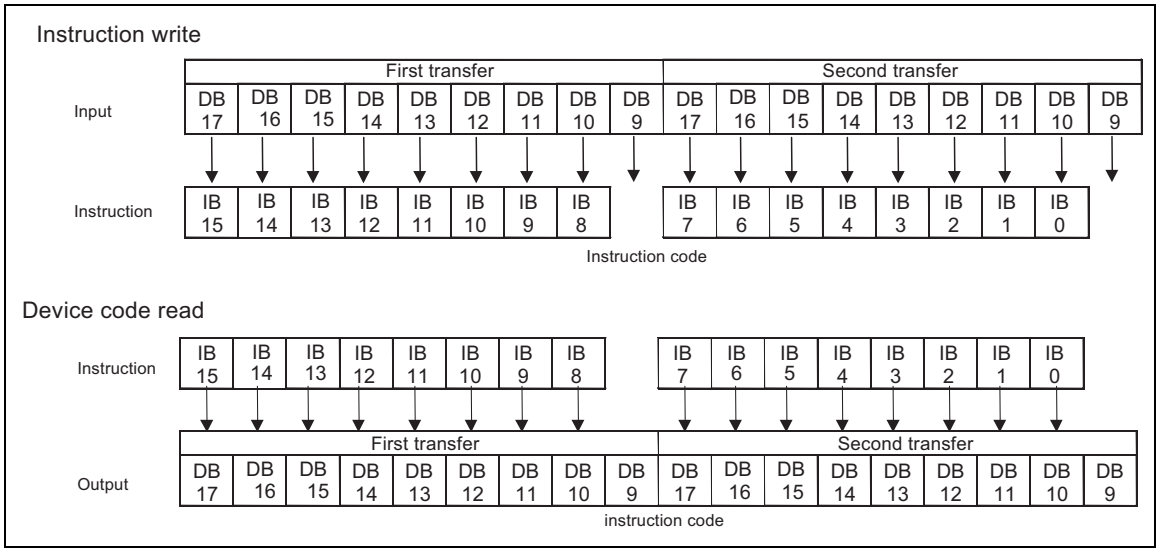


Figure 20 9-bit Interface Data Format (Instruction Write / Device Code Read)

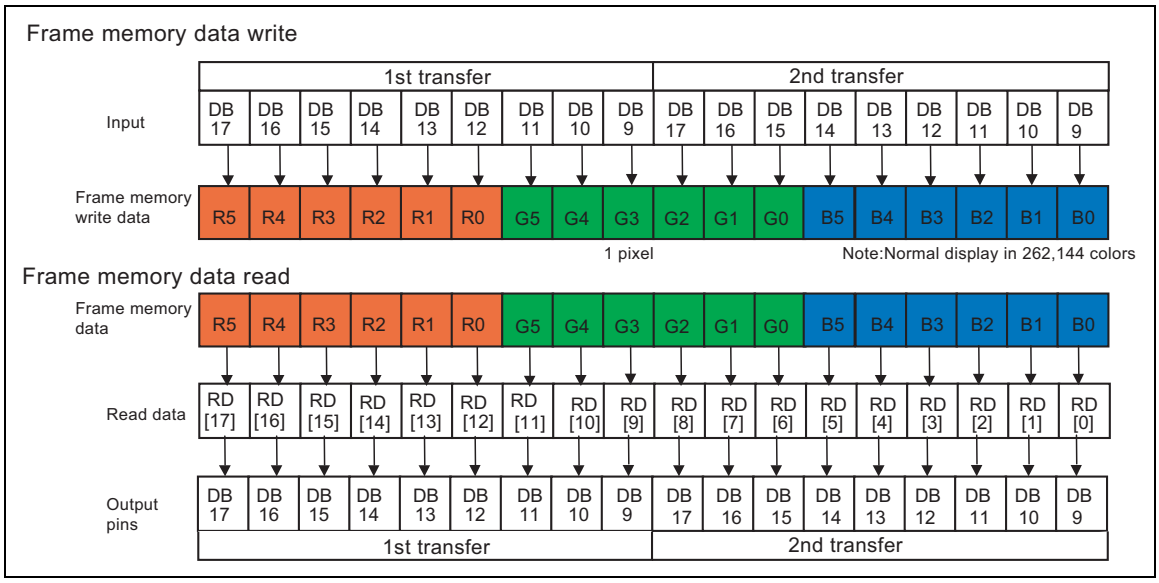


Figure 21 9-bit Interface Data Format (Frame Memory Data Write/ Frame Memory Data Read)

Data Transfer Synchronization in 9-bit Bus Interface Operation

The R61580 supports data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 9 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

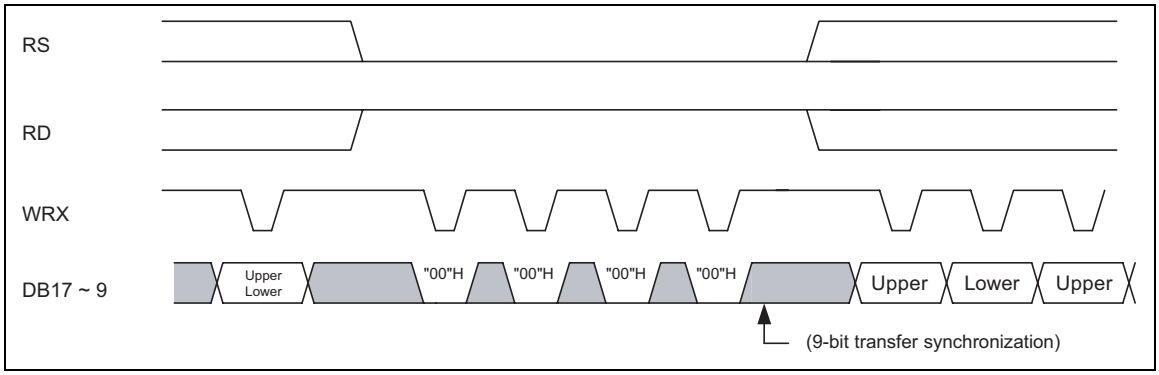


Figure 22 9-bit Data Transfer Synchronization

80-system 8-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The frame memory write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The frame memory write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either IOVCC or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

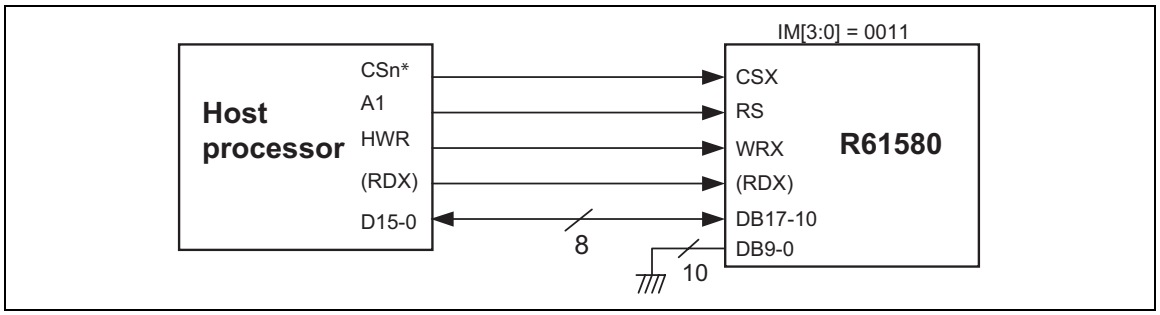


Figure 23 8-bit Interface

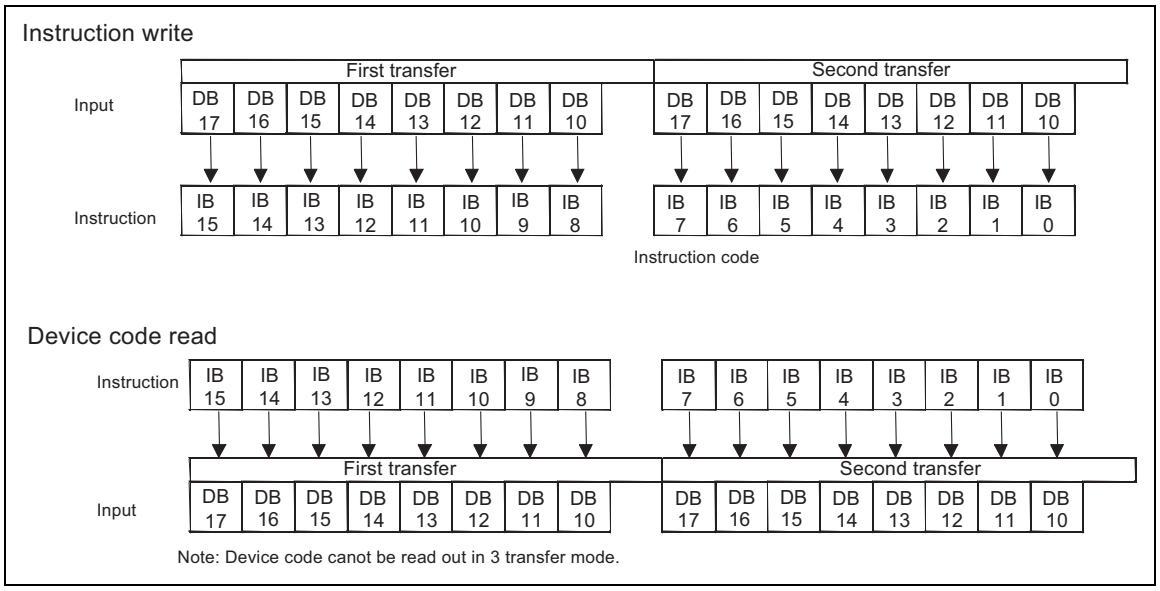


Figure 24 8-bit Interface Data Format (Instruction Write / Device Code Read)

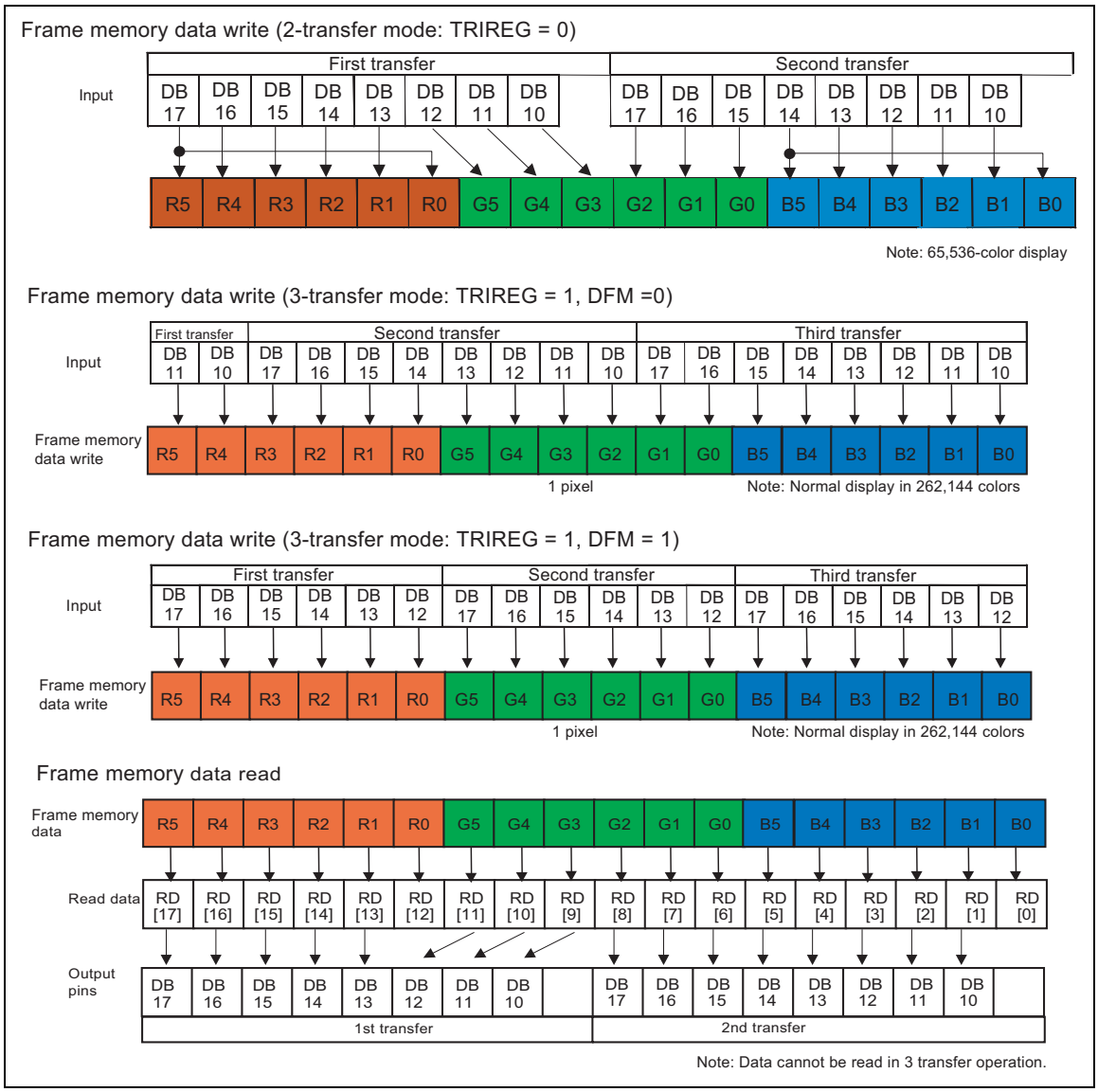


Figure 25 8-bit Interface Data Format (Frame Memory Data Write / Frame Memory Data Read)

Data Transfer Synchronization in 8-bit Bus Interface operation

The R61580 supports data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 8 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

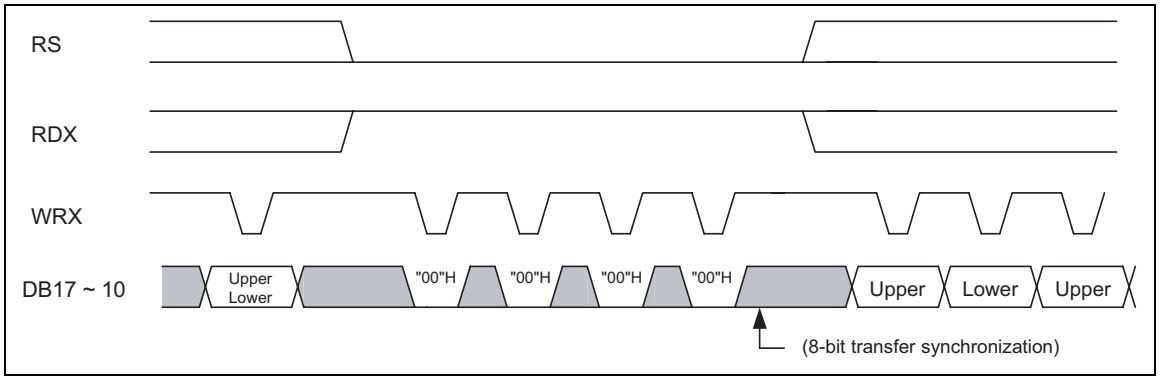


Figure 26 8-bit Data Transfer Synchronization

Serial Interface

The serial interface is selected by setting the IM3/2/1/0 pins to the GND/IOVCC/GND/GND levels, respectively. The data is transferred via chip select line (CSX), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, unused DB17-0 pins must be fixed at either IOVCC or GND level.

The R61580 recognizes the start of data transfer on the falling edge of CSX input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CSX input. The R61580 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code ("011100") assigned to the R61580 are compared and agreed. Then, the R61580 starts taking in subsequent data. Two different chip addresses must be assigned to the R61580 because the seventh bit of the start byte is register select bit (RS). When RS = 0, index register write operation is executed. When RS = 1, either instruction write operation or frame memory read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The R61580 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the frame memory via serial interface, the data is written to the frame memory after it is transferred in two bytes. The R61580 writes data to the frame memory in units of 18 bits by adding the same bits as the MSBs to the LSBs of R dot data and B dot data.

After receiving the start byte, the R61580 starts transferring or receiving data in units of bytes. The R61580 transfers data from the MSB. The R61580's instruction consists of 16 bits and it is executed inside the R61580 after it is transferred in two bytes (16 bits: DB15-0) from the MSB. The R61580 expands frame memory write data into 18 bits when writing them to the internal frame memory. The first byte received by the R61580 following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

When reading data from the frame memory, valid data is not transferred to the data bus until first five bytes of data are read from the frame memory following the start byte. The R61580 sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 77 Start Byte Format

Transferred Bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	0		

Table 78 Functions of RS, R/W Bits

RS	R/W	Function
0	0	Set index register
0	1	Setting inhibited
1	0	Write instruction or frame memory data
1	1	Read register settings or frame memory data

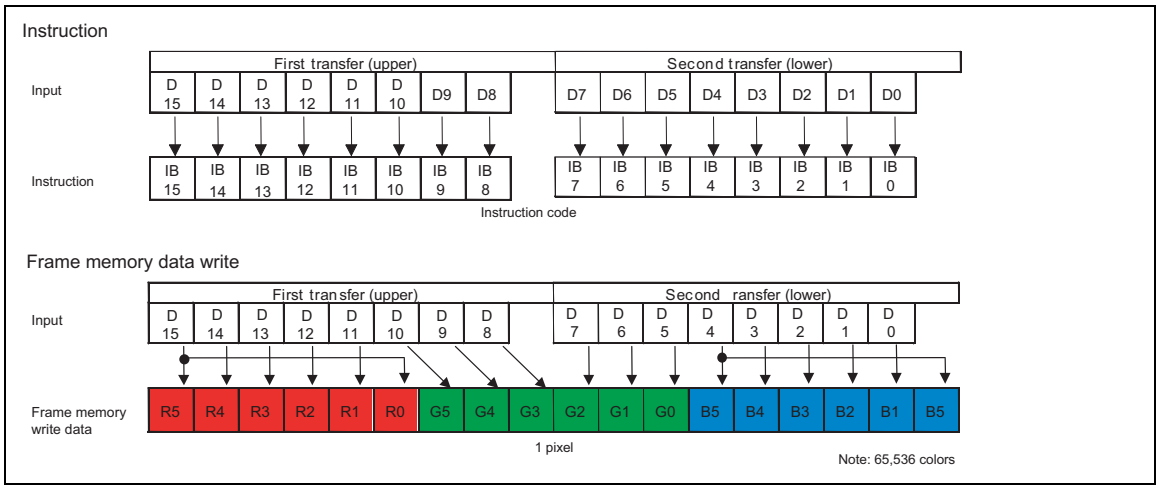


Figure 27 Serial Interface Data Format

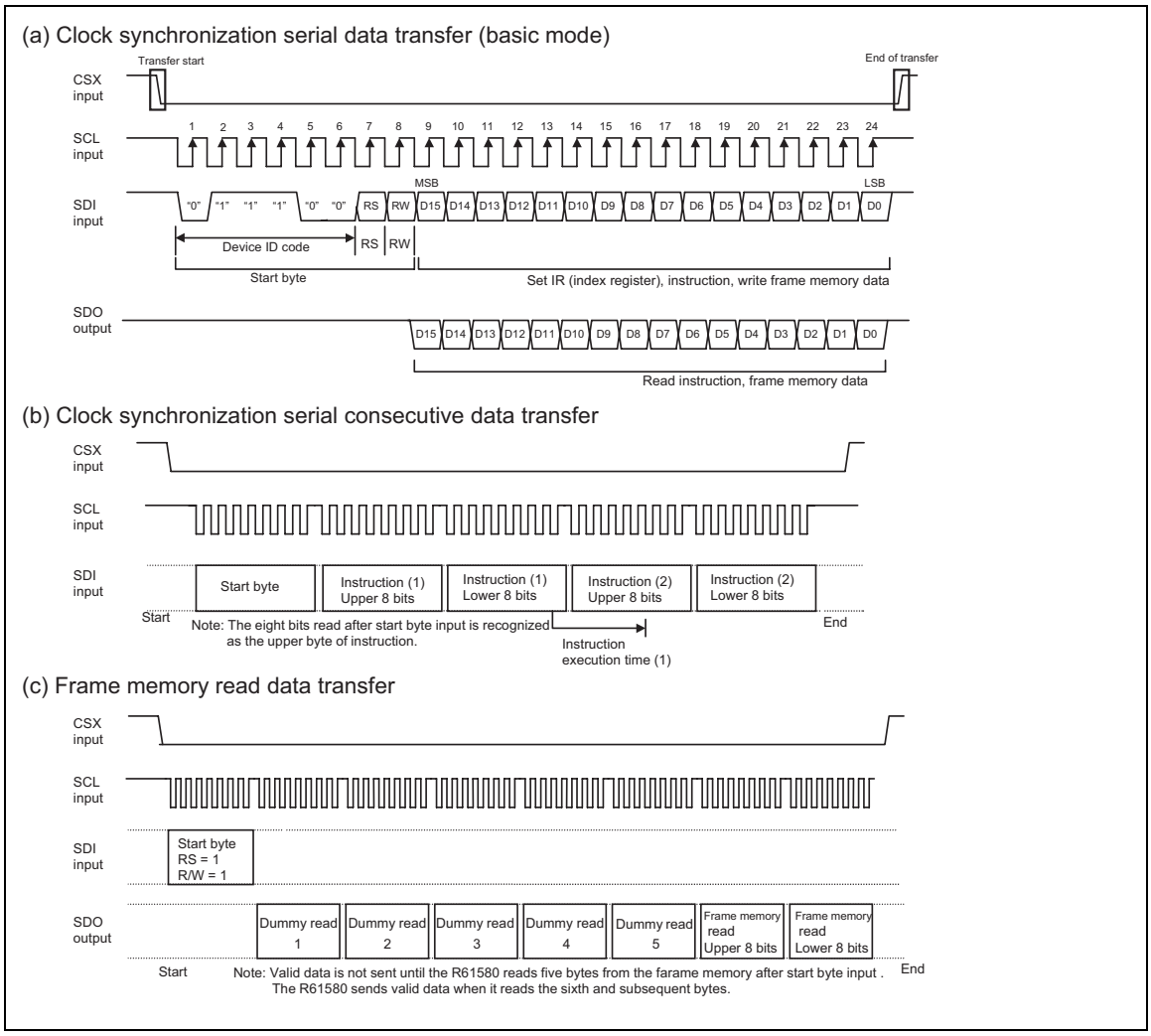


Figure 28 Data Transfer in Serial Interface

VSYNC Interface

The R61580 supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

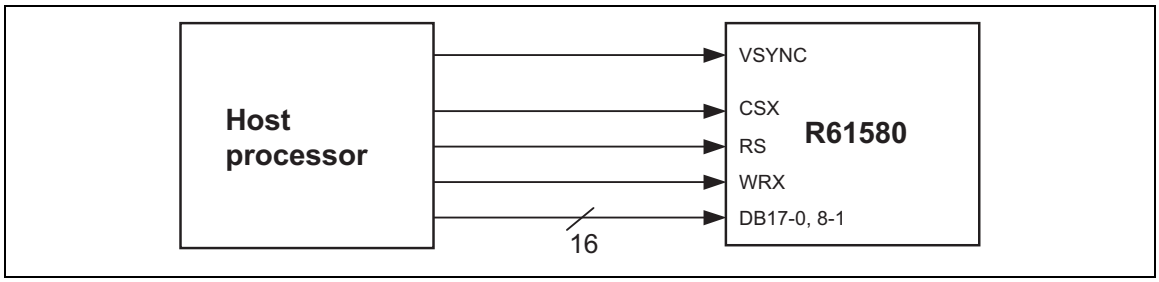


Figure 29 VSYNC Interface

The VSYNC interface is selected by setting DM1-0 = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal frame memory at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal frame memory so that the R61580 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display.

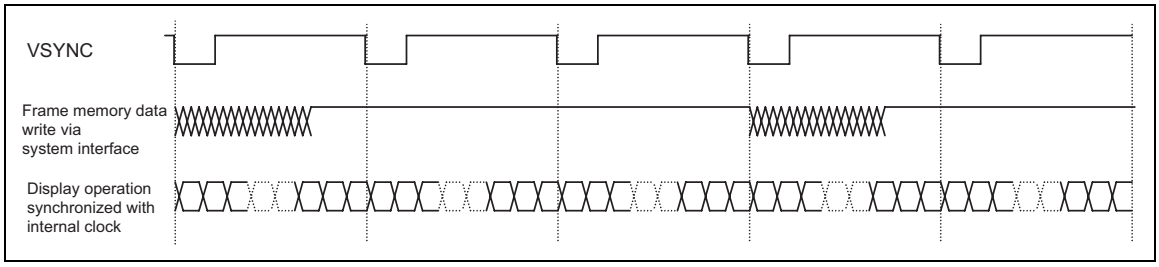


Figure 30 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum for frame memory data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$FrameMemoryWriteSpeed(\min.)[Hz] > \frac{240 \times DisplayLines(NL)}{((BackPorch(BP) + DisplayLines(NL) - m\arg ins) \times DivisionRatio \times ClockPer1H) \times \frac{1}{fosc}}$$

Note: When frame memory write operation does not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of frame memory write operation must also be taken into account.

An example of calculating minimum frame memory writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Panel size	240 RGB × 320 lines (NL = 6'h27: 320 lines)
Total number of lines (NL)	320 lines
Back/front porch	13/3 lines (BP = 8h'D, FP = 8'h3)
Frame frequency	60 Hz
Maximum internal oscillation frequency	678kHz x 1.07 = 726kHz
Clock division ratio (DIVE)	1
Number of clock per 1H period (RTNE)	30

RTN*: RTNI or RTNE. DIV*: DIVI or DIVE.

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±7% for variances and guarantee that display operation is completed within one VSYNC cycle.

2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for frame memory write [Hz]
> 240 × 320 / {((13 + 320 – 2) lines × 1 × 30 clocks) × 1/726 kHz} = 5.63MHz

Notes: 1. In this example, it is assumed that the R61580 starts writing data in the internal frame memory on the falling edge of VSYNC.

2. There must be at least a margin of 2 lines between the line to which the R61580 has just written data and the line where display operation on the LCD is performed.

In this example, the frame memory write operation at a speed of 5.63MHz or faster, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before

the R61580 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

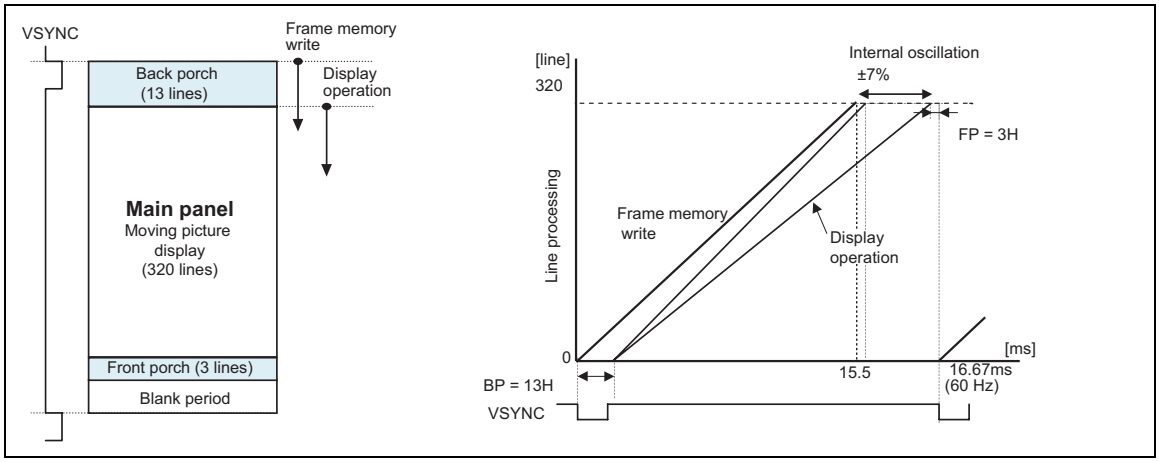


Figure 31 Write/Display Operation Timing via VSYNC Interface

Notes to VSYNC Interface Operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Have enough margins in setting frame memory write speed for VSYNC interface operation.

2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

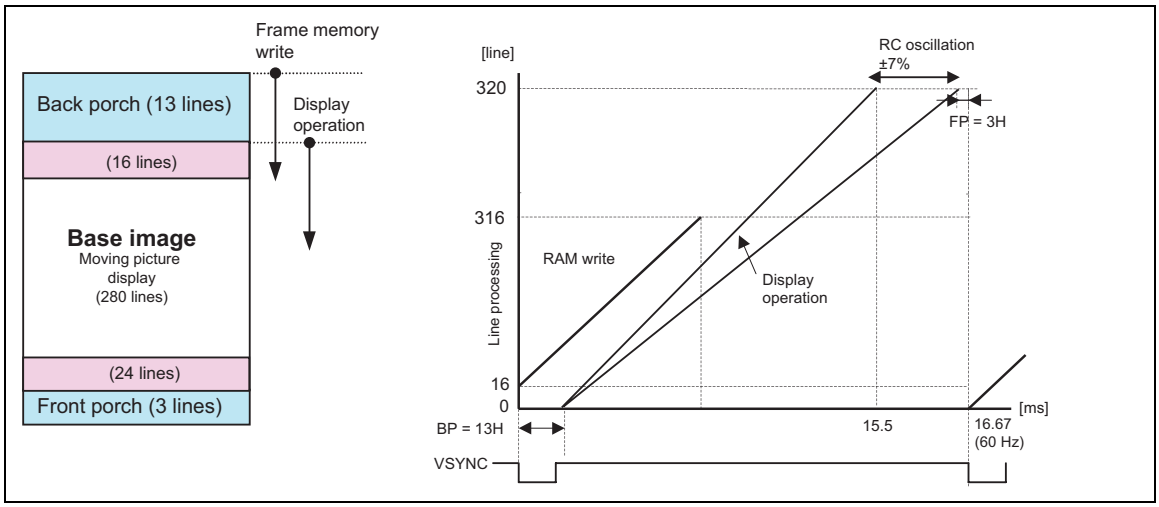


Figure 32 Frame Memory Write Speed Margins

3. The front porch period continues from the end of one frame period to the next VSYNC input.
4. The instructions to switch from internal clock operation (DM1-0 = 00) to VSYNC interface operation modes and vice versa are enabled from the next frame period.
5. The partial display and vertical scroll functions are not available in VSYNC interface operation.
6. In VSYNC interface operation, set AM = 0 to transfer display data correctly.

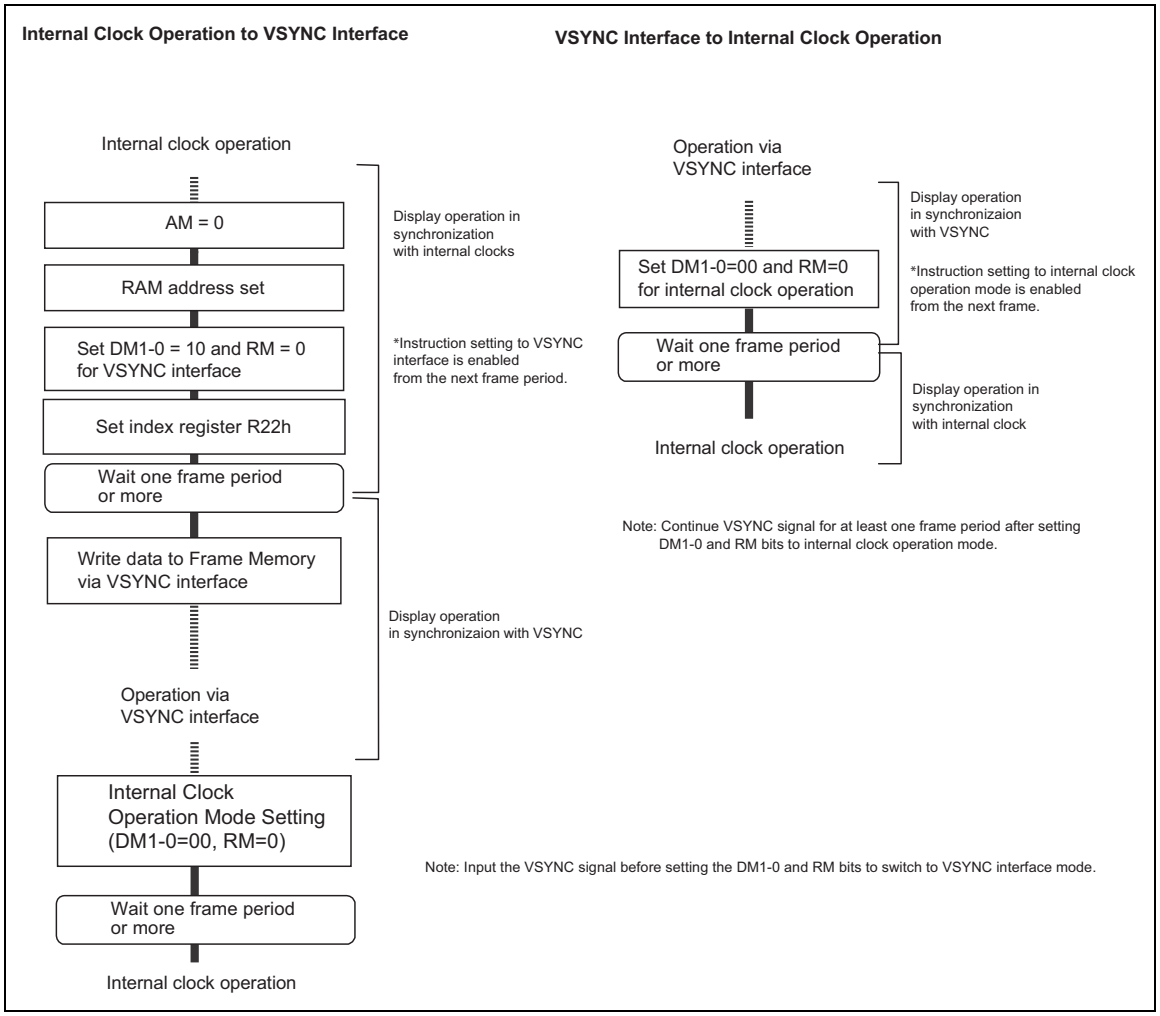


Figure 33 Sequences to Switch between VSYNC and Internal Clock Operation Modes

FMARK Interface

In the FMARK interface operation, data is written to internal frame memory via system interface synchronizing with the frame mark signal (FMARK), realizing tearing less video image while using conventional system interface. FMARK output position is set in units of line using FMP bit. Set the bit considering data transfer speed.

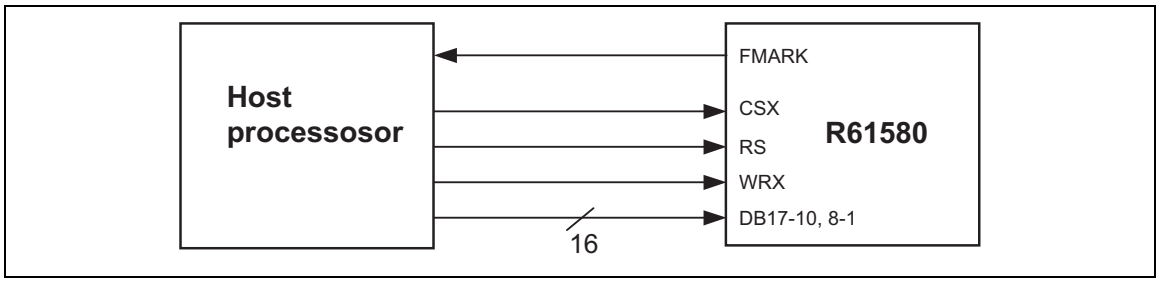


Figure 34 Display Synchronous Data Transfer Interface

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture frame memory area without causing flicker on the display.

The data is written in the internal frame memory. Therefore, when moving picture is displayed, data is written only to the moving picture display area without using RGB or VSYNC interface, minimizing number of data transfer required for moving picture display.

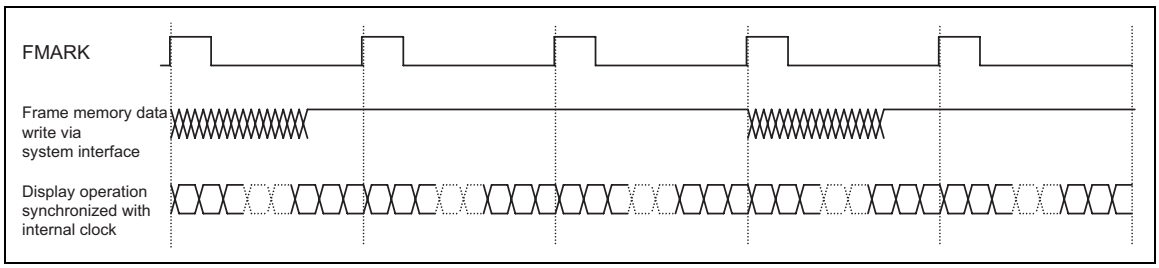


Figure 35 Moving Picture Data Transfers via FMARK Function

When transferring data in synchronization with FMARK signal, minimum frame memory data write speed must be taken into consideration. They must be more than the values calculated from the following equations.

$$FrameMemoryWriteSpeed(\min.)[Hz] > \frac{240 \times DisplayLines(NL)}{(FP + BP) + DisplayLines(NL) - m\arg ins) \times DivisionRatio(DIVE) \times ClockPer1H(RTNE) \times \frac{1}{fosc}}$$

Notes: When frame memory write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of frame memory write operation must also be taken into account. RTN*: RTNI or RTNE. DIV*: DIVI or DIVE.

Examples of calculating minimum frame memory data write speed is as follows. The above calculation shows frame memory write speed per 1 pixel and is different from write speed defined by data transfer format of each interface.

[Example]

Panel size	240 RGB × 320 lines
Total number of lines (NL)	320 lines
Back/front porch	13/3 lines (BP = 8h'D, FP = 8'h3)
Frame marker position (FMP)	Display end line (320th line)
Frame frequency	60 Hz
Maximum internal operation clock	678kHz x 1.07 = 726kHz
Clock division ratio (DIVE)	1
Number of clock per 1H period (RTNE)	30

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±7% for variances and guarantee that display operation is completed within one FMARK cycle.

2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for frame memory writing [Hz]
> 240 × 320 / {((3 + 13 + 320 – 2) lines × 1 × 30 clocks) × 1/726kHz} = 5.57MHz / pixel

Notes: 1. In this example, it is assumed that the R61580 starts writing data in the internal frame memory on the rising edge of FMARK.
2. There must be at least a margin of 2 lines between the line to which the R61580 has just written data and the line where display operation on the LCD is performed.
3. The FMARK signal output position is set to the line specified by register.

In this example, frame memory write operation at a speed of 5.57MHz/pixel or faster, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the R61580 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

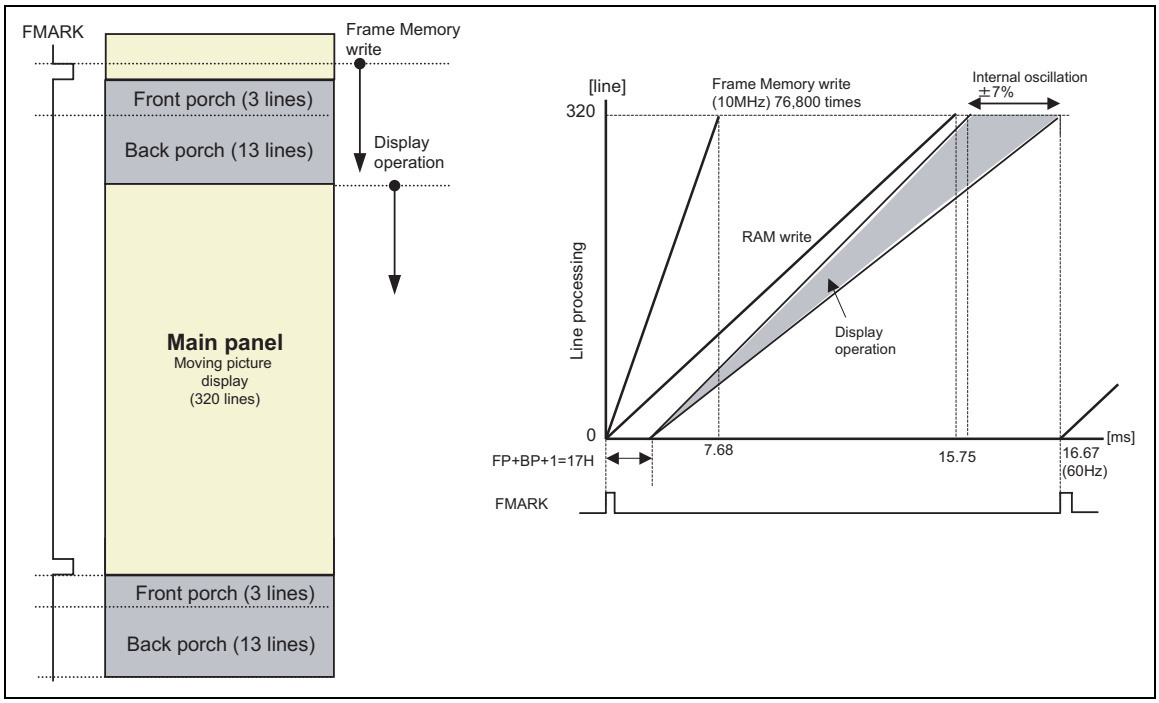


Figure 36

Note to display operation synchronous data transfer using FMARK signal

The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margins in setting frame memory write speed for this operation.

FMP Bit Setting

The host processor detects FMARK signal outputted at the position defined by FMP bit. The R61580 outputs an FMARK pulse when the R61580 is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

The FMARK output interval is set by FMI[2:0] bits. Set FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. This setting is enabled when FMARKOE = 1.

Table 79

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1st line
9'h002	2nd line
:	:
9'h14D	333rd line
9'h14E	334th line
9'h14F	335th line
9'h150 ~ 1FF	Setting disabled

Table 80

FMI[2]	FMI[1]	FMI[0]	FMARK output interval
0	0	0	1 frame period
0	0	1	2 frame periods
0	1	1	4 frame periods
1	0	1	6 frame periods
Other setting			Setting disabled

FMP Setting Example

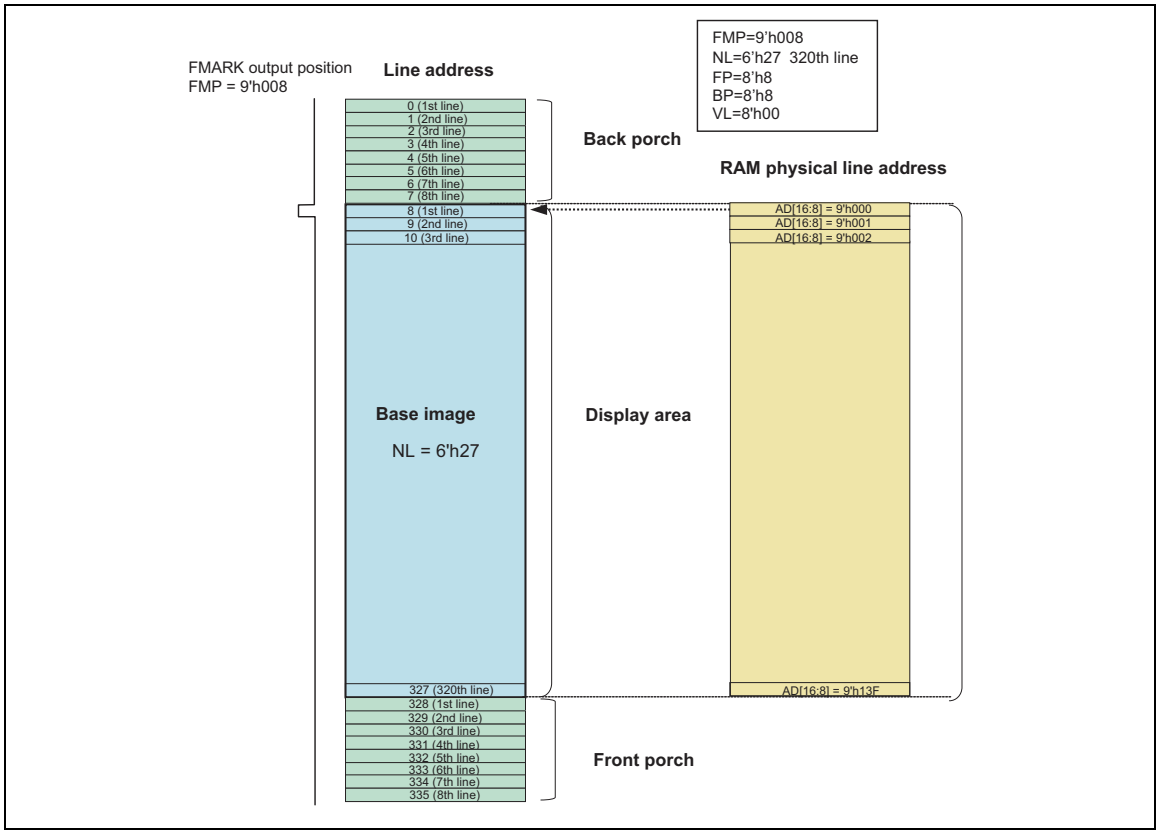


Figure 37

External Display Interface

The R61580 supports the RGB interface. The interface format is set by RM[1:0] bits. The internal frame memory is accessible via RGB interface.

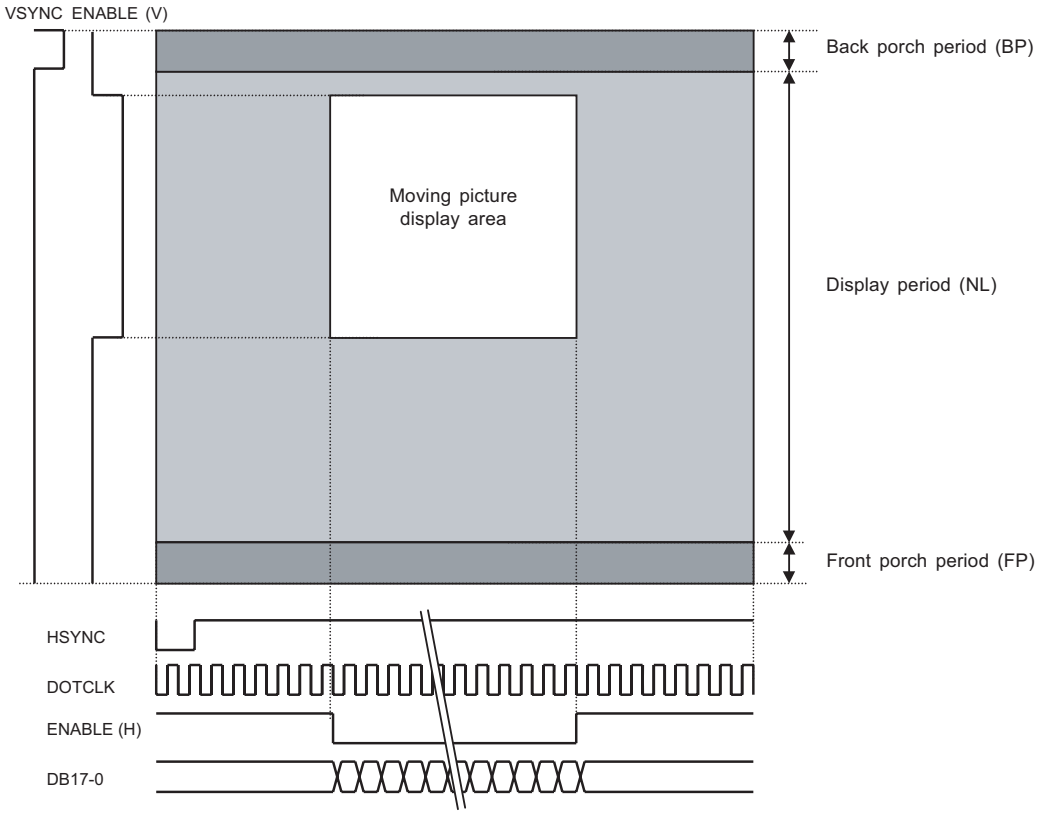
Table 81 RGB Interface

RIM1	RIM0	RGB interface	DB pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, DB11-1
1	0	Setting inhibited	-
1	1	Setting inhibited	-

Note: Using more than two interfaces at the same time is prohibited.

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The data can be written only within the specified area with low power consumption by using window address function. In RGB interface operation, front and back porch periods must be made before and after the display period.



VSYNC: Frame synchronization signal	Back porch period (BP):	14H ≧ BP ≧ 2H
HSYNC: Line synchronization signal	Front porch period (FP):	14H ≧ FP ≧ 3H
DOTCLK: Dot clock		FP + BP ≦ 16H
ENABLE: Data enable signal	Display period:	NL ≦ 320H
DB 17-0: RGB (6:6:6) display data	The number of lines for one frame:	FP + NL + BP

Notes: 1. The front porch period continues until next VSYNC input is detected.
2. Make sure to match the VSYNC, HSYNC, and DOTCLK frequencies to the resolution of liquid crystal panel.

Figure 38 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals can be changed by setting the DPL, EPL, HSPL, and VSPL bits respectively for convenience of system configuration.

RGB Interface Timing

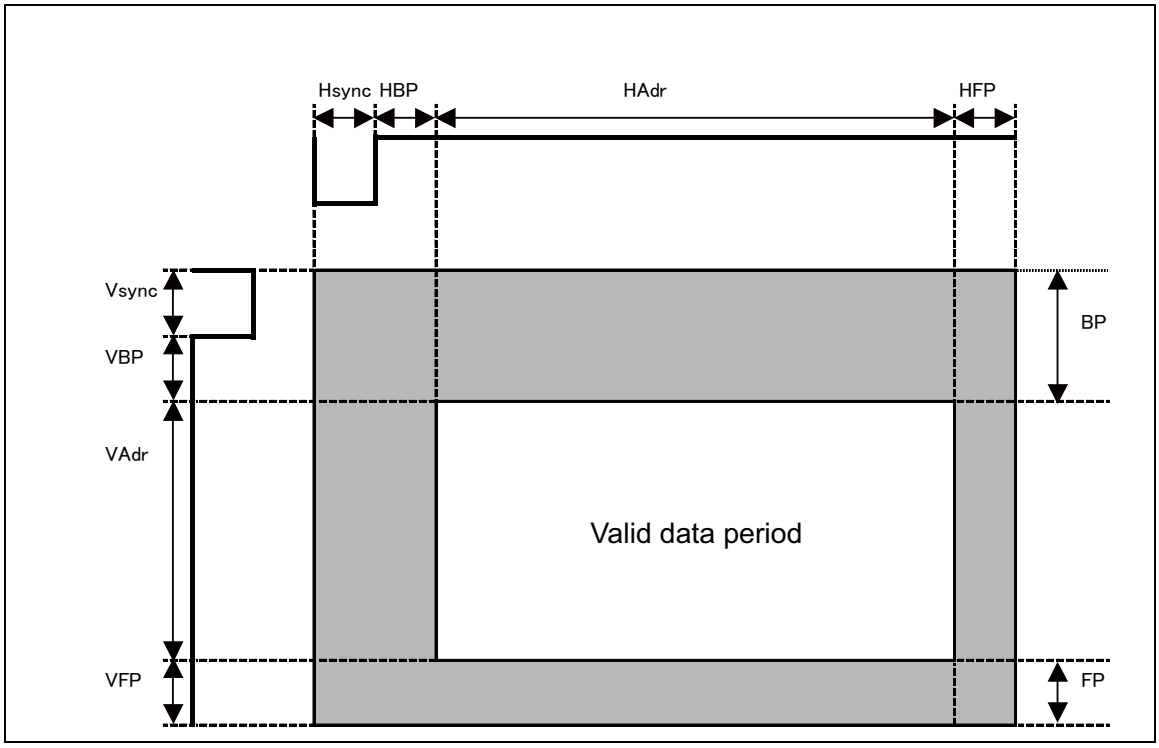


Figure 39

Table 82

Parameters	Symbols	Min.	Typ.	Max.	Step	Unit
Horizontal Synchronization	Hsync	2	10	16	1	DOTCLKCYC
Horizontal Back Porch	HBP	2	20	24	1	DOTCLKCYC
Horizontal Address	HAdr	—	240	—	1	DOTCLKCYC
Horizontal Front Porch	HFP	2	10	16	1	DOTCLKCYC
Vertical Synchronization	Vsync	1	2	4	1	Line
Vertical Back Porch	VBP	1	2	—	1	Line
Vertical Address	VAdr	—	320	—	1	Line
Vertical Front Porch	VFP	3	4	—	1	Line

Notes: 1. Typ. is the setting example under the following usage conditions (resolution of the panel = QVGA 240 x 320, clock frequency = 5.64 MHz, frame frequency = about 60 Hz).

2. In case of setting, make sure (Number of DOTCLK in 1H period) ≥ RTNE[5:0] (number of clocks) × DIVE[1:0] (Division ratio) × (PCDIVL + PCDIVH). The setting example is shown in next page.

Setting Example of Display Control Clock in RGB Interface Operation

Register

The display operation is performed by the internal clock (DOTCLKD) generated by dividing the frequency of DOTCLK.

PCDIVH[2:0] defines number of DOTCLK during DOTCLKD is high in the units of 1clock.
PCDIVL[2:0] defines number of DOTCLK during DOTCLKD is low in the units of 1clock.

Also, write PCDIVH and PCDIVL values so that DOTCLKD frequency is the closest to internal oscillation clock frequency (678KHz). Make sure that PCDIVL＝PCDIVH or PCDIVH-1. Make sure that (number of DOTCLKs in 1H) ≥ RTNE (number of clocks) * DIVE (division ratio) * (PCDIVL + PCDIVH).

Setting example: in case of setting the frame frequency to 60Hz

Internal clock: Internal oscillation clock = 678kHz
DIVI = 2'b1 (1/2)
RTN = 17 clocks
FP = 8'h8, BP = 8'h8, NL = 6'h27 (320 lines)
→ 59.34Hz

DOTCLK: Hsync = 10 clocks
HBP = 20 clocks
HFP = 10 clocks
60Hz × (8+320+8) lines × (10+20+240+10) clocks = 5.64MHz
DOTCLK frequency = 5.64MHz
5.64MHz / 678kHz = 8.3 → Write PCDIVH and PCDIVL values so that DOTCLK frequency is divided into 8.
5.64 / 8 = 705kHz
(705kHz / 2) / 17 clocks / 336 lines = 61.7Hz

PCDIVH: 3'h4
PCDIVL: 3'h4

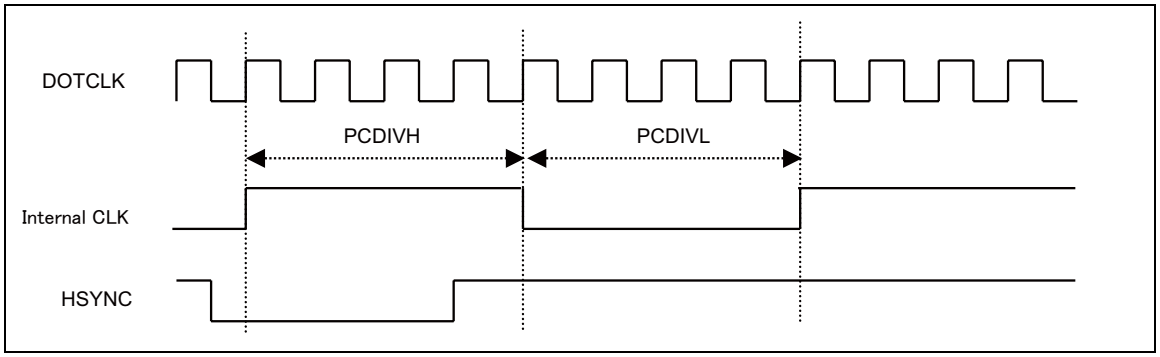


Figure 40

RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

16-/18-bit RGB Interface Timing

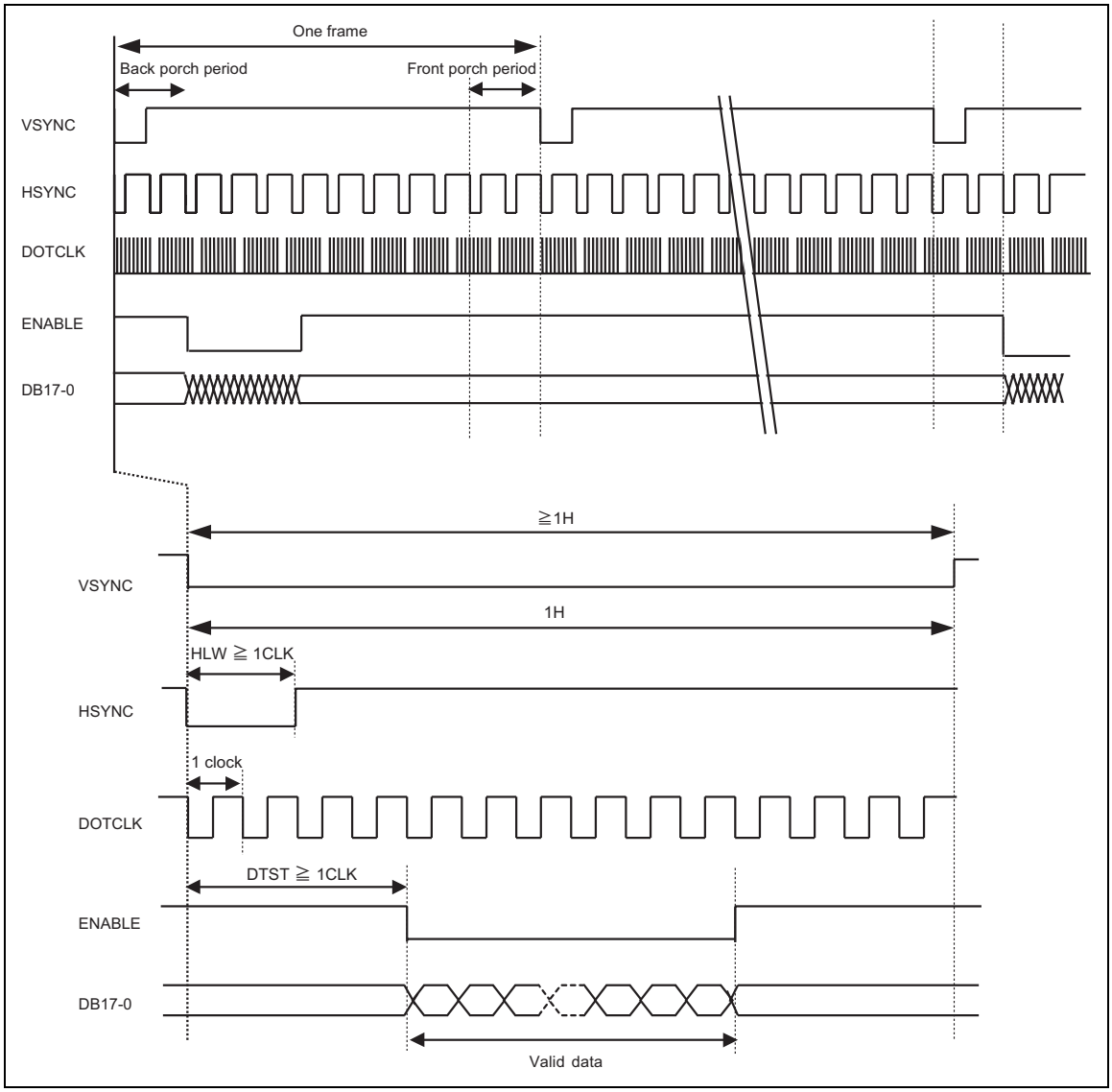


Figure 41

Note: VLW: VSYNC Low period
HLW: HSYNC Low period
DTST: Data transfer setup time

Moving Picture Display via RGB Interface

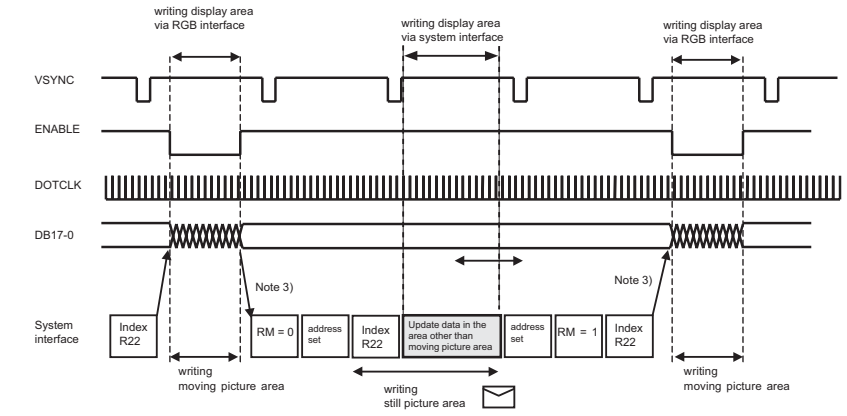
The R61580 supports RGB interface for moving picture display and incorporates frame memory for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function enables transferring data only within the moving picture area
2. It becomes possible to transfer only the data written over the moving picture area
3. By reducing data transfer, it can contribute to lowering the power consumption of the whole system
4. The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface

Frame Memory Access via System Interface in RGB Interface Operation

The R61580 allows frame memory access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal frame memory in synchronization with DOTCLK while ENABLE is "Low". When writing data to the frame memory via system interface, set ENABLE "High" to stop writing data via RGB interface. Then set RM = "0" to enable frame memory access via system interface. When reverting to the RGB interface operation, wait for the read/write bus cycle time. Then, set RM = "1" and the index register to R22h to start accessing frame memory via RGB interface. If there is a conflict between frame memory accesses via two interfaces, there is no guarantee that the data is written in the frame memory.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.



Notes: 1. In RGB interface operation, frame memory address defined by AD bits is set in the address counter on the falling edge of VSYNC.
2. Set AD bits and the index R22h before starting frame memory access via RGB interface.
3. When switching to the system interface operation after writing data via RGB interface, wait at least one write cycle (tcycw).

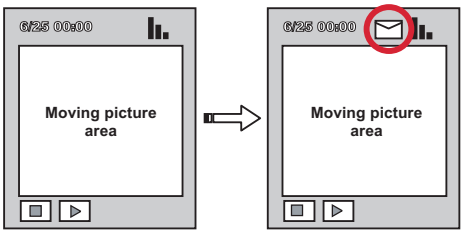


Figure 42 Updating the Still Picture Area while Displaying Moving Picture

16-bit RGB Interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal frame memory in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows frame memory access via RGB interface.

Instruction bits can be transferred only via system interface.

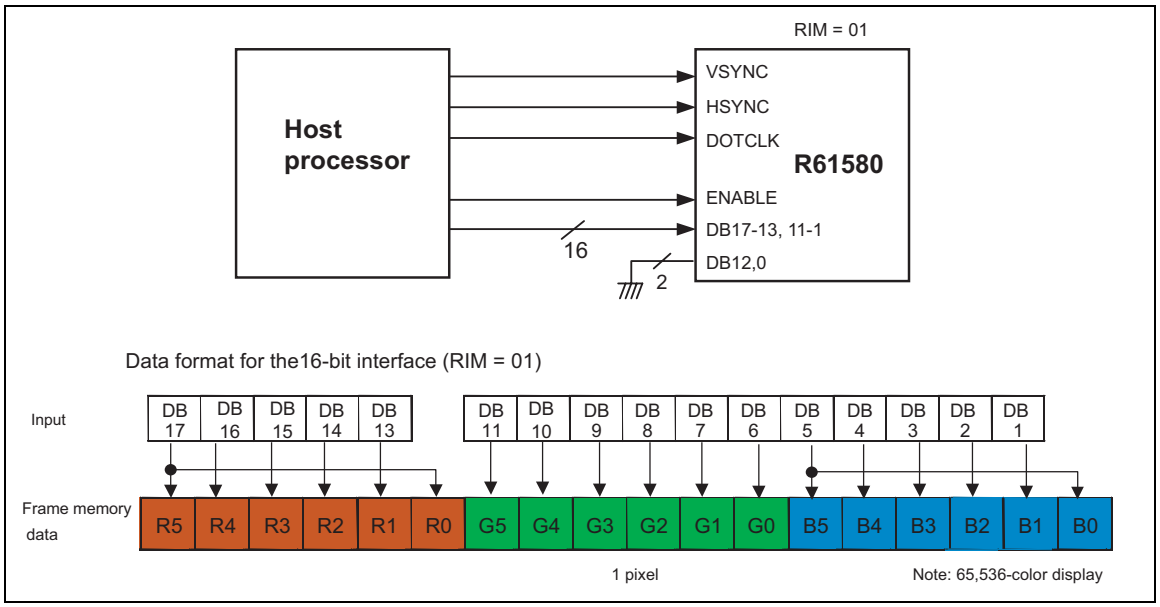


Figure 43 Example of 16-Bit RGB Interface and Data Format

18-bit RGB Interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal frame memory in synchronization with the display operation via 18-bit ports (DB17-0) while data enable signal (ENABLE) allows frame memory access via RGB interface.

Instruction bits can be transferred only via system interface.

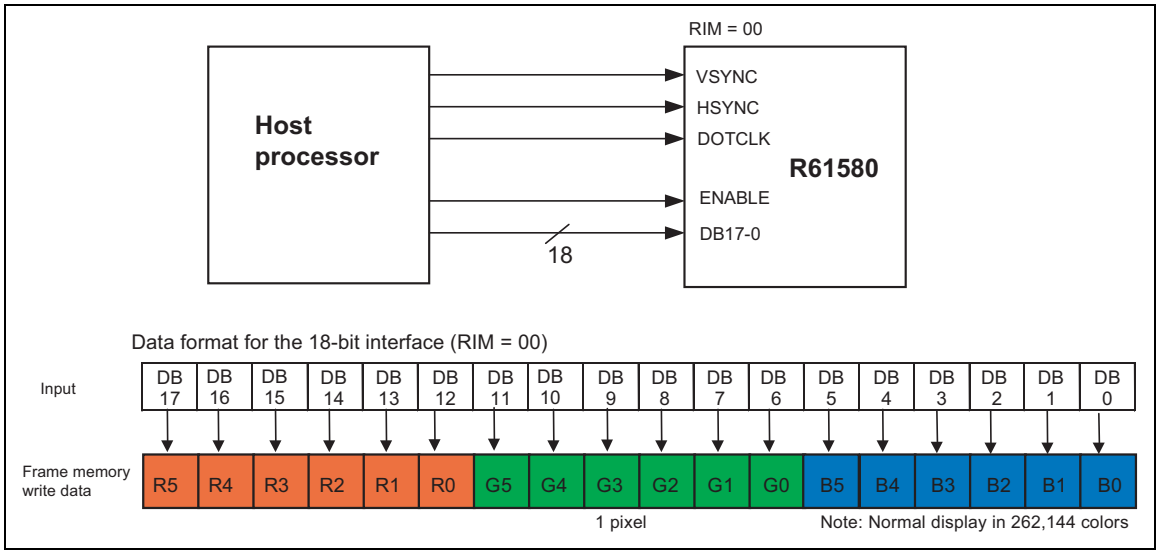


Figure 44 Example of 18-bit RGB Interface and Data Format

Notes to RGB Interface Operation

a. The following functions are not available in external display interface operation.

Table 83 Functions Not Available in External Display Interface Operation

Function	External display interface	Internal display operation
Partial display	Not available	Available
Scroll function	Not available	Available

b. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.

c. The reference clock to generate liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.

d. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

e. In RGB interface operation, front porch period continues after the end of frame period until next VSYNC input is detected.

f. In RGB interface operation, frame memory address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

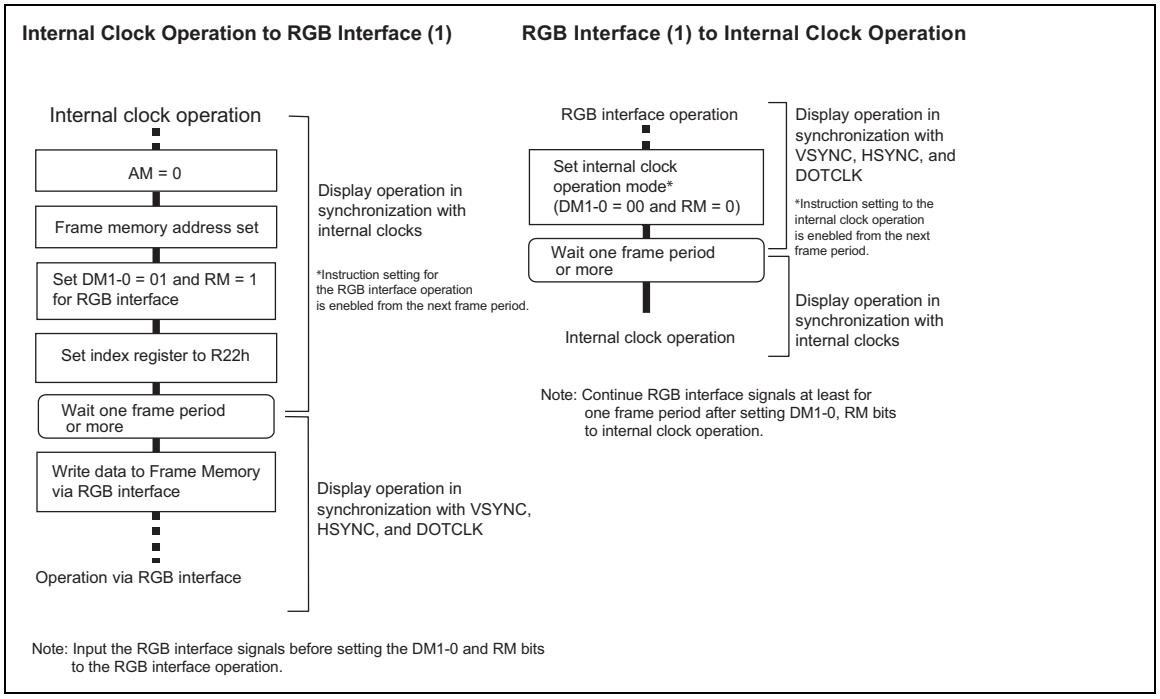


Figure 45 RGB and Internal Clock Operation Mode Switching Sequences

Frame Memory Address and Display Position on the Panel

The R61580 has memory to store display data of 240RGB x 320 lines. The R61580 incorporates a circuit to control partial display, which allows switching driving method between full-screen display mode and partial display mode.

The R61580 makes display arrangement setting and panel driving position control setting separately and specifies frame memory area for each image displayed on the panel. For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set PTSA and PTEA bits to specify the frame memory area for a partial image
2. Set the display position of the partial image on the base image by setting PTDP.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE and PTDE) to display images

Normal display	BASEE = 1, PTDE=0
Partial display	BASEE = 0, PTDE = 1

5. Rewrite BASEE and PTDE bits when switching full display and partial display of the base image.

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing frame memory data.

Table 84

	Display ENABLE	Numbers of lines	Frame Memory area
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h13F)

Notes 1: The base image is displayed from the first line of the screen.
2: Make sure NL ≤ 320 (lines) = BEA – BSA when setting a base image frame memory area. BSA and BEA are fixed to 9'h000, 9'h13F, respectively.

Table 85

	Display ENABLE	Display position	Frame Memory area
Partial image	PTDE	PTDP	(PTSA, PTEA)

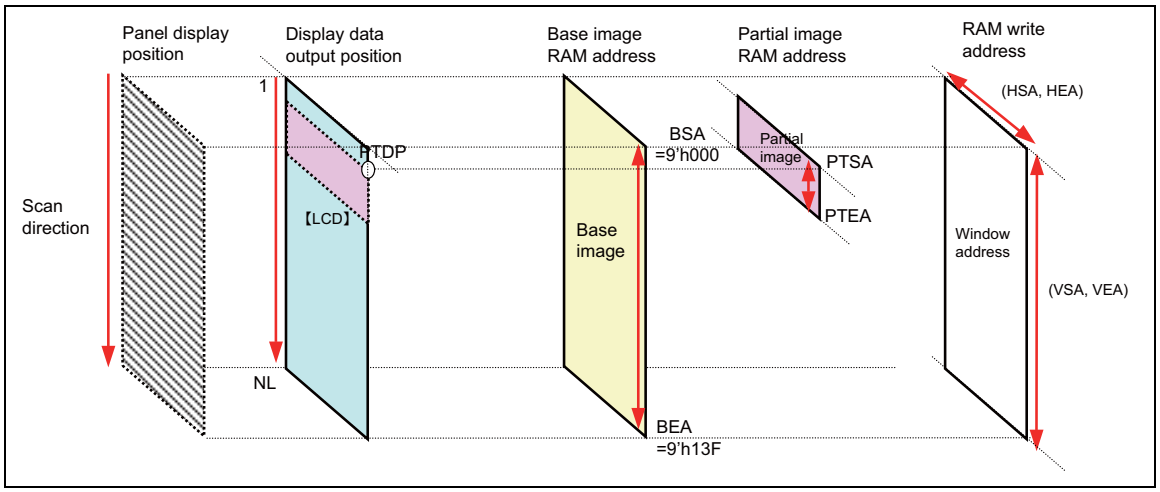


Figure 46 Frame Memory Address, Display Position and Drive Position

Restrictions in Setting Display Control Instruction

There are restrictions in coordinates setting for display data, display position and partial display.

(1) Screen Setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is 320 lines or less (NL ≤ 320 lines).

(2) Base Image Display

1. The base image is displayed from the first line of the screen: BSA = 1st line (of the display panel)
2. The base image frame memory area (specified by BSA = 000, BEA = 13F) must include the same or more number of lines set by NL bits (liquid crystal panel drive lines): BEA – BSA = 320 lines ≥ NL

The following figure shows the relationship among the frame memory address, display position, and the lines driven for the display.

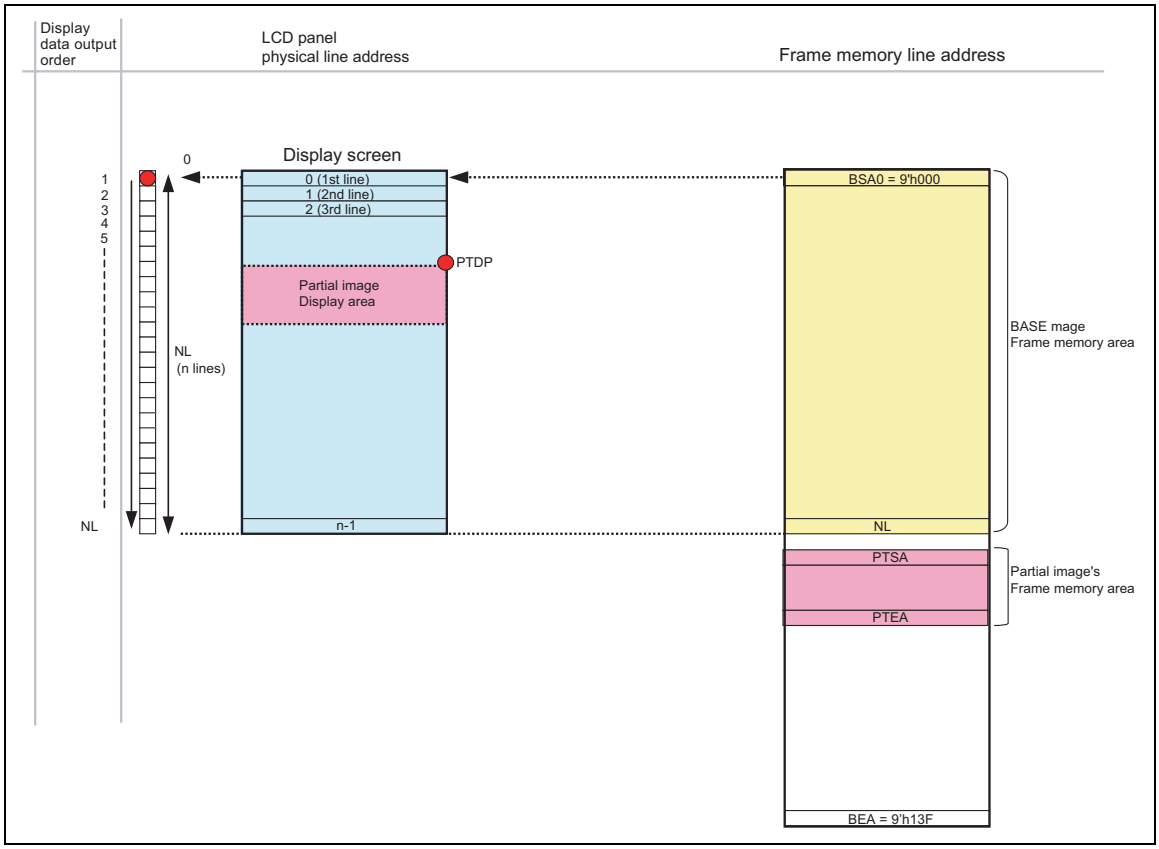


Figure 47 Display Frame Memory Address and Panel Display Position

Note: This figure shows the relationship between frame memory line address and the display position on the panel. In the R61580's internal operation, the data is written in the frame memory area specified by the window address setting registers.

Instruction Setting Example

The followings are examples of settings for 240 (RGB) x 320 (lines) panel.

1. Full Screen Display with no Partial Image

The following is an example of settings for full screen display.

Table 86

Base image display instruction	
BASEE	1
NL[5:0]	6'h27

PTDE	0

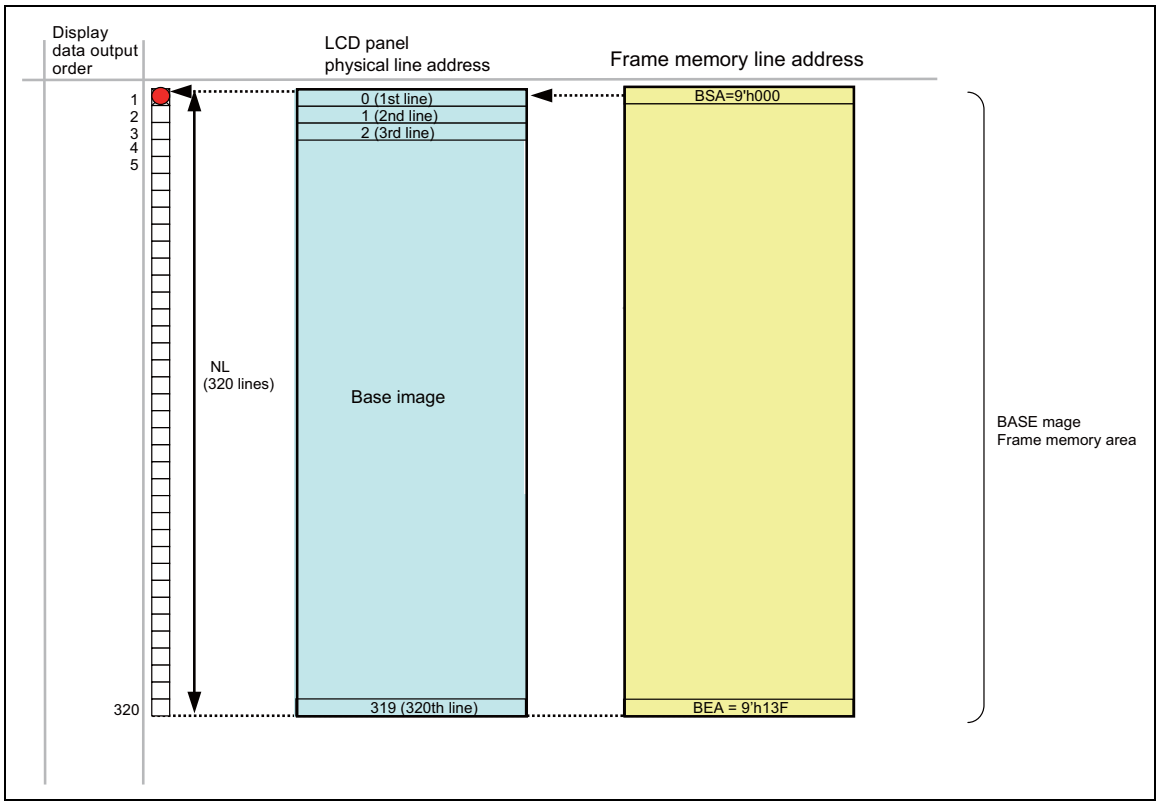


Figure 48 Full Screen Display with no Partial Image

2. Partial Display

The following is an example of settings for displaying only partial image and turning off the base image. The partial image is displayed at the designated position.

Table 87

Base image display instruction	
BASEE	0
NL[5:0]	6'h27

Partial image display instruction	
PTDE	1
PTSA [8:0]	9'h000
PTEA [8:0]	9'h00F
PTDP [8:0]	9'h080

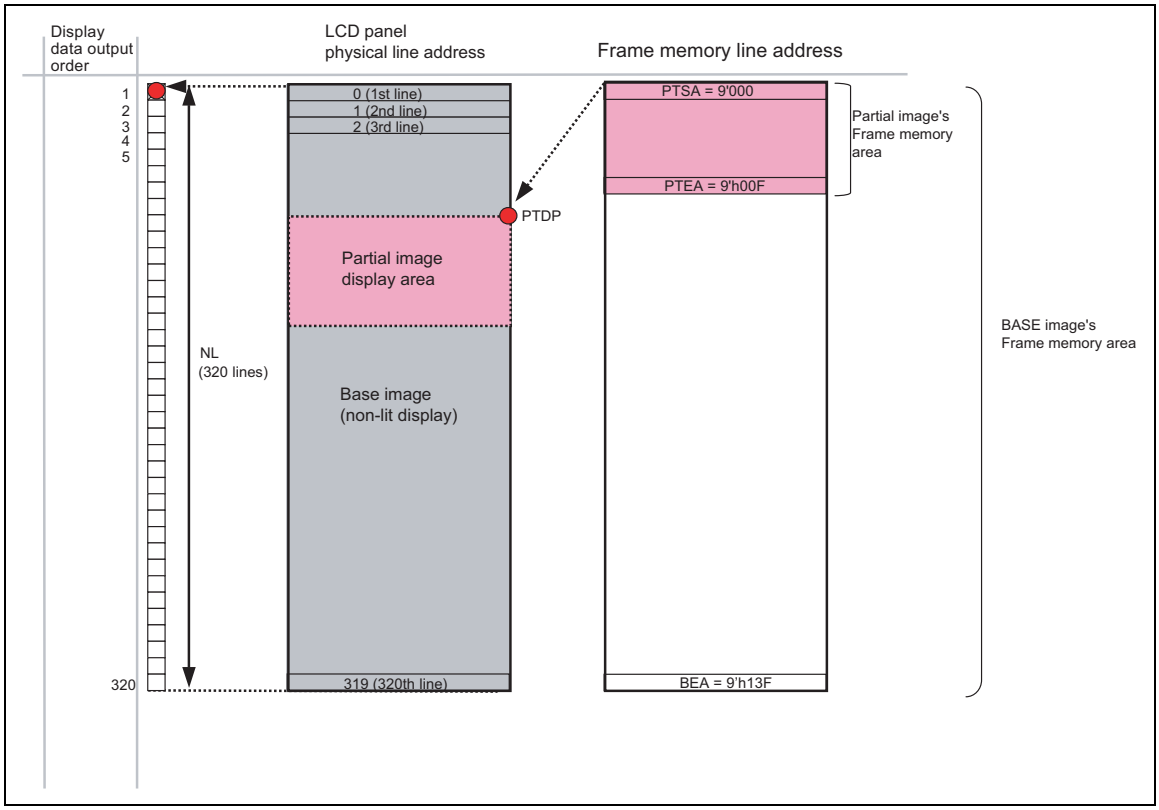


Figure 49 Partial Display

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal frame memory. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of frame memory address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the R61580 to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the frame memory address map area. Also, the AD16-0 bits (frame memory address set register) must be set to an address within the window address area.

[Window address area setting range]
(Horizontal direction) 8'h00 ≤ HSA < HEA ≤ 8'hEF
(Vertical direction) 9'h000 ≤ VSA < VEA ≤ 9'h13F

[Frame Memory Address setting range]
(Frame memory address) HSA ≤ AD [7:0] ≤ HEA
VSA ≤ AD [16:8] ≤ VEA

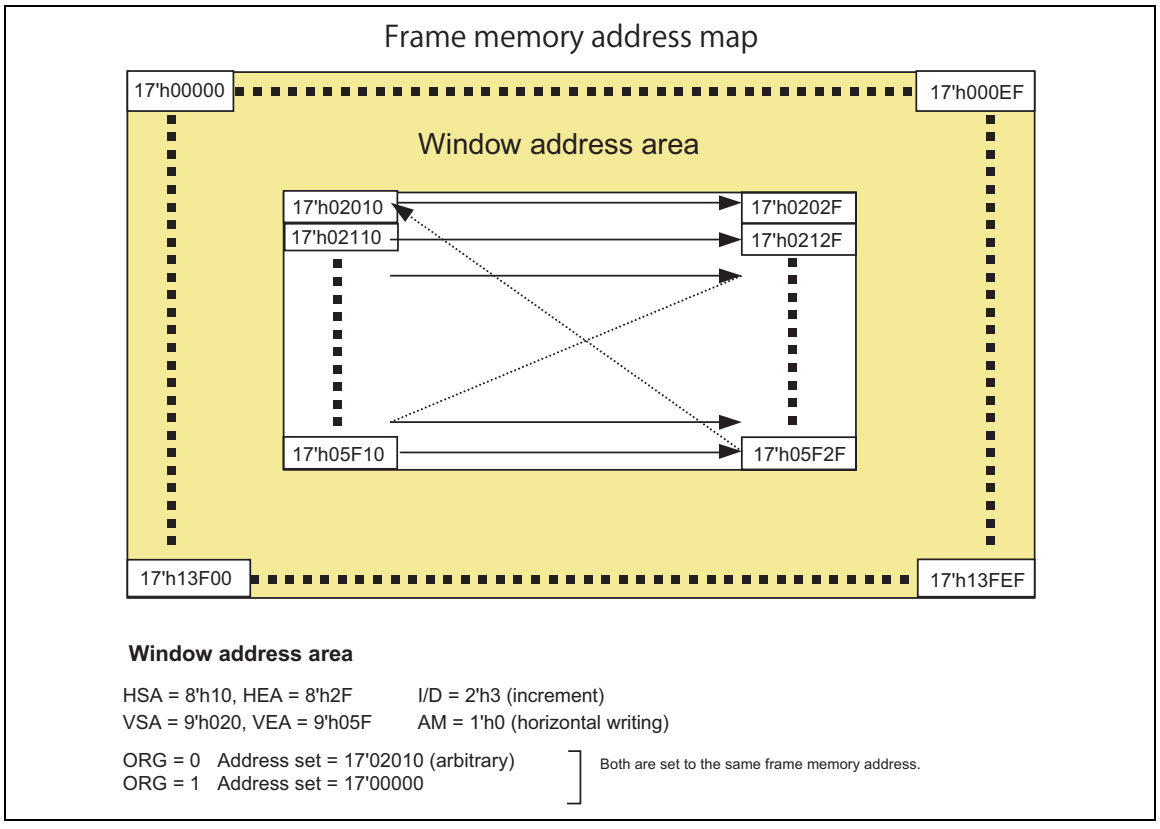
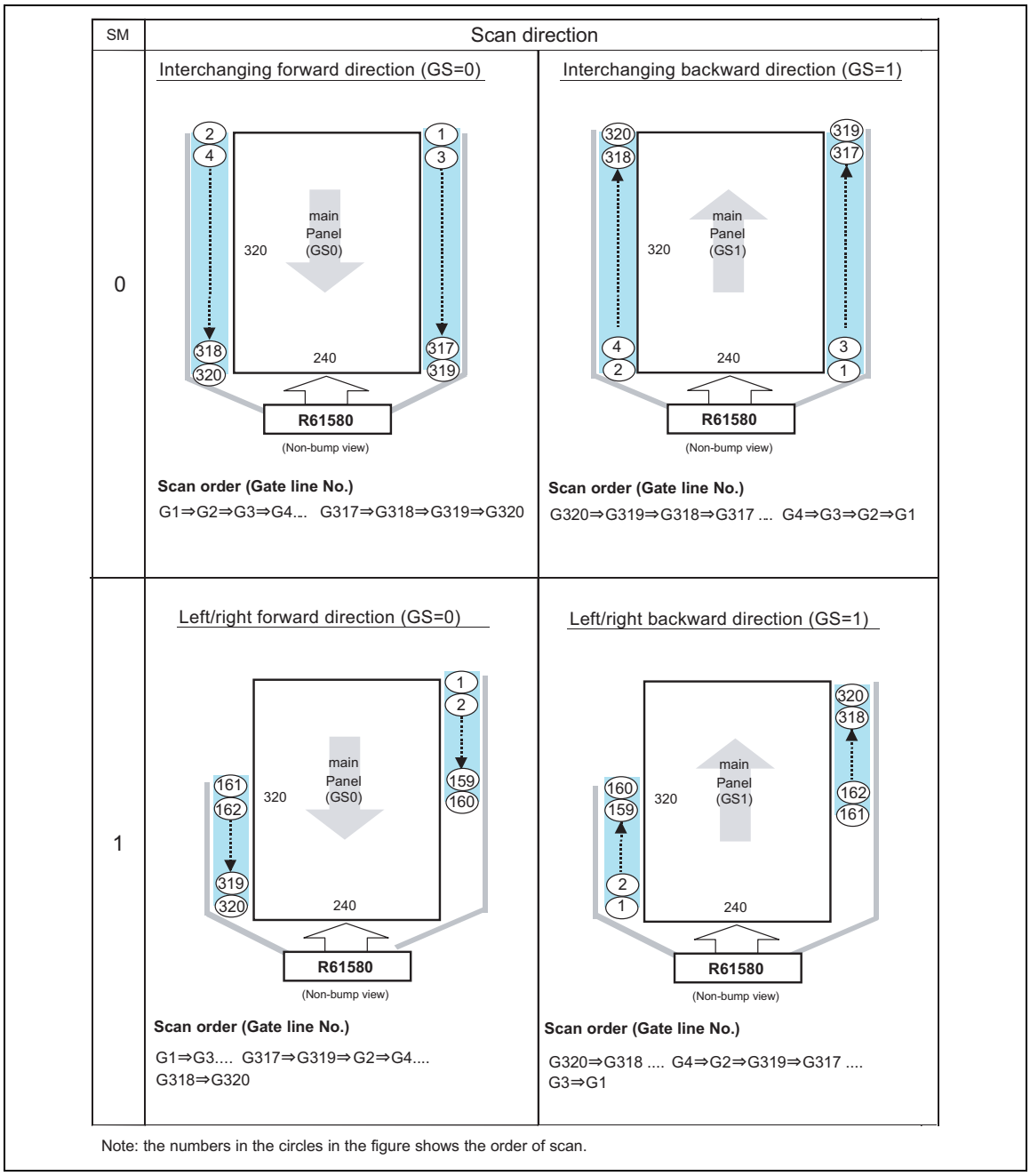


Figure 50 Automatic Address Update within a Window Address Area

Gate Scan Mode Setting

The R61580 can set the gate pin assignment and the scan direction in the following 4 different ways by setting SM and GS bits to realize various connections between the R61580 and the LCD panel.



Note: the numbers in the circles in the figure shows the order of scan.

Figure 51

8-color Display Mode

The R61580 has a function to display in eight colors. In this display mode, only V0 and V63 are used and power supplies to other grayscales (V1 to V62) are turned off to reduce power consumption.

In 8-color display mode, the γ-adjustment registers R30h-R39h are disabled and the power supplies to V1 to V62 halt. The R61580 does not require rewriting frame memory data for 8-color display. Only MSBs of red, green and blue data is used to display image on the panel.

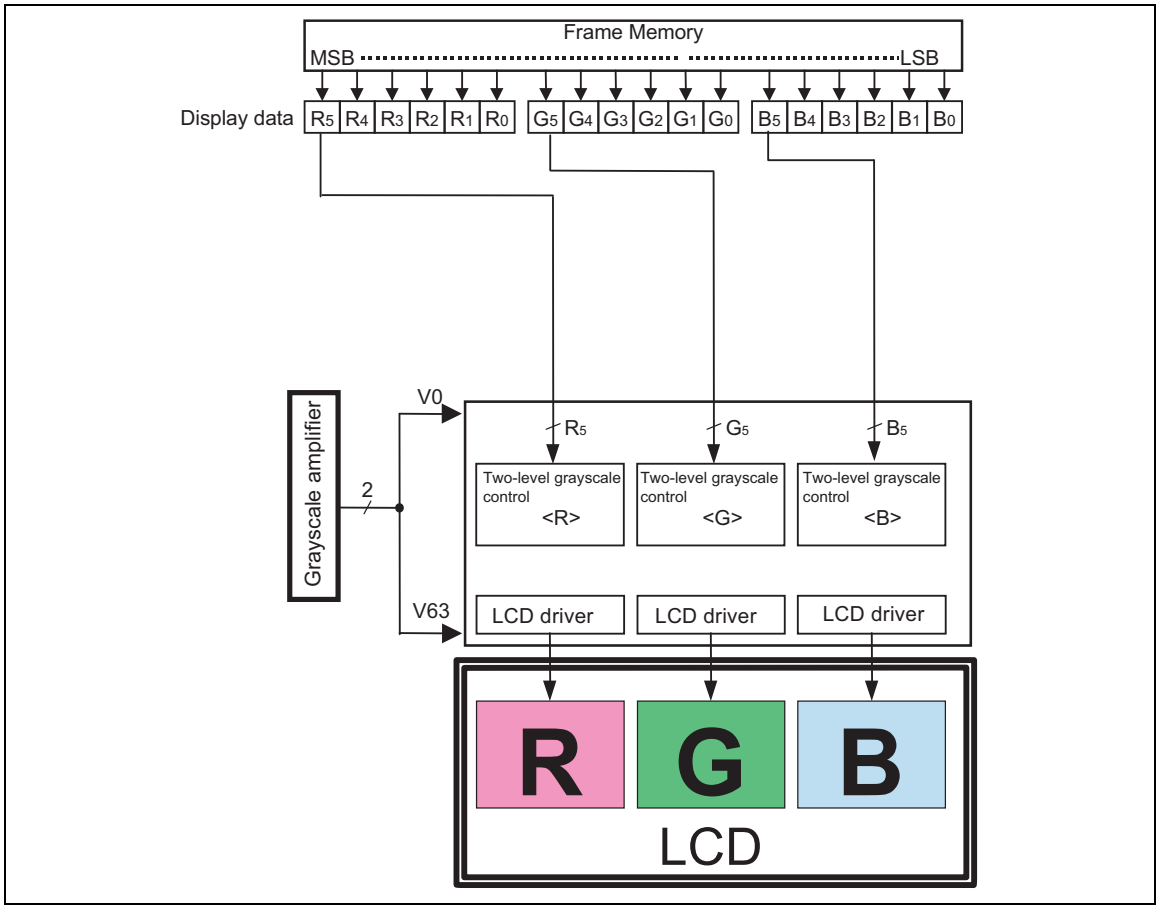


Figure 52 8-color Display Mode

Line Inversion AC Drive

The R61580 supports n-line inversion alternating current drive in addition to frame-inversion liquid crystal alternating current drive. The timing to invert the electric current can be set to either every line or every two lines. Set line number of inversion timing checking display quality on liquid crystal display. Note that less number of line leads to higher inversion frequency of liquid crystal and more charge/discharge battery in liquid crystal display.

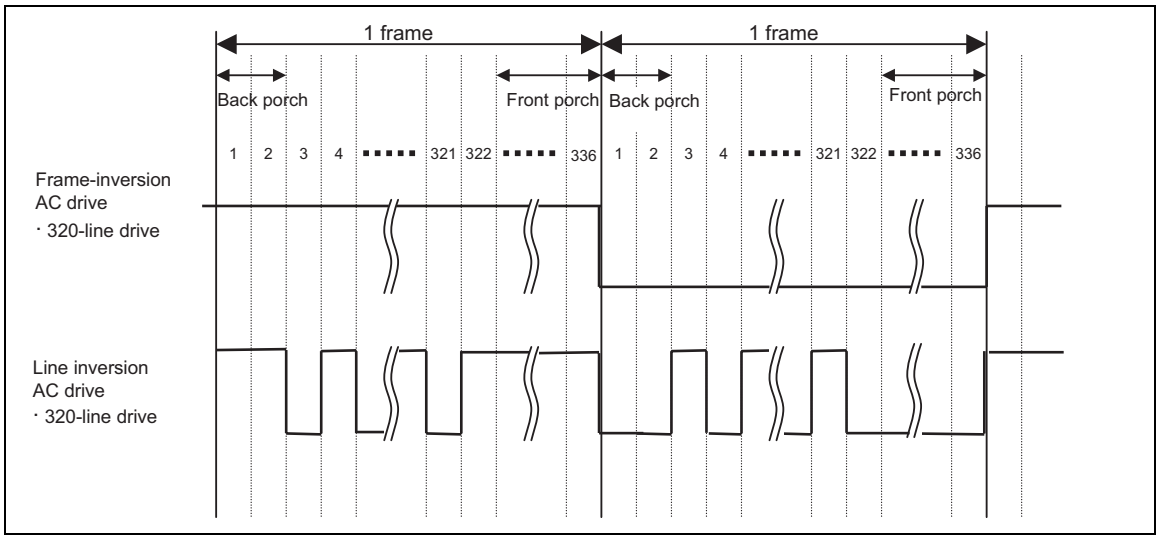


Figure 53 Example of Alternating Signals for n-line Inversion

Note: Polarity of signals does not invert during blank periods, namely back and front porch periods. N-line inversion operation starts from the first line of a display area.

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the R61580 draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In case of line inversion AC drive, selected by setting BC0=1 (R02h), polarity is inverted as the R61580 draws one line, and a blank period lasting for (BP+FP) periods is inserted when the R61580 draws one frame.

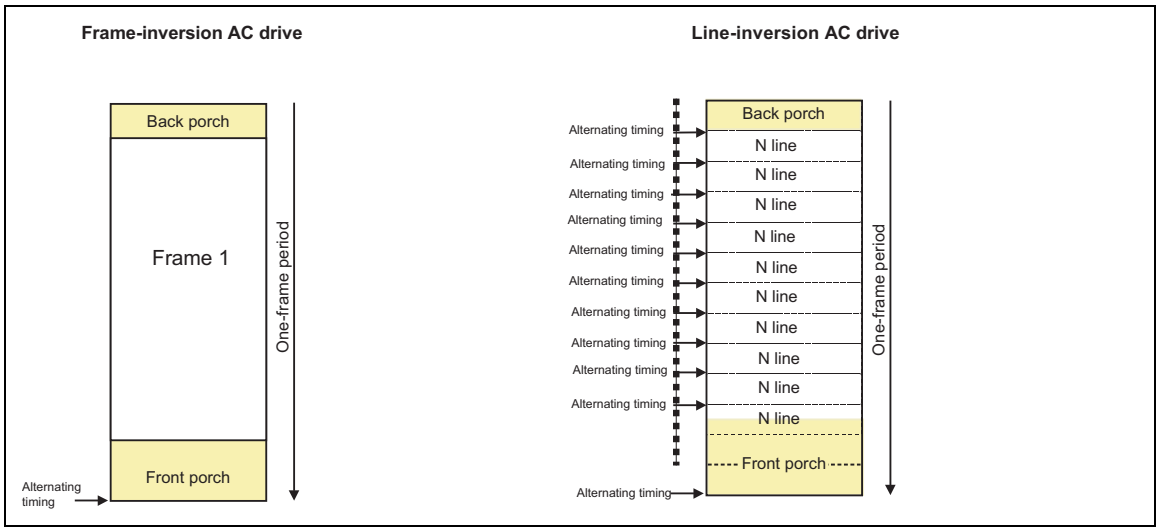


Figure 54 Alternating Timing

Note: Frame inversion AC drive is available only in 8-color display mode. Check the quality of display on the panel.

Frame-Frequency Adjustment Function

The R61580 supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIV, RTN bits without changing the oscillation frequency.

The R61580 allows changing the frame frequency depending on whether moving picture or still picture is displayed on the screen. In this case, set a high oscillation frequency. By changing the DIVI and RTNI settings, the R61580 can operate at high frame frequency when displaying a moving picture, which requires the R61580 to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The following equation represent the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTNI) and the operation clock frequency division ratio setting bit (DIVI).

Equation for calculating frame frequency

$$FrameFrequency(f_{FLM}) = \frac{fosc}{NumberofClocks/line \times DivisionRatio \times (Line + FP + BP)}[Hz]$$

fosc: clock frequency for internal operation (678kHz)
Number of clocks per line: RTNI bit
Division ratio: DIVI bit
Line: number of lines to drive the LCD panel (NL bit)
Number of lines for front porch : FP
Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

fosc: 678kHz
Number of lines: 320 lines
1H period: 17 clock cycles (RTNI[4:0] = “11”)
Division ratio of operating clock: 2
Front porch: 8 lines
Back porch: 8 lines

f_{FLM} = 678kHz/(17 clocks x 1/2 x (320 + 8 + 8) (lines) ≒ 60Hz

Partial Display Function

The partial display function allows the R61580 to drive lines selectively to display partial image by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

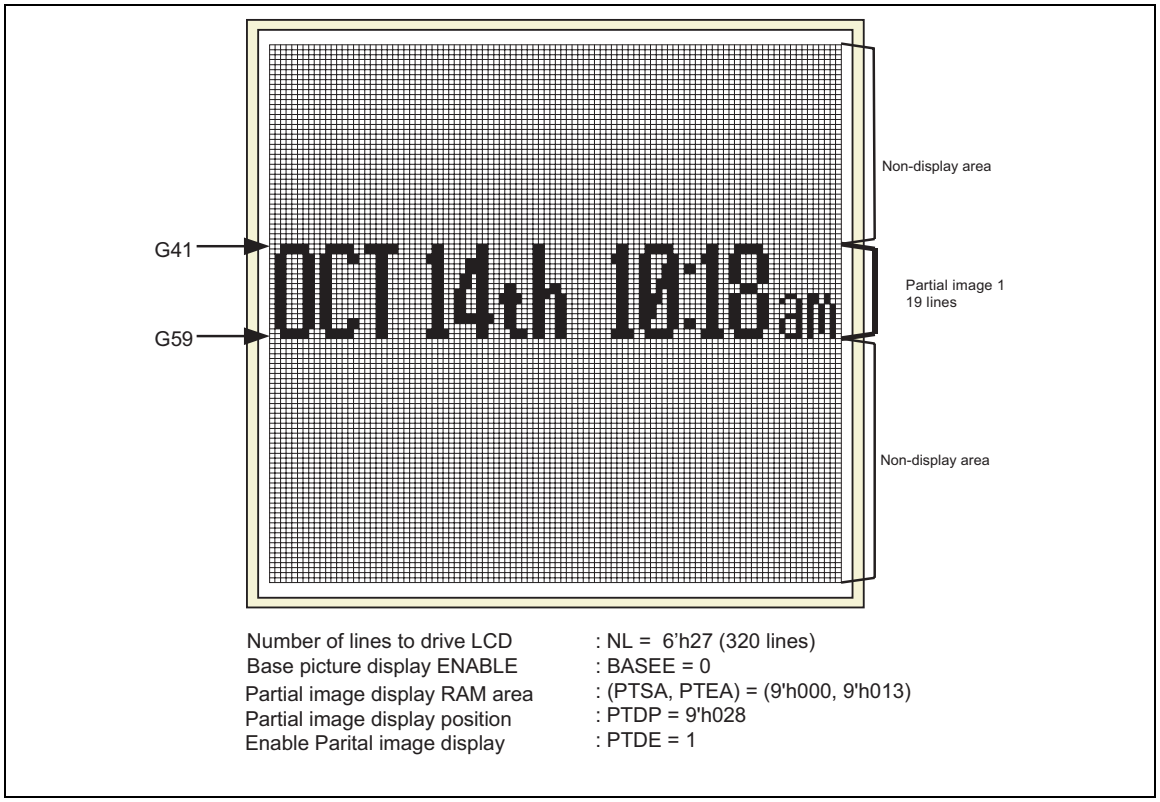


Figure 55 Partial Display Example

Note: See the "Frame Memory Address and Display Position on the Panel" for details on the relationship between the display positions of partial images and respective frame memory area setting.

Dynamic Backlight Control Function

The R61580 supports BLC (backlight control) function to control brightness of backlight and to process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image.

The display image is dynamically controlled by BLC function. The availability of this function ranges from moving picture such as TV image to still picture such as menu. The histogram of display data is analyzed by BLC function, according to the brightness range of backlight set by parameters. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image.

Note 1: The BLC setting is enabled by BLCON bit setting (B8h: Back Light Control).

Note 2: The effect of BLC function on power efficiency and display quality depends on image data and the setting. Check display quality on the panel.

Note 3: The BLC function is disabled in Idle Mode On and Display Invert Mode On. Use BLC function (BLCON = 1) in Idle Mode Off and Display Invert Mode Off.

- Control backlight dynamically according to the image histogram.
- PWM pin for LED backlight adjustment
- PWM signal control register set by the host processor. Backlight dimmer is adjusted by calculating internally decided PWM value and maximum PWM value from the host processor.

System Configuration

1. The PWM signal is used to directly control the R61580 and LED driver IC. The LED driver IC is controlled entirely via the R61580.

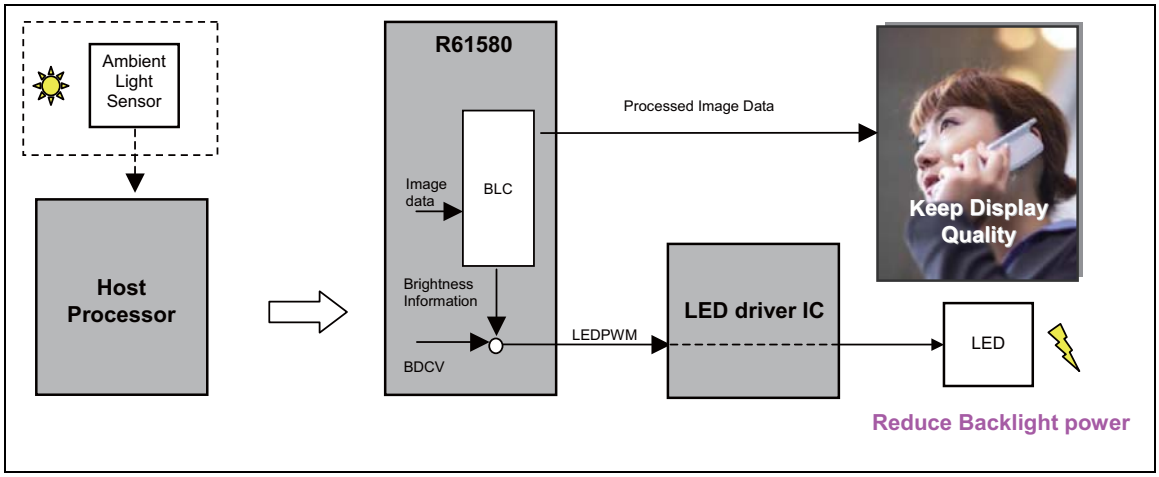


Figure 56

2. The host processor reads LED brightness information internally generated by BLC processing from the R61580 via MIPI DBI. Then, the LED driver IC is controlled from the host processor. There is the time difference between brightness adjustment by PWM and displaying data processed from the R61580. Check the effect on the image.

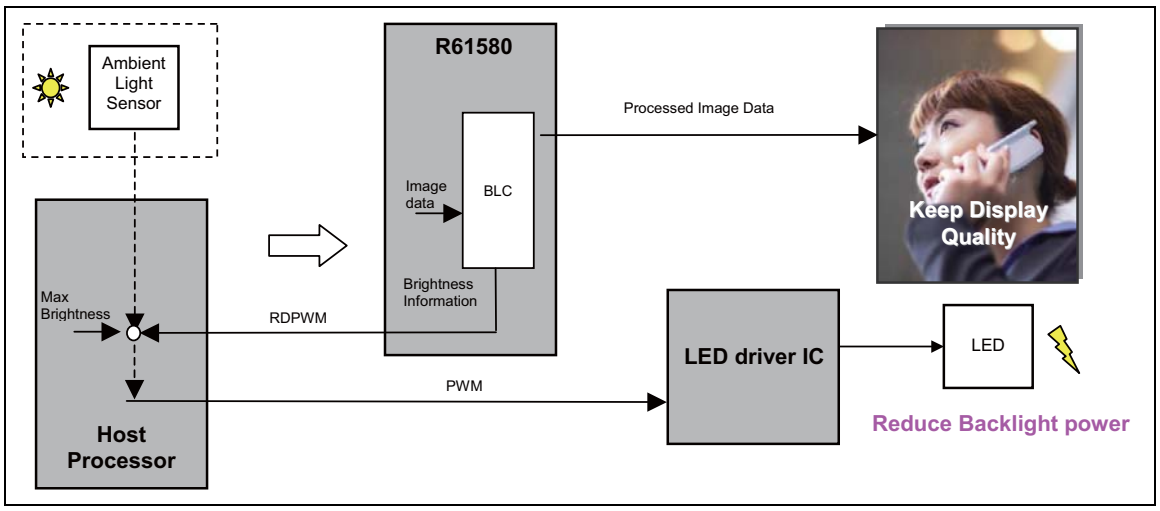


Figure 57

BLC Parameter Setting

The backlight control function has the following two functions.

- Image processing and backlight control processing
- Retain the grayscale of the display image that is turned into white

These functions are set by the following parameters.

(1) BLC operating threshold (THREW)

(2) Set the amount of change of threshold grayscale value (Dth) per frame (PITCHW[3:0])

(3) Difference between two grayscale values counted by the histogram counter (CGAPW)

(4) Backlight brightness adjustment range (ULMTW and LLMTW)

(5) Gamma conversion table (TBL_MIN and TBL[7:0])

(6) Interpolation to prevent display image from being white (COEFK)

(1) THREW[4:0]

This parameter sets the ratio (percentage) of the maximum number of pixels that makes display image white (= data “63) to the total of pixels by image processing. The ratio can be set from zero percent to sixty two percent in units of two percent. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (Dth) that makes display image white is set so that the number of the pixels set by this parameter does not change.

To reduce the power by about 30 percent, set the above ratio to thirty percent (THREW = 5'h0F). When the value set by this parameter exceeds the range of Dth mentioned later, the priority is given to the range of threshold grayscale value (Dth).

According to the relationship between threshold grayscale value (Dth) and gamma conversion table (see (5)), the rate of backlight brightness reduction (= the rate of power reduction) and image correction factor are set.

- The larger THREW value tends to enhance the effect of reducing backlight power, and increases the image correction factor. In this case, the effect on display image increases (see note 1).
- The smaller THREW value tends to reduce the effect of reducing backlight power, and decreases the image correction factor. In this case, the effect on display image decreases (see note 1).

Notes: 1. The tendency for backlight power reduction and the effect on image by BLC function depend on image data. Check display quality.
2. The histogram analysis result is enabled from the next frame.

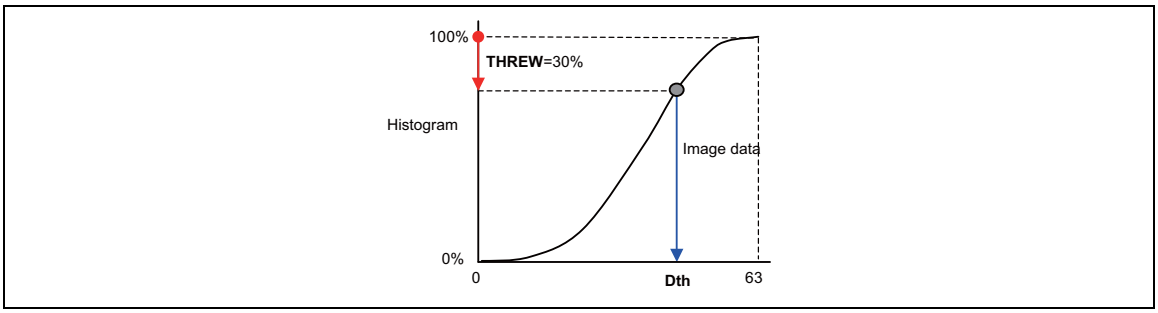


Figure 58

(2) PITCHW[3:0]

This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one eighth of the grayscale. When the target (Dth_t) is changed by the histogram change of input image including video image, this parameter can adjust the amount of changing threshold grayscale value (Dth). So, this parameter is effective in reducing sharp change of backlight brightness.

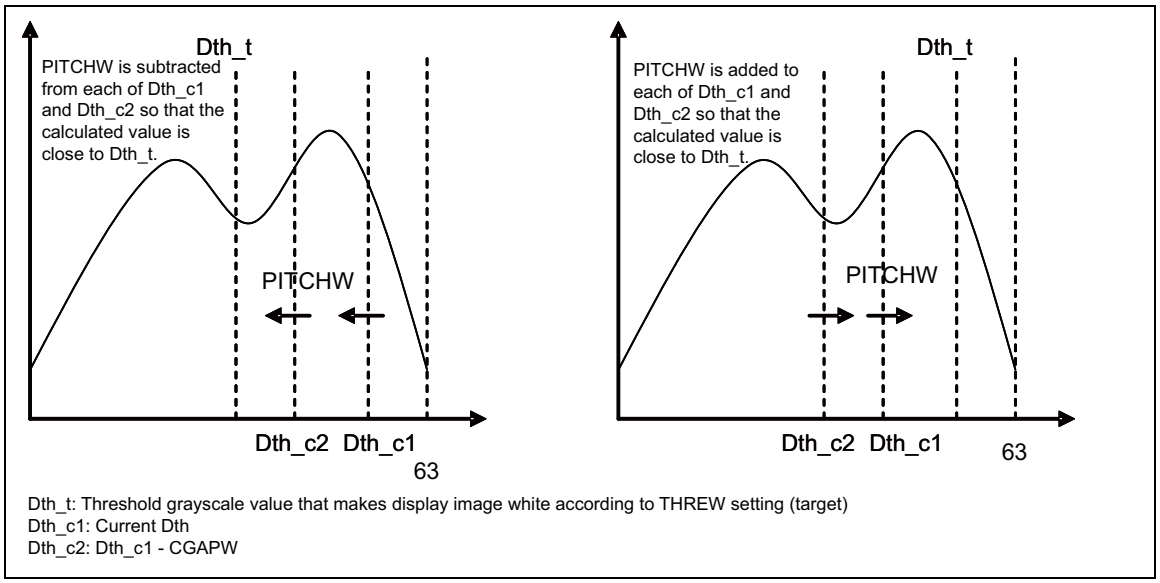


Figure 59

(3) CGAPW[4:0]

The difference of the two grayscales (Dth_c1 and Dth_c2) counted by the present threshold counter is set in units of one eighth of the grayscale. This parameter is effective in slowing the change of threshold grayscale value (Dth). So, the speed of the change of Dth is adjusted to reduce subtle change and flicker.

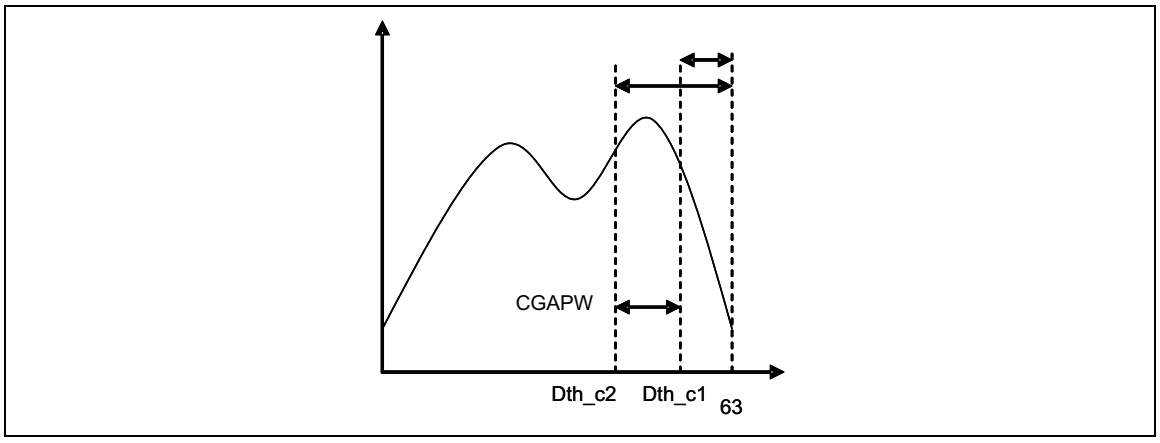


Figure 60

(4) ULMTW[5:0], LLMTW[5:0]

The possible range of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale. ULMTW and LLMTW set the maximum grayscale and the minimum grayscale, respectively. Dth can be changed within the range set by ULMTW and LLMTW.

When there is no effect in saving power consumption due to a large number of pixels displaying white color, that is, in a case such as GUI, the R61580 can save power consumption by setting ULMTW lower than the maximum grayscale if saving power consumption precedes the display quality.

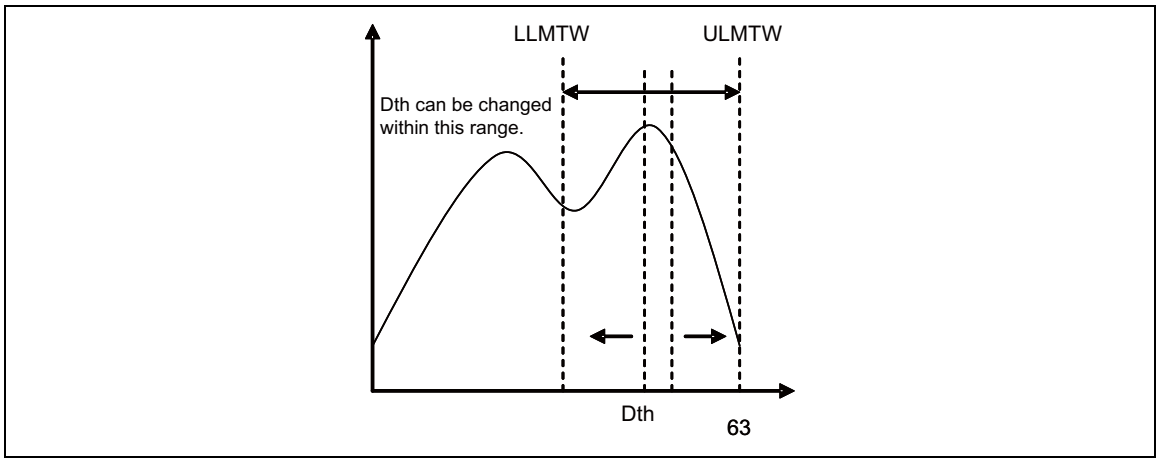


Figure 61

(5) TBL_*[7:0]

The reference value used for interpolation calculation in gamma table are set by 8-bit TBL_*[7:0]. Interpolation is performed as follows. First, nine grayscale values are specified by TBL_*[7:0]. Then, the output data corresponding to the input data to thirty one grayscale values specified at even interval between the adjacent two grayscale values of the nine grayscale values specified by TBL_*[7:0] is calculated by linear interpolation.

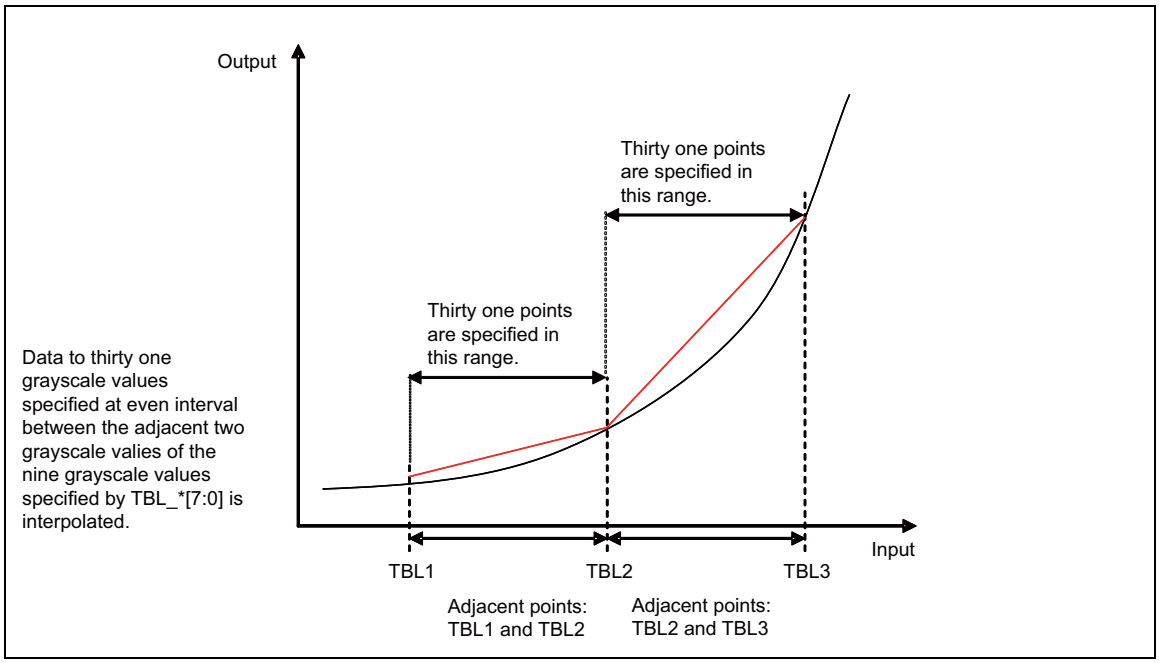


Figure 62

The table setting value is calculated by the following formula according to panel gamma value.

Table setting value = 255 x (table input grayscale / 255) ^ gamma

As the input table grayscale, the above calculation formula is applied to the nine grayscale values (grayscales 0, 31, 63, 95, 127, 159, 191, 223 and 255) to calculate the table values. The table value is set as TBL*. The following table is applied to the case that gamma is set to 2.2.

Table 88

Register	TBL_NIN	TBL0	TBL1	TBL2	TBL3	TBL4	TBL5	TBL6	TBL7
Table input grayscale	0	31	63	95	127	159	191	223	255
Table setting value	0	2	12	29	55	90	135	190	255

(6) COEFK[4:0]

This register sets the range of the grayscale that prevent display image from being white, according to the ratio of the grayscale mentioned here to the grayscale number that makes data white. The ratio can be set from 0 percent to 100 percent. The first grayscale (S) that starts grayscale interpolation to prevent display image from being white is calculated by this register and Dth. Then, the number of grayscales between this grayscale (S) and the maximum grayscale is calculated by interpolation function, and it is used as image processing pixel value.

The larger COEFK[4:0] setting value increases the number of grayscales available in interpolation and relatively decreases the contrast between interpolation sections. As a result, the gamma value changes, and then, the brightness decreases. Also, the color of the section changes. In interpolation factor, there is a trade-off between contrast between interpolation section and the interpolation that the gamma value changes.

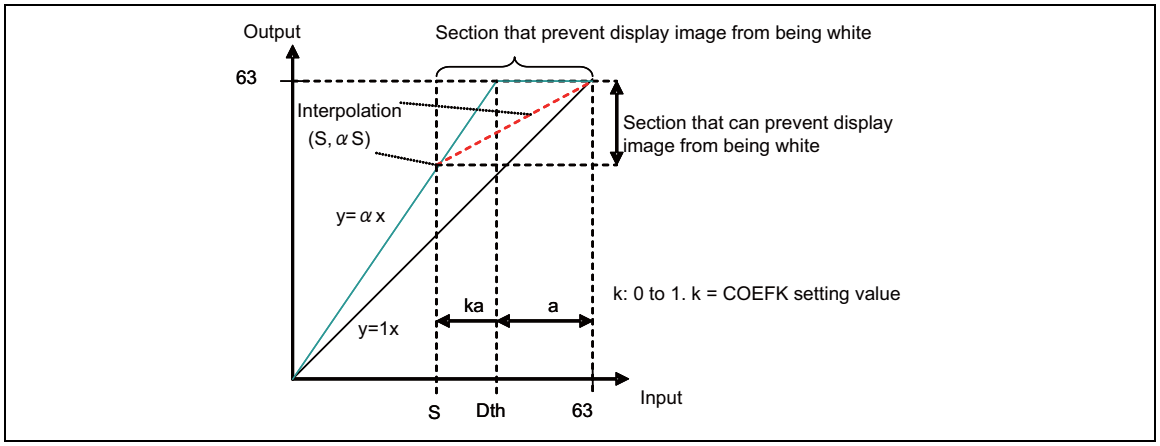


Figure 63

PWM Signal Setting

The PWM signal is output from the LEDPWM pin according to BDCV[7:0] bit settings and brightness information (8 bits) output from BLC control circuit.

PWM output specification (LEDPWMPOL = 0)

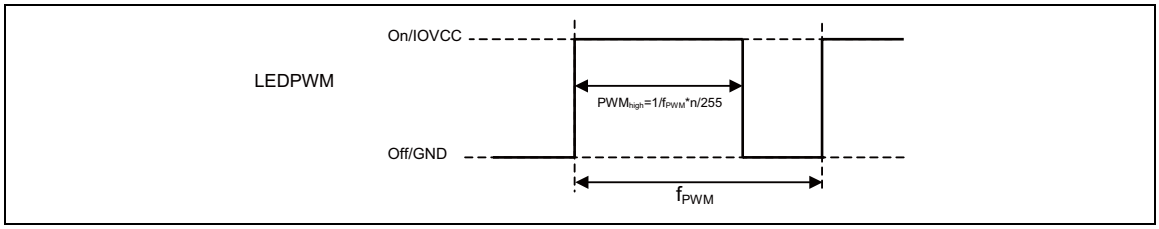


Figure 64

Table 89

PWMDIV[7:0]	LEDPWM frequency (f_{PWM})
8'h00	45.20 kHz
8'h01	22.60 kHz
8'h02	15.07 kHz
8'h03	11.30 kHz
8'h07	6.46 kHz
8'h0F	3.01 kHz
8'h1F	1.46 kHz
8'h3F	0.72 kHz
8'h7F	0.36 kHz
8'hFF	0.18 kHz

Note: These values are (Typ). The maximum variance is ±7%.

Table 90

Dimming data	$Duty_{PWM}$
8'h00	0 (fixed at Low)
8'h01	1/255
8'h02	2/255
8'h03	3/255
:	:
8'h0D	253/255
8'h0E	254/255
8'hFF	1 (fixed at High)

Note: These are Typical values. The maximum variance is ±7%.

Liquid Crystal Panel Interface Timing

The relationships between RGB interface signals and liquid crystal panel control signals in internal operation and RGB interface operations are as follows

Internal Clock Operation

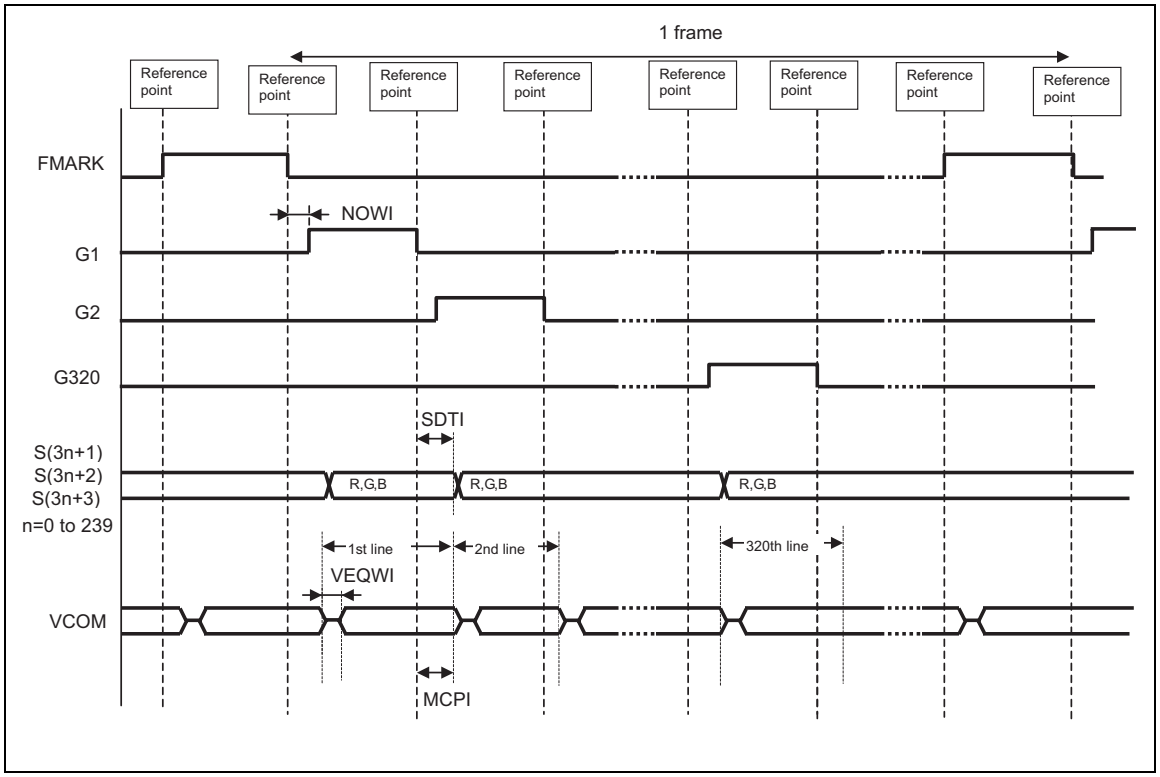


Figure 65

VCOM alternating position and source output alternating position can be set separately.

RGB Interface Operation

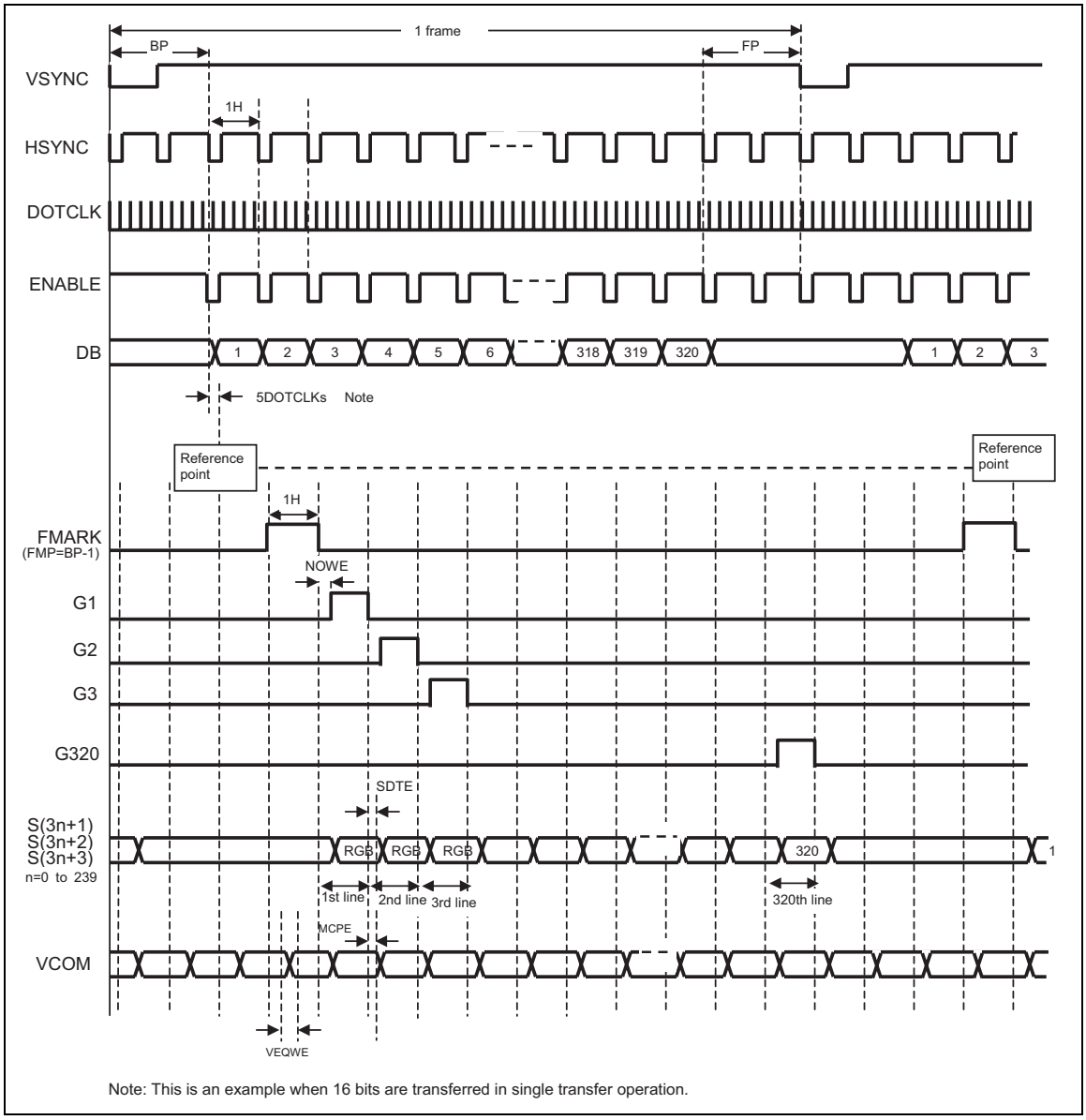


Figure 66

γ Correction Function

γ Correction Function

The R61580supports γ-correction function to make the optimal colors according to the characteristics of the panel. The R61580 has registers for positive and negative polarities to allow different settings.

γ Correction Circuit

The following figure shows the γ-correction circuit. According to the settings of variable resistors R0 to R8, the voltage the level of which is the difference is between VREG1OUT and VGS is evenly divided into 8 grayscale reference voltages (V0, V1, V8, V20, V43, V55, V62 and V63). Other 42-grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltage, see "Grayscale Voltage Calculation Formula".

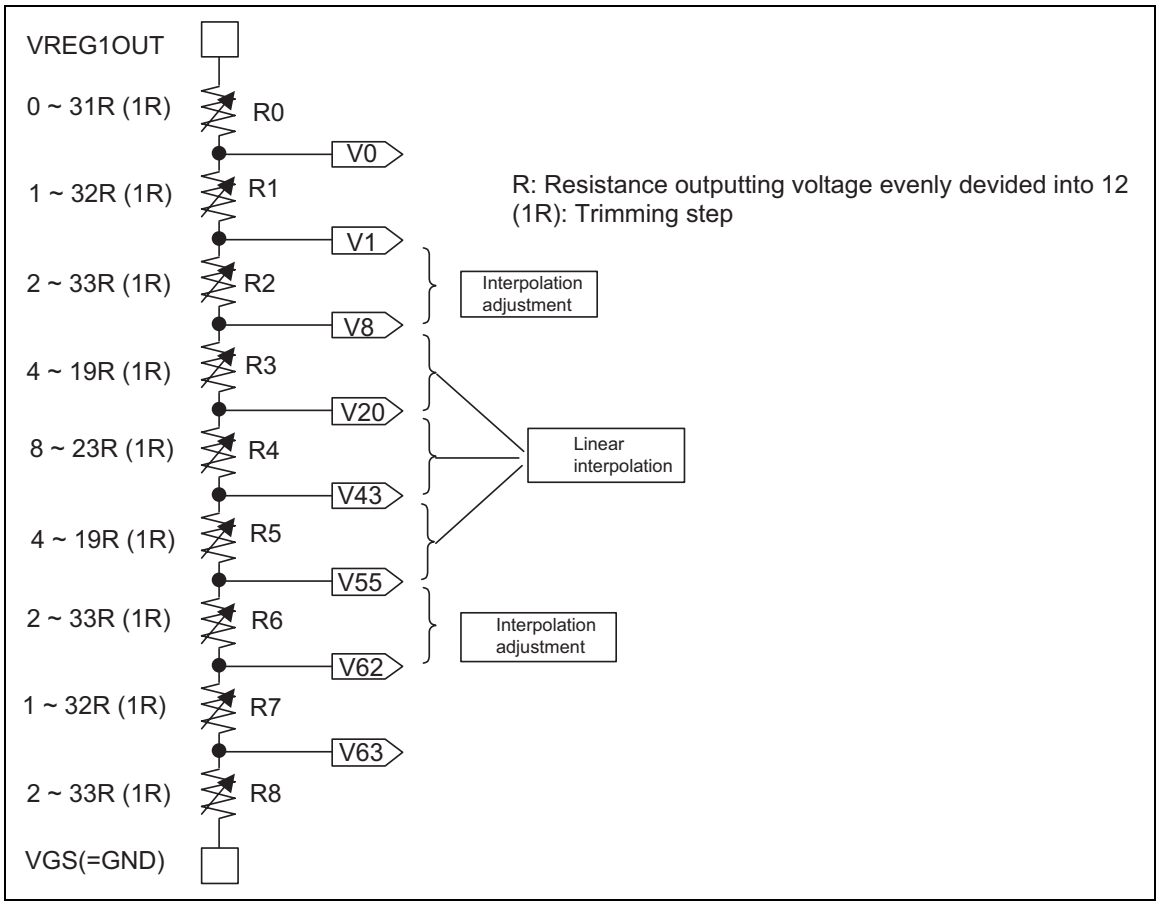


Figure 67

γ Correction Registers

The γ-correction registers include 42-bit reference level adjustment registers for each of positive polarity and negative polarity and 8-bit interpolation adjustment registers.

Reference Level Adjustment Registers

Table 91 Reference Level Adjustment Registers

Resistor	Gamma	
	Positive polarity	Negative polarity
R0	PR0P00[4:0]	PR0N00[4:0]
R1	PR0P01[4:0]	PR0N01[4:0]
R2	PR0P02[4:0]	PR0N02[4:0]
R3	PR0P03[3:0]	PR0N03[3:0]
R4	PR0P04[3:0]	PR0N04[3:0]
R5	PR0P05[3:0]	PR0N05[3:0]
R6	PR0P06[4:0]	PR0N06[4:0]
R7	PR0P07[4:0]	PR0N07[4:0]
R8	PR0P08[4:0]	PR0N08[4:0]

Table 92 Reference Level Adjustment Registers and Resistors

Resistor	Register		Resistance	Resistor	Register		Resistance
	Name	Value			Name	Value	
R0	PR**0[4:0]	5'h00	0R	R5	PR**5[3:0]	4'h0	4R
		5'h01	1R			4'h1	5R
		5'h02	2R			4'h2	6R
		⋮	⋮			⋮	⋮
		5'h1F	31R			4'hF	19R
R1	PR**1[4:0]	5'h00	1R	R6	PR**6[4:0]	5'h00	2R
		5'h01	2R			5'h01	3R
		5'h02	3R			5'h02	4R
		⋮	⋮			⋮	⋮
		5'h1F	32R			5'h1F	33R
R2	PR**2[4:0]	5'h00	2R	R7	PR**7[4:0]	5'h00	1R
		5'h01	3R			5'h01	2R
		5'h02	4R			5'h02	3R
		⋮	⋮			⋮	⋮
		5'h1F	33R			5'h1F	32R
R3	PR**3[3:0]	4'h0	4R	R8	PR**8[4:0]	5'h00	2R
		4'h1	5R			5'h01	3R
		4'h2	6R			5'h02	4R
		⋮	⋮			⋮	⋮
		4'hF	19R			5'h1F	33R
R4	PR**4[3:0]	4'h0	8R				
		4'h1	9R				
		4'h2	10R				
		⋮	⋮				
		4'hF	23R				

Note: ** in the above table represents 0P/0N.

Interpolation Registers

Table 93 Interpolation Registers

Interpolation adjustment	Gamma	
	Positive polarity	Negative polarity
V2 ~ V7	PI0P0[1:0]	PI0N0[1:0]
	PI0P1[1:0]	PI0N1[1:0]
V56 ~ V61	PI0P2[1:0]	PI0N2[1:0]
	PI0P3[1:0]	PI0N3[1:0]

Table 94 Interpolation Factor for V2 to V7

(See "Grayscale Voltage Calculation Formula" for IPV* level)

PI**0[1:0]	PI**1[1:0]	IPV2	IPV3	IPV4	IPV5	IPV6	IPV7
2'h0	2'h0	81%	67%	52%	39%	26%	13%
	2'h1	78%	61%	43%	33%	22%	11%
	2'h2	73%	52%	31%	23%	15%	8%
	2'h3	72%	50%	28%	21%	14%	7%
2'h1	2'h0	80%	68%	56%	42%	28%	14%
	2'h1	76%	62%	48%	36%	24%	12%
	2'h2	70%	52%	35%	26%	17%	9%
	2'h3	69%	50%	31%	23%	16%	8%
2'h2	2'h0	78%	70%	61%	46%	30%	15%
	2'h1	74%	63%	53%	39%	26%	13%
	2'h2	66%	53%	39%	29%	20%	10%
	2'h3	64%	50%	36%	27%	18%	9%
2'h3	2'h0	78%	70%	63%	47%	31%	16%
	2'h1	73%	64%	54%	41%	27%	14%
	2'h2	65%	53%	41%	31%	20%	10%
	2'h3	63%	50%	37%	28%	19%	9%

Table 95 Interpolation Factor for V56 to V61

PI**3[1:0]	PI**2[1:0]	IPV56	IPV57	IPV58	IPV59	IPV60	IPV61
2'h0	2'h0	87%	74%	61%	48%	33%	19%
	2'h1	89%	78%	67%	57%	39%	22%
	2'h2	92%	85%	77%	69%	48%	27%
	2'h3	93%	86%	79%	72%	50%	28%
2'h1	2'h0	86%	72%	58%	44%	32%	20%
	2'h1	88%	76%	64%	52%	38%	24%
	2'h2	91%	83%	74%	65%	48%	30%
	2'h3	92%	84%	77%	69%	50%	31%
2'h2	2'h0	85%	70%	54%	39%	30%	22%
	2'h1	87%	74%	61%	47%	37%	26%
	2'h2	90%	80%	71%	61%	47%	34%
	2'h3	91%	82%	73%	64%	50%	36%
2'h3	2'h0	84%	69%	53%	38%	30%	22%
	2'h1	86%	73%	59%	46%	36%	27%
	2'h2	90%	80%	69%	59%	47%	35%
	2'h3	91%	81%	72%	63%	50%	37%

Note: ** in the above tables represents 0P/0N.

Table 96 Grayscale Voltage Calculation Formula

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	ΔV x Σ（R1 ~ R8)/SUMR	V32	V43 + (V20 - V43) x 11/23
V1	ΔV x Σ（R2 ~ R8)/SUMR	V33	V43 + (V20 - V43) x 10/23
V2	V8 + (V1 - V8) x IPV2	V34	V43 + (V20 - V43) x 9/23
V3	V8 + (V1 - V8) x IPV3	V35	V43 + (V20 - V43) x 8/23
V4	V8 + (V1 - V8) x IPV4	V36	V43 + (V20 - V43) x 7/23
V5	V8 + (V1 - V8) x IPV5	V37	V43 + (V20 - V43) x 6/23
V6	V8 + (V1 - V8) x IPV6	V38	V43 + (V20 - V43) x 5/23
V7	V8 + (V1 - V8) x IPV7	V39	V43 + (V20 - V43) x 4/23
V8	ΔV x Σ（R3 ~ R8）/SUMR	V40	V43 + (V20 - V43) x 3/23
V9	V20 + (V8 - V20) x 11/12	V41	V43 + (V20 - V43) x 2/23
V10	V20 + (V8 - V20) x 10/12	V42	V43 + (V20 - V43) x 1/23
V11	V20 + (V8 - V20) x 9/12	V43	ΔV x Σ（R5 ~ R8)/SUMR
V12	V20 + (V8 - V20) x 8/12	V44	V55 + (V43 - V55) x 11/12
V13	V20 + (V8 - V20) x 7/12	V45	V55 + (V43 - V55) x 10/12
V14	V20 + (V8 - V20) x 6/12	V46	V55 + (V43 - V55) x 9/12
V15	V20 + (V8 - V20) x 5/12	V47	V55 + (V43 - V55) x 8/12
V16	V20 + (V8 - V20) x 4/12	V48	V55 + (V43 - V55) x 7/12
V17	V20 + (V8 - V20) x 3/12	V49	V55 + (V43 - V55) x 6/12
V18	V20 + (V8 - V20) x 2/12	V50	V55 + (V43 - V55) x 5/12
V19	V20 + (V8 - V20) x 1/12	V51	V55 + (V43 - V55) x 4/12
V20	ΔV x Σ（R4 ~ R8）/SUMR	V52	V55 + (V43 - V55) x 3/12
V21	V43 + (V20 - V43) x 22/23	V53	V55 + (V43 - V55) x 2/12
V22	V43 + (V20 - V43) x 21/23	V54	V55 + (V43 - V55) x 1/12
V23	V43 + (V20 - V43) x 20/23	V55	ΔV x Σ（R6 ~ R8)/SUMR
V24	V43 + (V20 - V43) x 19/23	V56	V62 + (V55 - V62) x IPV56
V25	V43 + (V20 - V43) x 18/23	V57	V62 + (V55 - V62) x IPV57
V26	V43 + (V20 - V43) x 17/23	V58	V62 + (V55 - V62) x IPV58
V27	V43 + (V20 - V43) x 16/23	V59	V62 + (V55 - V62) x IPV59
V28	V43 + (V20 - V43) x 15/23	V60	V62 + (V55 - V62) x IPV60
V29	V43 + (V20 - V43) x 14/23	V61	V62 + (V55 - V62) x IPV61
V30	V43 + (V20 - V43) x 13/23	V62	ΔV x (R7 + R8)/SUMR
V31	V43 + (V20 - V43) x 12/23	V63	ΔV x R8/SUMR

Note: Make sure that
ΔV = VREG1OUT – VGS
SUMR = Σ(R0 ~ R8) ≥ 70R
V63 ≥ 0.2V

Table 97 Frame Memory Data and the Grayscale Voltage

Frame Memory data	Grayscale voltage				Frame Memory data	Grayscale voltage			
	REV = 1		REV = 0			REV = 1		REV = 0	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity		Positive polarity	Negative polarity	Positive polarity	Negative polarity
6'h00	V0	V63	V63	V0	6'h20	V32	V31	V31	V32
6'h01	V1	V62	V62	V1	6'h21	V33	V30	V30	V33
6'h02	V2	V61	V61	V2	6'h22	V34	V29	V29	V34
6'h03	V3	V60	V60	V3	6'h23	V35	V28	V28	V35
6'h04	V4	V59	V59	V4	6'h24	V36	V27	V27	V36
6'h05	V5	V58	V58	V5	6'h25	V37	V26	V26	V37
6'h06	V6	V57	V57	V6	6'h26	V38	V25	V25	V38
6'h07	V7	V56	V56	V7	6'h27	V39	V24	V24	V39
6'h08	V8	V55	V55	V8	6'h28	V40	V23	V23	V40
6'h09	V9	V54	V54	V9	6'h29	V41	V22	V22	V41
6'h0A	V10	V53	V53	V10	6'h2A	V42	V21	V21	V42
6'h0B	V11	V52	V52	V11	6'h2B	V43	V20	V20	V43
6'h0C	V12	V51	V51	V12	6'h2C	V44	V19	V19	V44
6'h0D	V13	V50	V50	V13	6'h2D	V45	V18	V18	V45
6'h0E	V14	V49	V49	V14	6'h2E	V46	V17	V17	V46
6'h0F	V15	V48	V48	V15	6'h2F	V47	V16	V16	V47
6'h10	V16	V47	V47	V16	6'h30	V48	V15	V15	V48
6'h11	V17	V46	V46	V17	6'h31	V49	V14	V14	V49
6'h12	V18	V45	V45	V18	6'h32	V50	V13	V13	V50
6'h13	V19	V44	V44	V19	6'h33	V51	V12	V12	V51
6'h14	V20	V43	V43	V20	6'h34	V52	V11	V11	V52
6'h15	V21	V42	V42	V21	6'h35	V53	V10	V10	V53
6'h16	V22	V41	V41	V22	6'h36	V54	V9	V9	V54
6'h17	V23	V40	V40	V23	6'h37	V55	V8	V8	V55
6'h18	V24	V39	V39	V24	6'h38	V56	V7	V7	V56
6'h19	V25	V38	V38	V25	6'h39	V57	V6	V6	V57
6'h1A	V26	V37	V37	V26	6'h3A	V58	V5	V5	V58
6'h1B	V27	V36	V36	V27	6'h3B	V59	V4	V4	V59
6'h1C	V28	V35	V35	V28	6'h3C	V60	V3	V3	V60
6'h1D	V29	V34	V34	V29	6'h3D	V61	V2	V2	V61
6'h1E	V30	V33	V33	V30	6'h3E	V62	V1	V1	V62
6'h1F	V31	V32	V32	V31	6'h3F	V63	V0	V0	V63

Power Supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the R61580.

Power Supply Circuit Connection Example 1

VCI1 voltage level is defined by VC bit (R11h).

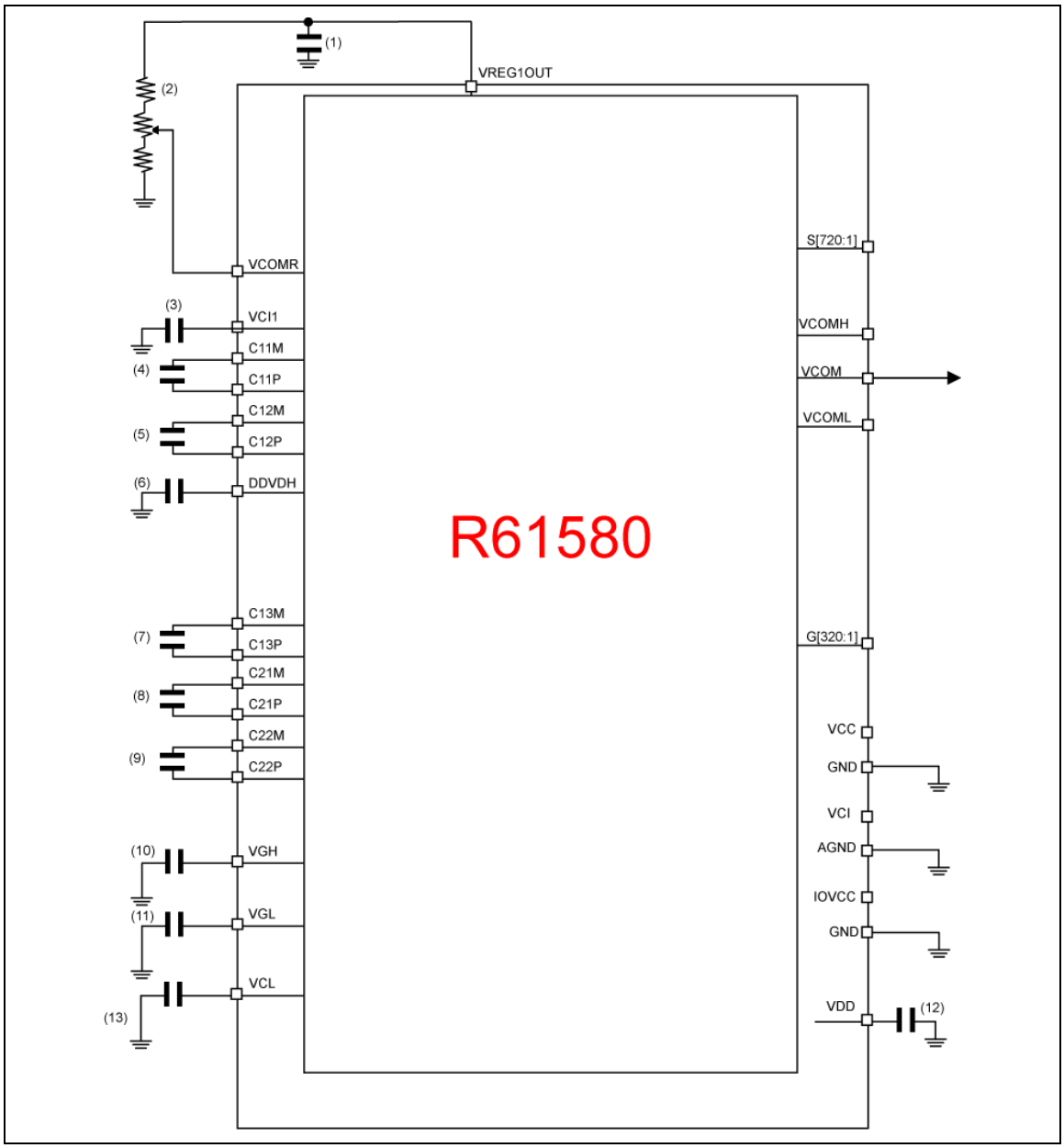


Figure 68

Power Supply Circuit Connection Example 2 (VCI voltage is directly applied to VCI1 pin)

In the following example, the electrical potential VCI is directly applied to VCI1. In this case, step-up operation is more effective although VCI1 voltage level cannot be defined by VC bit (R11h).

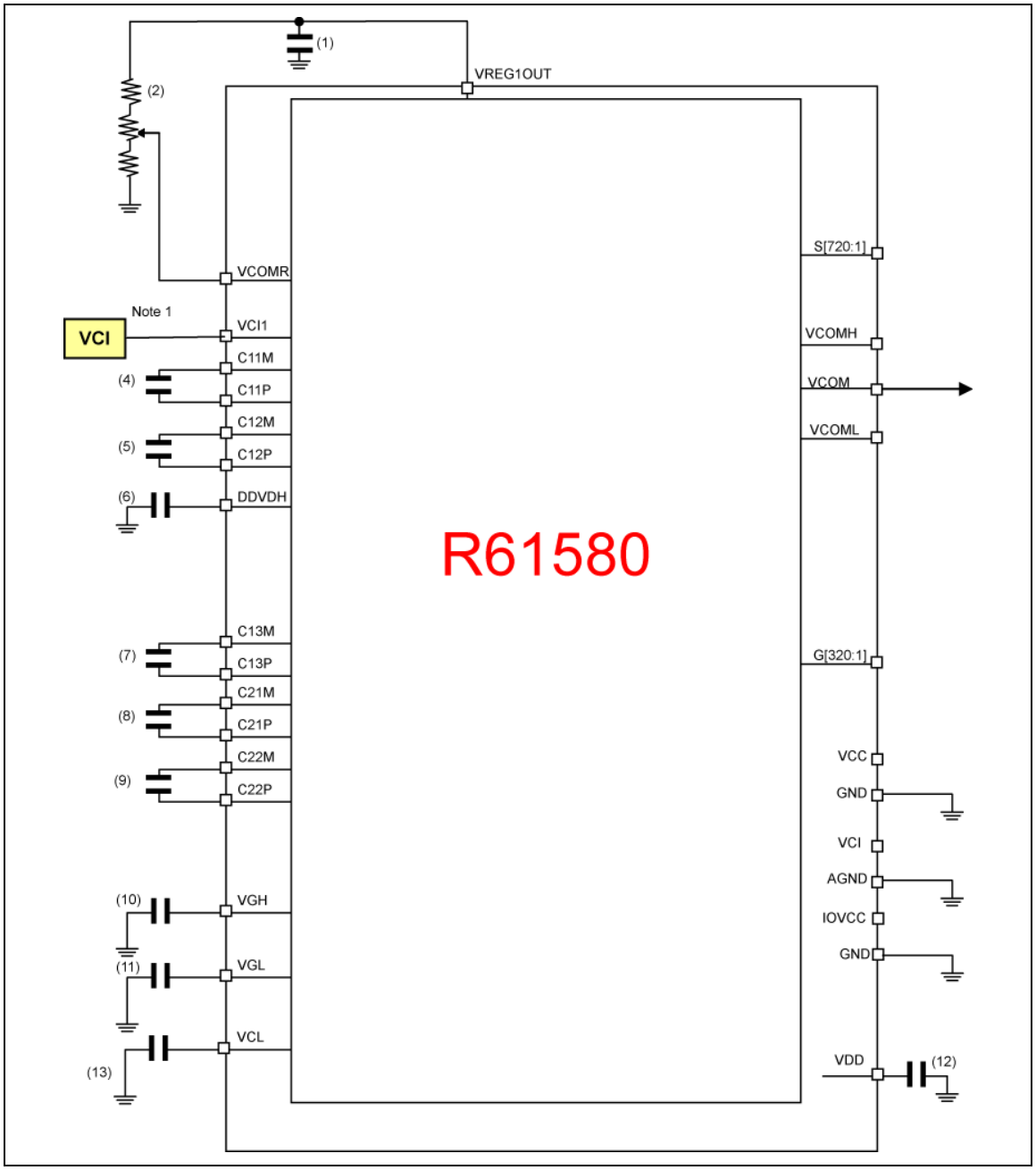


Figure 69

Note 1: When directly applying the VCI level to VCI1, set VC = 3'h7. Capacitor connection to VCIOUT is not required.

Specifications of Power Supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the R61580 are as follows. The numbers in the parentheses correspond with the numbers of the elements in the section “Power Supply Generating Circuit”.

Table 98 Capacitor

Capacitance	Voltage proof	Pin Connection
1μF (B characteristics)	6V	(1)VREG1OUT, (3)VCI1, (4)C11P, C11M (5)C12P, C12M, (7)C13P, C13M (13)VCL
	3V	(12)VDD
	10V	(6)DDVDH, (8)C21P/C21M, (9)C22P, C22M
	25V	(10)VGH, (11)VGL

Table 99 Variable Resistor

Specification	Pin Connection
> 200 kΩ	(2) VCOMR

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61580 and the TFT display application voltage waveforms and electrical potential relationship.

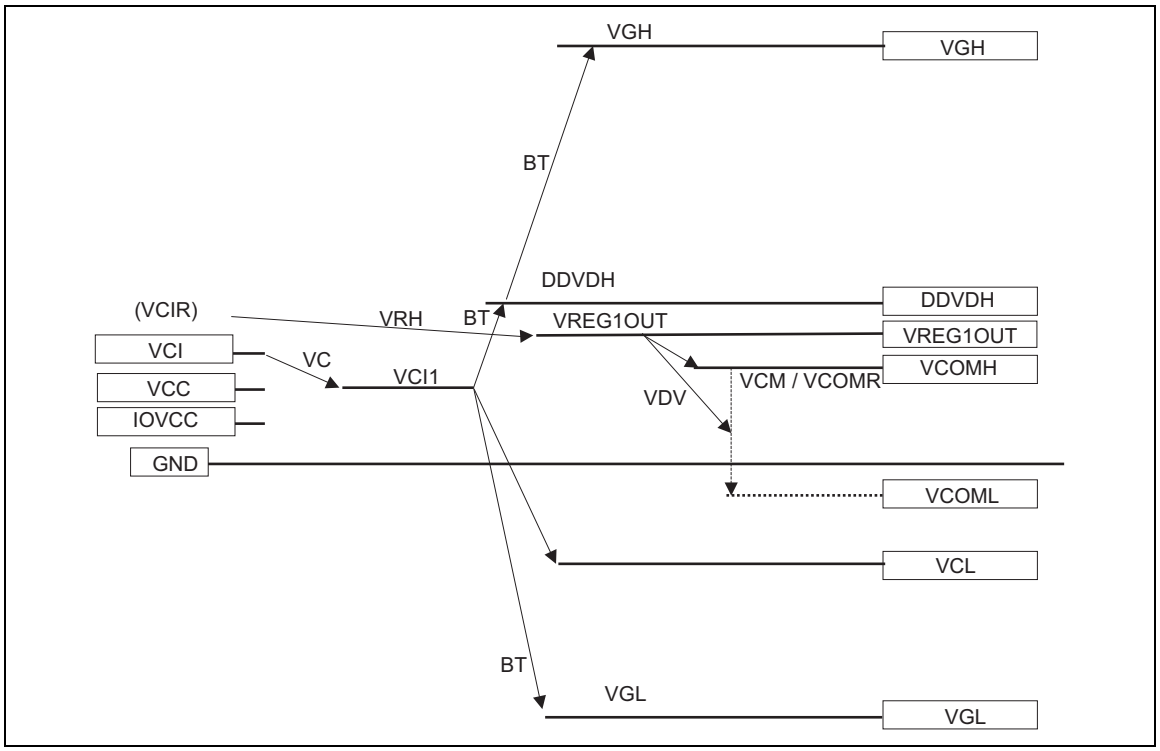


Figure 70

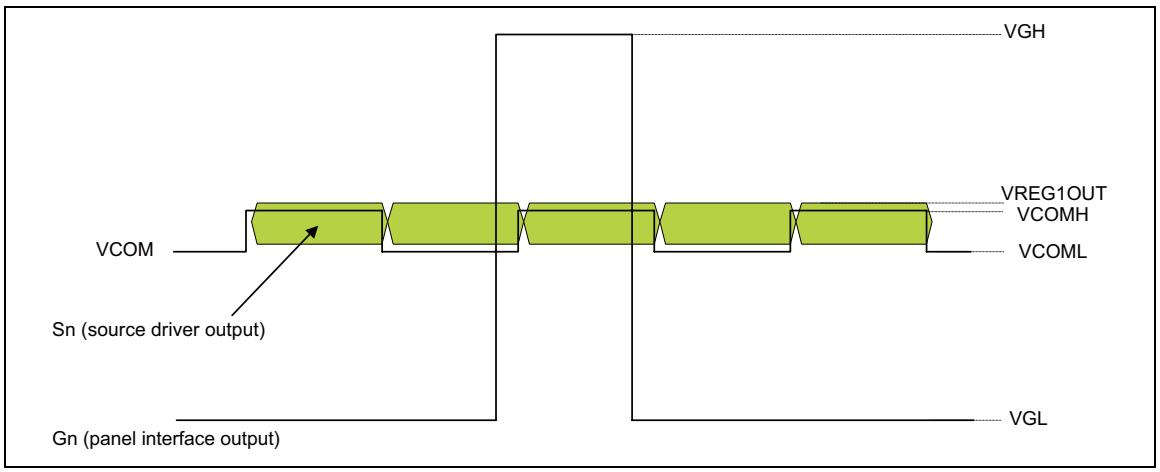


Figure 71 Liquid Crystal Application Voltage Waveform and Electrical Potential

VCOMH Voltage Adjustment Sequence

When adjusting the VCOMH voltage by setting VCM1 [6:0] in the R29'h register (internal VCOMH level adjustment circuit), follow the sequence below. The R61580 can retain the VCOMH level adjustment setting values in NVM, which allows erasing 5 times.

To write data onto the NVM, set VCOMH adjusting register VCM1 [6:0] (R29h), VCMSEL and VCM2[6:0] (R2Ah) so that these registers correspond with NVM write data register NVDAT [15:0]. See NVM write, read and erase sequences in the section "NVM Control Sequence".

If data has been erased from the bit, the bit value is set to "1". The bit to which data is not written should be set to 1.

If VCMSEL＝1, VCM1 is enabled. If VCMSEL=0、VCM2 is enabled.

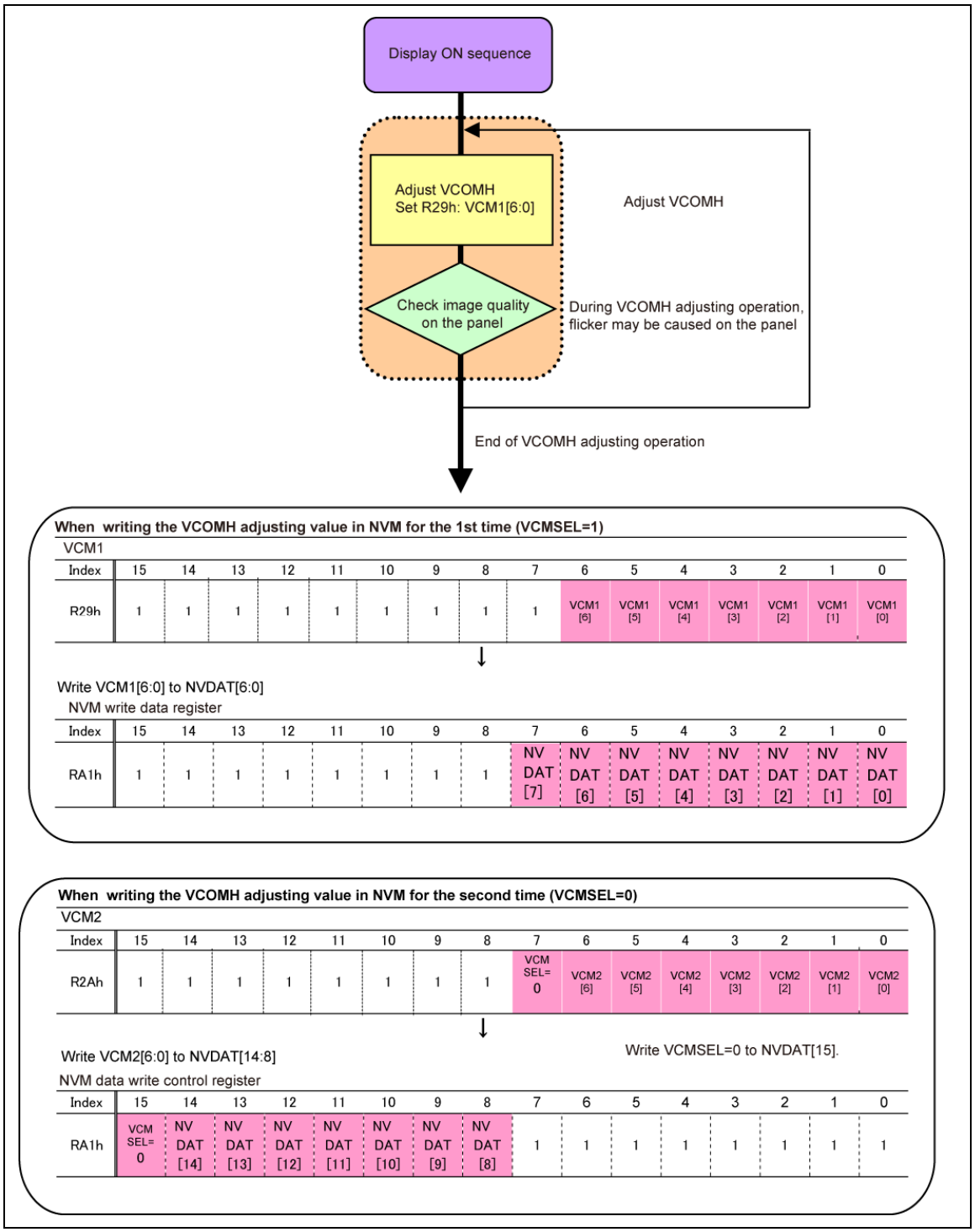

Display ON sequence
Adjust VCOMH
Set R29h: VCM1[6:0]
Check image quality on the panel
Adjust VCOMH
During VCOMH adjusting operation, flicker may be caused on the panel
End of VCOMH adjusting operation
When writing the VCOMH adjusting value in NVM for the 1st time (VCMSEL=1)
VCM1
Index 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
R29h 1 1 1 1 1 1 1 1 1 VCM1 [6] VCM1 [5] VCM1 [4] VCM1 [3] VCM1 [2] VCM1 [1] VCM1 [0]
Write VCM1[6:0] to NVDAT[6:0]
NVM write data register
Index 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RA1h 1 1 1 1 1 1 1 1 NV DAT [7] NV DAT [6] NV DAT [5] NV DAT [4] NV DAT [3] NV DAT [2] NV DAT [1] NV DAT [0]
When writing the VCOMH adjusting value in NVM for the second time (VCMSEL=0)
VCM2
Index 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
R2Ah 1 1 1 1 1 1 1 1 VCM SEL= 0 VCM2 [6] VCM2 [5] VCM2 [4] VCM2 [3] VCM2 [2] VCM2 [1] VCM2 [0]
Write VCM2[6:0] to NVDAT[14:8]
Write VCMSEL=0 to NVDAT[15].
NVM data write control register
Index 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RA1h VCM SEL= 0 NV DAT [14] NV DAT [13] NV DAT [12] NV DAT [11] NV DAT [10] NV DAT [9] NV DAT [8] 1 1 1 1 1 1 1 1

Figure 72

NVM Control Sequence

(NVM write/erase temperature: +20 ~ +30C)

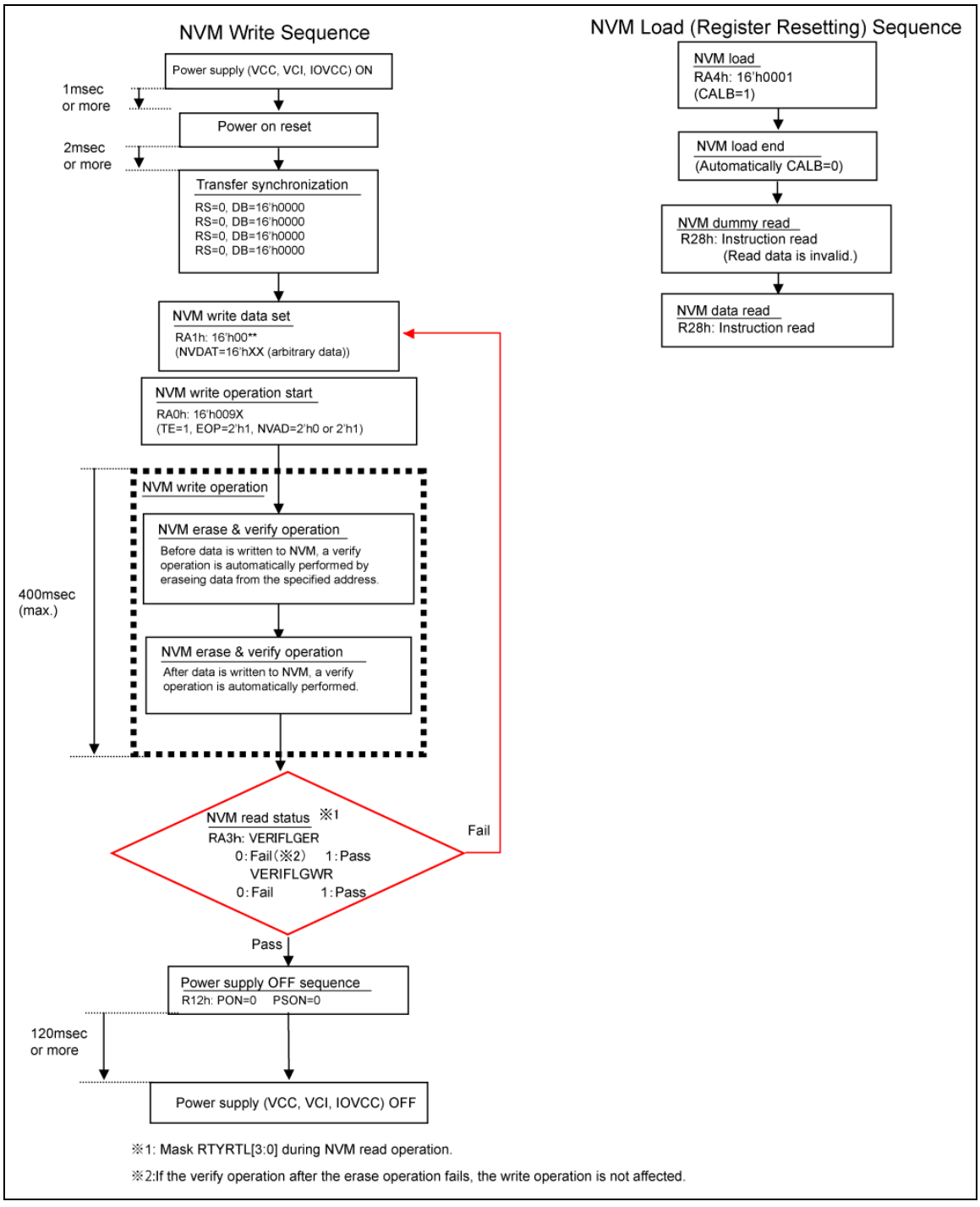


Figure 73

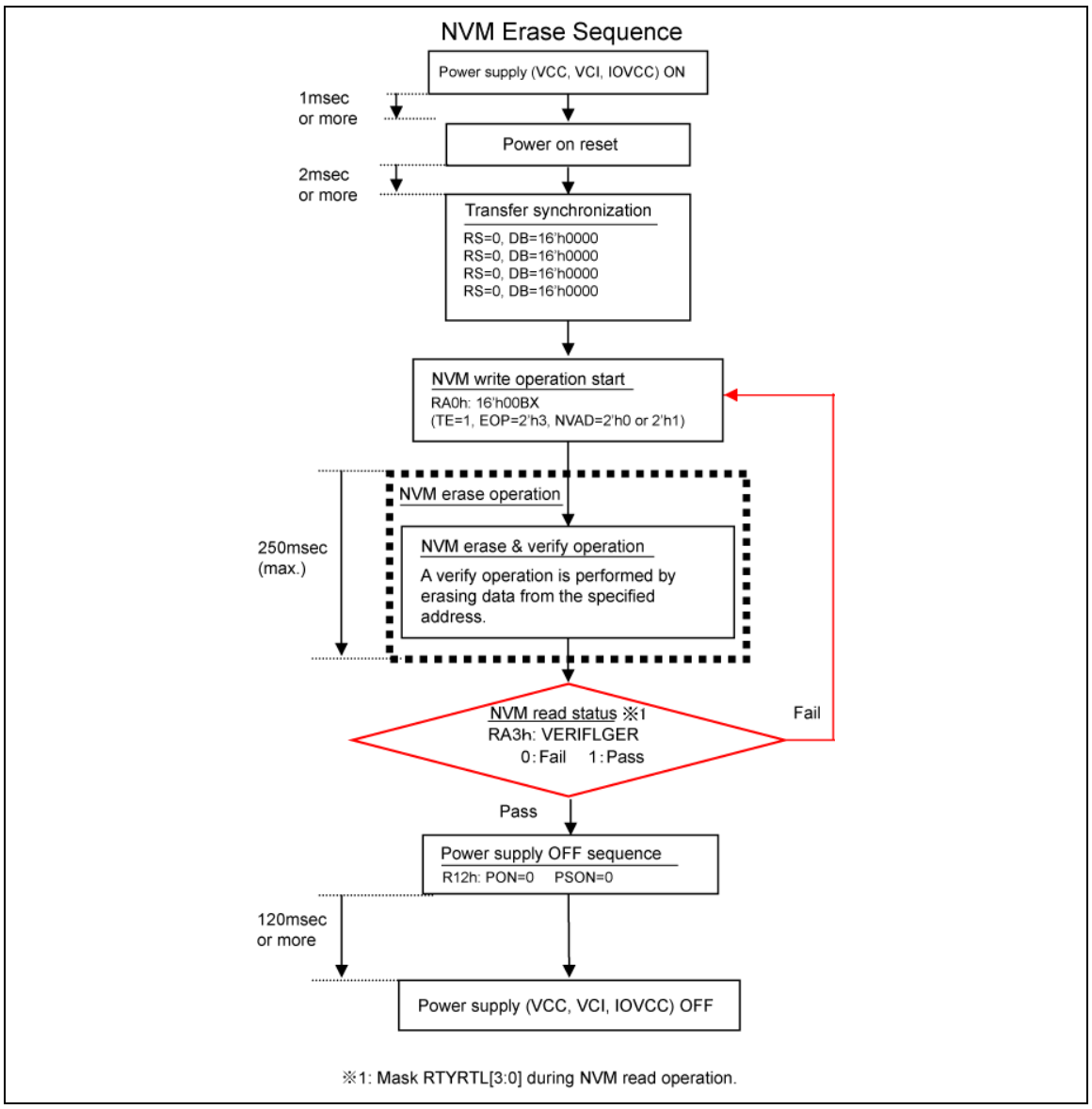

NVM Erase Sequence
Power supply (VCC, VCI, IOVCC) ON
1msec
or more
Power on reset
2msec
or more
Transfer synchronization
RS=0, DB=16'h0000
RS=0, DB=16'h0000
RS=0, DB=16'h0000
RS=0, DB=16'h0000
NVM write operation start
RA0h: 16'h00BX
(TE=1, EOP=2'h3, NVAD=2'h0 or 2'h1)
NVM erase operation
250msec
(max.)
NVM erase & verify operation
A verify operation is performed by erasing data from the specified address.
NVM read status ※1
RA3h: VERIFLGER
0: Fail 1: Pass
Fail
Pass
Power supply OFF sequence
R12h: PON=0 PSON=0
120msec
or more
Power supply (VCC, VCI, IOVCC) OFF
※1: Mask RTYRTL[3:0] during NVM read operation.

Figure 74

Power Supply Setting Sequence

R61580 Setting Sequence

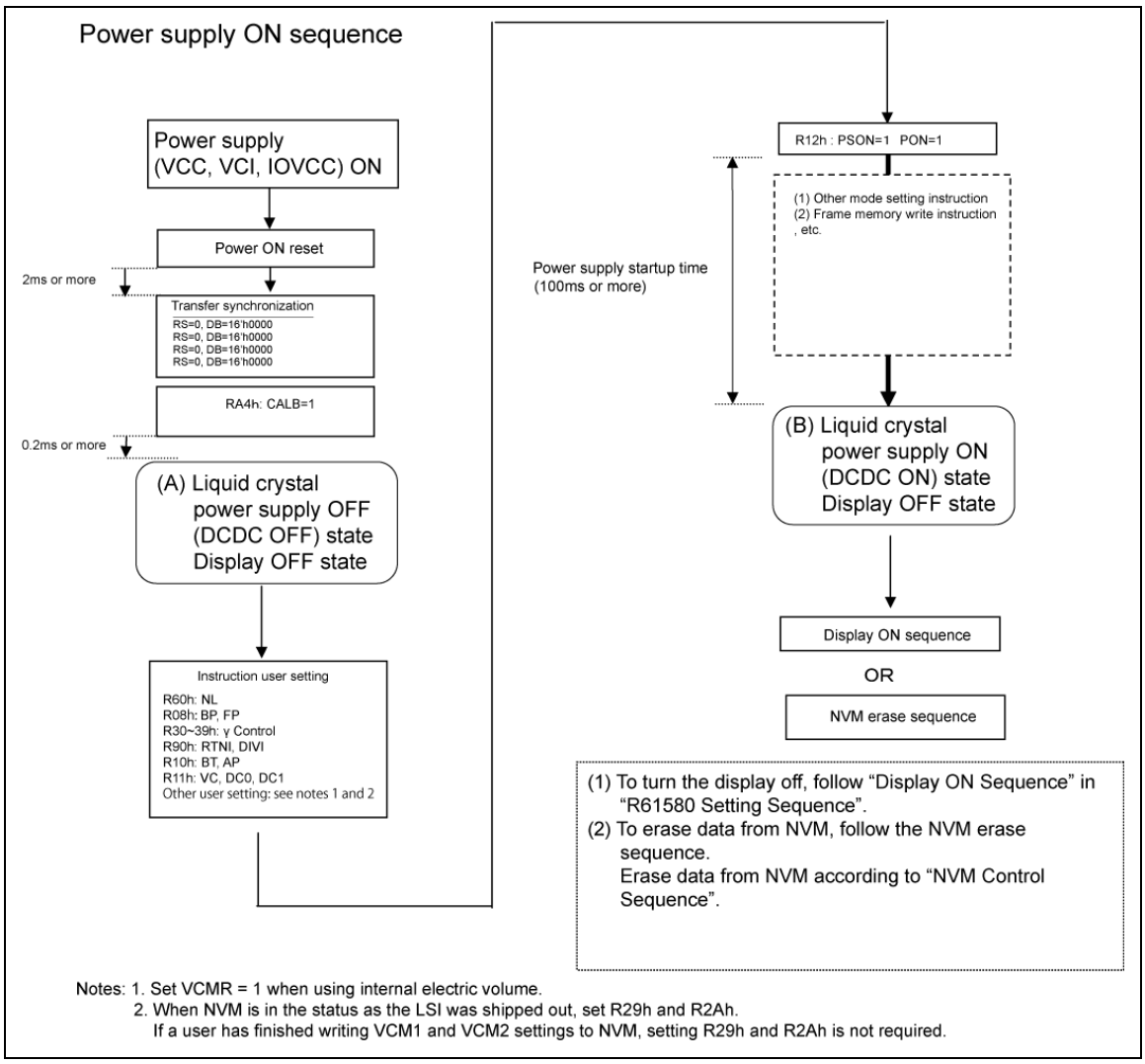


Figure 75

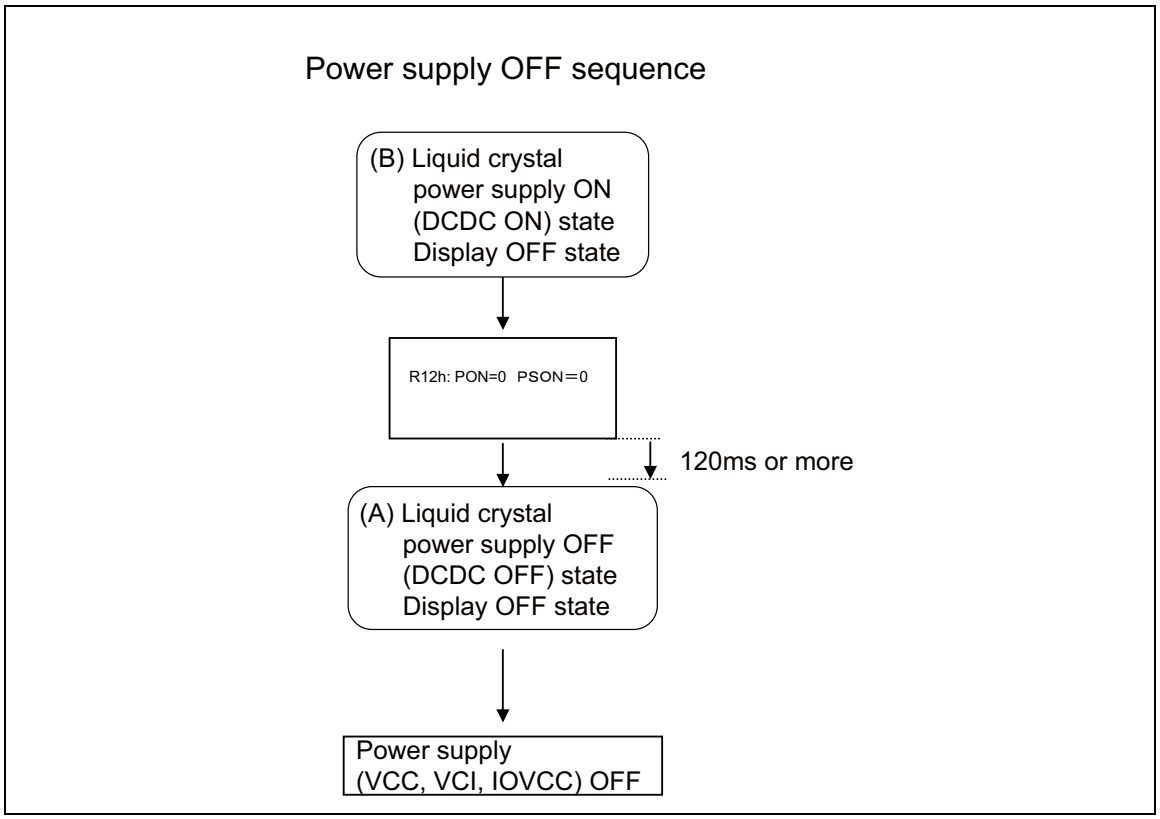

Power supply OFF sequence
(B) Liquid crystal
power supply ON
(DCDC ON) state
Display OFF state
R12h: PON=0 PSON=0
120ms or more
(A) Liquid crystal
power supply OFF
(DCDC OFF) state
Display OFF state
Power supply
(VCC, VCI, IOVCC) OFF

Figure 76

Instruction Setting Sequence

R61580 Setting Sequence

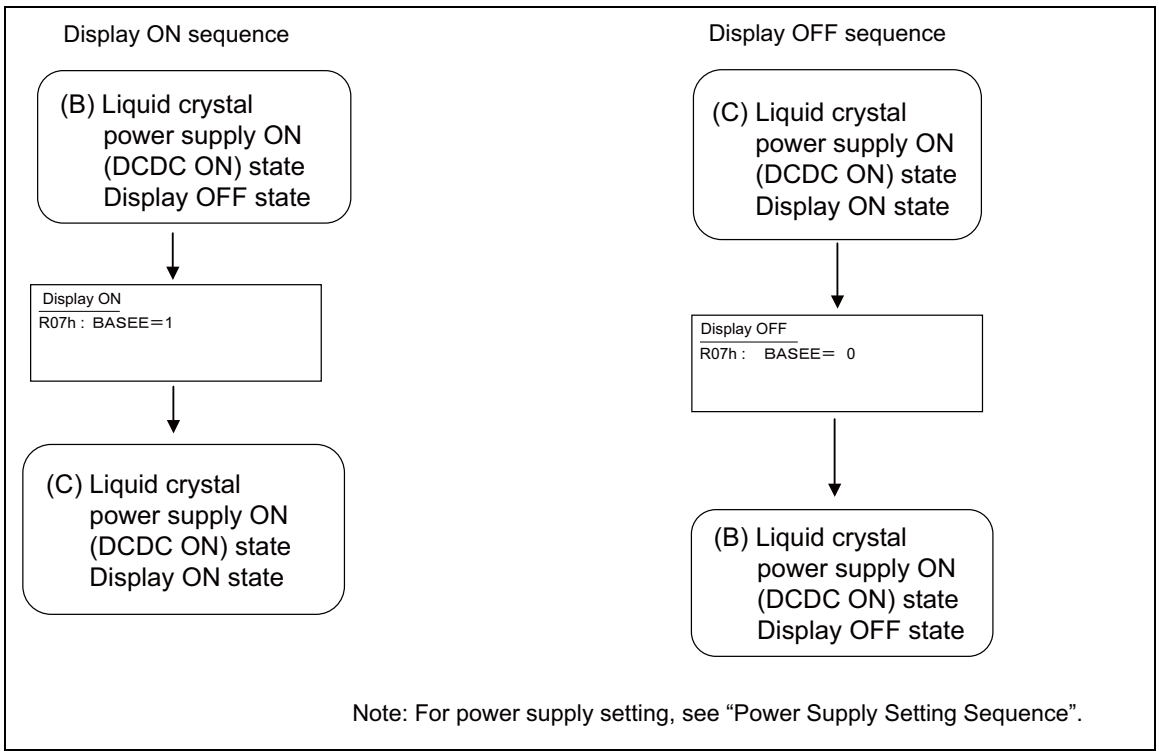


Figure 77

Other Mode Transition Setting Sequences

Deep Standby Mode IN/EXIT Sequences

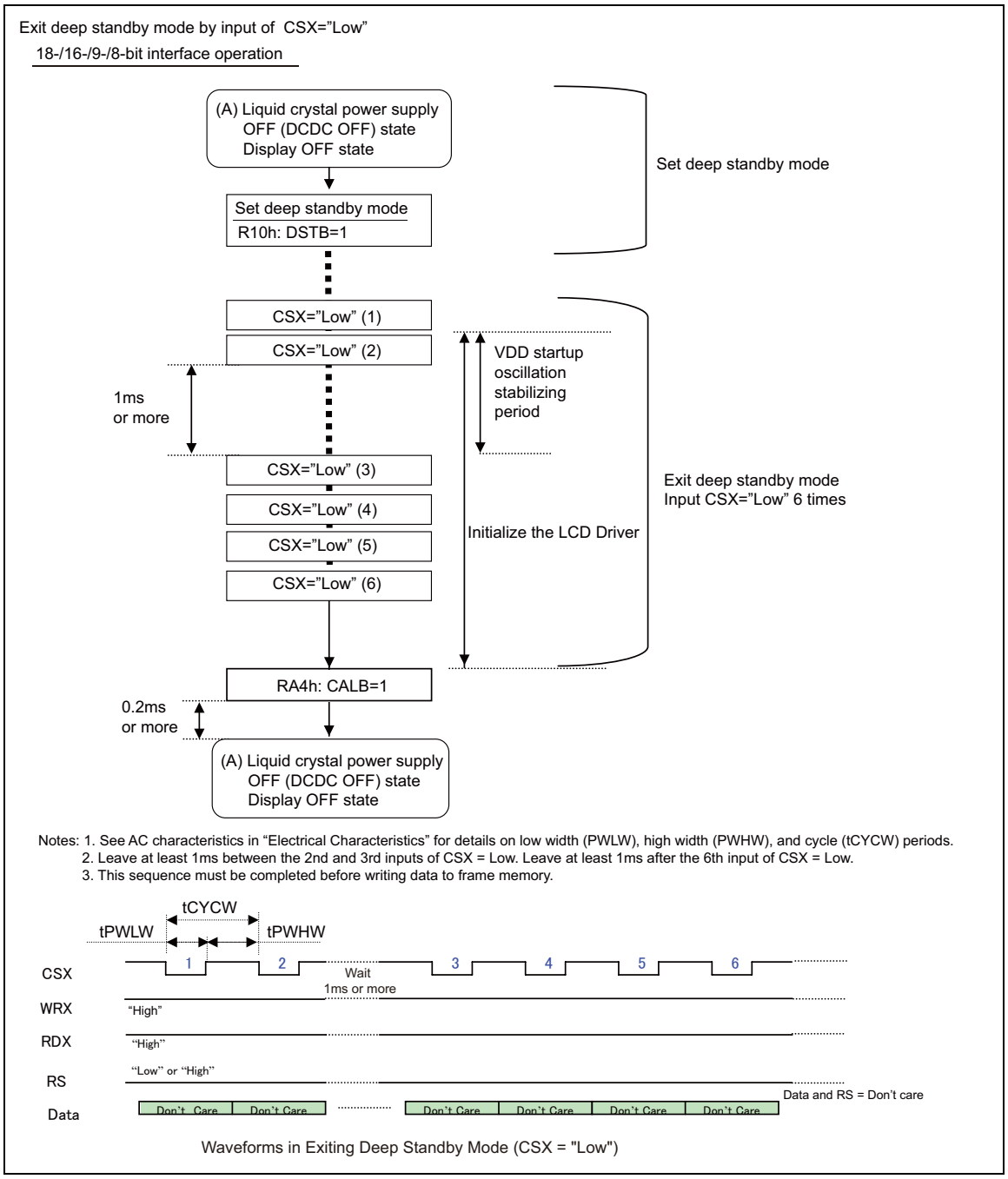


Figure 78 Exit Deep Standby Mode by Input of CSX ="Low" (18-/ 16-/ 9-/ 8-bit Interface)

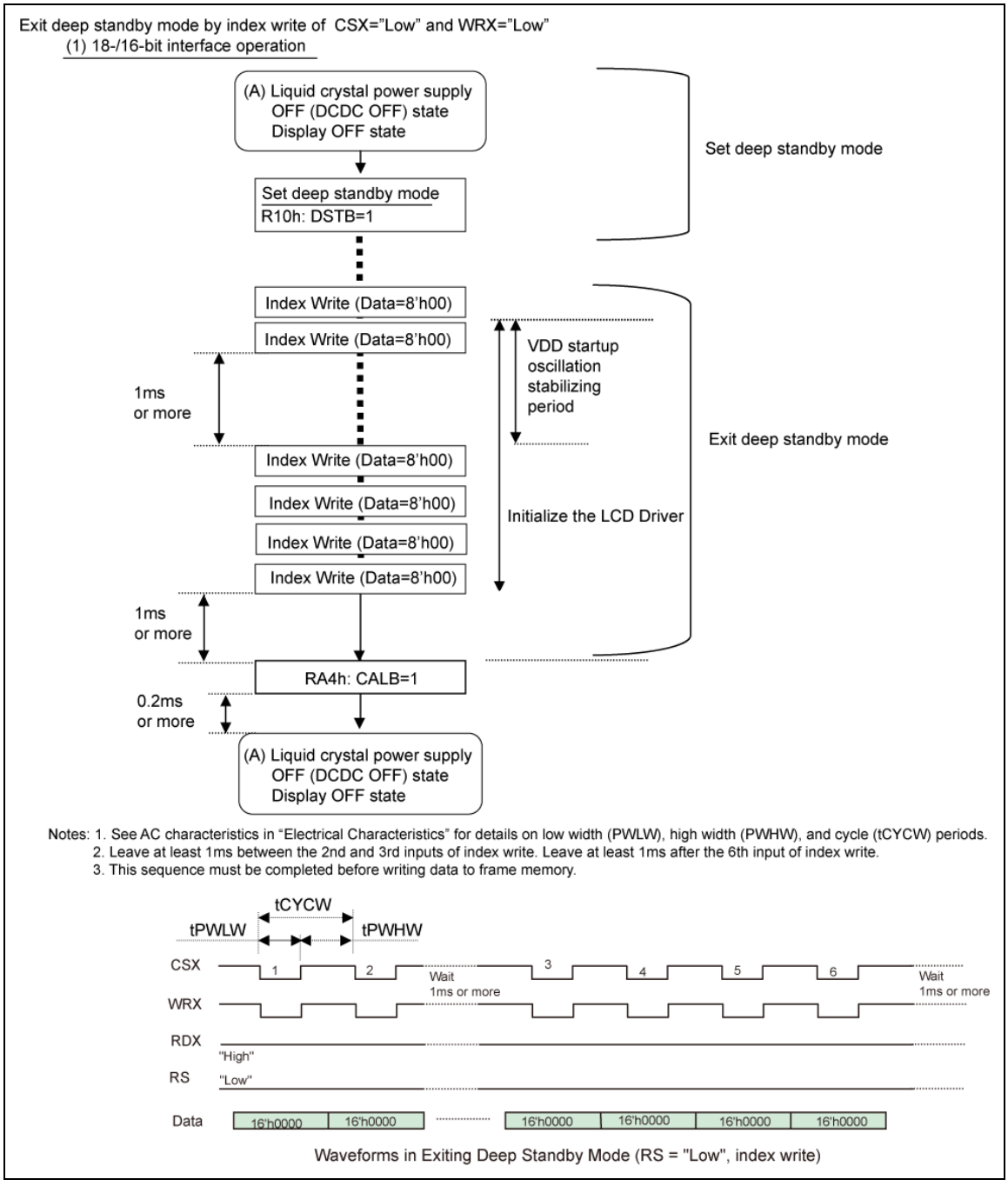


Figure 79 Exit Deep Standby Mode by Index Writes CSX="Low" and WRX="Low" (18-/16-bit Interface Operation)

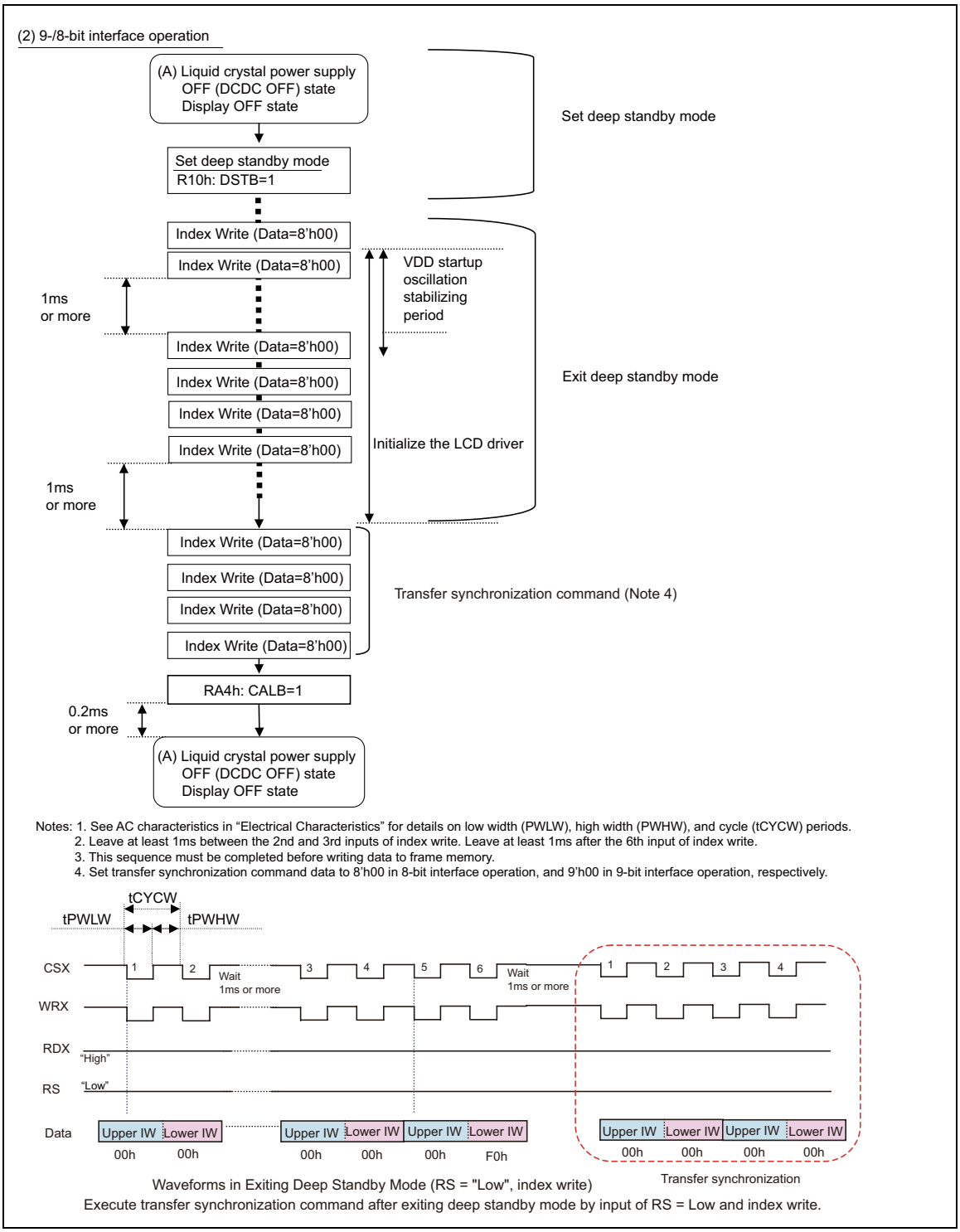


Figure 80 Exit Deep Standby Mode by Index Write of CSX="Low" and WRX="Low" (9-/8-bit Interface Operation)

8-color Mode Setting

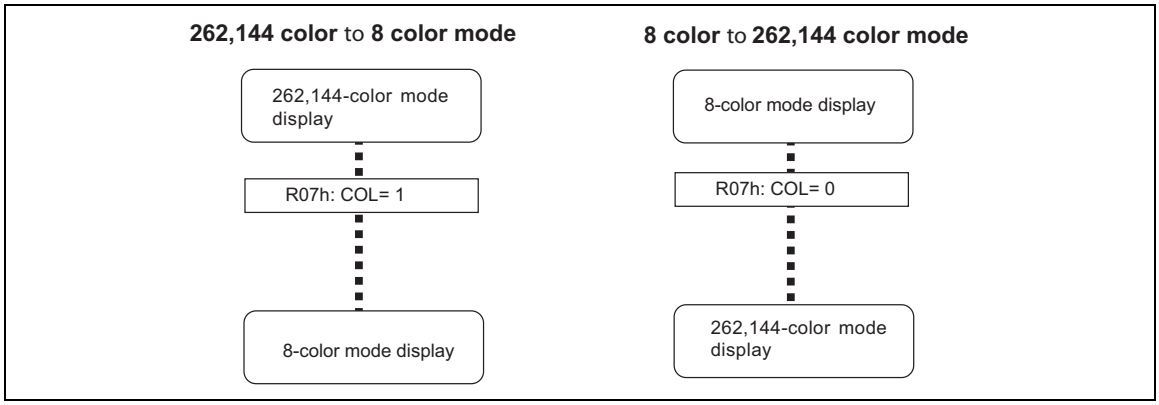


Figure 81

Partial Display Setting

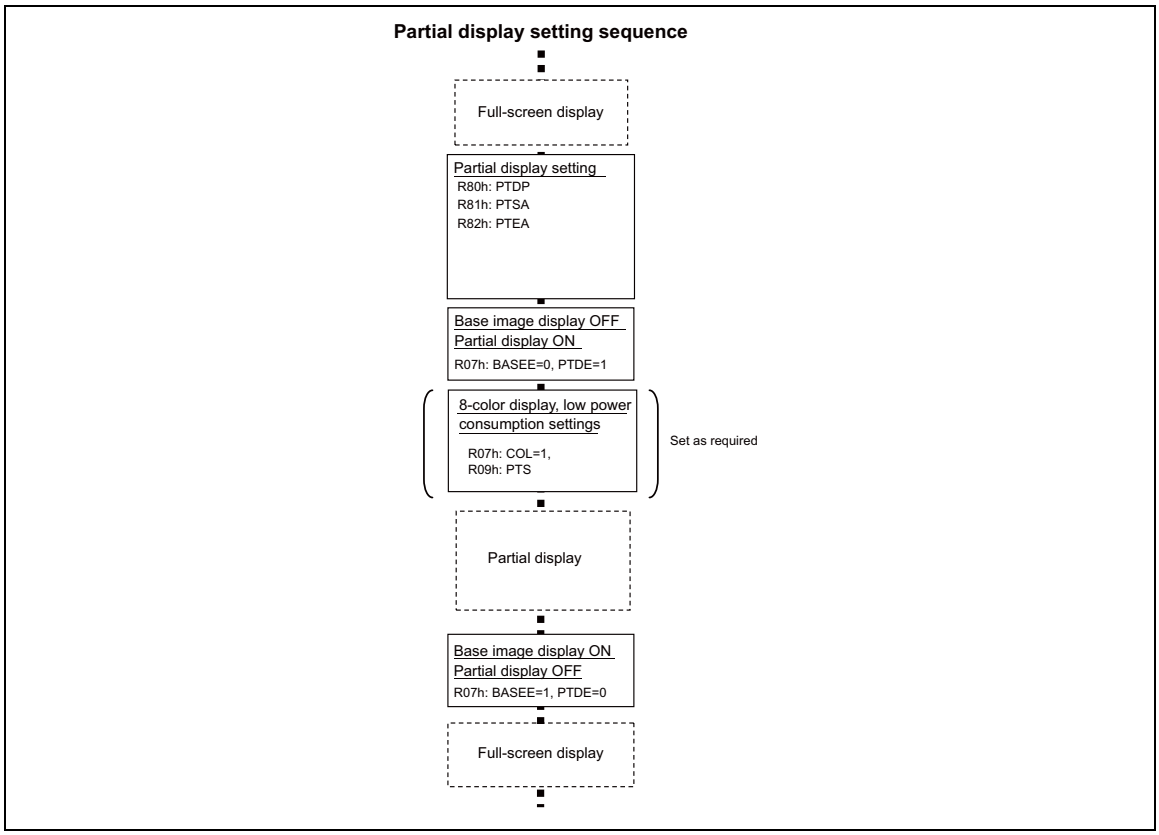


Figure 82

Absolute Maximum Ratings

Table 100

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VCC, IOVCC	V	-0.3 ~ +4.6	1, 2
Power Supply Voltage 2	VCI – AGND	V	-0.3 ~ +4.6	1, 3
Power Supply Voltage 3	DDVDH – AGND	V	-0.3 ~ +6.5	1, 4
Power Supply Voltage 4	AGND – VCL	V	-0.3 ~ +4.6	1
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ~ +9.0	1, 5
Power Supply Voltage 7	AGND – VGL	V	-0.3 ~ +13.0	1, 6
Power Supply Voltage 8	VGH– VGL	V	-0.3 ~ +30.0	1
Input Voltage	Vt	V	-0.3 ~ IOVCC + 0.3	1
Operating Temperature	Topr	℃	-40 ~ +85	1, 7
Storage Temperature	Tstg	℃	-55 ~ +110	1

Notes 1. If the R61580 is used beyond the absolute maximum ratings, the LSI may be permanently damaged. It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure VCC(high)≥GND(low), IOVCC(high)≥GND(low) .
3. Make sure VCI(high)≥AGND(low) .
4. Make sure DDVDH(high)≥AGND(low).
5. Make sure DDVDH(high) ≥VCL(low).
6. Make sure AGND(high)≥VGL(low).
7. The DC/AC characteristics of die and wafer products are guaranteed at 85C.

Electrical Characteristics

DC Characteristics

Table 101 DC Characteristics 1
(VCC= 2.50V~3.30V, IOVCC=1.65V~3.30V, Ta=-40C~+85C Note 1)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Input ”High” level voltage 1 Except for RESETX pin	VIH1	V	IOVCC=1.65V～3.30V	0.80× IOVCC	—	IOVCC	2, 3
Input ”Low” level voltage 1 Except for RESETX pin	VIL1	V	IOVCC=1.65V～3.30V	-0.3	—	0.20× IOVCC	2, 3
Input ”High” level voltage 2 RESETX pin	VIH2	V	IOVCC=1.65V～3.30V	0.90× IOVCC	—	IOVCC	2, 3
Input ”Low” level voltage 2 RESETX pin	VIL2	V	IOVCC=1.65V～3.30V	-0.3	—	0.10× IOVCC	2, 3
Output ”High” level voltage 1 DB0-17, FMARK	VOH	V	IOVCC=1.65V～3.30V, IOH=-0.1mA	0.8× IOVCC	—	—	2
Output ”Low” level voltage 1 DB0-17, FMARK	VOL	V	IOVCC=1.65V～3.30V, IOL=0.1mA	—	—	0.20× IOVCC	2
I/O leakage current	ILI	µA	Vin=0～IOVCC	-1	—	1	4
Current consumption ((IOVCC-GND) + (VCC-GND)) Normal operation (260k color)	IOP1	mA	fosc=678kHz (320 line drive), IOVCC=VCC=3.00V, fFLM=70Hz, Ta=25C, frame memory data: 18’h000000, BLCON=0, see below for other conditions	—	0.6	0.8	5
Current consumption ((IOVCC-GND) + (VCC-GND)) Normal operation (260k color) BLC ON	IOP1	mA	fosc=678kHz (320 line drive), IOVCC=VCC=3.00V, fFLM=70Hz, Ta=25℃, frame memory data: 18’h000000, BLCON=1, see below for other conditions	—	0.8	1.0	5
Current consumption ((IOVCC-GND) + (VCC-GND)) 8-color display operation (64 line partial display)	Iop2	µA	fosc=678kHz (64 line partial display), IOVCC=VCC=3.00V, fFLM=40Hz, Ta=25℃, frame memory data: 18h’000000, BLCON=0, see below for other conditions	—	140	350	5

Current consumption ((IOVCC-GND) + (VCC-GND)) Deep standby mode	IDST	μA	IOVCC=VCC=3.00V, Ta=25℃	—	0.1	1.0	5
Current consumption ((IOVCC-GND) + (VCC-GND)) Frame memory access mode	IRAM1	mA	IOVCC=2.40V,VCC=3.00 V, tCYCW=125ns, Ta=25℃, I80-8bit-I/F, TRIREG=1'h1, Consecutive frame memory access during display operation	—	2.6	3.2	5
LCD power supply current (VCI-GND) 260k color display operation	Ici1	mA	IOVCC=1.8V, VCC=VCI=2.8V, 320 line drive, fFLM=60Hz, Ta=25C, frame memory data: 18'h00000, REV=0, BC0=0, FP0=8, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4 DC10=3'h4, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) No load on the panel	—	3.2	5.0	5

LCD power supply current (VCI-GND) 8-color display operation (64 line partial display)	Ici2	mA	IOVCC=1.8V, VCC=VCI=2.8V, 64 line partial display, fFLM=40Hz, Ta=25℃, Frame memory data: 18'h00000, REV=0, BC2=0, FP2=4, BP2=8, VC=3'h1, BT=3'h4, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP2=2'h3, DC02=3'h4, DC12=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) No load on the panel, COL=1	—	0.8	1.5	5
Output voltage dispersion	ΔVO	mV	—	—	5	—	6
Average output variance	ΔVΔ	mV	—	-35	—	35	7

Table 102 DC Characteristics 2: Step-up circuit characteristics

Item		Unit	Test condition	Min.	Typ.	Max.	Note
Step-up output voltage	DDVDH	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h3, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, No load on the panel, Iload1=-3 [mA]	4.8	5.1	-	
	VGH	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h3, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload2=-100[uA], No load on the panel	14.4	15.1	-	
	VGL	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25℃, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h3, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload3=+100[uA], No load on the panel	-	-10.0	-9.6	
	VCL	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25℃, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h3, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload4=+200[uA], No load on the panel	-	-2.55	-2.4	

Table 103 Internal Reference Voltage (VCC = 2.50V ~ 3.30V, Ta = 25°C)

Item	Symbol	Unit	Min.	Typ.	Max.	Note
Internal Reference Voltage	VCIR	V	-	2.50	-	11

AC Characteristics

(VCC= 2.50V~3.30V, IOVCC=1.65V~3.30V, Ta=-40C~+85C) [See note 1]

Clock Characteristics

Table 104

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
Internal oscillation clock	fosc	kHz	IOVCC=VCC=3.0V 25℃	631	678	726

80-System Bus Interface Timing Characteristics (18-/16-bit Interface)

Table 105 (IOVCC=1.65V ~ 3.30V)

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	Figure A	75	—	—
	Read	tCYCR	ns	Figure A	450	—	—
Write low-level pulse width		PWLW	ns	Figure A	40	–	—
Read low-level pulse width		PWLR	ns	Figure A	170	–	—
Write high-level pulse width		PWHW	ns	Figure A	25	–	—
Read high-level pulse width		PWHR	ns	Figure A	250	–	–
Write / Read rise/ fall time		tWRr, WRf	ns	Figure A	-	–	25
Setup time	Write (RS to CSX, WRX)	tAS	ns	Figure A	0	—	—
	Read (RS to CSX, RDX)		ns	Figure A	10	—	—
Address hold time		tAH	ns	Figure A	2	–	—
Write data setup time		tDSW	ns	Figure A	25	–	—
Write data hold time		tH	ns	Figure A	10	–	—
Read data delay time		tDDR	ns	Figure A	-	—	150
Read data hold time		tDHR	ns	Figure A	5	–	—

80-System Bus Interface Timing Characteristics (9-/8-bit Interface)

Table 106 (IOVCC=1.65V ~ 3.30V)

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	Figure A	70	—	—
	Read	tCYCR	ns	Figure A	450	—	—
Write low-level pulse width		PWLW	ns	Figure A	30	—	—
Read low-level pulse width		PWLR	ns	Figure A	170	—	—
Write high-level pulse width		PWHW	ns	Figure A	25	—	—
Read high-level pulse width		PWHR	ns	Figure A	250	—	—
Write / Read rise/ fall time		tWRr,WRf	ns	Figure A	—	—	25
Setup time	Write (RS to CSX, WRX)	tAS	ns	Figure A	0	—	—
	Read (RS to CSX, RDX)		ns	Figure A	10	—	—
Address hold time		tAH	ns	Figure A	2	—	—
Write data setup time		tDSW	ns	Figure A	25	—	—
Write data hold time		tH	ns	Figure A	10	—	—
Read data delay time		tDDR	ns	Figure A	—	—	150
Read data hold time		tDHR	ns	Figure A	5	—	—

Clock Synchronous Serial Interface Timing Characteristics

Table 107 (IOVCC=1.65V ~ 3.30V)

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (receive)	tSCYC	ns	Figure B	100	—	20,000
	Read (transmit)	tSCYC	ns	Figure B	350	—	20,000
Serial clock high-level width	Write (receive)	tSCH	ns	Figure B	40	—	—
	Read (transmit)	tSCH	ns	Figure B	150	—	—
Serial clock low-level width	Write (receive)	tSCL	ns	Figure B	40	—	—
	Read (transmit)	tSCL	ns	Figure B	150	—	—
Serial clock rise/fall time		tSCr,tSCf	ns	Figure B	—	—	20
Chip select setup time		tCSU	ns	Figure B	20	—	—
Chip select hold time		tCH	ns	Figure B	60	—	—
Serial input data setup time		tSISU	ns	Figure B	30	—	—
Serial input data hold time		tSISH	ns	Figure B	30	—	—
Serial output data delay time		tSOD	ns	Figure B	—	—	130
Serial output data hold time		tSOH	ns	Figure B	5	—	—

Reset Timing Characteristics

Table 108 (IOVCC = 1.65V ~ 3.30V)

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Reset wait time	tRW	ms	Figure C-1	1	—	—
Reset low-level width	tRES	ms	Figure C-2	1	—	—
Reset rise time	trRES	µs	Figure C-2	—	—	10

RGB Interface Timing Characteristics

Table 109 18-/16-bit RGB Interface (IOVCC=1.65V ~ 3.30V)

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	clock	Figure D	0.5	—	1.5
ENABLE setup time	tENS	ns	Figure D	10	—	—
ENABLE hold time	tENH	ns	Figure D	20	—	—
DOTCLK low-level pulse width	PWDL	ns	Figure D	40	—	—
DOTCLK high-level pulse width	PWDH	ns	Figure D	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure D	100	—	—
Data setup time	tPDS	ns	Figure D	10	—	—
Data hold time	tPDH	ns	Figure D	40	—	—
DOTCLK, VSYNC and HSYNC rise/fall time	trgbr, trgbf	ns	Figure D	—	—	25

LCD Driver Output Characteristics

Table 110

Item	Symbol	Unit	Test condition	Min.	Typ	Max	Note
Source driver output delay time	tdds	µs	IOVCC=1.80V, VCC=VCI=2.80V, Ta=25C, REV=0, BC0=0, FP0=4, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0, PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) Same change from same grayscale at all-time division source output pin. Time to reach ±35mV when VCOM polarity changes. Load resistance R=10kohm, Load capacitance C=20pF	—	25	30	9
VCOM output delay time	tddv	µs	IOVCC=1.80V, VCC=VCI=2.80V, Ta=25C, REV=0, BC0=0, FP0=4, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, SEPVCM=0 Time to reach ±35mV when voltages on V0~V63 pins change. Load resistance R=100ohm, Load capacitance C=10nF	—	25	30	10

Notes on Electrical Characteristics

1. DC/AC electrical characteristics of bare die and wafer products are guaranteed at +85℃.
2. The followings illustrate the configurations of input, I/O, and output pins.

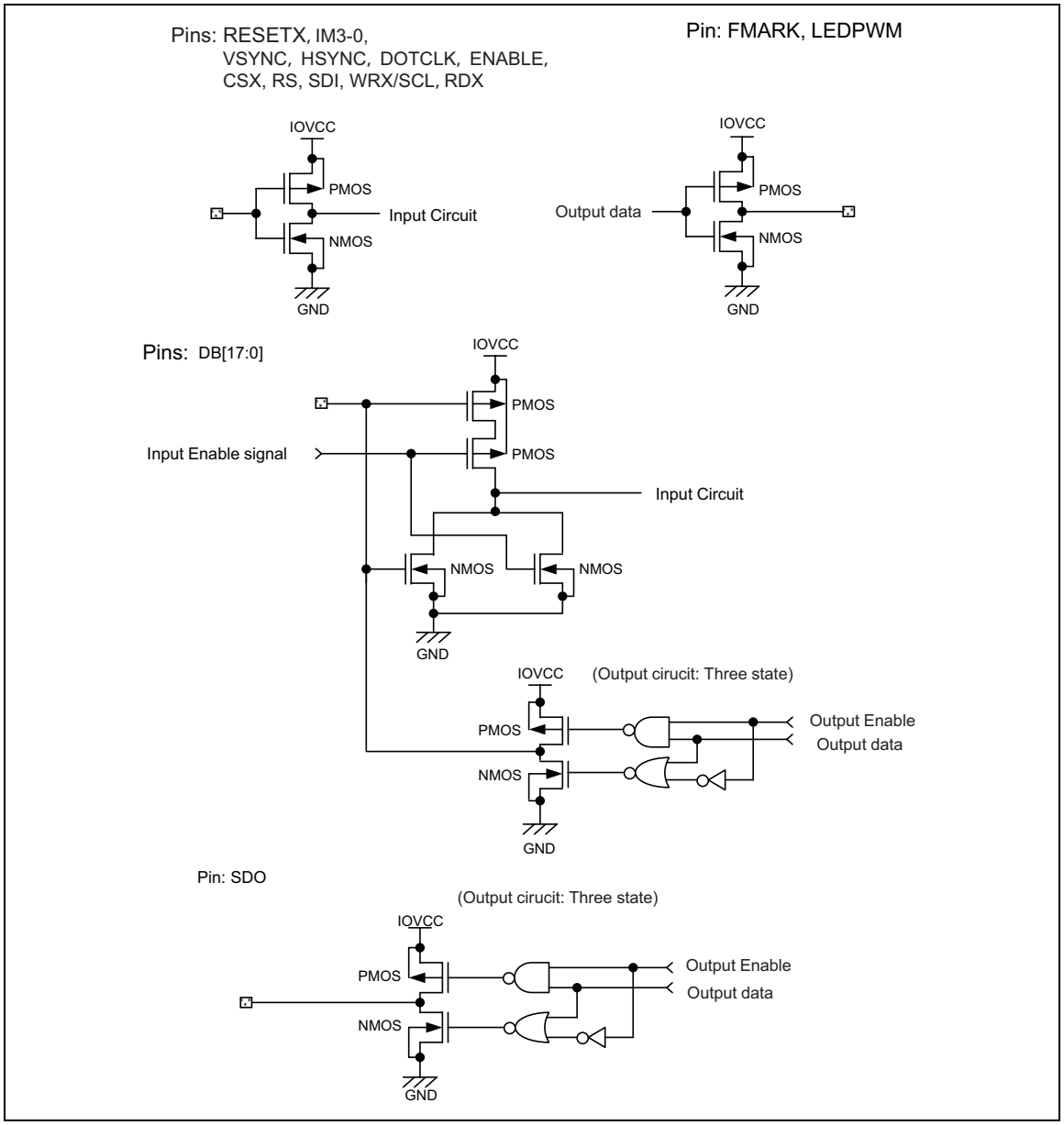


Figure 83

3. Connect IM3/2/1/0 pins to IOVCC or ground (GND).
4. This excludes the current in the output-drive MOS.

5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CSX pin is “high” or “low” while not accessing via interface pins.

6. The output voltage deviation is the difference in the voltages between output pins that are placed side by side in same display mode.

7. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with same display data.

8. This applies to internal oscillators when using an internal oscillator.

9. The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality on the actual panel in use.

10. VCOM output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line checking the quality on the actual panel in use.

11. Internal reference voltage VCIR depends on temperature as shown in following graph.

Test Circuits

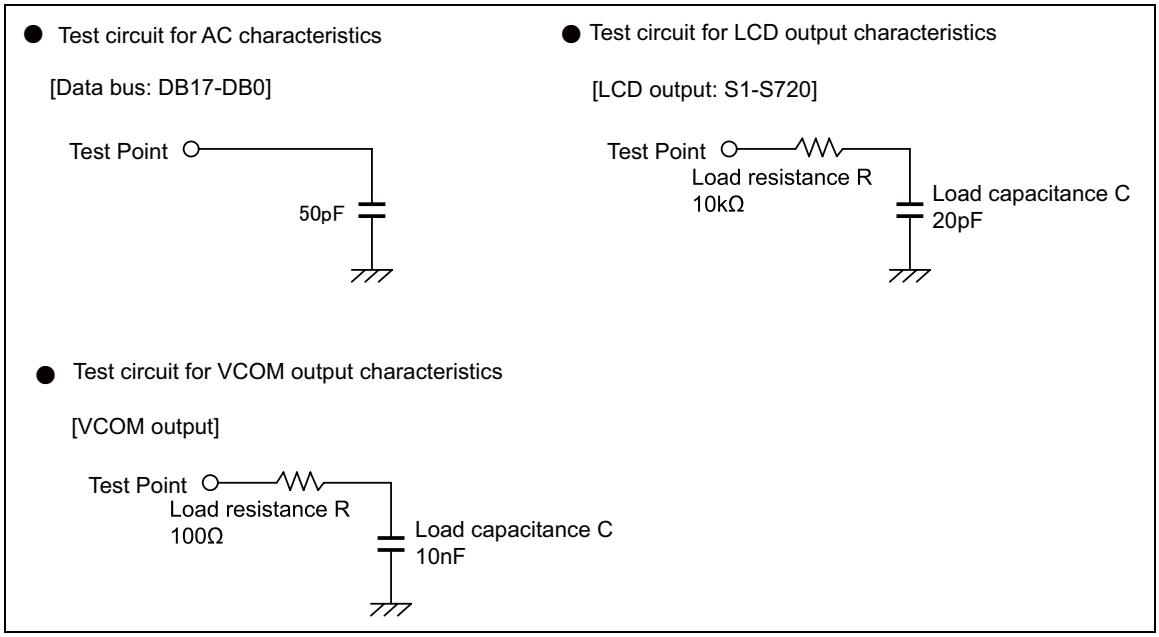
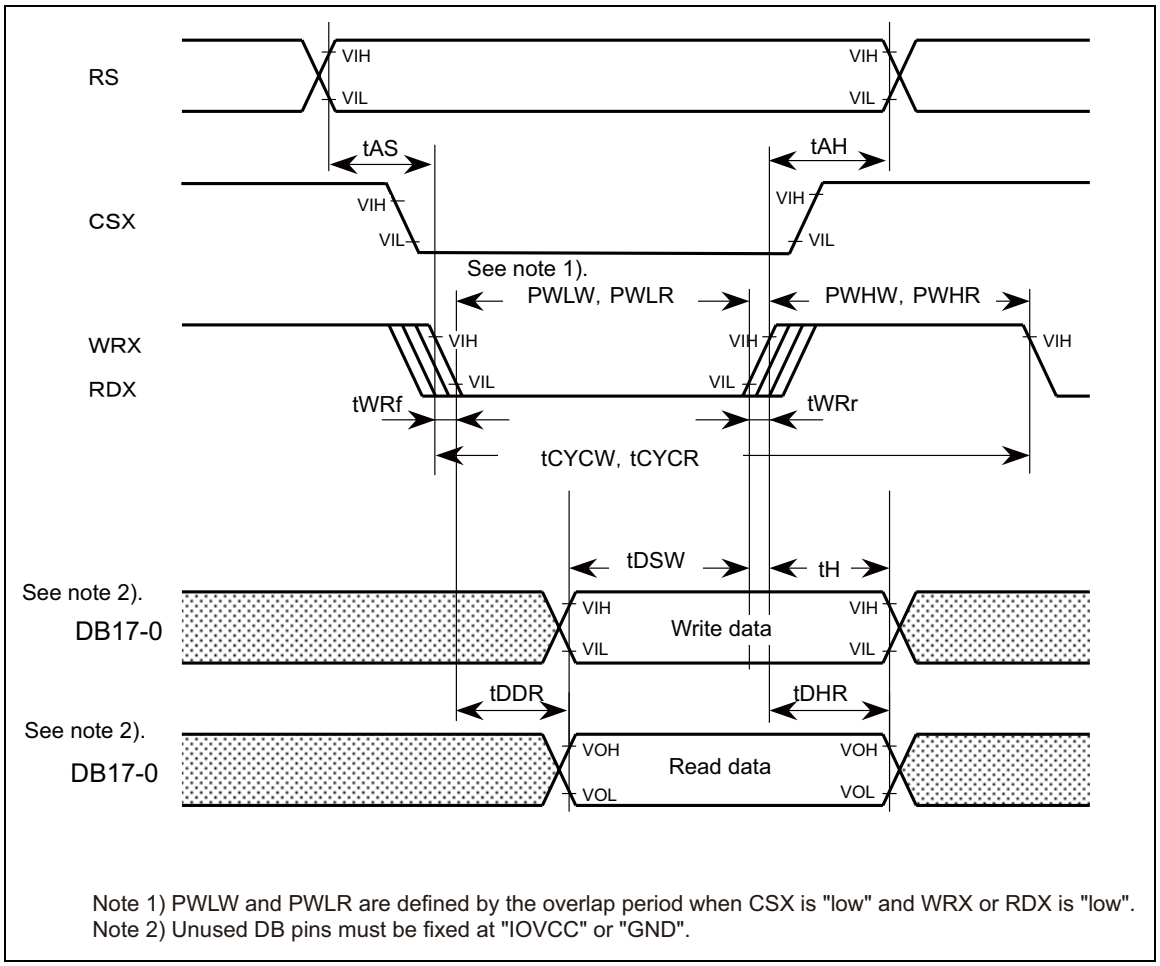


Figure 84

Timing Characteristics

80-System Bus Interface



Note 1) PWLW and PWLR are defined by the overlap period when CSX is "low" and WRX or RDX is "low".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".

Figure A

Clock Synchronous Serial Interface

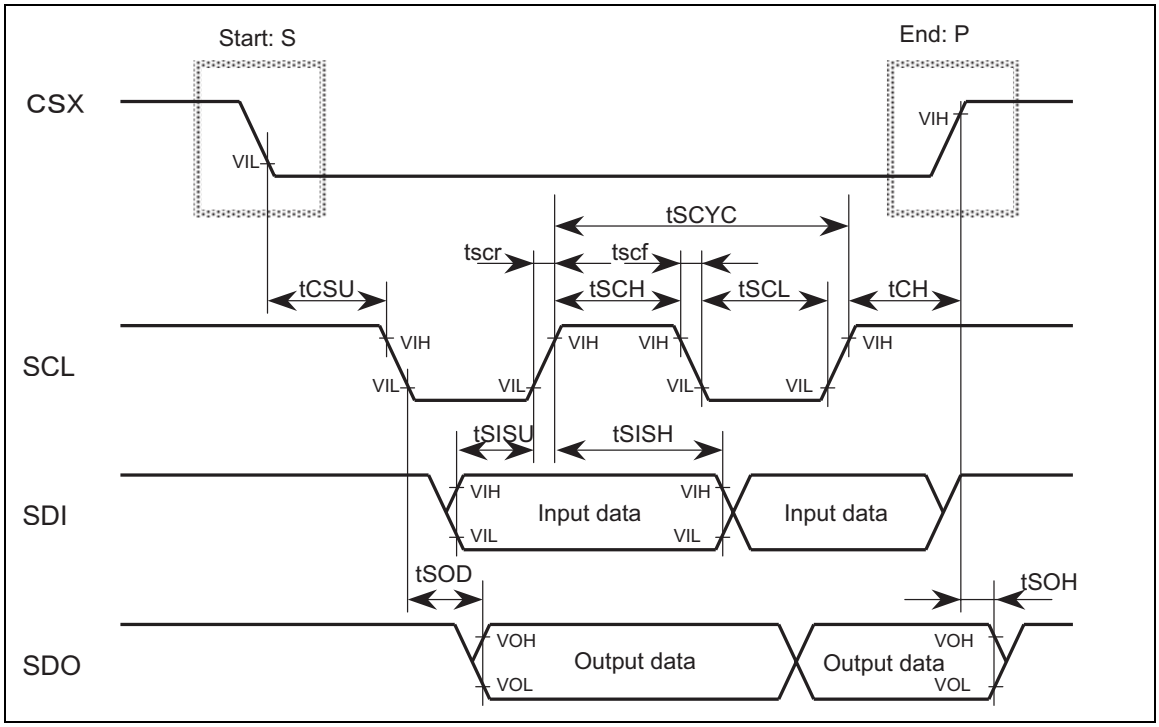


Figure B

Reset Operation

Figure C-1 Reset timing when power supply is input

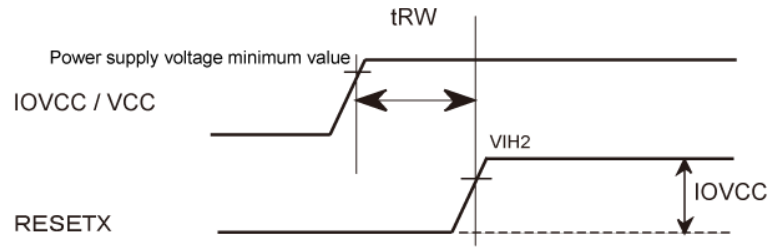


Figure C-2 Reset timing during normal operation

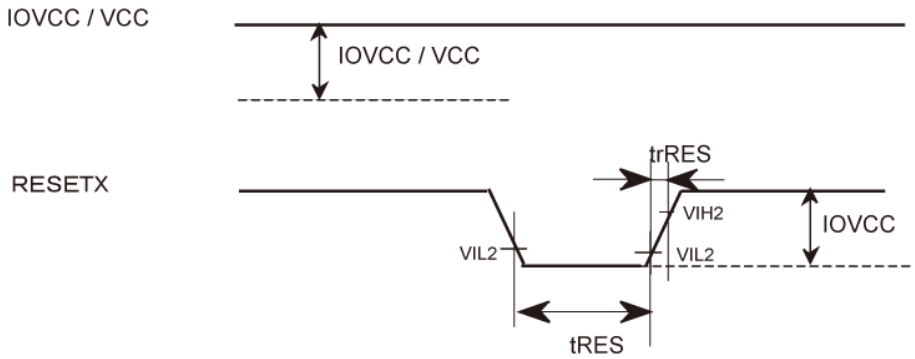


Figure C-1, C-2

RGB Interface

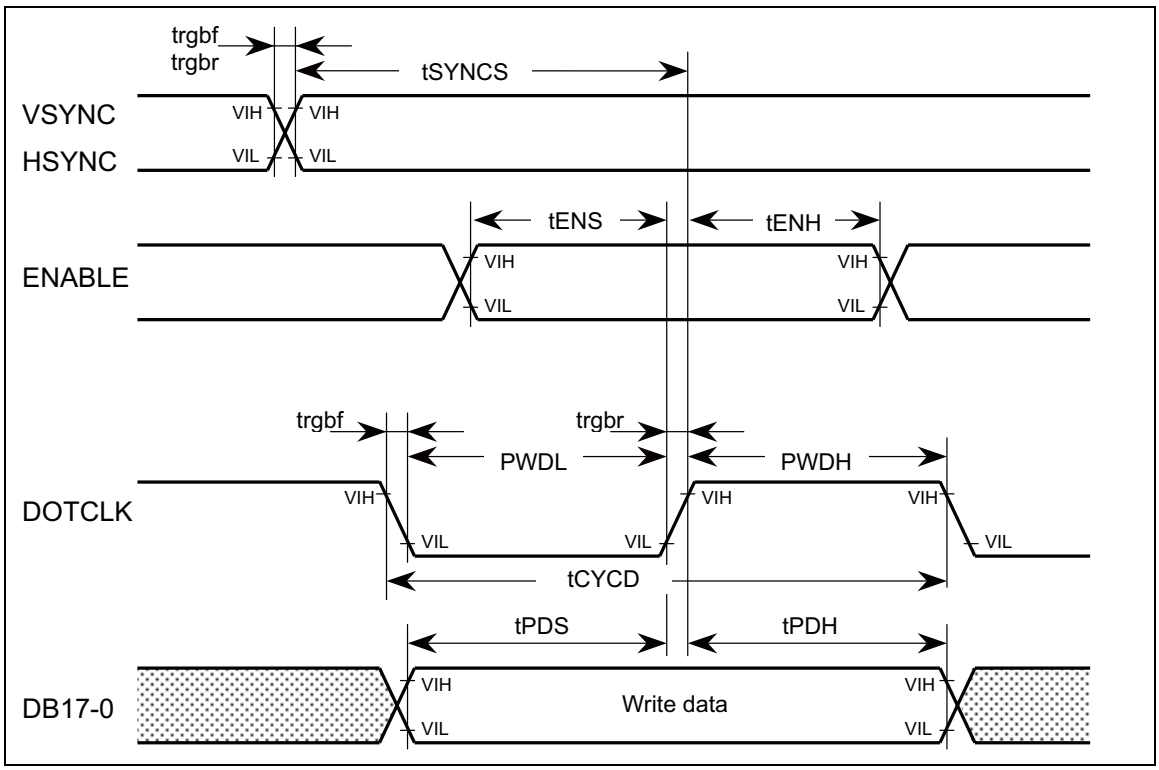


Figure D RGB Interface Timing

LCD Driver Output and VCOM Output

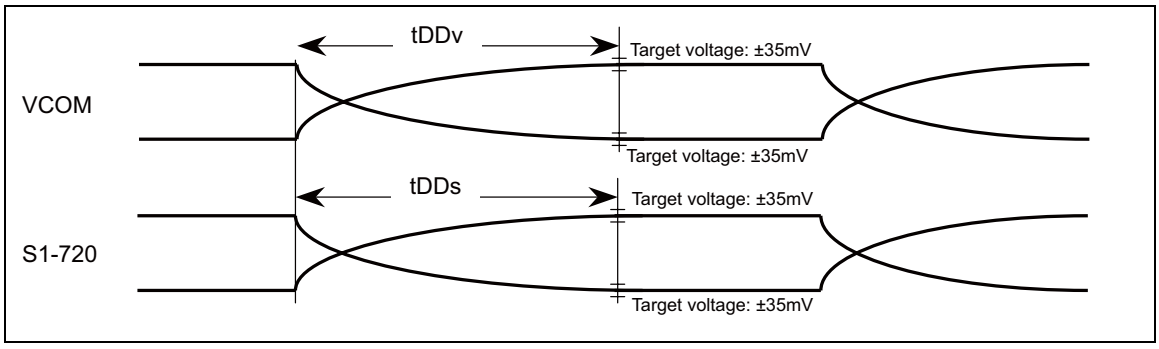


Figure E LCD Driver Output and VCOM Output

Revision Record

Rev.	Date	Page No.	Contents of Modification
0.00	September 29, 2008		First issue
0.01	December 5, 2008	18	Table 11: TEST pin connection when not used “GND” → “-“
		21	Pad coordinates Rev 0.10→ 0.20.
		33	Pad coordinate page 13: Error correction. Pins No. 1292~1209 deleted.
		47	“Make sure that FP+BP＝even number. “ added.
		89	RA0h: IB1: NVAD[1] → 0, IB0: NVAD[0] → NVAD
			Table 61: NVAD 2’hx → 1’hx
		90	RA3h: RTYRTL bit added.
		93	RC0h~RD3h: BLCON description: Deleted “and REV=1 (reverse mode)”
		103	BLC control 4 (RF9h) added.
		104	Instruction List: Rev 0.01 → 0.02.
		174	Figure 73: NVM Write and Load Sequences, error correction.
		175	Figure 74: NVM Erase Sequence, error correction.
		185	Table 97: Ici2 error correction. FP2=5 → FP2=4. COL=0 → COL1
		191	Table 108: tdds, error correction. FP0=5 → FP=4.
			tddv error correction. FP0=5 → FP=4.
0.02	January 8, 2009	9	Figure 1: Block diagram error correction. (TEST1→ TEST)
		17	Table 10: VCOMH, VCOML: Connect to Stabilizing capacitor → “-“. “Make sure to connect to stabilizing capacitor. “ deleted.
		35	Wiring Example & Recommended Wiring Resistance Rev 0.00→ 0.01 (SBD deleted.)
		95	Table 64 (ULMTW0/1): Maximum grayscale → Frame memory data
		96	Table 65 (LLMTW0/1): Minimum grayscale → Frame memory data.
		168	Figure 68 (Power supply circuit connection example 1): Note 1 deleted. VCOMH/VCOML stabilizing capacitor, SBD between VGL-GND / VGH-DDVDH deleted.
		169	Figure 69 (Power supply circuit connection example 2): Note 1 deleted. (Note 2→ Note 1) VCOMH/VCOML stabilizing capacitor, SBD between VGL-GND / VGH-DDVDH deleted.
		170	Table 98 Capacitor (15)VCOMH, (16)VCOML deleted. Numbers corrected. Table for SBD deleted.
		191	Table 10: tdds FP0=5 → FP0=4. tddv FP0=5 → FP0=4.
		192	Note 3: Error correction. Deleted “Fix pins as follows; TEST1 to TEST5 pins to GND, VDDTEST and VREFC pins to ground (AGND)”
1.00	April 7, 2009	19	Pad arrangement: Final version.
		21	Pad coordinates: Final version.
		35	Connection Example: Final version.

		54	Default values changed. VEM[1] "0" → "1", VEM[0] "0" → "1" Table 27 2'h0 Normal VCOM drive (No equalizing) → "Setting inhibited" 2'h1 Equalize VCOMH (VCOMH → VCOML) → "Setting inhibited" 2'h2 Equalize VCOML (VCOML → VCOMH) → "Setting inhibited"
		80	Default value changed. VEQWI[0] "0" → "1" Table 49 3'h0 0 clocks → "Setting inhibited"
		86	Default value changed. VEQWE[0] "0" → "1" Table 56 3'h0 0 clocks → "Setting inhibited"
		104	Instruction List Rev0.02 → 1.00.
		176	Figure 75 Power Supply On Sequence: Power supply setup time (6 frames x 1/osc) → (100ms or more)
		184-198	Electrical characteristics: Final values.
1.01	April 9, 2009	35	Connection example: Error correction. Rev1.0 → 1.01
		89	Error correction. Table61 NVAD[1:0] → NVAD

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