

a-Si TFT LCD Single Chip Driver 320RGBx480 Resolution and 262K color

Datasheet *Preliminary*

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1. Introduction

ILI9481 is a 262,144-color single-chip SoC driver for a-TFT liquid crystal display with resolution of 320RGBx480 dots, comprising a 960-channel source driver, a 480-channel gate driver, 345,600 bytes GRAM for graphic data of 320RGBx480 dots, and power supply circuit.

The ILI9481 supports 18-/16-/9-/8-bit data bus interface (DBI) and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface (DPI) for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9481 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9481 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9481 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

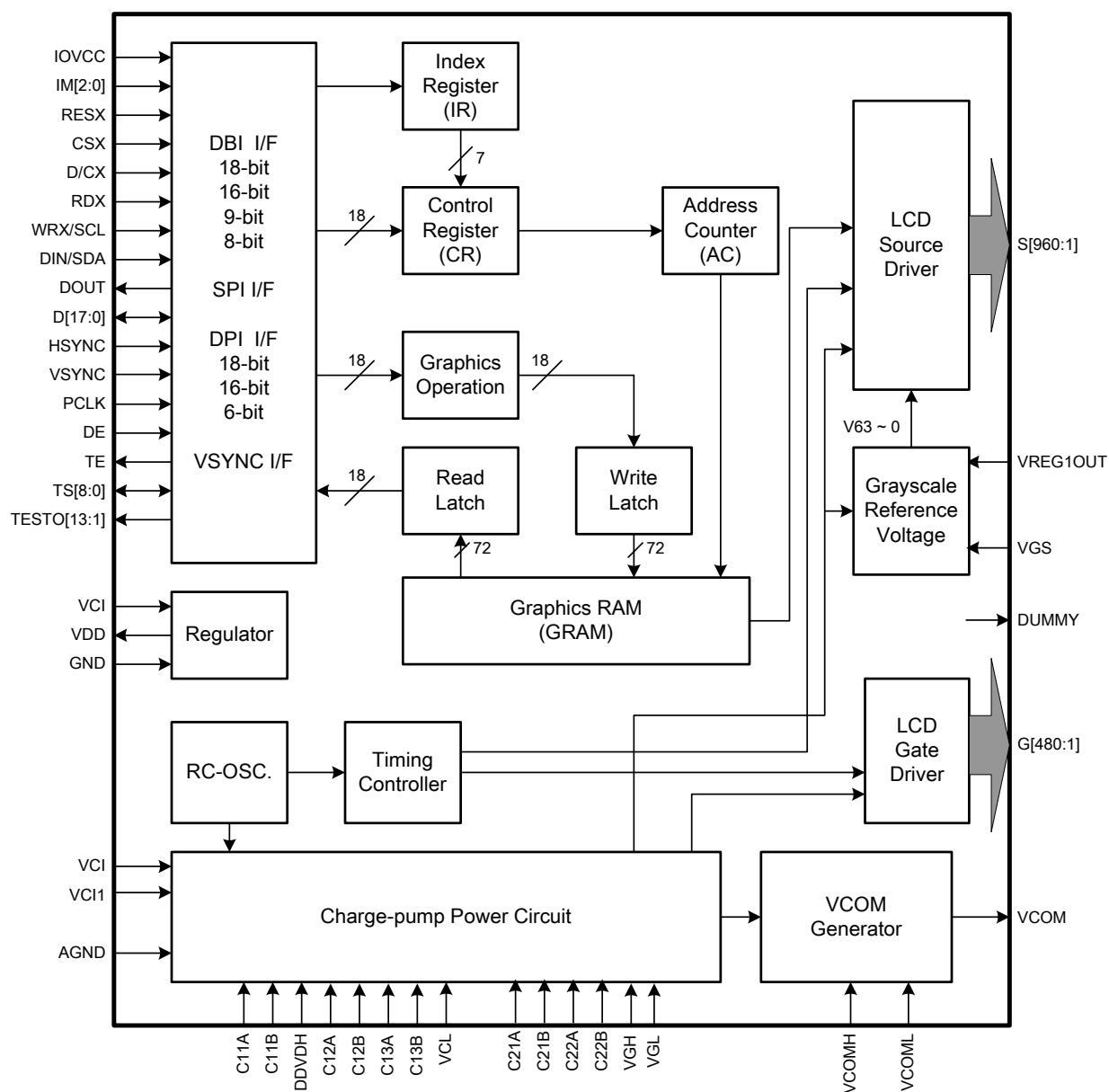
2. Features

- ◆ Display resolution: [320xRGB](H) x 480(V)
- ◆ Output:
 - 960 source outputs
 - 480 gate outputs
 - Common electrode output
- ◆ a-TFT LCD driver with on-chip full display RAM: 345,600 bytes
- ◆ MCU Interface
 - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
 - 16-bits, 18-bits RGB (DPI) interface
 - MIPI DCS command Sets
 - 3-pin/4-pin serial interface
- ◆ Display mode:
 - Full color mode: 262K-colors
 - Reduced color mode: 8-colors (3-bits MSB bits mode)
- ◆ On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Line/frame inversion
- ◆ MTP:
 - 16-bit ID1 and ID2
 - 7-bits for VCOM adjustment
- ◆ Low -power consumption architecture
 - Low operating power supplies:
 - IOVcc = 1.65V ~ 3.3V (interface I/O)
 - Vcc = 2.4V ~ 3.3V (internal logic)

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- $V_{ci} = 2.5V \sim 3.3V$ (analog)
- ◆ LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH - GND = 4.5V ~ 6.0V
 - VCL - GND = -1.0V ~ -3.0V
 - VCI - VCL \leq 6.0V
 - Gate driver output voltage
 - VGH - GND = 10V ~ 18V
 - VGL - GND = -5V ~ -12.5V
 - VGH - VGL \leq 32V
 - VCOM driver output voltage
 - VCOMH = 3.0V ~ (DDVDH-0.5)V
 - VCOML = (VCL+0.5)V ~ 0V
 - VCOMH-VCOML \leq 6.0V
- ◆ Operate temperature range: -40°C to 85°C

3. Block Diagram



4. Pin Descriptions

Pin Name	I/O	Descriptions					
IM[2:0]	I	Select the MPU system interface mode					
		IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	Colors
		0	0	0	DBI Type B 18-bit	DB[17:0]	262K
		0	0	1	DBI Type B 9-bit	DB[8:0]	262K
		0	1	0	DBI Type B 16-bit	DB[15:0]	65K/262K
		0	1	1	DBI Type B 8-bit	DB[7:0]	65K/262K
		1	0	0	Setting prohibited	-	-
		1	0	1	DBI Type C 9-bit	DIN, DOUT	8/262K
		1	1	0	Setting prohibited	-	-
		1	1	1	DBI Type C 8-bit	DIN, DOUT	8/262K
RESX	I	This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active					
CSX	I	Chip select input pin ("Low" enable).					
D/CX	I	Display data / Command selection pin D/CX='1': Display data. D/CX='0': Command data. If not used, please fix this pin at GND level.					
RDX	I	Read control pin for the DBI interface. If not used, please connect this pin to IOVCC.					
WRX/SCL	I	Write control pin for the DBI interface. When the DBI type C is selected, this pin is used as serial clock pin. If not used, please connect this pin to IOVCC.					
DB[17:0]	I/O	These pin are data bus. If not used, please connect these pins to GND.					
DIN/SDA	I/O	Serial data input pin and used for the DBI type C mode. If not used, please connect this pin to ground.					
DOUT	O	Serial data output pin and used for the DBI type C mode.					
TE	O	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, please open this pin.					
PCLK	I	Pixel clock signal in DPI interface mode. If not used, please fix this pin at GND level.					
VSYNC	I	Vertical sync. signal in DPI interface mode. If not used, please fix this pin at GND level.					
HSYNC	I	Horizontal sync. signal in DPI interface mode. If not used, please fix this pin at GND level.					
DE	I	Data enable signal in DPI interface mode. If not used, please fix this pin at GND level.					

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Pin Name	I/O	Descriptions							
SD	I	Control pin to shut down display, only used in the DPI interface mode.							
		<table border="1"> <thead> <tr> <th>SD</th><th>Shut Down Control</th></tr> </thead> <tbody> <tr> <td>0</td><td>Normal Display</td></tr> <tr> <td>1</td><td>Power shut down</td></tr> </tbody> </table>		SD	Shut Down Control	0	Normal Display	1	Power shut down
SD	Shut Down Control								
0	Normal Display								
1	Power shut down								
CM	I	Control pin for switching between normal color and reduced color mode, only used in the DPI interface mode.							
		<table border="1"> <thead> <tr> <th>CM</th><th>Color Mode</th></tr> </thead> <tbody> <tr> <td>0</td><td>Normal Display Color</td></tr> <tr> <td>1</td><td>Reduced Color Mode (8-color)</td></tr> </tbody> </table>		CM	Color Mode	0	Normal Display Color	1	Reduced Color Mode (8-color)
CM	Color Mode								
0	Normal Display Color								
1	Reduced Color Mode (8-color)								
Power Input Pins									
IOVCC	P	Power supply to interface pins Connect to external power supply (IOVCC= 1.65~3.3V).							
VCI	P	Power supply to liquid crystal power supply analog circuit. Connect to external power supply (VCI=2.5~3.3V).							
DGND AGND	P	Power ground pin. Make sure GND=0V.							
VPG	P	Power supply pin for the NV memory programming. Please provide 5 volt to this pin for NV memory programming.							
LCD signals Pins									
S1 ~ S960	O	Source driver output pins.							
G1 ~ G480	O	Gate driver output pins.							
VDD	O	Internal logic regulator output. Used as internal logic power supply. Connect to stabilizing capacitor.							
VCI1	P	Reference voltage for the step-up circuit 1. Set VCI1 level so that DDVDH, VGH and VGL are within the ratings.							
DDVDH	P	Power supply for the source driver and VCOM.							
VGH	P	Power supply to drive liquid crystal.							
VGL	P	Power supply for LCD drive.							
VCL	P	Power supply to drive VCOML.							
C11A, C11B, C12A, C12B	P	Make sure to connect to capacitor that is used in internal step-up circuit 1.							
C13A, C13B, C21A, C21B, C22A, C22B,	P	Make sure to connect to capacitor that is used in internal step-up circuit 2. Connect to capacitors according to the step-up factors in use.							
VREG1OUT	P	Outputs voltage level generated from VRH VCILVL. The step-up factor applied to VRH VCILVL is set by VRH bits. Used as source driver grayscale reference voltage VREG1OUT, reference voltage to VCOMH, and Vcom amplitude reference voltage. Connect to stabilizing capacitor when in use.							

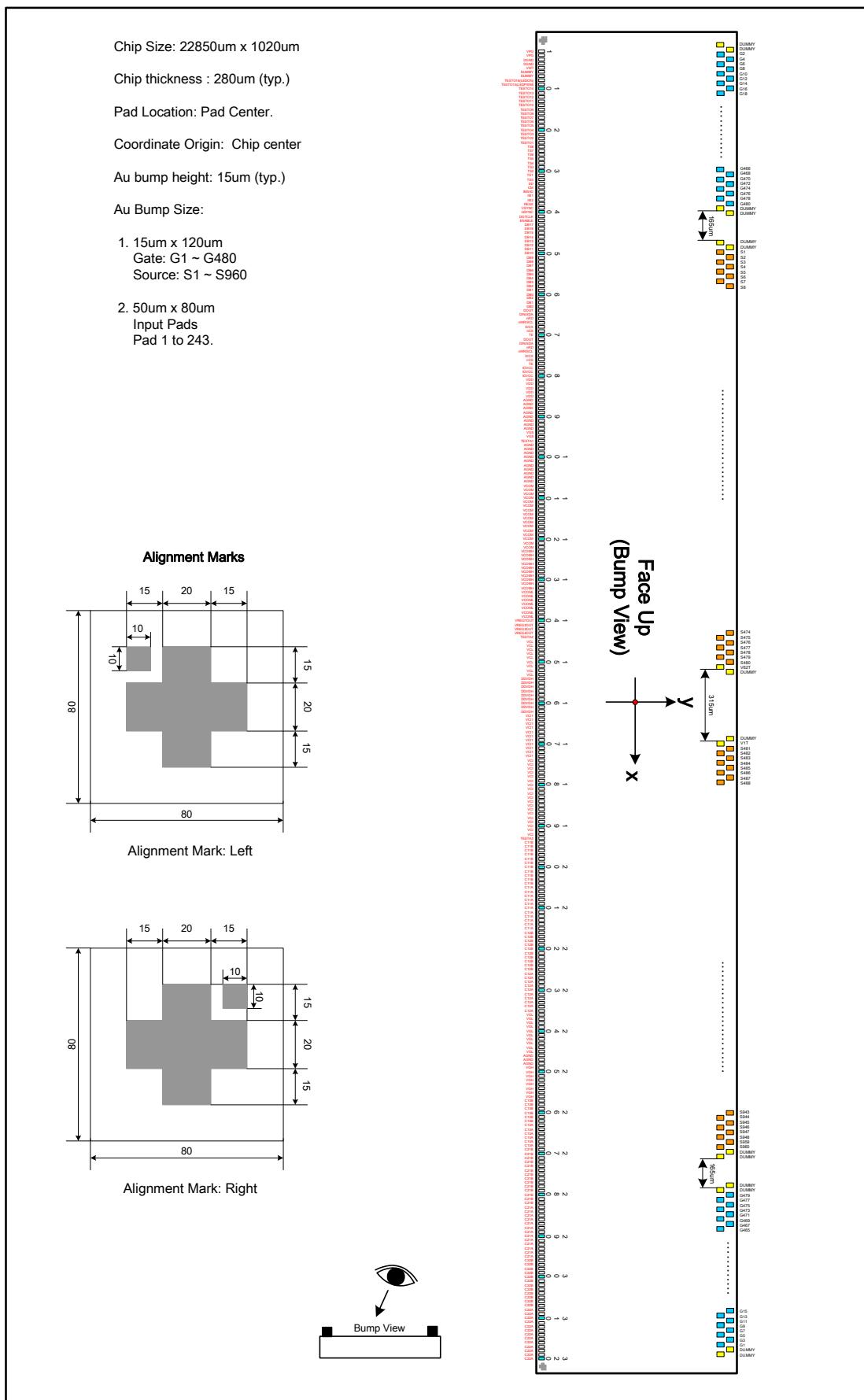
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Pin Name	I/O	Descriptions
		VREG1OUT=4.0~(DDVDH-0.500)[V]
VCOM	P	TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML. Registers set the alternating cycle. Registers set the alternating cycle and operate or halt VCOM.
VCOMH	P	VCOM high level. Adjust the voltage by internal electronic volume (VCM)
VCOML	P	VCOM low level. Adjust the voltage by VDV bits. VCOML=(VCL+0.5)~0[V]
VGS	I	Reference level for grayscale generating circuit.
TEST pins		
TS[8:0]	I	Test pins These pins are internal pulled low. Please leave these pins as open.
TESTO[16:1]	O	Test pins Please leave these pins as open.
TESTA1-A3	I/O	Test pins Please leave these pins as open.
VWT	-	Test pin Please leave this pin as open.
DUMMY	-	Dummy Pins These pins are floating.

Liquid crystal power supply specifications Table

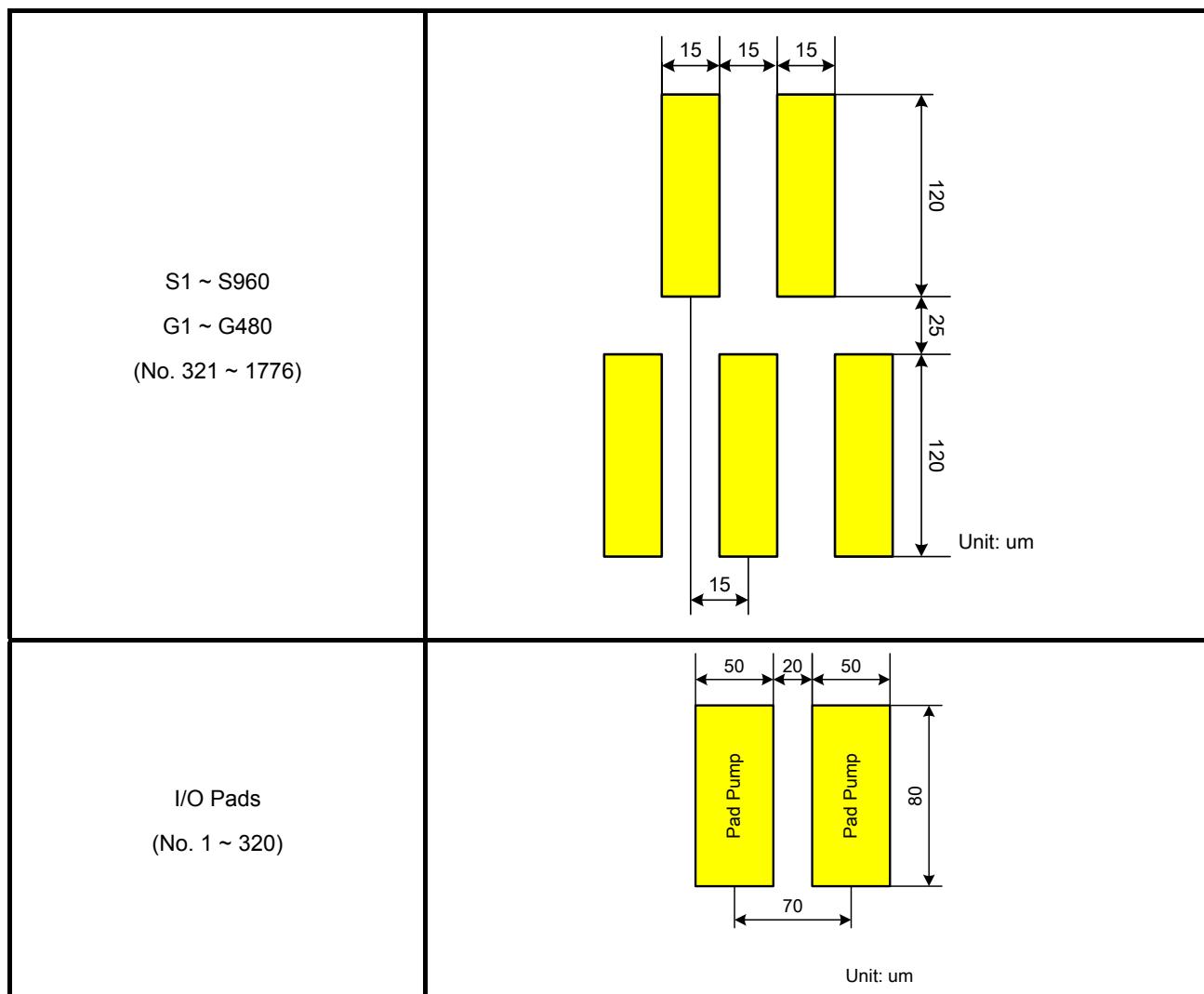
No.	Item	Description
1	TFT Source Driver	960 pins (320 x RGB)
2	TFT Gate Driver	480 pins
3	TFT Display's Capacitor Structure	Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S960
		G1 ~ G480
		VCOM
5	Input Voltage	IOVcc
		Vci
6	Liquid Crystal Drive Voltages	DDVDH
		VGH
		VGL
		VCL
		VGH - VGL
		Vci - VCL
7	Internal Step-up Circuits	DDVDH
		VGH
		VGL
		VCL

5. Pad Arrangement and Coordination



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No.	Name	X	Y
1751	G48	-10830	389
1752	G46	-10845	244
1753	G44	-10860	389
1754	G42	-10875	244
1755	G40	-10890	389
1756	G38	-10905	244
1757	G36	-10920	389
1758	G34	-10935	244
1759	G32	-10950	389
1760	G30	-10965	244
1761	G28	-10980	389
1762	G26	-10995	244
1763	G24	-11010	389
1764	G22	-11025	244
1765	G20	-11040	389
1766	G18	-11055	244
1767	G16	-11070	389
1768	G14	-11085	244
1769	G12	-11100	389
1770	G10	-11115	244
1771	G8	-11130	389
1772	G6	-11145	244
1773	G4	-11160	389
1774	G2	-11175	244
1775	DUMMY	-11190	389
1776	DUMMY	-11205	244
Alignment mark -Left		-11300	-400
Alignment mark -Right		11300	-400



6. Block Function Description

Interface

The ILI9481 incorporates command method 18-/16-/9-/8-bits bus display command interface, which consists of 8 bits command registers and 8 bits parameter registers. Parameter registers consist of 8 bits write data register (WDR) and 8bit read data register (RDR).

WDR stores data to be written into GRAM or parameters temporarily while RDR stores data read out from GRAM temporarily. When data is written from microcomputer to GRAM, the ILI9481 writes firstly to WDR, and then the data is written to GRAM automatically by internal operation. Because read out operation from GRAM is conducted through RDR, first read out data is invalid. Normal data is read out from 2nd read out data.

Register selection

DCX	RDX	WRX	Operation
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

Address Counter (AC)

Address counter (AC) gives address to GRAM. When command setting address is written to CDR, the data is transferred from CDR to AC.

When data is written to GRAM, address counter (AC) increments by +1 or -1 automatically. AC after data is read out increments by +1 or -1 likewise. The ILI9481 writes data to only rectangular area that was specified by GRAM.

Graphic RAM (GRAM)

The graphic RAM (GRAM) stores 345,600 byte bit pattern data using 18 bits for one pixel, enabling a maximum 320RGB x 480 dot graphic display at the maximum.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the y correction register. The ILI9481 displays 262,144 colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to a-TFT panel, VREG1OUT, VGH, VGL, VCOMH and VCOML.

Timing Generating

The timing generator generates timing signals for internal circuits such as the internal GRAM. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is outputted separately so that they do not interfere with each other.

Oscillator

The ILI9481 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The liquid crystal display driver circuit consists of 960 source drivers (S1~S960). Display pattern data is latched when 960 byte data is input. This latched data controls source drivers and outputs drive waveform.

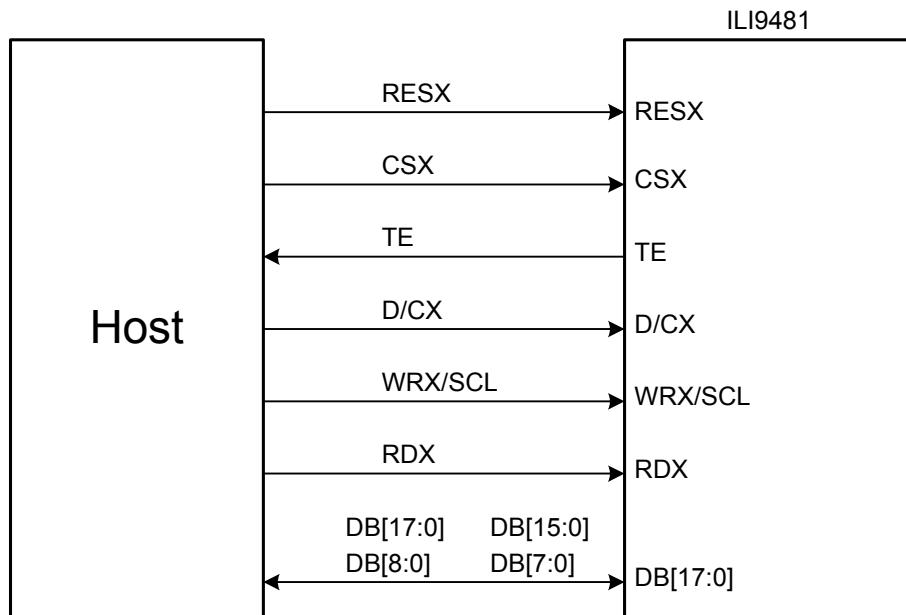
The shift direction of 960-bit output from the source driver can be changed by setting commands.

The gate driver consists of 480 gate drivers (G1~G480) and outputs either VGH or VGL level. The shift direction of gate driver is set by GS bit. Scan direction of gate driver is set by SM bit enabling users to set the ILI9481 so that it suits mounting method

7. Function Description

7.1. Display Bus Interface (DBI)

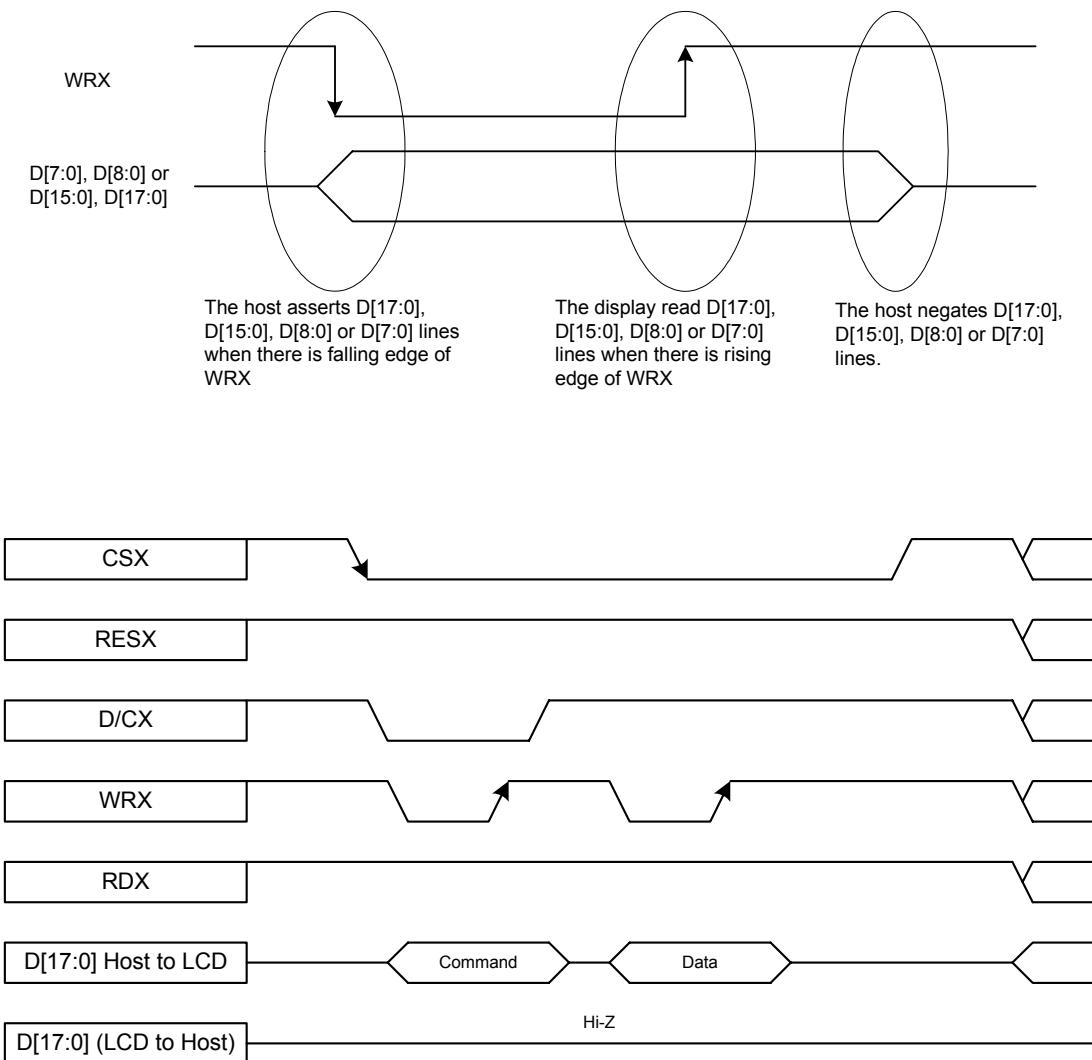
The ILI9481 uses a 22-wires 18-bit parallel interface. The chip-select CSX (active low) enables and disables the DBI interface. RESX (active low) is an external reset signal. WRX is the data write, RDX is the data read and D[17:0] is parallel DBI data. There are four 17/16/9/8-bit types interface supported for the display data transfer. The Graphics Controller Chip reads the data at the rising edge of RDX signal. The D/CX is data/command flag. When D/CX = "1", D17 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.



7.1.1. Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. D/CX is driven low while command information is on the interface and is pulled high when data is present.

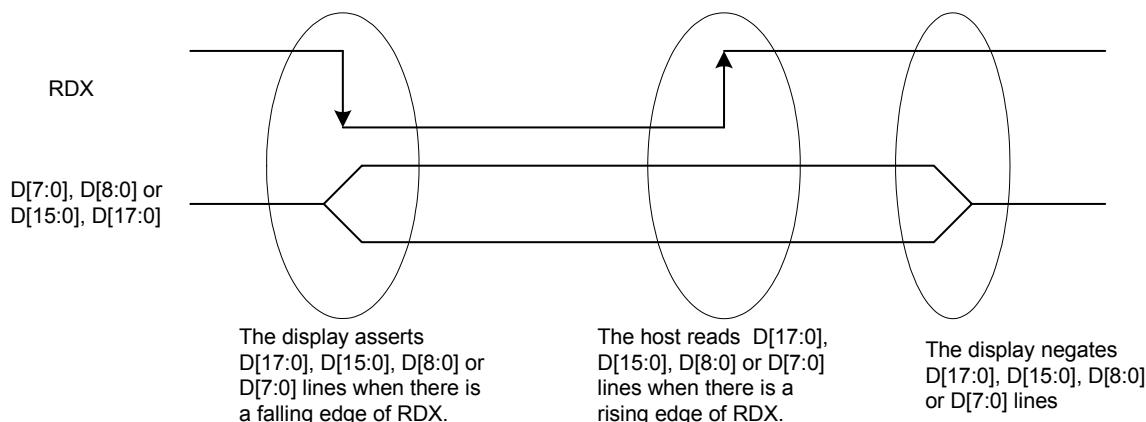
The following figure shows a write cycle for the type B interface.



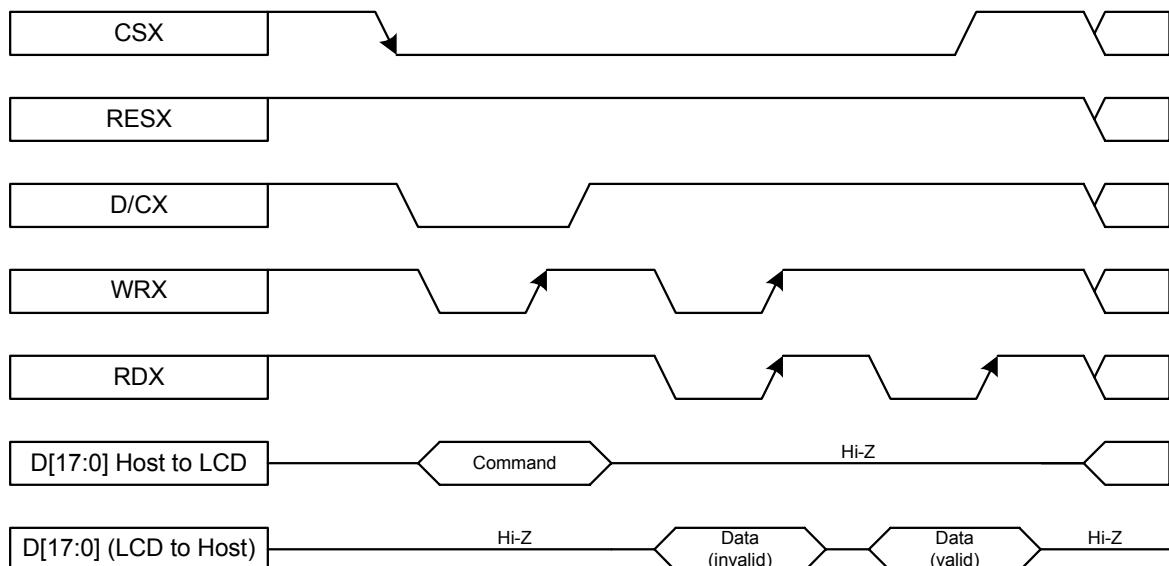
7.1.2. Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. D/CX is driven high during the read cycle.

The following figure shows the read cycle for the type B interface.



Note: RDX is an unsynchronized signal (It can be stopped).



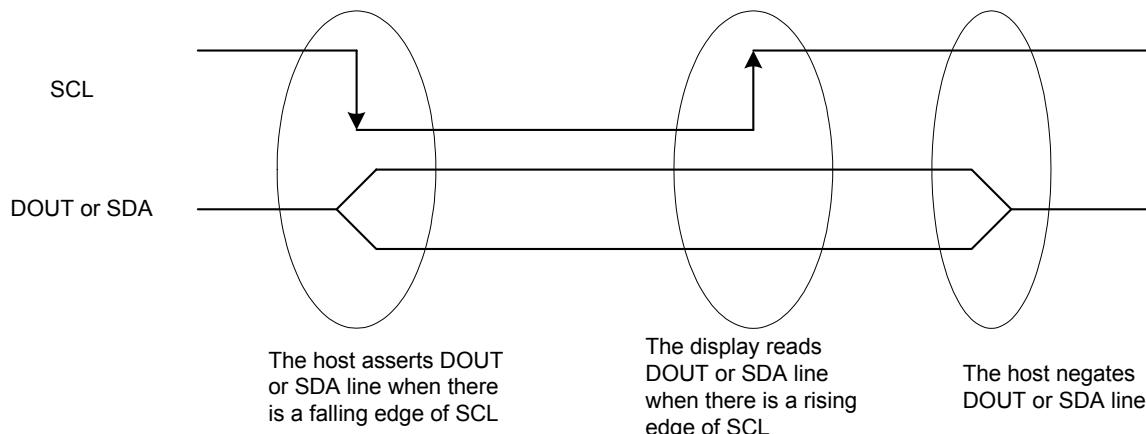
Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.2. Serial Interface (Type C)

7.2.1. Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The Type C interface utilizes CSX, SCL and SDA or DOUT signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

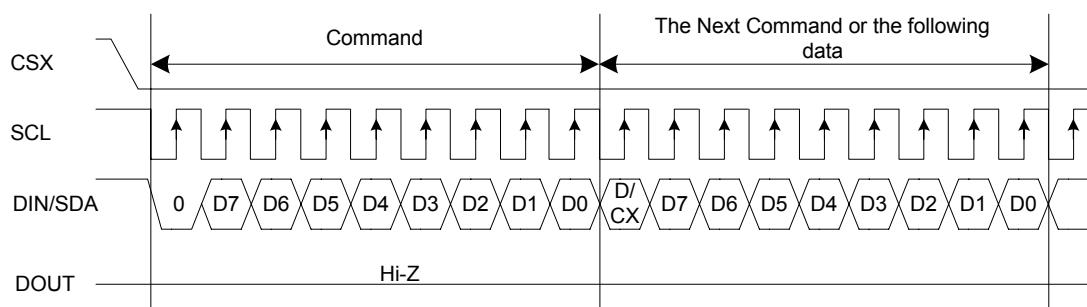
The following figure shows the write cycle for the type C interface.



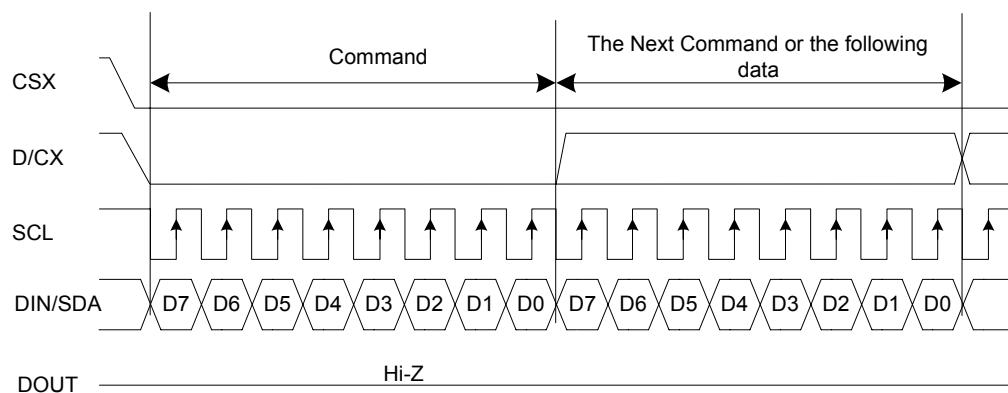
Note: SCL is an unsynchronized signal; it can be stopped.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight write cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface write sequences are described in the following Figure



DBI Type C Interface Write Sequence – Option 1



DBI Type C Interface Write Sequence – Option 3

Note:

1. D7 is MSB and D0 is LSB of byte.
2. When the Interface control register (C6h) SDA_EN is set as '1', the DIN/SDA pin is bi-direction and DOUT pin is not used.
3. When the Interface control register (C6h) SDA_EN is set as '0', the DIN/SDA pin is uni-direction and DIN and DOUT pins are used for data write and read.

DBI Type C Interface IM[2:0]=101/111

	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3bpp Frame Memory Write	3'h1	0		R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]		R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]		R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]			
	3'h1	1		R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]		R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]		R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]			
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]		B[5]	B[4]	B[3]	B[2]	B[1]	B[0]				
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]		g[5]	g[4]	g[3]	g[2]	g[1]	g[0]		b[5]	b[4]	b[3]	b[2]	b[1]	b[0]				

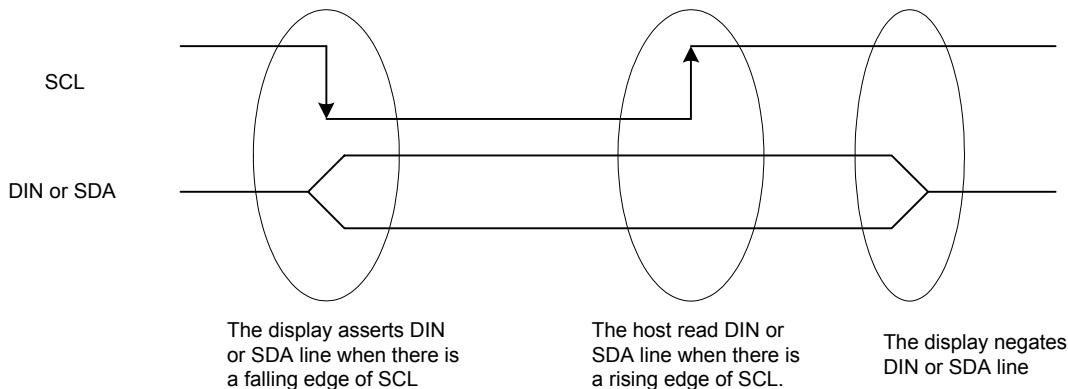
3/16-bit data extend to 18-bit

		Frame Memory Data (18bpp)																								
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0							
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]							
3bpp	*	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	G[0]	G[0]	G[0]	G[0]	G[0]	G[0]	B[0]	B[0]	B[0]	B[0]	B[0]	B[0]							

7.2.2. Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The Type C interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL. D/CX is driven during the read cycle if it is used in option 3.

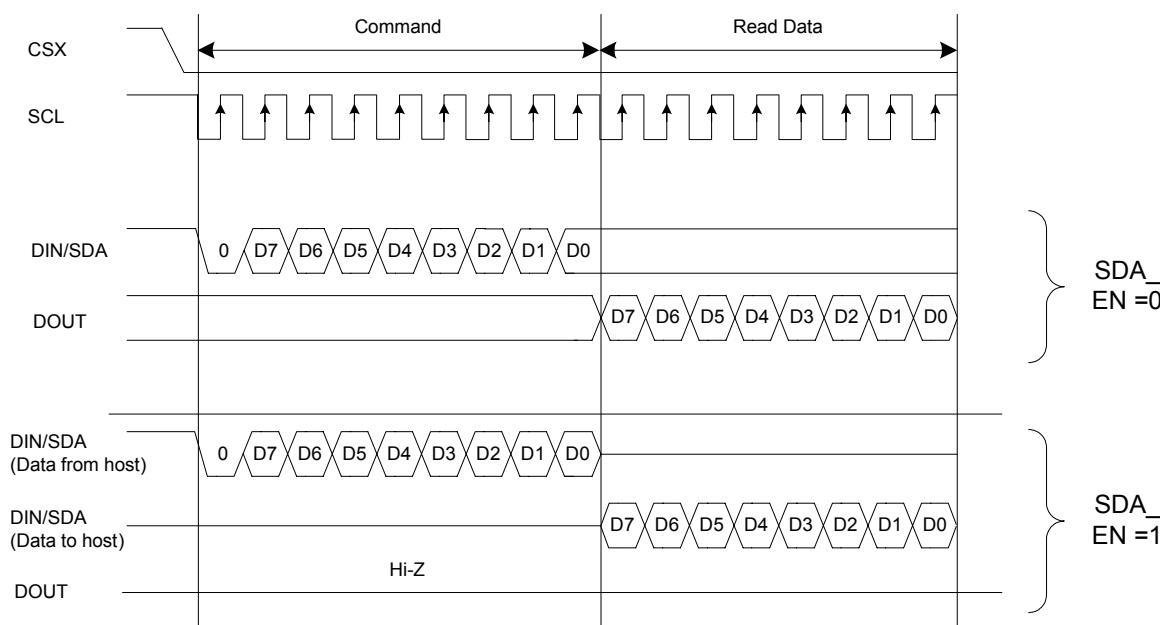
The following figure shows the read cycle for the type C interface.



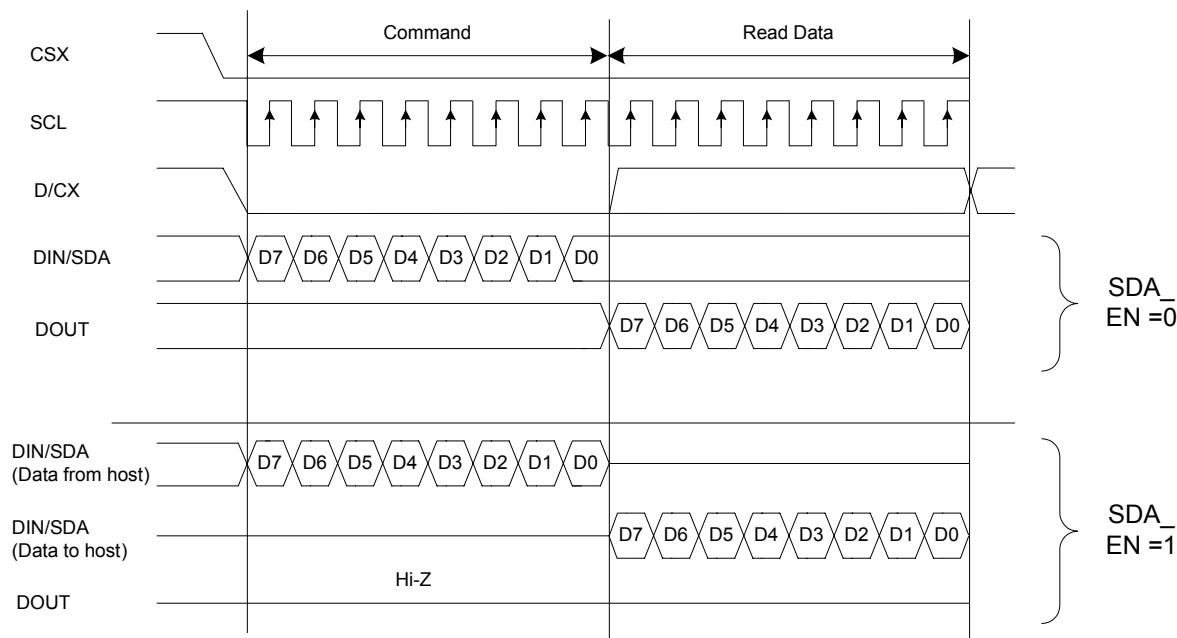
Note: SCL is an unsynchronized signal; it can be stopped.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight read cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface read sequences are shown in the following figures



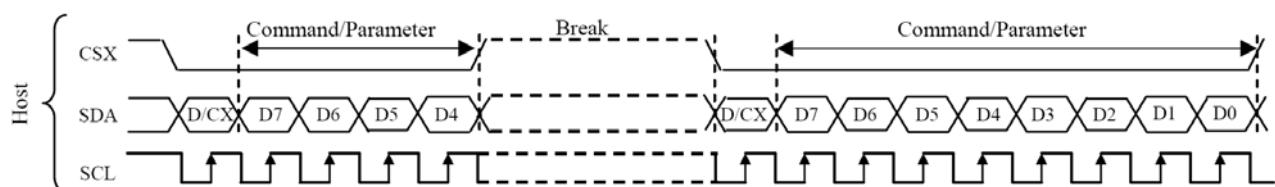
Note: D7 is MSB and D0 is LSB of byte.



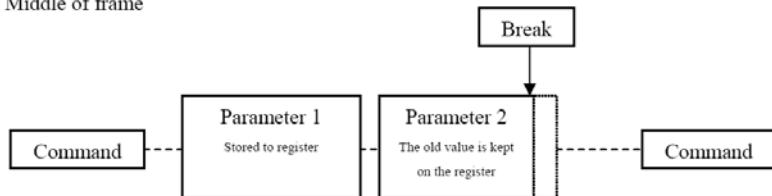
7.2.3. Break and Pause Sequences

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

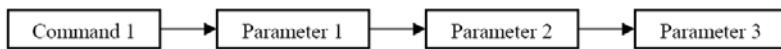


1. Middle of frame

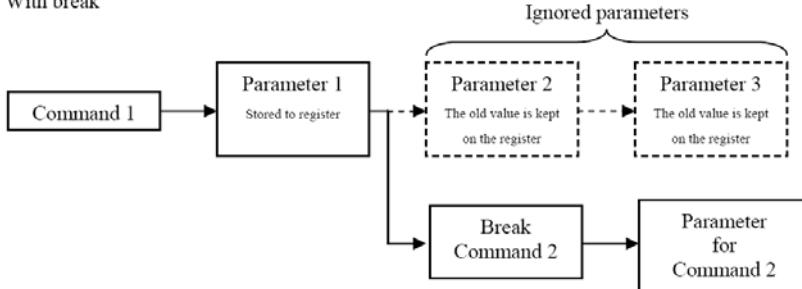


2. Between frames

Without break



With break



Break can be e.g. another command or noise pulse.

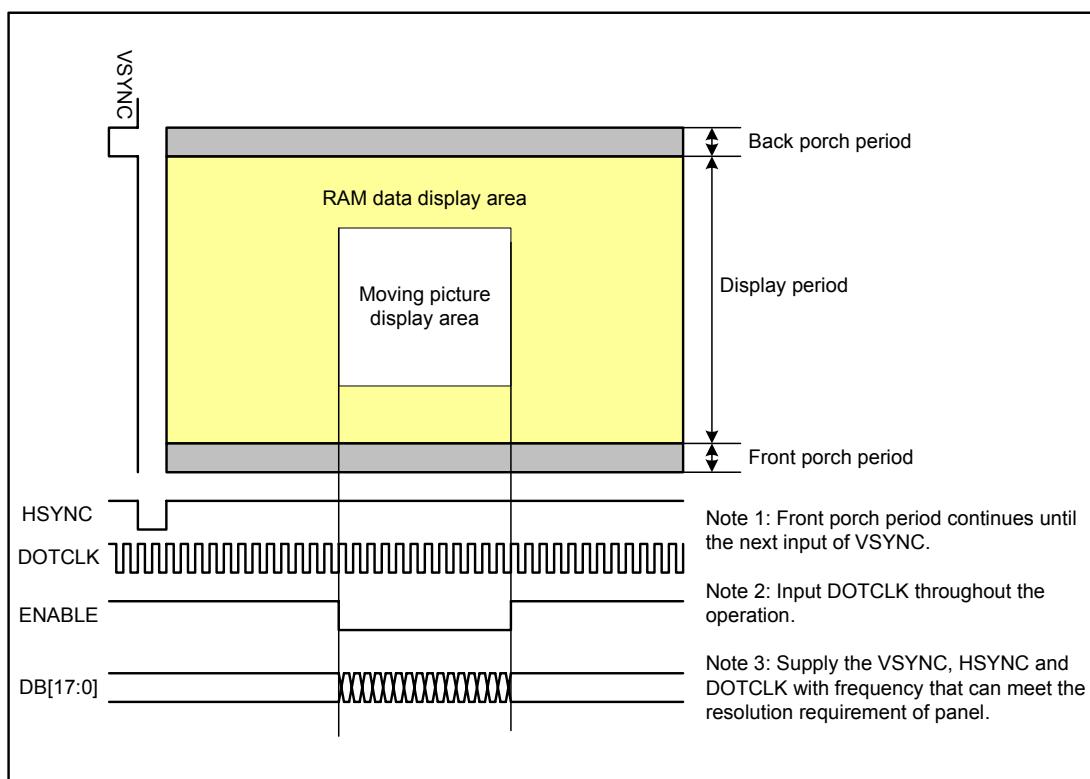
7.3. Display Pixel Interface (DPI)

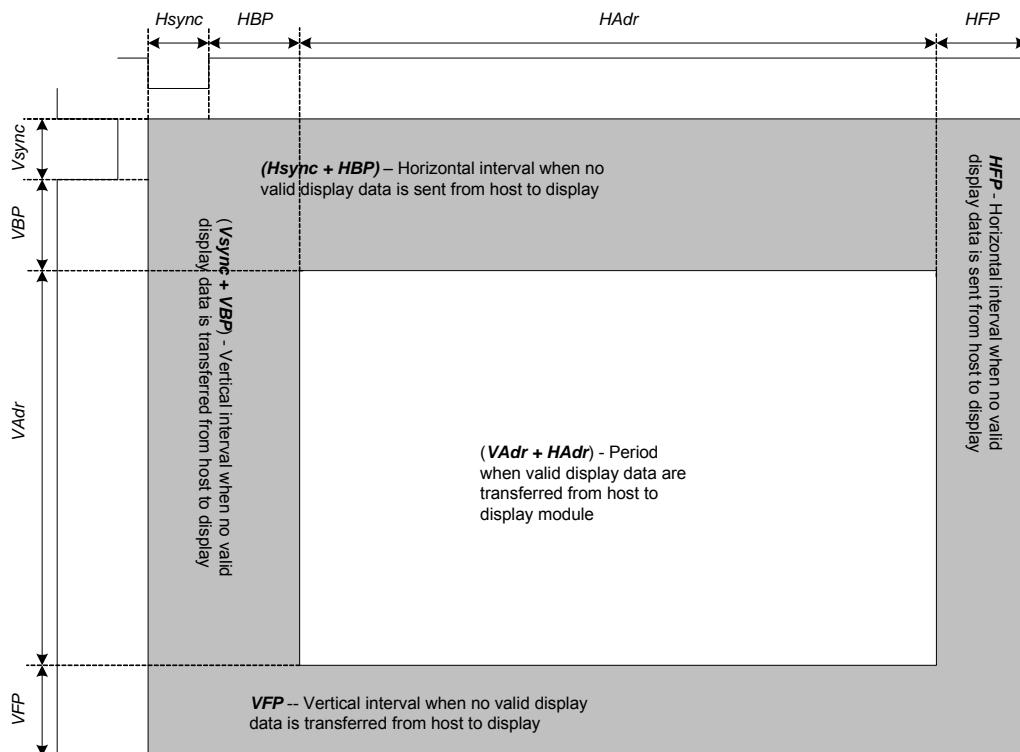
In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image.

Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16 or 18-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.





Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
PCLK Cycle	PCLKCYC		-	88	-	ns
Horizontal Synchronization	Hsync		-	10	-	PCLK
Horizontal Back Porch	HBP		-	20	-	PCLK
Horizontal Address	HAdr		-	320	-	PCLK
Horizontal Front Porch	HFP		-	40	-	PCLK
Vertical Synchronization	Vsync		-	2	-	Line
Vertical Back Porch	VBP		-	2	-	Line
Vertical Address	VAdr		-	480	-	Line
Vertical Front Porch	VFP		-	4	-	Line
Vsync setup time	VSST				-	Hz
Vsync hold time	VSHT				-	Hz
Hsync setup time	HSST				-	Hz
Hsync hold time	HSHT				-	Hz
Data setup time	DST				-	Hz
Data hold time	DHT				-	Hz
Vertical Frequency(*)				60	-	Hz
Horizontal Frequency(*)			-	29.282	-	KHz
PCLK Frequency(*)			-	11.42Mhz	-	MHz

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

8. Command

8.1. Command List

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	ILI9418 Implementation
00h	nop	C	0	Yes	Yes
01h	soft_reset	C	0	Yes	Yes
06h	get_red_channel	R	1	No	No
07h	get_green_channel	R	1	No	No
08h	get_blue_channel	R	1	No	No
0Ah	get_power_mode	R	1	Yes	Yes
0Bh	get_address_mode	R	1	Yes (Bit[7:0])	Yes (Bit[7:3] , Only)
0Ch	get_pixel_format	R	1	Yes	Yes
0Dh	get_display_mode	R	1	Yes	Yes
0Eh	get_signal_mode	R	1	Yes	Yes
0Fh	get_diagnostic_result	R	1	Bit7/6 : Yes Bit5/4 : Optional	Yes (Bit7/6 Only)
10h	enter_sleep_mode	C	0	Yes	Yes
11h	exit_sleep_mode	C	0	Yes	Yes
12h	enter_partial_mode	C	0	Yes	Yes
13h	enter_normal_mode	C	0	Yes	Yes
20h	exit_invert_mode	C	0	Yes	Yes
21h	enter_invert_mode	C	0	Yes	Yes
26h	set_gamma_curve	W	1	Yes	No
28h	set_display_off	C	0	Yes	Yes
29h	set_display_on	C	0	Yes	Yes
2Ah	set_column_address	W	4	Yes	Yes
2Bh	set_page_address	W	4	Yes	Yes
2Ch	write_memory_start	W	Variable	Yes	Yes
2Dh	wite_LUT	W	Variable	Optional	No
2Eh	read_memory_start	R	Variable	Yes	Yes
30h	set_partial_area	W	4	Yes	Yes
33h	set_scroll_area	W	6	Yes	Yes
34h	set_tear_off	C	0	Yes	Yes
35h	set_tear_on	W	1	Yes	Yes
36h	set_address_mode	W	1	Yes (Bit7-0)	Yes (Bit[7:3], Bit[1:0] Only)
37h	set_scroll_start	W	2	Yes	Yes
38h	exit_idle_mode	C	0	Yes	Yes
39h	enter_idle_mode	C	0	Yes	Yes
3Ah	set_pixel_format	W	1	Yes	Yes
3Ch	write_memory_continue	W	Variable	Yes	Yes
3Eh	read_memory_continue	R	Variable	Yes	Yes
44h	set_tear_scanline	W	2	Yes	Yes
45h	get_scanline	R	2	Yes	Yes
A1h	read_DDB_start	R	5	Yes	Yes
A8h	read_DDB_continue	R	Variable	Yes	Yes

Operational Code (Hex)	Function	Command(C) Read(R)/Write(W)	Number Of Parameter
B0h	Command Access Protect	W/R	1
B1h	Low Power Mode Control	W/R	1
B3h	Frame Memory Access and Interface setting	W/R	5
B4h	Display Mode and Frame Memory Write Mode setting	W/R	1
BFh	Device code Read	R	4
C0h	Panel Driving Setting	W/R	7
C1h	Display Timing Setting for Normal Mode	W/R	3
C2h	Display Timing Setting for Partial Mode	W/R	3
C3h	Display Timing Setting for Idle Mode	W/R	3
C5h	Frame rate and Inversion Control	W/R	1
C6h	Interface Control	W/R	1
C8h	Gamma Setting	W/R	12
D0h	Power Setting	W/R	3
D1h	VCOM Control	W/R	3
D2h	Power Setting for Normal Mode	W/R	2
D3h	Power Setting for Partial Mode	W/R	2
D4h	Power Setting for Idle Mode	W/R	2
E0h	NV Memory Write	W/R	1
E1h	NV Memory Control	W/R	1
E2h	NV Memory Status	W/R	3
E3h	NV Memory Protection	W/R	2
E8h	EEPROM Write Enable	C	0
E9h	EEPROM Write Disable	C	0
EAh	EEPROM Word Write	W/R	2
EBh	EEPROM Word Read	R	3
ECh	EEPROM Address Set	W/R	1
EDh	EEPROM Erase	W/R	1
EEh	EEPROM Erase All	C	0
B0~FF Except above command	LSI TEST Registers	W/R	Variable

8.2. Command Description

8.2.1. NOP (00h)

NOP (No Operation)																										
00H	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00													
Parameter	NO PARAMETER																									
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.																									
Restriction	None																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																									
Power On Sequence	N/A																									
SW Reset	N/A																									
HW Reset	N/A																									
Flow Chart	None																									

8.2.2. Soft_reset (01h)

Soft_reset																										
01H	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01													
Parameter	NO PARAMETER																									
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are affected by this command. X = Don't care																									
Restriction	Software Reset Command cannot be sent during Sleep Out sequence. Any new command is cannot be sent for 10-frame period until the ILI9481 enters Sleep-In mode. Do not send any command.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																									
Power On Sequence	N/A																									
SW Reset	N/A																									
HW Reset	N/A																									
Flow Chart	<pre> graph TD SWRESET[SWRESET] --> Display[Display whole blank screen] Display --> Set[Set Commands to S/W Default Value] Set --> SleepIn[Sleep In Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

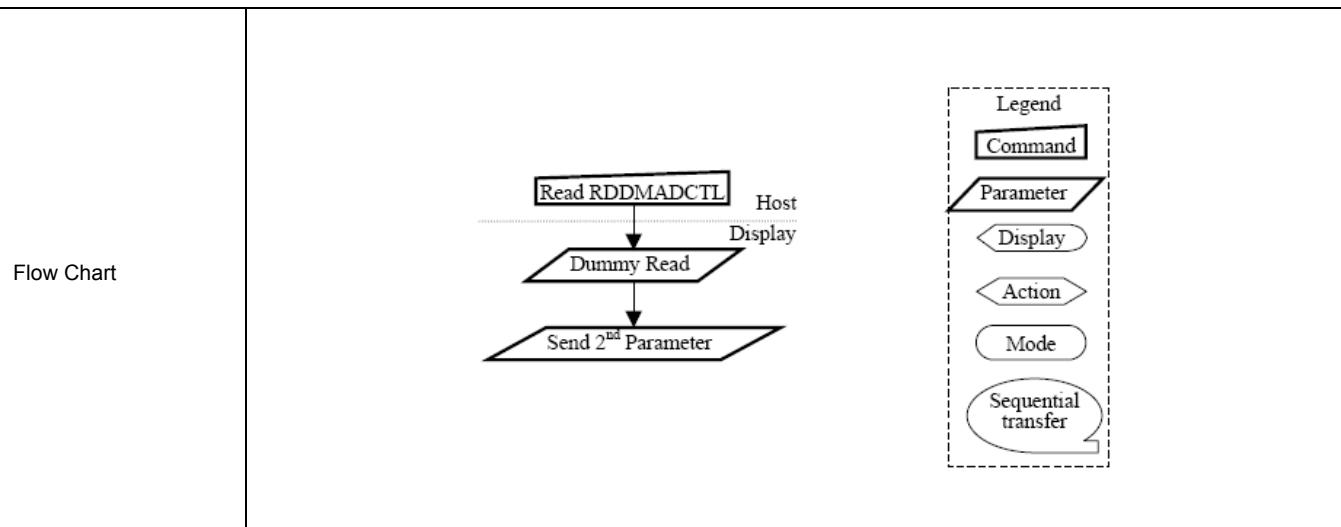
8.2.3. Get_power_mode (0Ah)

0AH	Get_power_mode																																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0A																												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																												
2 nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	0	0	xx																												
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> <tr> <td>D6</td> <td>Idle Mode On/Off</td> <td></td> </tr> <tr> <td>D5</td> <td>Partial Mode On/Off</td> <td></td> </tr> <tr> <td>D4</td> <td>Sleep In/Out</td> <td></td> </tr> <tr> <td>D3</td> <td>Display Normal Mode On/Off</td> <td></td> </tr> <tr> <td>D2</td> <td>Display On/Off</td> <td></td> </tr> <tr> <td>D1</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> </tbody> </table> Bit D7 – Booster Voltage Status '0' = Booster Off or has a fault. '1' = Booster On and working OK (Meets Nokia's optical requirements). Bit D6 - Idle Mode On/Off '0' = Idle Mode Off. '1' = Idle Mode On. Bit D5 – Partial Mode On/Off '0' = Partial Mode Off. '1' = Partial Mode On. Bit D4 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode. Bit D3 – Display Normal Mode On/Off '0' = Display Normal Mode Off. '1' = Display Normal Mode On. Bit D2 – Display On/Off '0' = Display is Off. '1' = Display is On. Bit D1 – Not Defined 'This bit is not applicable for this project, so it is set to '0' Bit D0 – Not Defined 'This bit is not applicable for this project, so it is set to '0' X = Don't care														Bit	Description	Comment	D7	Not Defined	Set to '0'	D6	Idle Mode On/Off		D5	Partial Mode On/Off		D4	Sleep In/Out		D3	Display Normal Mode On/Off		D2	Display On/Off		D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
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Status	Default Value													
Power On Sequence	08 _{HEX}													
SW Reset	08 _{HEX}													
HW Reset	08 _{HEX}													
<pre> graph TD A[Read RDDPM] --> B{Dummy Read} B --> C[Send 2nd Parameter] style A fill:#fff,stroke:#000 style B fill:#fff,stroke:#000 style C fill:#fff,stroke:#000 style B fill:#fff,stroke:#000 style C fill:#fff,stroke:#000 </pre>														
<table border="1"> <tr> <td>Legend</td> </tr> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>		Legend	Command	Parameter	Display	Action	Mode	Sequential transfer						
Legend														
Command														
Parameter														
Display														
Action														
Mode														
Sequential transfer														

8.2.4. Get_address_mode (0Bh)

0BH	Get_address_mode																																									
	D/CX	RDX	WRX	D17-0	D7	D6	D5	D4	D3	D2	D1	D0	HEX																													
Command	0	1	↑	x	0	0	0	0	1	0	1	1	0B																													
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																													
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D1	Reserved	Set to '0'																																								
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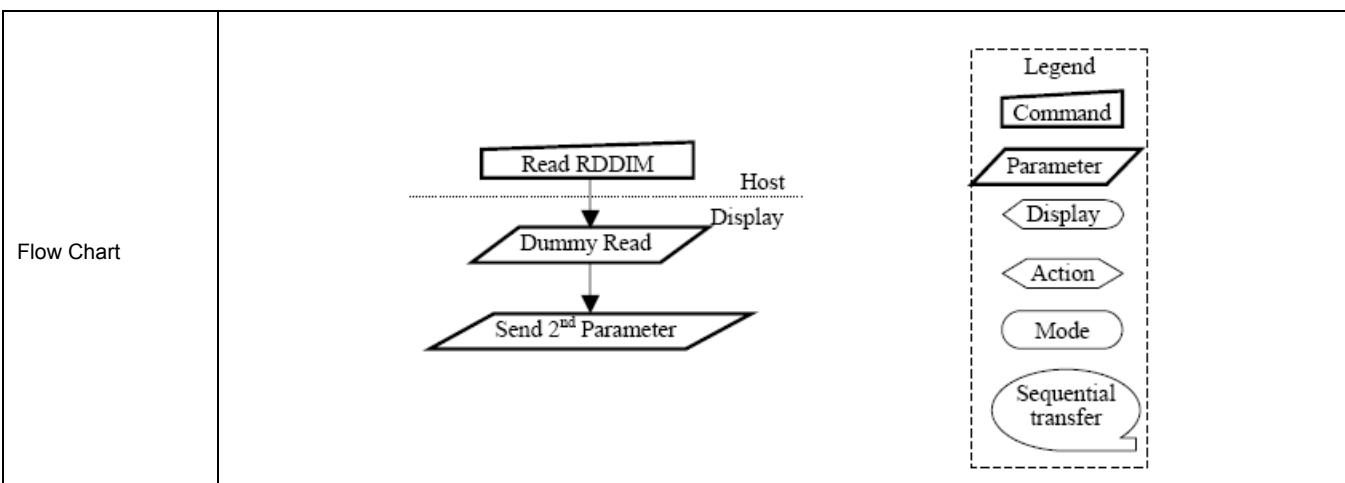


8.2.5. Get_pixel_format (0Ch)

0CH	Get_pixel_format																																																																																																																																	
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																					
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0C																																																																																																																					
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																																																																																																																					
2 nd Parameter	1	↑	1	x	0	D6	D5	D4	0	D2	D1	D0	xx																																																																																																																					
	This command indicates the current status of the display as described in the table below:																																																																																																																																	
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Sleep In	Yes																																																																																																																																	
Flow Chart	<p>The flowchart illustrates the communication sequence between the Host and the Display. The Host initiates the process by sending the command "Read RDDCOLMOD". The Display responds with a "Dummy Read" and then sends the "Send 2nd Parameter" back to the Host.</p> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																																																																																																	

8.2.6. Get_display_mode (0Dh)

0DH		Get_display_mode																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	x	0	0	0	0	1	1	0	1	0D																											
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																											
2 nd Parameter	1	↑	1	x	0	0	0	0	0	0	0	0	xx																											
Description	The display module returns the Display Image Mode status. <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Symbol</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Vertical Scrolling Status</td><td>VSSON</td></tr> <tr> <td>D6</td><td>Reserved</td><td></td></tr> <tr> <td>D5</td><td>Inversion On/Off</td><td>DSPINVON</td></tr> <tr> <td>D4</td><td>Reserved</td><td></td></tr> <tr> <td>D3</td><td>Reserved</td><td></td></tr> <tr> <td>D2</td><td>Gamma Curve Selection</td><td></td></tr> <tr> <td>D1</td><td>Gamma Curve Selection</td><td></td></tr> <tr> <td>D0</td><td>Gamma Curve Selection</td><td></td></tr> </tbody> </table> This command indicates the current status of the display as described in the table below: <ul style="list-style-type: none"> ♦ Bit D7 – Vertical Scrolling On/Off '0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On. ♦ Bit D6 – Reserved ♦ Bit D5 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On. ♦ Bit D4 – Reserved ♦ Bit D3 – Reserved ♦ Bits D2, D1, D0 – Gamma Curve Selection These bits are not applicable for this project, so they are set to '000' 													Bit	Description	Symbol	D7	Vertical Scrolling Status	VSSON	D6	Reserved		D5	Inversion On/Off	DSPINVON	D4	Reserved		D3	Reserved		D2	Gamma Curve Selection		D1	Gamma Curve Selection		D0	Gamma Curve Selection	
Bit	Description	Symbol																																						
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Status	Availability																																							
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Normal Mode On, Idle Mode On, Sleep Out	Yes																																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																																							
Sleep In	Yes																																							



8.2.7. Get_signal_mode (0Eh)

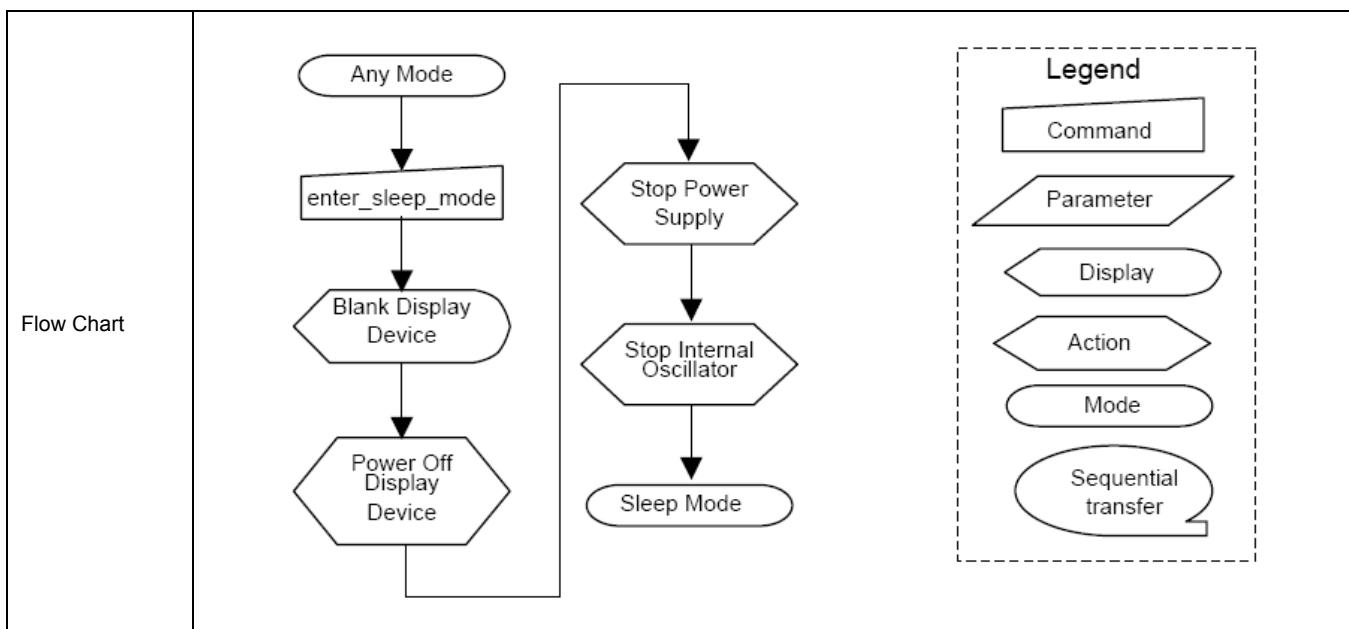
0EH	RDDSM (Read Display Signal Mode)																																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	x	0	0	0	0	1	1	1	0	0E																											
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																											
2 nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	xx																											
Description	The display module returns the Display Signal Mode.																																							
	<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Symbol</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Tearing Effect Line On/Off</td><td>TEON</td></tr> <tr> <td>D6</td><td>Tearing Effect Line Output Mode</td><td>TEOM</td></tr> <tr> <td>D5</td><td>Reserved</td><td></td></tr> <tr> <td>D4</td><td>Reserved</td><td></td></tr> <tr> <td>D3</td><td>Reserved</td><td></td></tr> <tr> <td>D2</td><td>Reserved</td><td></td></tr> <tr> <td>D1</td><td>Reserved</td><td></td></tr> <tr> <td>D0</td><td>Reserved</td><td></td></tr> </tbody> </table>													Bit	Description	Symbol	D7	Tearing Effect Line On/Off	TEON	D6	Tearing Effect Line Output Mode	TEOM	D5	Reserved		D4	Reserved		D3	Reserved		D2	Reserved		D1	Reserved		D0	Reserved	
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D2	Reserved																																							
D1	Reserved																																							
D0	Reserved																																							
	<p>This command indicates the current status of the display as described in the table below:</p> <ul style="list-style-type: none"> Bit D7 – Tearing Effect Line On/Off <ul style="list-style-type: none"> '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 8.3 for mode definitions. <ul style="list-style-type: none"> '0' = Mode 1. '1' = Mode 2. Bit D[5:0] – Reserved 																																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes															
Status	Availability																																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																							
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																																							
Sleep In	Yes																																							
Flow Chart	<p>The flowchart illustrates the communication sequence between the Host and the Display. It starts with a 'Read RDDIM' command from the Host to the Display. This is followed by a 'Dummy Read' response from the Display back to the Host. Finally, the Host sends a 'Send 2nd Parameter' command to the Display. A legend on the right side defines the symbols: Command (rectangle), Parameter (diamond), Display (left-pointing triangle), Action (right-pointing triangle), Mode (oval), and Sequential transfer (elliptical arrow).</p>																																							

8.2.8. Get_diagnostic_result (0Fh)

0FH		Get_diagnostic_result																																																																																																																																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0F																																																																																																																																
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																																																																																																																																
2 nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	xx																																																																																																																																
Description	The display module returns the self-diagnostic results following a Sleep Out command.																																																																																																																																												
	<table border="1"> <thead> <tr> <th>Bit</th><th colspan="8">Description</th><th colspan="5">Symbol</th></tr> </thead> <tbody> <tr> <td>D7</td><td colspan="8">Register Loading Detection</td><td colspan="5">SDR</td></tr> <tr> <td>D6</td><td colspan="8">Functionality Detection</td><td colspan="5">FUNCD</td></tr> <tr> <td>D5</td><td colspan="8">Chip attachment Detection</td><td colspan="5">Set '0'</td></tr> <tr> <td>D4</td><td colspan="8">Display Glass Break Detection</td><td colspan="5">Set '0'</td></tr> <tr> <td>D3</td><td colspan="8">Reserved</td><td colspan="5">Set '0'</td></tr> <tr> <td>D2</td><td colspan="8">Reserved</td><td colspan="5">Set '0'</td></tr> <tr> <td>D1</td><td colspan="8">Reserved</td><td colspan="5">Set '0'</td></tr> <tr> <td>D0</td><td colspan="8">Reserved</td><td colspan="5" rowspan="2">Set '0'</td></tr> </tbody> </table>															Bit	Description								Symbol					D7	Register Loading Detection								SDR					D6	Functionality Detection								FUNCD					D5	Chip attachment Detection								Set '0'					D4	Display Glass Break Detection								Set '0'					D3	Reserved								Set '0'					D2	Reserved								Set '0'					D1	Reserved								Set '0'					D0	Reserved								Set '0'				
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Flow Chart	<p>The flowchart illustrates the communication sequence between the Host and the Display. It starts with the Host sending a "Read RDDIM" command to the Display. This triggers a "Dummy Read" response from the Display back to the Host. Finally, the Host sends the "Send 2nd Parameter" command to the Display.</p> <p>Legend:</p> <ul style="list-style-type: none"> Command (Solid rectangle) Parameter (Dashed rectangle) Display (Trapezoid) Action (Solid triangle pointing right) Mode (Solid circle) Sequential transfer (Oval) 																																																																																																																																												

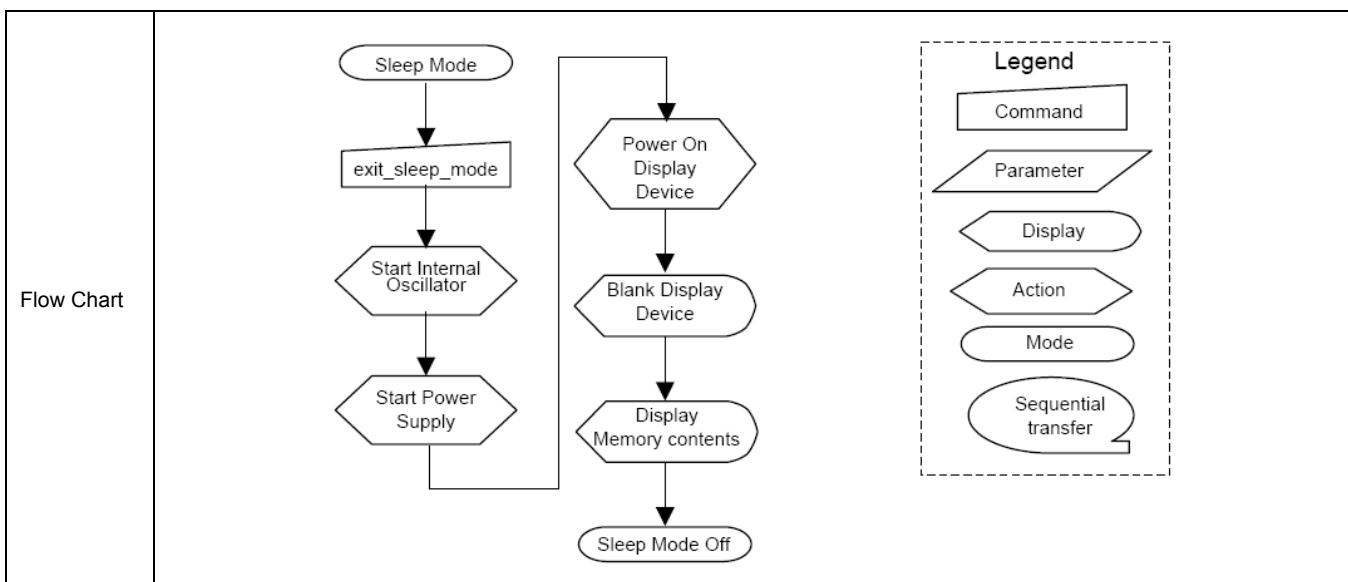
8.2.9. Enter_sleep_mode (10h)

Enter_sleep_mode																									
10H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10												
Parameter	No Parameter																								
Description	<p>This command causes the display module to enter the Sleep mode.</p> <p>This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop.</p> <p>DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to Type 2 and Type 3 display modules for two frames after this command is sent when the display module is in Normal mode.</p>																								
Restriction	<p>This command has no effect when the display module is already in Sleep mode.</p> <p>The host processor must wait five milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.</p> <p>The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>SW Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>HW Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
SW Reset	Sleep In Mode																								
HW Reset	Sleep In Mode																								



8.2.10. Exit_sleep_mode (11h)

11H	Exit_sleep_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11												
Parameter	No Parameter																								
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to Type 2 and Type 3 display modules two frames before this command is sent when the display module is in Normal Mode.																								
Restriction	<p>This command shall not cause any visible effect on the display device when the display module is not in Sleep mode.</p> <p>The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize.</p> <p>The host processor must wait 120 milliseconds after sending an <code>exit_sleep_mode</code> command before sending an <code>enter_sleep_mode</code> command.</p> <p>The display module loads the display module's default values to the registers when exiting the Sleep mode.</p> <p>There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode.</p> <p>The display module runs the self-diagnostic functions after this command is received. See section 5.3 for a description of the self-diagnostic functions.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Sleep In Mode</td></tr> <tr> <td>SW Reset</td><td>Sleep In Mode</td></tr> <tr> <td>HW Reset</td><td>Sleep In Mode</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
SW Reset	Sleep In Mode																								
HW Reset	Sleep In Mode																								



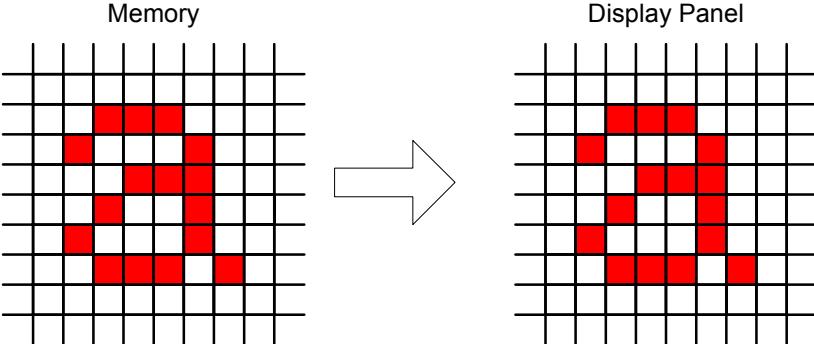
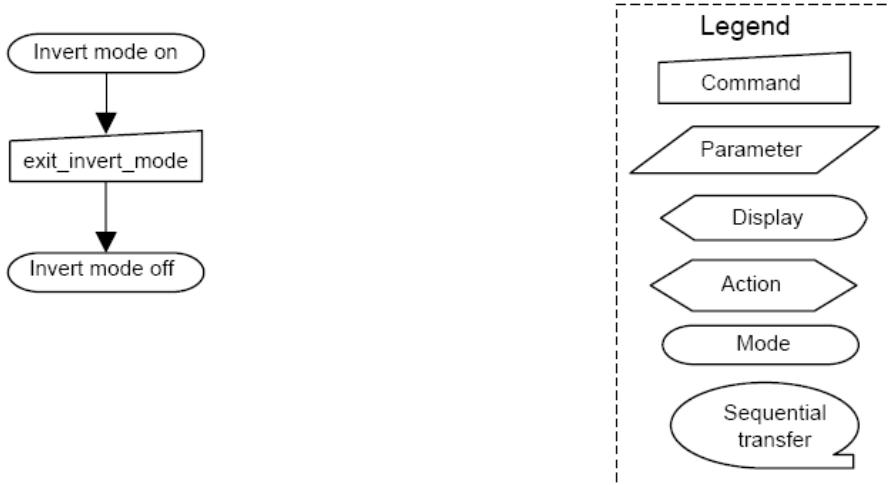
8.2.11. Enter_Partial_mode (12h)

Enter_Partial_mode																										
12H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12													
Parameter	No Parameter																									
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area (30h) command. To leave Partial Display Mode, the enter_normal_mode (13h) command should be written. The host processor continues to send PCLK, HS and VS information to Type 2 display modules for two frames after this command is sent when the display module is in Normal Display Mode.																									
Restriction	This command has no effect when Partial Display Mode is already active.																									
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode On</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display Mode On</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display Mode On</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On				
Status	Default Value																									
Power On Sequence	Normal Display Mode On																									
SW Reset	Normal Display Mode On																									
HW Reset	Normal Display Mode On																									
Flow Chart	Refer to Partial Area (30h)																									

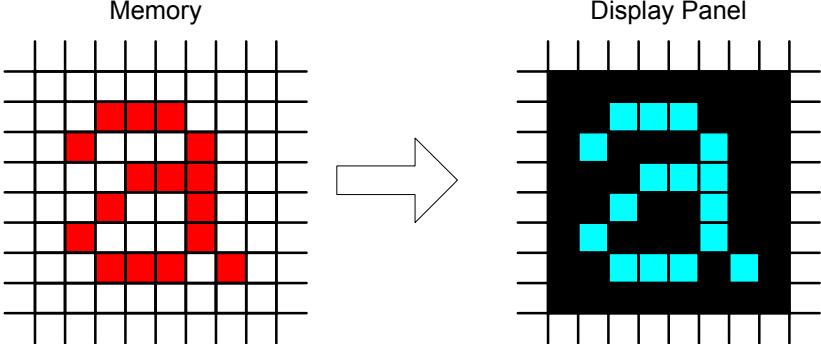
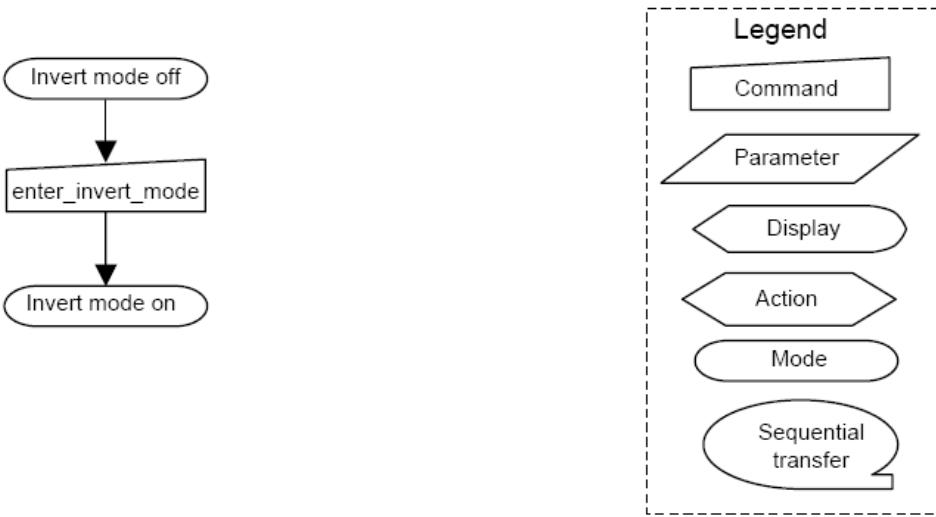
8.2.12. Enter_normal_mode (13h)

13H		Enter_normal_mode																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	1	1	13												
Parameter	No Parameter																								
Description	This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode and Scroll mode are off. The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.																								
Restriction	This command has no effect when Normal Display mode is already active.																								
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode On</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display Mode On</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display Mode On</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On				
Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	Refer to the description of set_partial_area(30h) and set_scroll_area(33h)																								

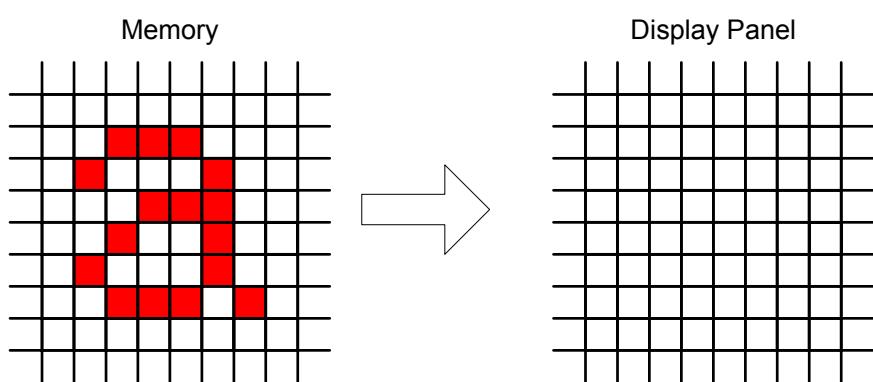
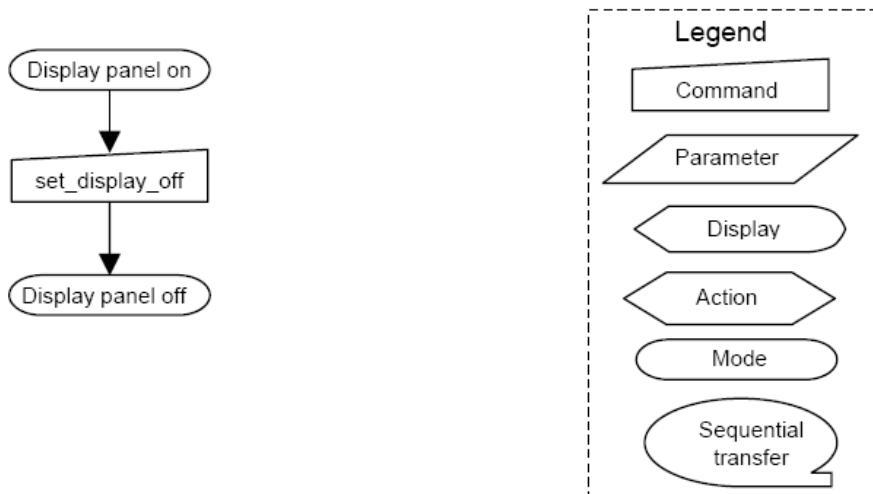
8.2.13. Exit_invert_mode (20h)

20H		Exit_invert_mode																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	0	0	0	0	20												
Parameter	No Parameter																								
Description	This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 																								
Restriction	This command has no effect when the display module is not inverting the display image.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Exit_invert_mode</td> </tr> <tr> <td>SW Reset</td> <td>Exit_invert_mode</td> </tr> <tr> <td>HW Reset</td> <td>Exit_invert_mode</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Exit_invert_mode	SW Reset	Exit_invert_mode	HW Reset	Exit_invert_mode				
Status	Default Value																								
Power On Sequence	Exit_invert_mode																								
SW Reset	Exit_invert_mode																								
HW Reset	Exit_invert_mode																								
Flow Chart	 <pre> graph TD A([Invert mode on]) --> B[exit_invert_mode] B --> C([Invert mode off]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.14. Enter_invert_mode (21h)

21H		Enter_invert_mode																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	0	0	0	1	21												
Parameter	No Parameter																								
Description	This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed. 																								
Restriction	This command has no effect when module is already in inversion on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Exit_invert_mode</td> </tr> <tr> <td>SW Reset</td> <td>Exit_invert_mode</td> </tr> <tr> <td>HW Reset</td> <td>Exit_invert_mode</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Exit_invert_mode	SW Reset	Exit_invert_mode	HW Reset	Exit_invert_mode				
Status	Default Value																								
Power On Sequence	Exit_invert_mode																								
SW Reset	Exit_invert_mode																								
HW Reset	Exit_invert_mode																								
Flow Chart	 <pre> graph TD A([Invert mode off]) --> B[enter_invert_mode] B --> C([Invert mode on]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.15. Set_display_off (28h)

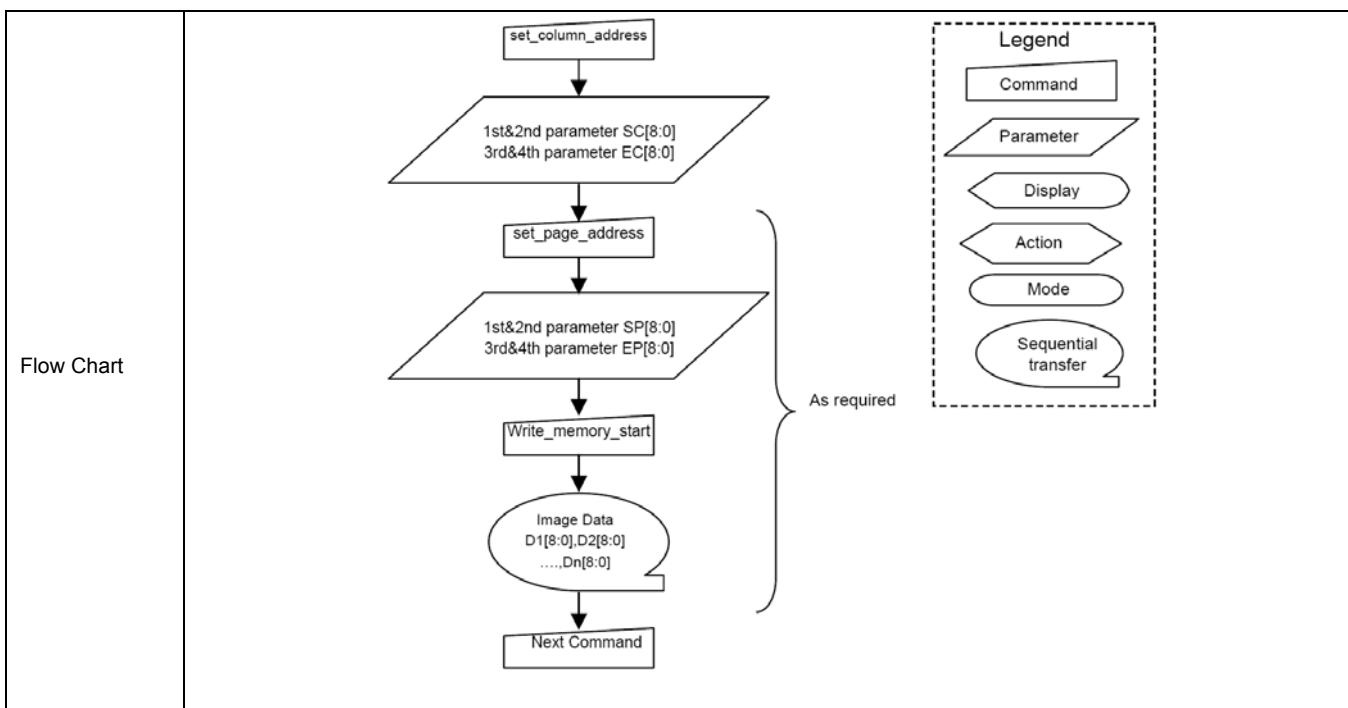
28H		Set_display_off																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28												
Parameter	No Parameter																								
Description	This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
SW Reset	Display Off																								
HW Reset	Display Off																								
Flow Chart	 <pre> graph TD A([Display panel on]) --> B[set_display_off] B --> C([Display panel off]) </pre>																								

8.2.16. Set_display_on (29h)

29H		Set_display_on																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	0	1	29												
Parameter	No Parameter																								
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 																								
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
SW Reset	Display Off																								
HW Reset	Display Off																								
Flow Chart	<pre> graph TD A([Display panel off]) --> B[set_display_on] B --> C([Display panel on]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

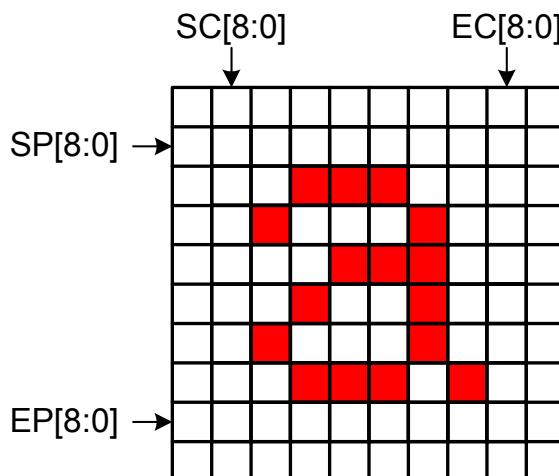
8.2.17. Set_column_address (2Ah)

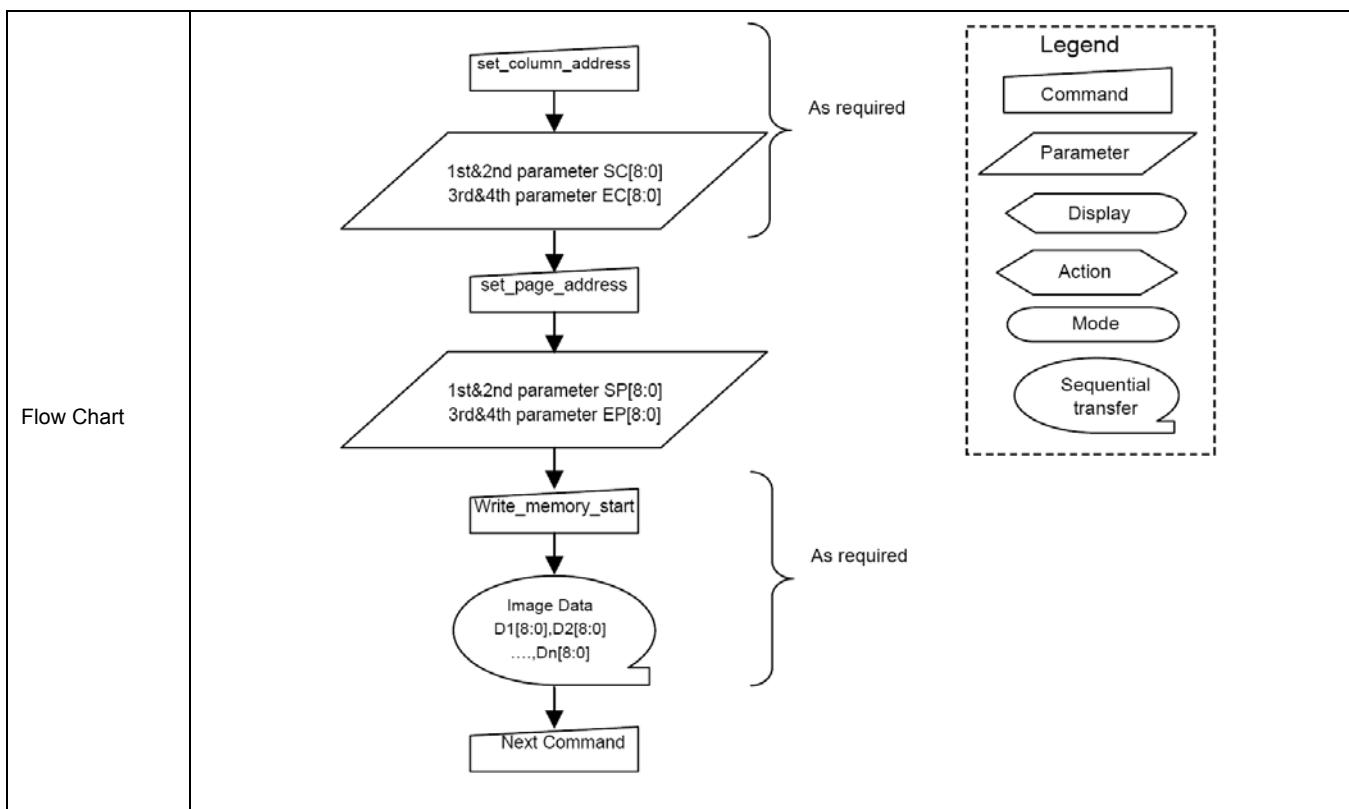
Set_column_address																									
2AH	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2A												
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SC8	Note 1												
2 nd Parameter	1	1	↑	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0													
3 rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	EC8	Note 2												
4 th Parameter	1	1	↑	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0													
Description	This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands. No status bits are changed.																								
Restriction	SC [8:0] always must be equal to or less than EC[8:0]. If SC[8:0] or EC[8:0] is greater than the available frame memory then the parameter is not updated.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>SC[15:0]=0000_{HEX}</td><td>SC[8:0]=000_{HEX} SE[8:0]=013F_{HEX}</td></tr> <tr> <td>SW Reset</td><td>SC[15:0]=0000_{HEX}</td><td>If Set_address_mode(36h) B5=0 : EC[8:0]=013F_{HEX} If Set_address_mode(36h) B5=1 : EC[8:0]=01DF_{HEX}</td></tr> <tr> <td>HW Reset</td><td>SC[15:0]=0000_{HEX}</td><td>SC[8:0]=000_{HEX} SE[8:0]=013F_{HEX}</td></tr> </tbody> </table>													Status	Default Value		Power On Sequence	SC[15:0]=0000 _{HEX}	SC[8:0]=000 _{HEX} SE[8:0]=013F _{HEX}	SW Reset	SC[15:0]=0000 _{HEX}	If Set_address_mode(36h) B5=0 : EC[8:0]=013F _{HEX} If Set_address_mode(36h) B5=1 : EC[8:0]=01DF _{HEX}	HW Reset	SC[15:0]=0000 _{HEX}	SC[8:0]=000 _{HEX} SE[8:0]=013F _{HEX}
Status	Default Value																								
Power On Sequence	SC[15:0]=0000 _{HEX}	SC[8:0]=000 _{HEX} SE[8:0]=013F _{HEX}																							
SW Reset	SC[15:0]=0000 _{HEX}	If Set_address_mode(36h) B5=0 : EC[8:0]=013F _{HEX} If Set_address_mode(36h) B5=1 : EC[8:0]=01DF _{HEX}																							
HW Reset	SC[15:0]=0000 _{HEX}	SC[8:0]=000 _{HEX} SE[8:0]=013F _{HEX}																							



8.2.18. Set_page_address (2Bh)

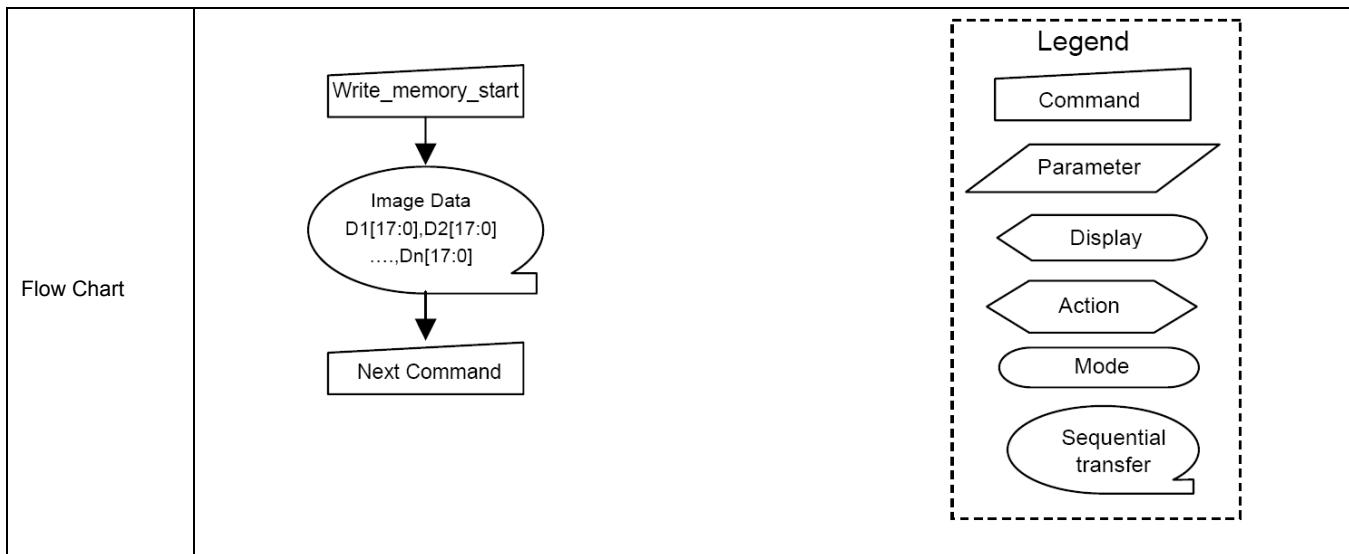
Set_page_address																														
2BH	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2B																	
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SP8	xxx																	
2 nd Parameter	1	1	↑	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0																		
3 rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	EP8	xxx																	
4 th Parameter	1	1	↑	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0																		
Description	This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. No status bits are changed.																													
Restriction	SP [8:0] always must be equal to or less than EP [8:0]. If SP[8:0] or EP[8:0] is greater than the available frame memory then the parameter is not updated.																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes					
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Normal Mode On, Idle Mode Off, Sleep Out	Yes																													
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Status	Default Value																													
Power On Sequence	SP[15:0]=0000 _{HEX}	EP[15:0]=01DF _{HEX}																												
SW Reset	SP[15:0]=0000 _{HEX}	If Set_address_mode(36h) B5=0 : EP[8:0]=01DF _{HEX} If Set_address_mode(36h) B5=1 : EP[8:0]=013F _{HEX}																												
HW Reset	SP[15:0]=0000 _{HEX}	EP[15:0]=01DF _{HEX}																												





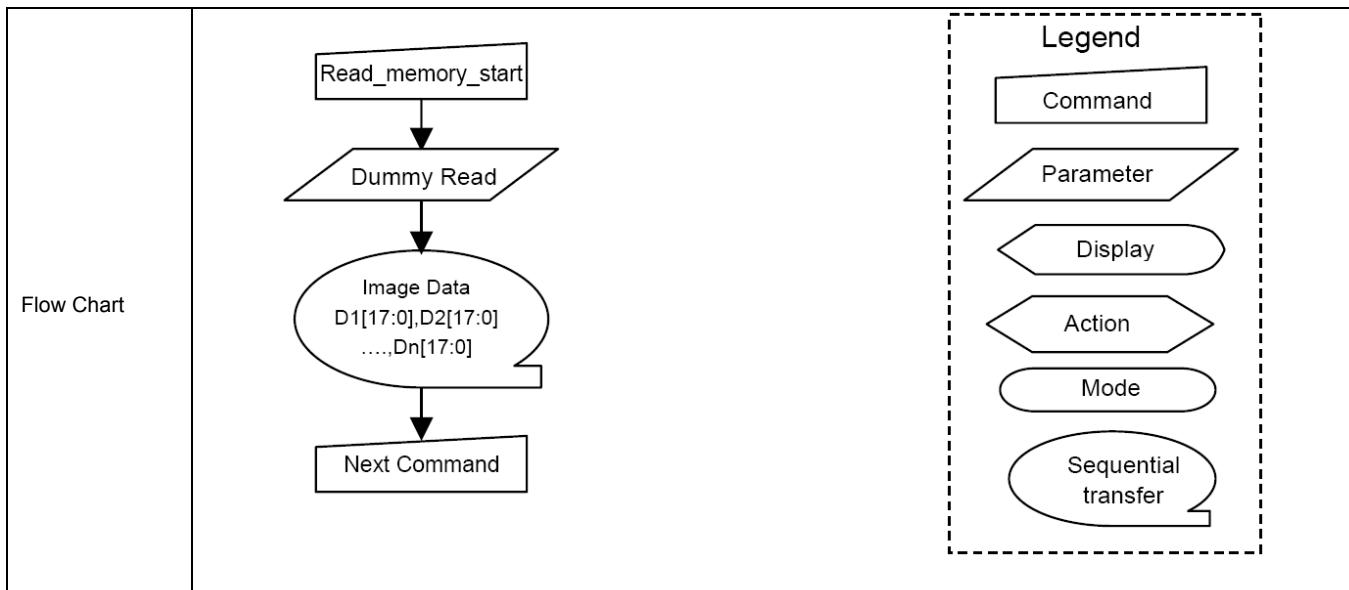
8.2.19. Write_memory_start (2Ch)

Write_memory_start																									
2CH	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	xx	0	0	1	0	1	1	0	0	2C												
1 st pixel data	1	1	↑	D1 [17..8]	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	00000..3FFF												
:	1	1	↑	Dx [17..8]	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	00000..3FFF												
N TH pixel data	1	1	↑	Dn [17..8]	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	00000..3FFF												
Description	This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address (2Ah) and set_page_address (2Bh) commands. <u>If set_address_mode (36h) B5 = 0:</u> The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. <u>If set_address_mode (36h) B5 = 1:</u> The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.																								
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write location. Otherwise, data written with write_memory_start and any following write_memory_continue commands is written to undefined locations..																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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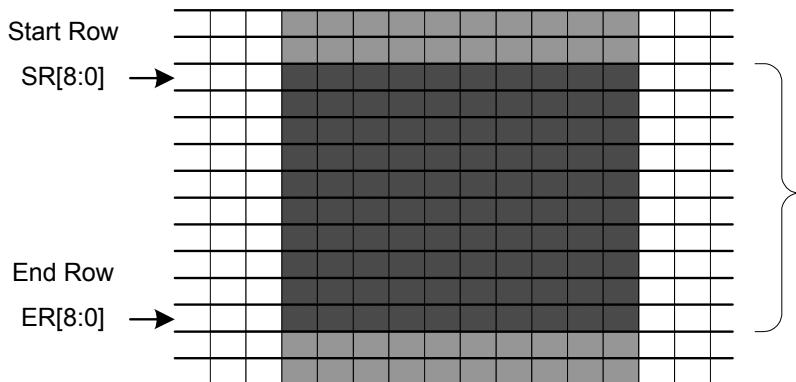
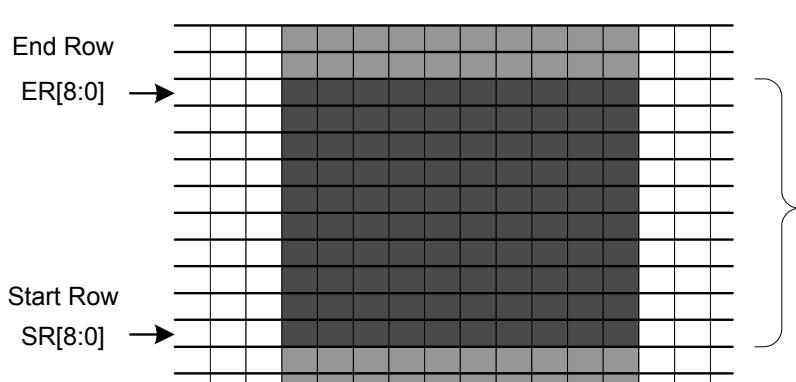


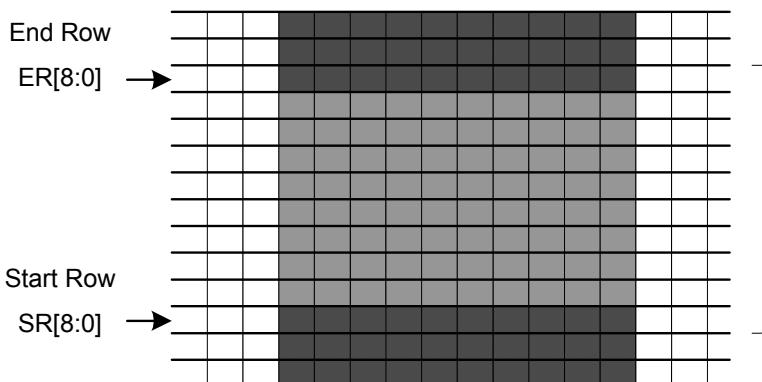
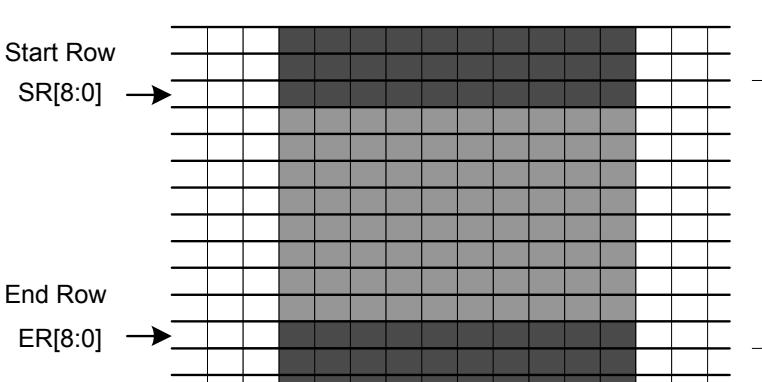
8.2.20. Read_memory_start (2Eh)

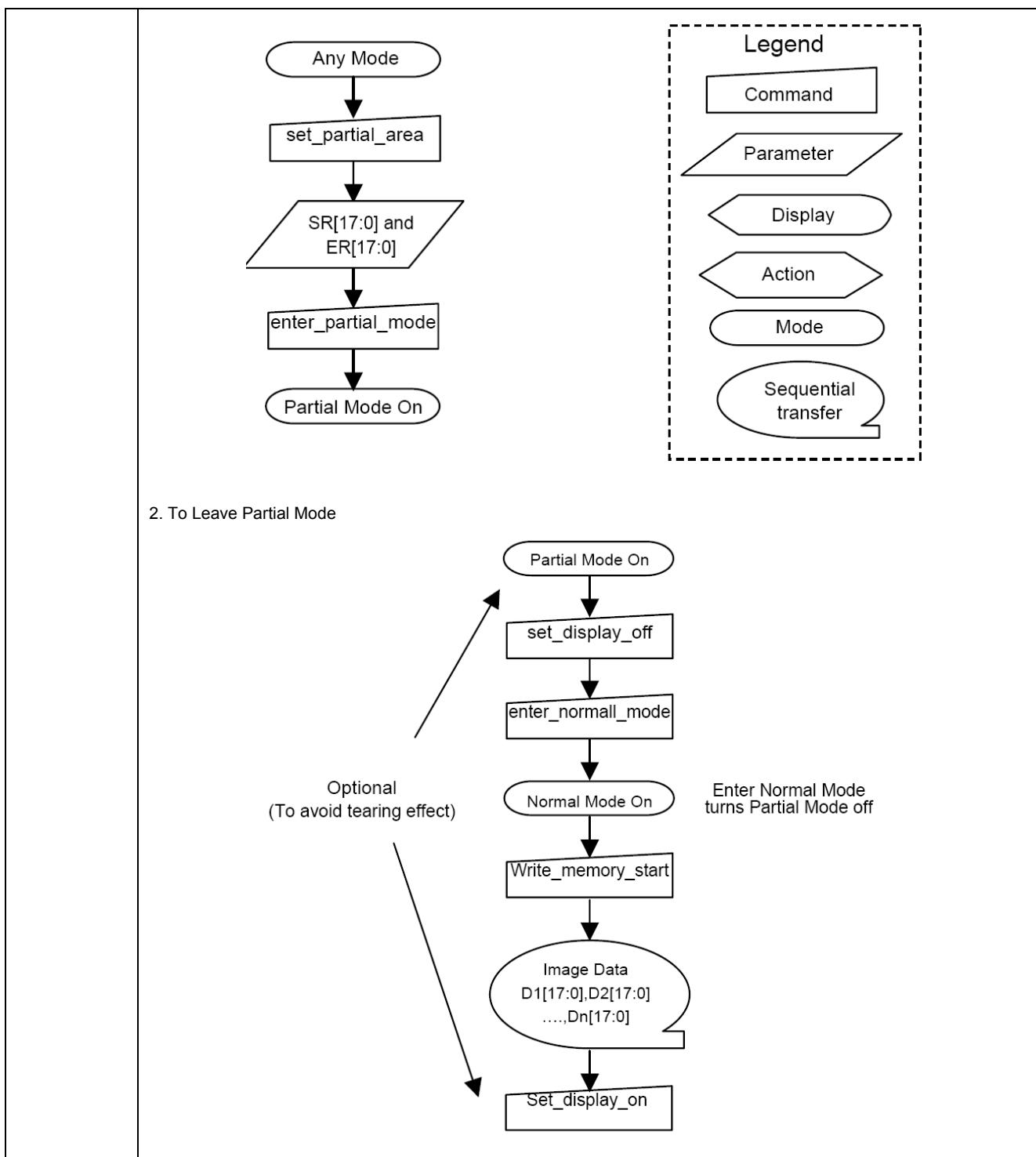
2EH		RAMRD (Memory Read)																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	x	0	0	1	0	1	1	1	0	2E											
1 st Parameter		1	↑	1	x	x	x	x	x	x	x	x	x	x											
2 nd Parameter		1	↑	1	D1 [17..8]	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	00000..3FF											
:		1	↑	1	Dx [17..8]	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	00000..3FF											
(N+1) TH Parameter		1	↑	1	Dn [17..8]	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	00000..3FF											
Description	This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands. <u>If set_address_mode B5 = 0:</u> The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. <u>If set_address_mode B5 = 1:</u> The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.																								
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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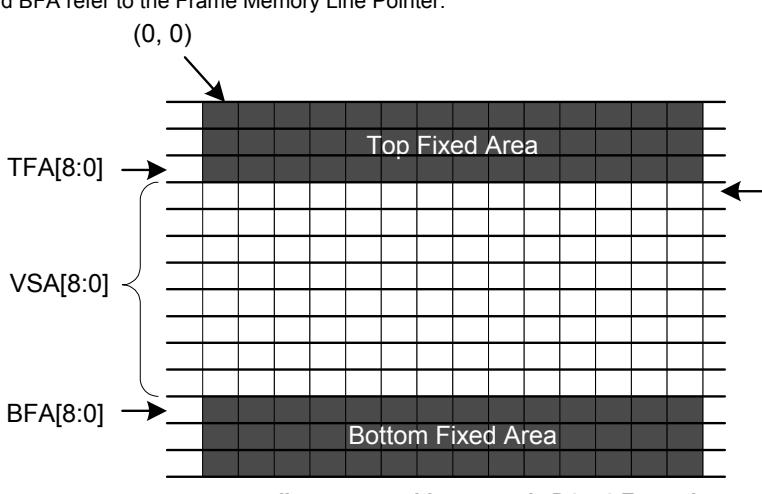
8.2.21. Set_partial_area (30h)

30H	Set_partial_area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SR8	000..1DFh
2 nd Parameter	1	1	↑	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
3 rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	ER8	000..1DFh
4 th Parameter	1	1	↑	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	
Description	This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory <p>If End Row > Start Row and set_address_mode B4 = 0:</p>  <p>If End Row > Start Row and set_address_mode B4 = 1:</p> 												

	<p>End Row < Start Row (set_address_mode(36h) B4=0)</p> 												
	<p>End Row < Start Row (set_address_mode(36h) B4=1)</p> 												
	<p>If End Row = Start Row then the Partial Area will be one row deep.</p>												
Restriction	SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number (01DFh).												
Register Availability	<table border="1" data-bbox="579 1459 1166 1662"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" data-bbox="468 1706 1277 1841"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>SR[15:0]=0000_{HEX}</td><td>ER[15:0]=01DF_{HEX}</td></tr> <tr> <td>SW Reset</td><td>SR[15:0]=0000_{HEX}</td><td>ER[15:0]=01DF_{HEX}</td></tr> <tr> <td>HW Reset</td><td>SR[15:0]=0000_{HEX}</td><td>ER[15:0]=01DF_{HEX}</td></tr> </tbody> </table>	Status	Default Value		Power On Sequence	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}	SW Reset	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}	HW Reset	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}
Status	Default Value												
Power On Sequence	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}											
SW Reset	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}											
HW Reset	SR[15:0]=0000 _{HEX}	ER[15:0]=01DF _{HEX}											
Flow Chart	1. To Enter Partial Mode												



8.2.22. Set_scroll_area (33h)

33H		Set_scroll_area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	1	1	0	0	1	1	33	
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	TFA [8]	0000 ... 01E0	
2 nd Parameter	1	1	↑	x	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA [3]	TFA [2]	TFA [1]	TFA [0]		
3 rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	VSA [8]	0000 ... 01E0	
4 th Parameter	1	1	↑	x	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]		
5 th Parameter	1	1	↑	x	0	0	0	0	0	0	0	BFA [8]	0000 ... 01E0	
6 th Parameter	1	1	↑	x	BFA [7]	BFA [6]	BFA [5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]		
Description	This command defines the display vertical scrolling area. set_address_mode (36h) B4 = 0: The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area. The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned. TFA, VSA and BFA refer to the Frame Memory Line Pointer.													
	 <p style="text-align: center;">set_scroll_area set_address_mode B4 = 1 Example</p>													
	set_address_mode (36h) B4 = 1: The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area. The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. TFA, VSA and BFA refer to the Frame Memory Line Pointer.													

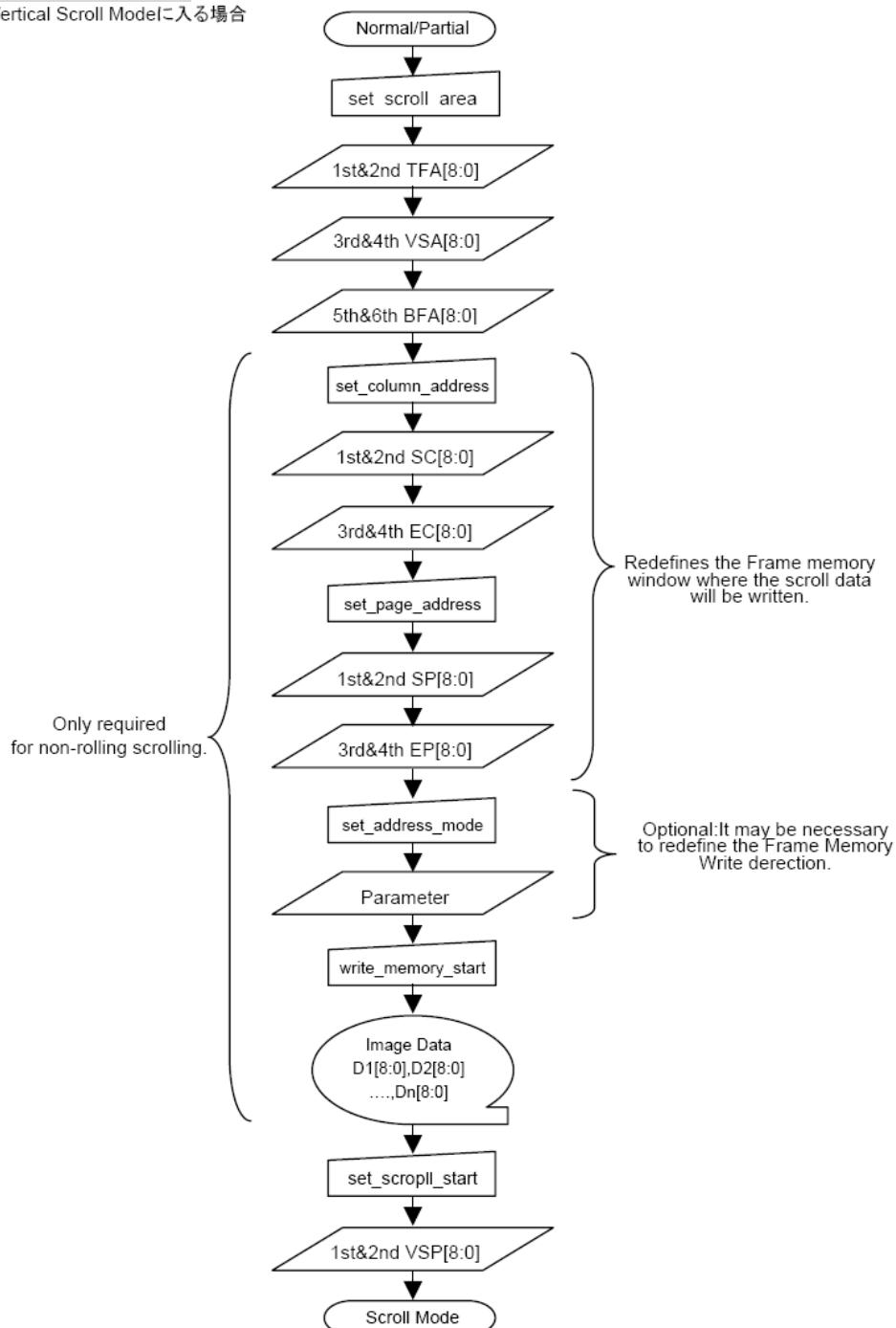
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	<p>set_scroll_area set_address_mode B4 = 1 Example</p>																
Restriction	The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to '0' – this only affects the Frame Memory Write.																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
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Sleep In	Yes																
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Status	Default Value																
Power On Sequence	TFA[15:0]=0000 _{HEX}	VSA[15:0]=01E0 _{HEX}	BFA[15:0]=0000 _{HEX}														
SW Reset	TFA [15:0]=0000 _{HEX}	VSA[15:0]=01E0 _{HEX}	BFA[15:0]=0000 _{HEX}														
HW Reset	TFA [15:0]=0000 _{HEX}	VSA[15:0]=01E0 _{HEX}	BFA[15:0]=0000 _{HEX}														
Flow Chart																	

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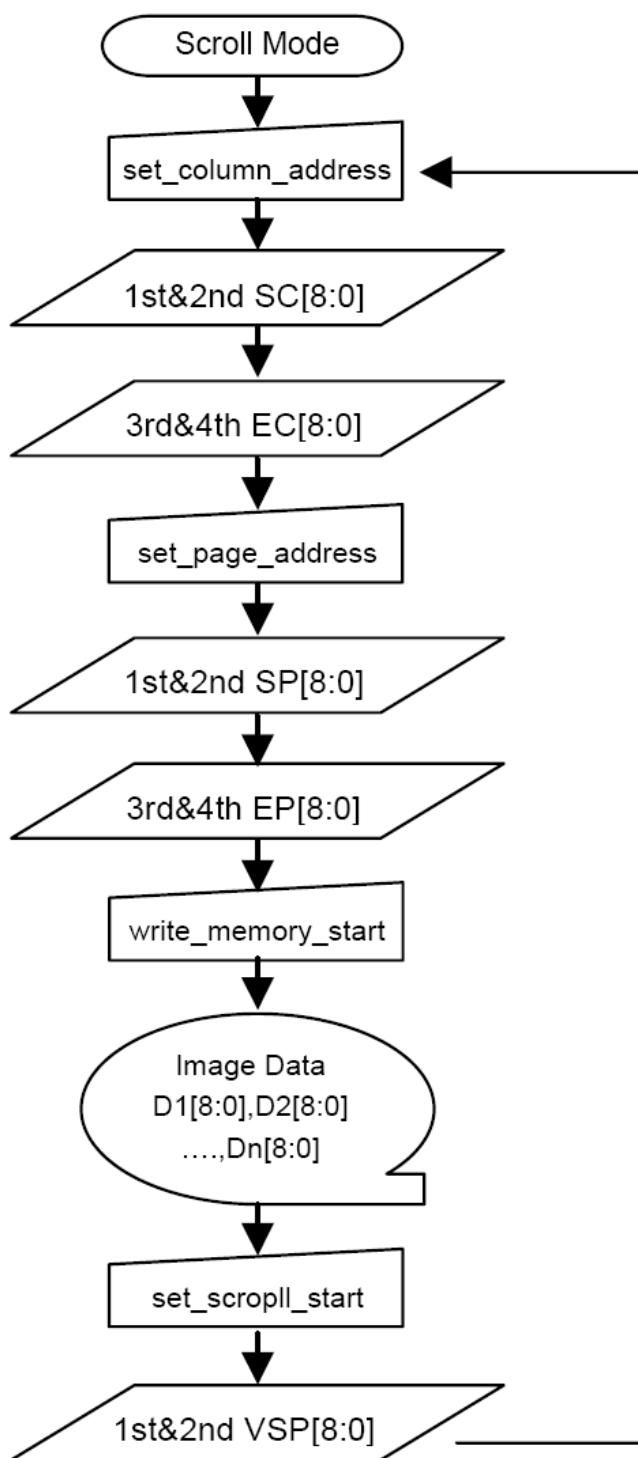
1. To enter Vertical Scroll Mode:

/vertical Scroll Modelに入る場合

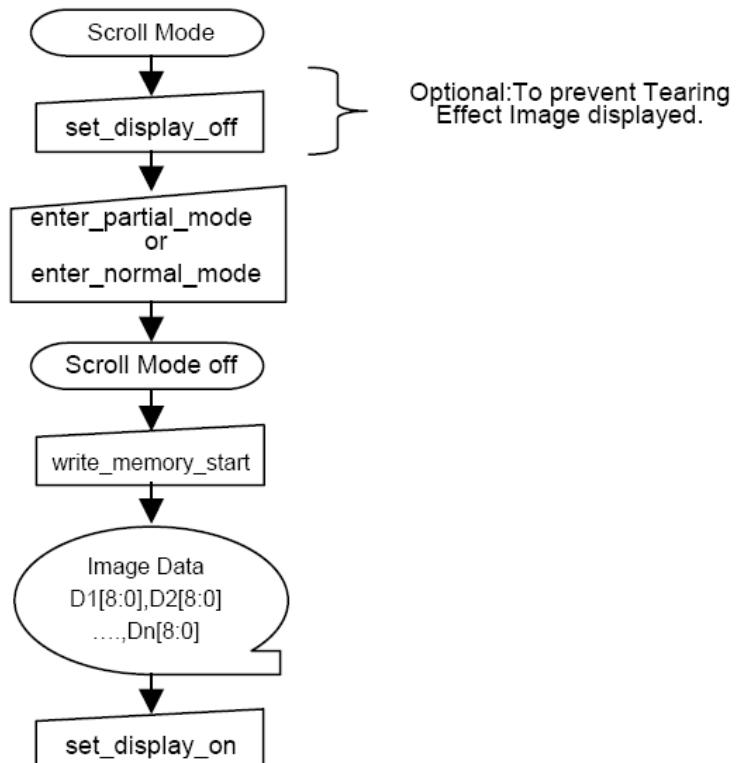


Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise an undesirable image may be shown on the Display Panel.

2. Continuous Scroll:



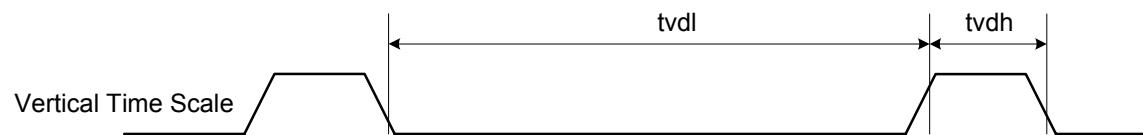
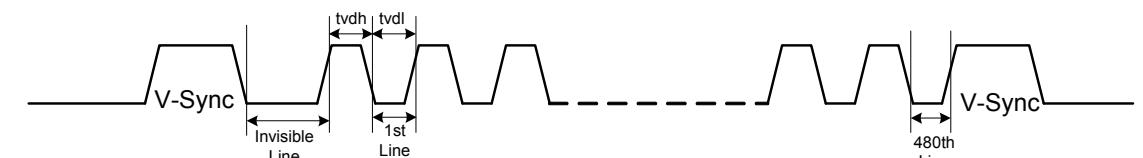
3. To Leave Vertical Scroll Mode:

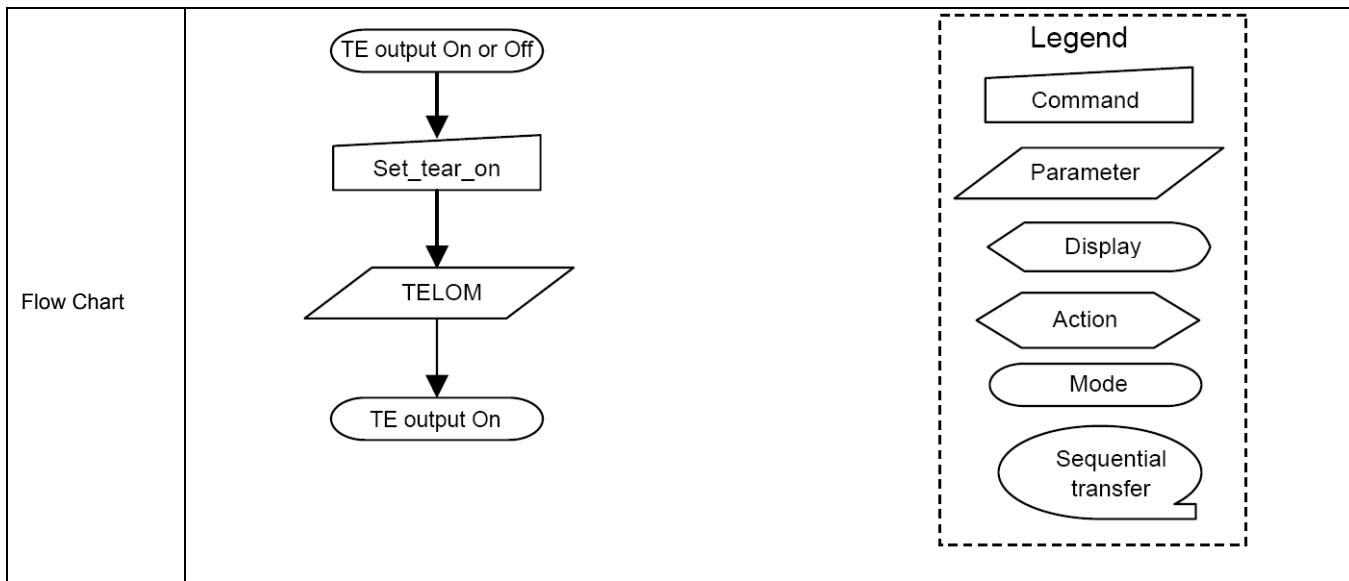


8.2.23. Set_tear_off (34h)

34H		Set_tear_off																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34												
Parameter	NO PARAMETER																								
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.																								
Restriction	This command has no effect when the Tearing Effect output is already off.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>SW Reset</td> <td>OFF</td> </tr> <tr> <td>HW Reset</td> <td>OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF				
Status	Default Value																								
Power On Sequence	OFF																								
SW Reset	OFF																								
HW Reset	OFF																								
Flow Chart	<pre> graph TD A([TE output On or Off]) --> B[Set_tear_off] B --> C([TE output off]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.24. Set_tear_on (35h)

Set_tear_on																									
35H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35												
1 st Parameter	1	1	↑	x	x	x	x	x	x	x	x	TELOM	xx												
Description	This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Address Order). The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. If TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only.  If TELOM = 1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.  <i>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</i>																								
Restriction	This command has no effect when Tearing Effect output is already ON.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>SW Reset</td> <td>OFF</td> </tr> <tr> <td>HW Reset</td> <td>OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF				
Status	Default Value																								
Power On Sequence	OFF																								
SW Reset	OFF																								
HW Reset	OFF																								



8.2.25. Set_address_mode (36h)

36H		Set_address_mode																																															
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	0	1	↑	x	0	0	1	1	0	1	1	0	36																																				
1 st Parameter	1	1	↑	x	B7	B6	B5	B4	B3	0	B1	B0	xx																																				
		This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.																																															
Description	<table border="1"> <thead> <tr> <th>Bit</th><th colspan="2">Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>B7</td><td colspan="2">Page Address Order</td><td></td></tr> <tr> <td>B6</td><td colspan="2">Column Address Order</td><td></td></tr> <tr> <td>B5</td><td colspan="2">Page/Column Selection</td><td></td></tr> <tr> <td>B4</td><td colspan="2">Vertical Order</td><td></td></tr> <tr> <td>B3</td><td colspan="2">RGB/BGR Order</td><td></td></tr> <tr> <td>B2</td><td colspan="2">Display data latch data order</td><td>Set to '0'</td></tr> <tr> <td>B1</td><td colspan="2">Horizontal Flip</td><td></td></tr> <tr> <td>B0</td><td colspan="2">Vertical Flip</td><td></td></tr> </tbody> </table> <ul style="list-style-type: none"> • Bit B7 – Page Address Order <ul style="list-style-type: none"> '0' = Top to Bottom '1' = Bottom to Top • Bit B6 – Column Address Order <ul style="list-style-type: none"> '0' = Left to Right '1' = Right to Left • Bit B5 – Page/Column Order <ul style="list-style-type: none"> '0' = Normal Mode '1' = Reverse Mode • Bit B4 – Line Address Order <ul style="list-style-type: none"> '0' = LCD Refresh Top to Bottom '1' = LCD Refresh Bottom to Top • Bit B3 – RGB/BGR Order <ul style="list-style-type: none"> '0' = Pixels sent in RGB order '1' = Pixels sent in BGR order • Bit B2 – Display Data Latch Data Order <ul style="list-style-type: none"> This bit is not applicable for this project, so it is set to '0'. (Not supported) • Bit B1 – Horizontal Flip <ul style="list-style-type: none"> '0' = Normal display '1' = Flipped display • Bit B0 – Vertical Flip <ul style="list-style-type: none"> '0' = Normal display '1' = Flipped display <p>X = Don't care</p>													Bit	Description		Comment	B7	Page Address Order			B6	Column Address Order			B5	Page/Column Selection			B4	Vertical Order			B3	RGB/BGR Order			B2	Display data latch data order		Set to '0'	B1	Horizontal Flip			B0	Vertical Flip		
Bit	Description		Comment																																														
B7	Page Address Order																																																
B6	Column Address Order																																																
B5	Page/Column Selection																																																
B4	Vertical Order																																																
B3	RGB/BGR Order																																																
B2	Display data latch data order		Set to '0'																																														
B1	Horizontal Flip																																																
B0	Vertical Flip																																																

	B5	B6	B7	Image in Frame Memory	B5	B6	B7	Image in Frame Memory				
	0	0	0		1	0	0					
	0	0	1		1	0	1					
	0	1	0		1	1	0					
	0	1	1		1	1	1					
	B3 = 0											
	Memory				Display Panel							
	Sent RGB											
	B3 = 1											
	Memory				Display Panel							
	Sent BGR											
Restriction												

Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability										
Normal Mode On, Idle Mode Off, Sleep Out	Yes										
Normal Mode On, Idle Mode On, Sleep Out	Yes										
Partial Mode On, Idle Mode Off, Sleep Out	Yes										
Partial Mode On, Idle Mode On, Sleep Out	Yes										
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000 0000_{HEX}</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>HW Reset</td><td>0000 0000_{HEX}</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	0000 0000 _{HEX}	SW Reset	No Change	HW Reset	0000 0000 _{HEX}		
Status	Default Value										
Power On Sequence	0000 0000 _{HEX}										
SW Reset	No Change										
HW Reset	0000 0000 _{HEX}										
Flow Chart	<pre> graph TD Start([Address mode]) --> Set[Set_address_mode] Set --> Decision{B7,B6,B5,B4,B0} Decision --> NewAddress([New Address mode]) Decision --> Set </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 										

8.2.26. Set_scroll_start (37h)

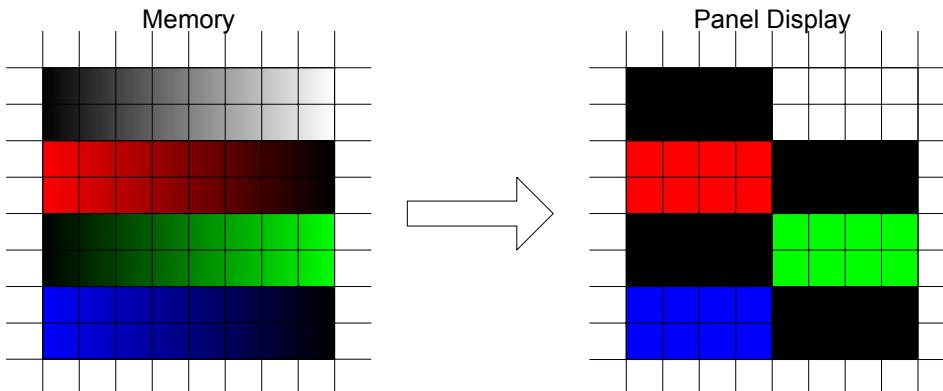
37H		Set_scroll_start												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37	
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP 8	xx	
2 nd Parameter	1	1	↑	x	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	xx	
Description	<p>This command sets the start of the vertical scrolling area in the frame memory. The vertical scrolling area is fully defined when this command is used with the set_scroll_area command.</p> <p>The set_scroll_start command has one parameter, the Vertical Scroll Pointer. The VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area.</p> <p>The displayed image also depends on the setting of the Line Address Order bit, B4, in the set_address_mode register. See the examples below.</p> <p>If set_address_mode (R36h) B4 = 0:</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 0, Vertical Scrolling Area = 480 and VSP = 3.</p> <p>If set_address_mode (R36h) B4 = 1:</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.</p> <p>Note: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid</p>													

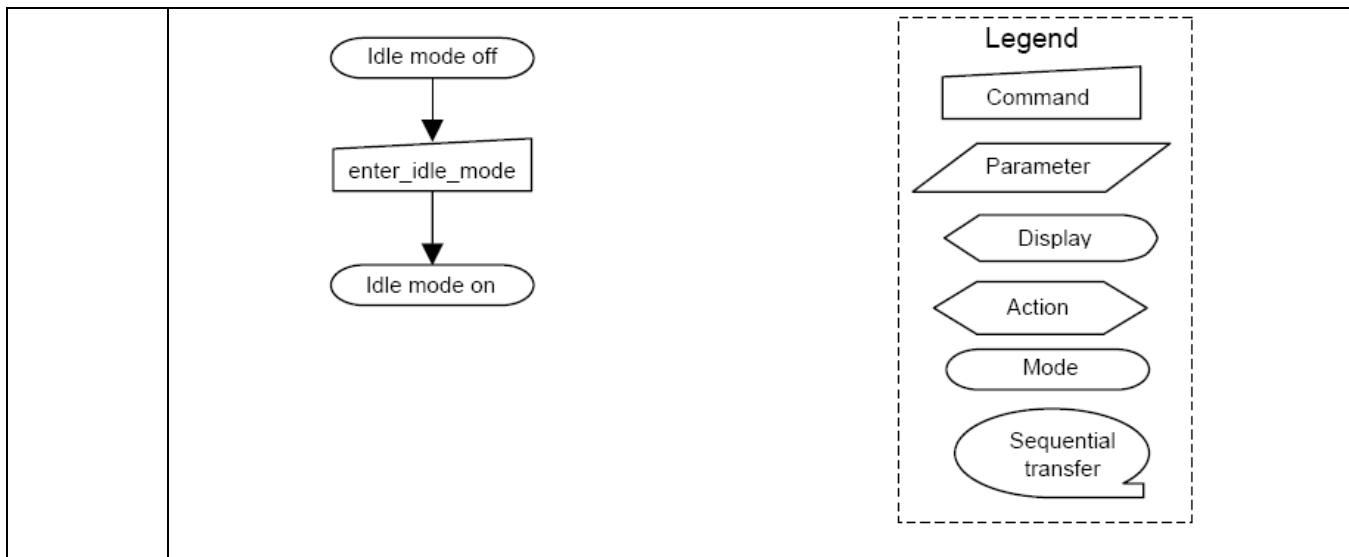
	tearing effect. VSP refers to the Frame Memory line Pointer.												
Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000_{HEX}</td></tr> <tr> <td>SW Reset</td><td>0000_{HEX}</td></tr> <tr> <td>HW Reset</td><td>0000_{HEX}</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	0000 _{HEX}	SW Reset	0000 _{HEX}	HW Reset	0000 _{HEX}				
Status	Default Value												
Power On Sequence	0000 _{HEX}												
SW Reset	0000 _{HEX}												
HW Reset	0000 _{HEX}												
Flow Chart	Refer to the description set_scroll_area (33h)												

8.2.27. Exit_idle_mode (38h)

Exit_idle_mode																									
38H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38												
Parameter	NO PARAMETER																								
Description	This command causes the display module to exit Idle mode.																								
Restriction	This command has no effect when the display module is not in Idle mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle Mode Off</td> </tr> <tr> <td>SW Reset</td> <td>Idle Mode Off</td> </tr> <tr> <td>HW Reset</td> <td>Idle Mode Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off				
Status	Default Value																								
Power On Sequence	Idle Mode Off																								
SW Reset	Idle Mode Off																								
HW Reset	Idle Mode Off																								
Flow Chart	<pre> graph TD A([Idle mode on]) --> B[Exit_idle_mode] B --> C([Idle mode off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Box Parameter: Parallelogram Display: Horizontal oval Action: Diamond Mode: Vertical oval Sequential transfer: Ellipse 																								

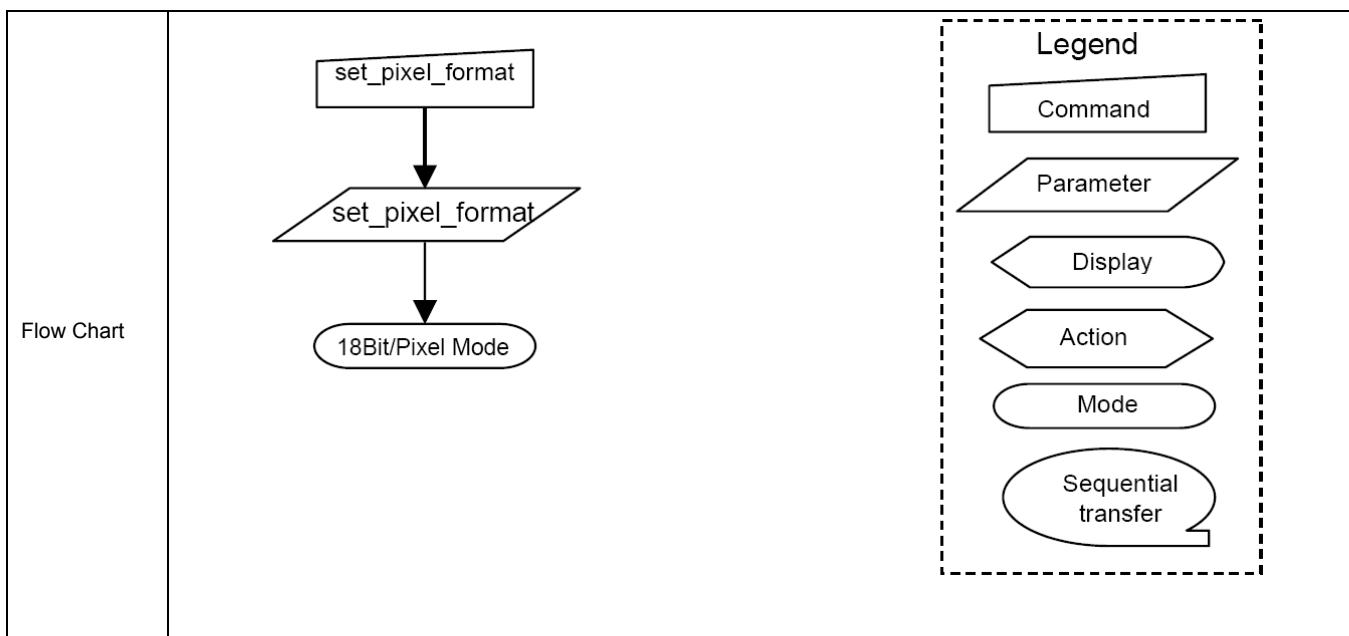
8.2.28. Enter_idle_mode (39h)

39H		Enter_idle_mode																																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	↑	x	0	0	1	1	1	0	0	1	39																																				
Parameter	NO PARAMETER																																																
Description	<p>This command causes the display module to enter Idle Mode.</p> <p>In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.</p>  <table border="1"> <thead> <tr> <th></th> <th>R5 R4 R3 R2 R1 R0</th> <th>G5 G4 G3 G2 G1 G0</th> <th>B5 B4 B3 B2 B1 B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> </tbody> </table>														R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0																																														
Black	0XXXXX	0XXXXX	0XXXXX																																														
Blue	0XXXXX	0XXXXX	1XXXXX																																														
Red	1XXXXX	0XXXXX	0XXXXX																																														
Magenta	1XXXXX	0XXXXX	1XXXXX																																														
Green	0XXXXX	1XXXXX	0XXXXX																																														
Cyan	0XXXXX	1XXXXX	1XXXXX																																														
Yellow	1XXXXX	1XXXXX	0XXXXX																																														
White	1XXXXX	1XXXXX	1XXXXX																																														
Restriction	This command has no effect when module is already in idle on mode.																																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
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Status	Default Value																																																
Power On Sequence	Idle Mode Off																																																
SW Reset	Idle Mode Off																																																
HW Reset	Idle Mode Off																																																
Flow Chart																																																	



8.2.29. Set_pixel_format (3Ah)

Set_pixel_format																									
3AH	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3A												
1 st Parameter	1	1	↑	x	x	D6	D5	D4	x	D2	D1	D0	3A												
Description	This command sets the pixel format for the RGB image data used by the interface. Bits D[6:4] – DPI Pixel Format Definition Bits D[2:0] – DBI Pixel Format Definition Bits D7 and D3 are not used. If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.																								
Restriction	There is no visible effect until the Frame Memory is written to.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>18bit/pixel</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>18bit/pixel</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	18bit/pixel	SW Reset	No change	HW Reset	18bit/pixel				
Status	Default Value																								
Power On Sequence	18bit/pixel																								
SW Reset	No change																								
HW Reset	18bit/pixel																								



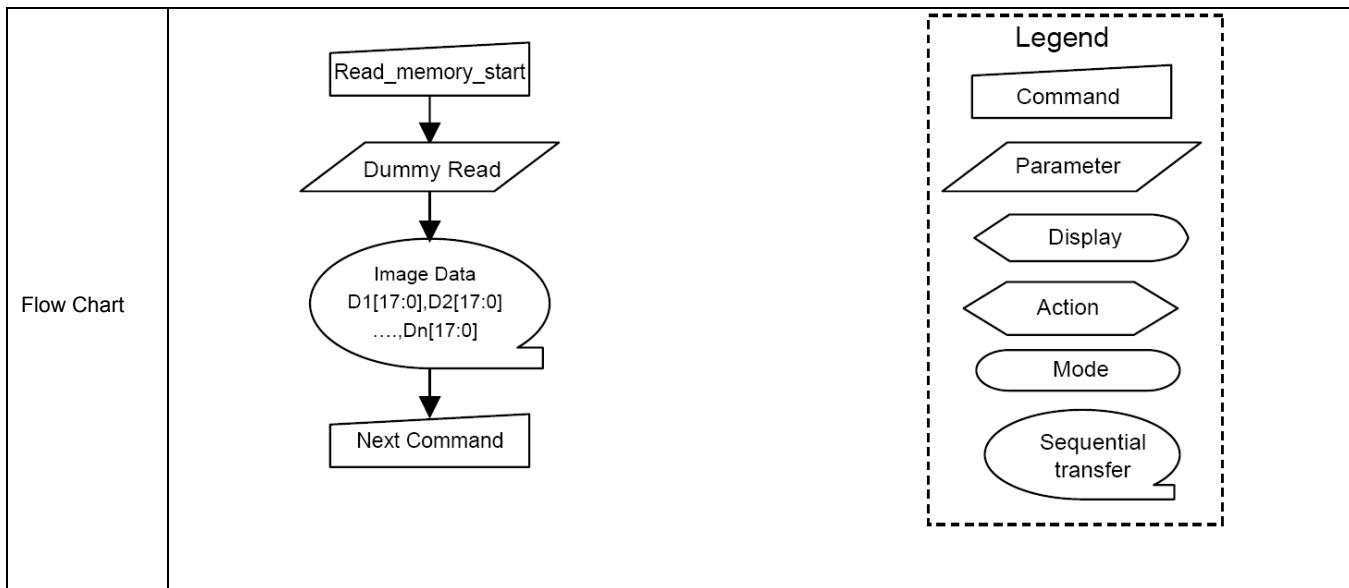
8.2.30. Write_Memory_Continue (3Ch)

Write_Memory_Continue																									
3CH	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3C												
1 st Parameter	1	1	↑	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF												
x st Parameter	1	1	↑	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF												
N st Parameter	1	1	↑	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF												
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. If set_address_mode B5 = 0: Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If set_address_mode B5 = 1: Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.																								
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

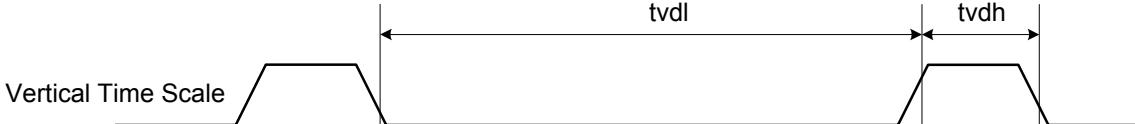
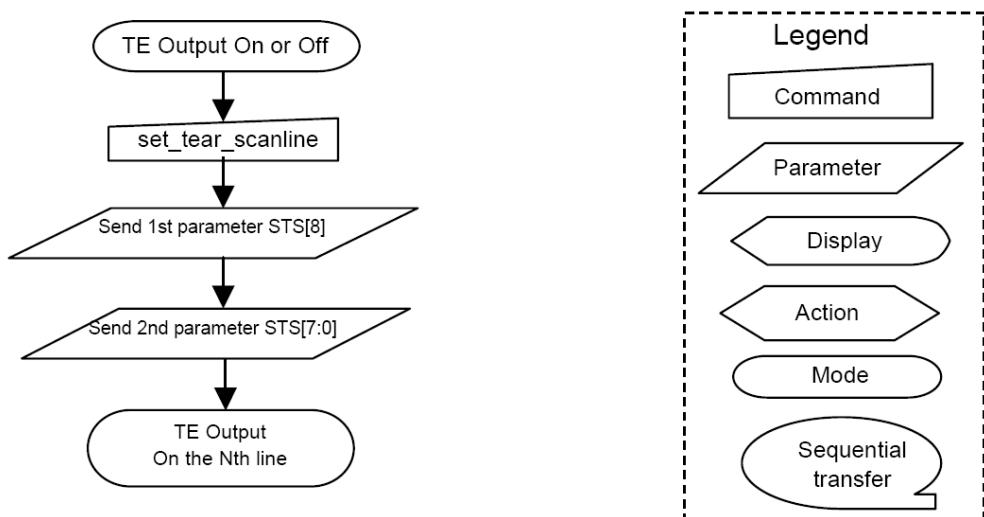
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center; padding: 2px;">Status</th><th style="text-align: center; padding: 2px;">Default Value</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Power On Sequence</td><td style="text-align: center; padding: 2px;">All zero</td></tr> <tr> <td style="text-align: center; padding: 2px;">SW Reset</td><td style="text-align: center; padding: 2px;">No change</td></tr> <tr> <td style="text-align: center; padding: 2px;">HW Reset</td><td style="text-align: center; padding: 2px;">All zero</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	All zero	SW Reset	No change	HW Reset	All zero
Status	Default Value								
Power On Sequence	All zero								
SW Reset	No change								
HW Reset	All zero								
Flow Chart	<pre> graph TD A[Write_memory_continue] --> B{Image Data D1[17:0], D2[17:0] ..., Dn[17:0]} B --> C[Next Command] </pre> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>								

8.2.31. Read_Memory_Continue (3Eh)

3EH		Read_Memory_Continue																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑		x	0	0	1	1	1	1	1	0	3E											
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x	x											
2 nd Parameter	1	↑	1	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF												
x st Parameter	1	↑	1	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF												
N st Parameter	1	↑	1	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF												
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If set_address_mode B5 = 0: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If set_address_mode B5 = 1: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.																								
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data. A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.																								
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Random data</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>Random data</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	Random data	SW Reset	No change	HW Reset	Random data				
Status	Default Value																								
Power On Sequence	Random data																								
SW Reset	No change																								
HW Reset	Random data																								



8.2.32. Set_Tear_Scanline (44h)

44H		Set_Tear_Scanline																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	0	0	1	0	0	44												
1 st Parameter	1	1	↑	xx	0	0	0	0	0	0	0	STS [8]	0x												
2 nd Parameter	1	1	↑	xx	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	xx												
Description	<p>This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>Note that set_tear_scanline with N = 0 is equivalent to set_tear_on with M = 0. The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																								
Restriction	This command has no effect when Tearing Effect output is already ON.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>STS[8:0]=8'h0000</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>STS[8:0]=8'h0000</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	STS[8:0]=8'h0000	SW Reset	No change	HW Reset	STS[8:0]=8'h0000				
Status	Default Value																								
Power On Sequence	STS[8:0]=8'h0000																								
SW Reset	No change																								
HW Reset	STS[8:0]=8'h0000																								
Flow Chart	 <pre> graph TD A([TE Output On or Off]) --> B[set_tear_scanline] B --> C[/Send 1st parameter STS[8]/] B --> D[/Send 2nd parameter STS[7:0]/] C --> E([TE Output On the Nth line]) D --> E </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

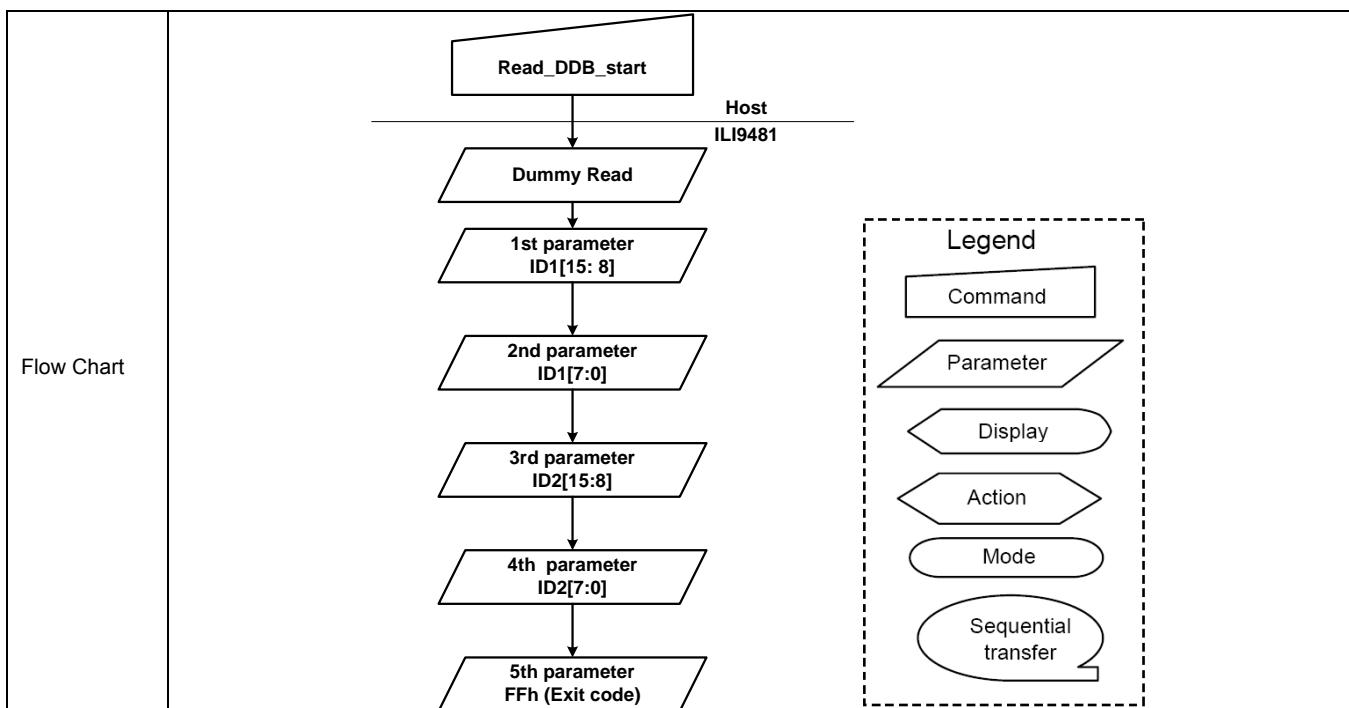
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8.2.33. Get_Scanline (45h)

45H		Get_Scanline																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	0	1	0	0	0	1	0	1	45													
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x													
2 nd Parameter	1	↑	1	xx	0	0	0	0	0	0	0	GTS [8]	0x													
3 rd Parameter	1	↑	1	xx	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	xx													
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.																									
Restriction	None																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Flow Chart	<pre> graph TD start[get_scanline] --> wait{Wait 3us} wait --> dummy[/Dummy Read/] dummy --> param1[/Send 1st parameter GTS[9:8]/] param1 --> param2[/Send 2nd parameter GTS[7:0]/] subgraph Legend [Legend] direction TB C[Command] P[Parameter] D[Display] A[Action] M[Mode] ST[Sequential transfer] end </pre>																									

8.2.34. Read_DDB_Start (A1h)

A1H		Read_DDB_Start																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	1	0	1	0	0	0	0	1	A1													
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x													
2 nd Parameter	1	↑	1	xx	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	xx													
3 rd Parameter	1	↑	1	xx	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	xx													
4 th Parameter	1	↑	1	xx	ID0 [15]	ID0 [14]	ID0 [13]	ID0 [12]	ID0 [11]	ID0 [10]	ID0 [9]	ID0 [8]	xx													
5 th Parameter	1	↑	1	xx	ID0 [7]	ID0 [6]	ID0 [5]	ID0 [4]	ID0 [3]	ID0 [2]	ID0 [1]	ID0 [0]	xx													
6 th Parameter	1	↑	1	xx	1	1	1	1	1	1	1	1	FF													
Description	1 st parameter: Dummy read 2 nd parameter: Supplier ID code ID1[15:8] 3 rd parameter: Supplier ID code ID1[7:0] 4 th parameter: Supplier Elective Data ID21[15:8] 5 th parameter: Supplier Elective Data ID2[7:0] 6 th Exit code (FFh). When using the external EEPROM (EEPROME=high), the Supplier ID code ID1 and Supplier Elective Data are read back from EEPROM. When using the internal NV memory (EEPROME=Low), the Supplier ID code ID1 and Supplier Elective Data are read back from NV memory.																									
Restriction																										
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									



8.2.35. Command Access Protect (B0h)

Command Access Protect																																															
B0H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																		
Command	0	1	↑	xx	1	0	1	1	0	0	0	0	B0																																		
1 st parameter	0	1	↑	xx	0	0	0	0	0	0	MCAP[1]	MCAP[0]	xx																																		
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">MCAP[1:0]</th> <th>User Command</th> <th>Protect command</th> <th colspan="3">Manufacturer Command</th> </tr> <tr> <th>00h ~ AFh</th> <th>B0h</th> <th>B1h ~ DFh</th> <th>E0h~EFh</th> <th>F0h~FFh</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> </tr> <tr> <td>2'h1</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>No</td> </tr> <tr> <td>2'h2</td> <td>Yes</td> <td>Yes</td> <td>Yes</td> <td>No</td> <td>No</td> </tr> <tr> <td>2'h3</td> <td>Yes</td> <td>Yes</td> <td>No</td> <td>No</td> <td>No</td> </tr> </tbody> </table>													MCAP[1:0]	User Command	Protect command	Manufacturer Command			00h ~ AFh	B0h	B1h ~ DFh	E0h~EFh	F0h~FFh	2'h0	Yes	Yes	Yes	Yes	Yes	2'h1	Yes	Yes	Yes	Yes	No	2'h2	Yes	Yes	Yes	No	No	2'h3	Yes	Yes	No	No	No
MCAP[1:0]	User Command	Protect command	Manufacturer Command																																												
	00h ~ AFh	B0h	B1h ~ DFh	E0h~EFh	F0h~FFh																																										
2'h0	Yes	Yes	Yes	Yes	Yes																																										
2'h1	Yes	Yes	Yes	Yes	No																																										
2'h2	Yes	Yes	Yes	No	No																																										
2'h3	Yes	Yes	No	No	No																																										
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																						
Status	Availability																																														
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																														
Sleep In	Yes																																														
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>MCAP[1:0]=2'h0</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>MCAP[1:0]=2'h0</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	MCAP[1:0]=2'h0	SW Reset	No change	HW Reset	MCAP[1:0]=2'h0																										
Status	Default Value																																														
Power On Sequence	MCAP[1:0]=2'h0																																														
SW Reset	No change																																														
HW Reset	MCAP[1:0]=2'h0																																														
Flow Chart	<pre> graph TD A([Sleep Mode]) --> B[Low Power Mode Control] B --> C{DSTB=1} C --> D([Deepstandby Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																														

8.2.36. Low Power Mode Control (B1h)

B1H	Low Power Mode Control																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	xx	1	0	1	1	0	0	0	1	B1												
1 st parameter	0	1	↑	xx	0	0	0	0	0	0	0	DSTB	xx												
Description	Deep standby mode control. The driver enters the Deep Standby Mode when DSTB=1. Internal logic power supply circuit (VDD) is turned down enabling low power consumption. In the Deep Standby mode, data stored in the Frame Memory and the Instructions are not retained. Rewrite them after the Deep Standby mode is exited.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>DSTB=0</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>DSTB=0</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	DSTB=0	SW Reset	No change	HW Reset	DSTB=0				
Status	Default Value																								
Power On Sequence	DSTB=0																								
SW Reset	No change																								
HW Reset	DSTB=0																								
Flow Chart	<pre> graph TD A([Sleep Mode]) --> B[Low Power Mode Control] B --> C{DSTB=1} C --> D([Deepstandby Mode]) style C fill:none,stroke:none </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.37. Frame Memory Access and Interface Setting (B3h)

Frame Memory Access and Interface Setting																														
B3H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
Command	0	1	↑	xx	1	0	1	1	0	0	1	1	B3																	
1 st parameter	0	1	↑	xx	0	0	0	0	0	0	WEMODE	0	xx																	
1 st parameter	0	1	↑	xx	0	0	0	0	0	TEI[2]	TEI[10]	TEI[0]	xx																	
2 nd parameter	0	1	↑	xx	0	0	0	0	0	DENC[2]	DENC[1]	DENC[0]	xx																	
4 th parameter	0	1	↑	xx	0	0	EPF[1]	EPF[0]	0	0	0	DFM	xx																	
Description	WEMODE: Memory write control WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.																													
	TEI[2:0]: ILI9481 starts to output TE signal in the output interval set by TEI[2:0] bits.																													
	<table border="1"> <thead> <tr> <th>TEI[2:0]</th><th>Output Interval</th></tr> </thead> <tbody> <tr> <td>000</td><td>1 frame</td></tr> <tr> <td>001</td><td>2 frame</td></tr> <tr> <td>011</td><td>4 frame</td></tr> <tr> <td>101</td><td>6 frame</td></tr> <tr> <td>Others</td><td>Setting Prohibited</td></tr> </tbody> </table>													TEI[2:0]	Output Interval	000	1 frame	001	2 frame	011	4 frame	101	6 frame	Others	Setting Prohibited					
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DENC[2:0]	GRAM Write Cycle (Frame periods)																													
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011	4 Frames																													
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101	6 Frames																													
110	7 Frames																													
111	8 Frames																													
DFM: The bit is used to define image data write/read format to the Frame Memory in DBI Type B (16bit bus interface) and DBI Type C serial interface operation.																														
EPF[1:0]: Set the data format when 16bbp (R,G,B) to 18 bdp (r, g, b) is stored in the internal GRAM.																														
<table border="1"> <thead> <tr> <th>EPF[1:0]</th><th>Expand 16bbp (R,G,B) to 18 bdp (R, G, B)</th></tr> </thead> <tbody> <tr> <td>00</td><td>MSB is inputted to LSB r[5:0] = {R[4:0], R[4]} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], B[4]}</td></tr> <tr> <td>01</td><td>“0” is inputted to LSB r[5:0] = {R[4:0], 0} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 0} Exception: R[4:0], B[4:0]=5'h1F → r[5:0], b[5:0] = 6'h3F</td></tr> <tr> <td>10</td><td>“1” is inputted to LSB r[5:0] = {R[4:0], 1}</td></tr> </tbody> </table>													EPF[1:0]	Expand 16bbp (R,G,B) to 18 bdp (R, G, B)	00	MSB is inputted to LSB r[5:0] = {R[4:0], R[4]} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], B[4]}	01	“0” is inputted to LSB r[5:0] = {R[4:0], 0} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 0} Exception: R[4:0], B[4:0]=5'h1F → r[5:0], b[5:0] = 6'h3F	10	“1” is inputted to LSB r[5:0] = {R[4:0], 1}										
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			<p>g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 1}</p> <p>Exception: R[4:0], B[4:0]=5'h00 → r[5:0], b[5:0] = 6'h00</p>											
		11	Setting disabled											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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8.2.38. Display Mode and Frame Memory Write Mode Setting (B4h)

Display Mode and Frame Memory Write Mode Setting																																									
B4H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	xx	1	0	1	1	0	1	0	0	B4																												
1 st parameter	0	1	↑	xx	0	0	0	RM	0	0	0	DM	xx																												
Description	DM Select the display operation mode. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">DM0</th> <th style="text-align: center;">Display Interface</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Internal system clock</td> </tr> <tr> <td style="text-align: center;">1</td> <td>DPI (RGB) interface</td> </tr> </tbody> </table> <p>The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode.</p> <p>RM Select the interface to access the GRAM.</p> <p>Set RM to "1" when writing display data by the RGB interface.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">RM</th> <th style="text-align: center;">Interface for RAM Access</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>DBI Interface (CPU)</td> </tr> <tr> <td style="text-align: center;">1</td> <td>DPI Interface (RGB)</td> </tr> </tbody> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">Display State</th> <th style="text-align: center;">Operation Mode</th> <th style="text-align: center;">RAM Access (RM)</th> <th style="text-align: center;">Display Operation Mode (DM[1:0])</th> </tr> </thead> <tbody> <tr> <td>Still pictures</td> <td>Internal clock operation</td> <td>System interface (RM = 0)</td> <td>Internal clock operation (DM = 0)</td> </tr> <tr> <td>Moving pictures</td> <td>RGB interface (1)</td> <td>RGB interface (RM = 1)</td> <td>RGB interface (DM = 1)</td> </tr> <tr> <td>Rewrite still picture area while RGB interface Displaying moving pictures.</td> <td></td> <td>System interface (RM = 0)</td> <td>RGB interface (DM = 1)</td> </tr> </tbody> </table> <p><i>Note 1: Registers are set only via the system interface or SPI interface.</i></p> <p><i>Note 2: Refer to the flowcharts of "RGB Input Interface" section for the mode switch.</i></p>													DM0	Display Interface	0	Internal system clock	1	DPI (RGB) interface	RM	Interface for RAM Access	0	DBI Interface (CPU)	1	DPI Interface (RGB)	Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0])	Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 0)	Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 1)	Rewrite still picture area while RGB interface Displaying moving pictures.		System interface (RM = 0)	RGB interface (DM = 1)
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Power On Sequence	DM=0, RM=0																																								
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8.2.39. Device Code Read (BFh)

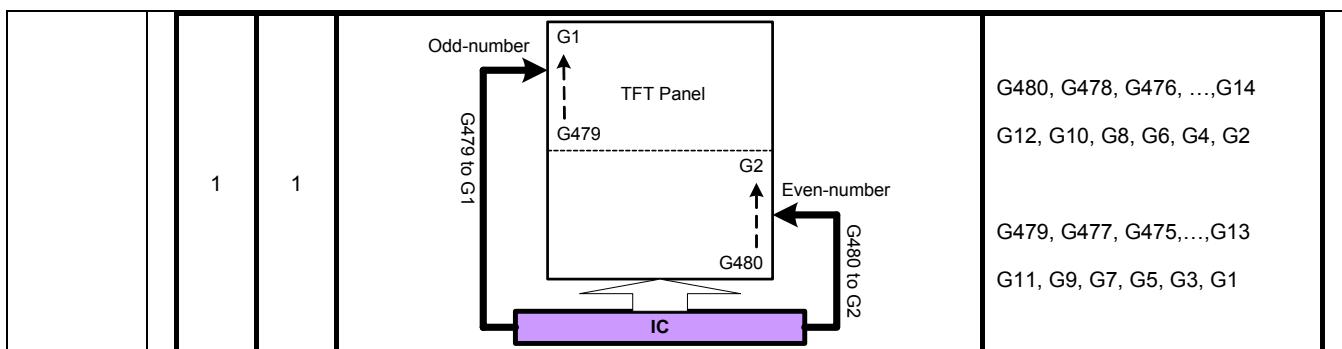
BFH	Device Code Read																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	xx	1	0	1	1	1	1	1	1	1	BF												
1 st parameter	0	↑	1	x	x	x	x	x	x	x	x	x	x	x												
2 nd parameter	0	↑	1	xx	0	0	0	0	0	0	1	0	0	02												
3 rd parameter	0	↑	1	xx	0	0	0	0	0	1	0	0	0	04												
4 th parameter	0	↑	1	xx	1	0	0	1	0	1	0	0	0	94												
5 th parameter	0	↑	1	xx	1	0	0	0	0	0	0	1	0	81												
6 th parameter	0	↑	1	xx	1	1	1	1	1	1	1	1	1	FF												
Description	1 st parameter : dummy read 2 nd parameter : MIPI Alliance code 3 rd parameter : MIPI Alliance code 4 th parameter : Device ID code of ILI9481 5 th parameter : Device ID code of ILI9481 6 th parameter : Exit code (FFh)																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																									
Power On Sequence																										
SW Reset	No change																									
HW Reset																										

8.2.40. Panel Driving Setting (C0h)

C0H	Panel Driving Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	0	C0
1 st Parameter	1	1	↑	0	0	0	0	REV	SM	0	0	0	x
2 nd Parameter	1	1	↑	0	0	NL [6]	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	xx
3 rd Parameter	1	1	↑	0	0	SCN [6]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	xxx
4 th Parameter	1	1	↑	0	0	0	0	0	0	0	0	PTV	xxx
5 th Parameter	1	1	↑	0	0	0	0	NDL	0	PTS [2]	PTS [1]	PTS [0]	xxx
6 th Parameter	1	1	↑	0	0	0	0	PTG	ISC [3]	ISC [2]	ISC [1]	ISC [0]	xxx

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

	SM	GS	Scan Direction	Gate Output Sequence
Description	0	0	<p>TFT Panel</p> <p>G1, G3, G477, G479, G480</p> <p>Odd-number: G1 to G479</p> <p>Even-number: G2 to G480</p>	<p>G1, G2, G3, G4, ..., G476</p> <p>G477, G478, G479, G480</p>
	0	1	<p>TFT Panel</p> <p>G479, G477, G480</p> <p>Odd-number: G479 to G1</p> <p>Even-number: G480 to G2</p>	<p>G480, G479, G478, ..., G9</p> <p>G7, G5, G4, G3, G2, G1</p>
	1	0	<p>TFT Panel</p> <p>G1, G3, G479</p> <p>Odd-number: G1 to G479</p> <p>Even-number: G2 to G480</p>	<p>G1, G3, G5, G7, ..., G471</p> <p>G473, G475, G477, G479</p> <p>G2, G4, G6, G8, ..., G472</p> <p>G474, G476, G478, G480</p>



REV: Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	Negative polarity
0	18'h000000 : 18'h3FFFF	V63 : V0	V0 : V63
1	18'h000000 : 18'h3FFFF	V0 : V63	V63 : V0

NL[6:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[6:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[6:0]	LCD Drive Line
7'h00 ~ 7'h3B	8 * (NL[6:0]+1) lines
Others	Setting inhibited

SCN[6:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h ~ 3Bh	G[1+SCN[6:0]*4]	G[480 - SCN[6:0]*4]	G[1+SCN[6:0]*8]	G[480 - SCN[6:0]*8]
3Ch ~ 77h	G[1+SCN[6:0]*4]	G[480 - SCN[6:0]*4]	G[2+(SCN[6:0]-3Ch)*8]	G[479 - (SCN[6:0]-3Ch)*8]
Others	Setting disabled	Setting disabled	Setting disabled	Setting disabled

PTV: Sets the Vcom output in non-display area drive period.

PTV	Vcom operation in non-display drive period
0	Normal Operation
1	Halts VCOM Operation

NDL: Sets the source output level in non-display area. Settings are different to normally black panels and normally white panels.

NDL	Non-display Area	
	Positive	Negative
0	V63	V0
1	V0	V63

PTG: Sets the scan mode in non-display area. Select frame-inversion AC drive when interval-scan is selected.

PTG	Scan Mode in non-display area
0	Normal Scan

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1

Interval Scan

ICS[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

ISC[3:0]	Scan cycle	(f_{FRAME})=60Hz
4'h0	Setting inhibited	—
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTS[2:0]:

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
000	V63	V0	V63 to V0	Register Setting(DC1, DC0)
001	Setting Prohibited	Setting Prohibited	-	-
010	GND	GND	V63 to V0	Register Setting(DC1, DC0)
011	Hi-Z	Hi-Z	V63 to V0	Register Setting(DC1, DC0)
100	V63	V0	V63 and V0	1/2 frequency setting by DC1, DC0
101	Setting Prohibited	Setting Prohibited	-	-
110	GND	GND	V63 and V0	1/2 frequency setting by DC1, DC0
111	Hi-Z	Hi-Z	V63 and V0	1/2 frequency setting by DC1, DC0

Notes: 1. The power efficiency can be improved by halting grayscale amplifiers and slowing down the step-up clock frequency only in non-display drive period.

2. The gate output level in non-lit display area drive period is determined by PTG[1:0].

Restriction

		Status	Availability
Register Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes
		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes
		Status	Default Value
Default		Power On Sequence	SM=0, REV=0, NL[6:0]=7'h3B, PTV=0, NDL=0, PTG=0, ISC[3:0]=4'h1, PTS[2:0]=3'h0
		SW Reset	No change
		HW Reset	SM=0, REV=0, NL[6:0]=7'h3B, PTV=0, BLS=0, PTG=0, ISC[3:0]=4'h1, PTS[2:0]=3'h0

8.2.41. Display_Timing_Setting for Normal Mode (C1h)

C1H	Display_Timing_Setting for Normal Mode																																																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																											
Command	0	1	↑	x	1	1	0	0	0	0	0	1	C1																																											
1 st Parameter	1	1	↑	0	0	0	0	BC0	0	0	DIV0[1]	DIV0[0]	x																																											
2 nd Parameter	1	1	↑	0	0	0	0	RTN0[4]	RTN0[3]	RTN0[2]	RTN0[1]	RTN0[0]	xx																																											
3 rd Parameter	1	1	↑	0	FP0[3]	FP0[2]	FP0[1]	FP0[0]	BP0[3]	BP0[2]	BP0[1]	BP0[0]	xxx																																											
Description	BC0: BC0 is used to select VCOM liquid crystal drive waveform. BC0 = 0: Frame inversion waveform is selected. BC0 = 1: Line inversion waveform is selected. DIV0[1:0]: DIV0[1:0] is used to set division ratio of internal clock frequency. The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed. The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DIV0[1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>1/1</td> </tr> <tr> <td>2'h1</td> <td>1/2</td> </tr> <tr> <td>2'h2</td> <td>1/4</td> </tr> <tr> <td>2'h3</td> <td>1/8</td> </tr> </tbody> </table> Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)] fosc. : internal oscillator frequency clocks per line : RTNn setting division ratio: DIVn setting Line: total driving line number BP: back porch line number FP: front porch line number													DIV0[1:0]	Division Ratio	2'h0	1/1	2'h1	1/2	2'h2	1/4	2'h3	1/8																																	
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	RTN0[4:0]: RTN0[4:0] is used to set 1H (line) period. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RTN[4:0]</th> <th>Clocks per line</th> <th>RTN[4:0]</th> <th>Clocks per line</th> <th>RTN[4:0]</th> <th>Clocks per line</th> </tr> </thead> <tbody> <tr> <td>5'h00~0F</td> <td>Setting prohibited</td> <td>5'h15</td> <td>21 clocks</td> <td>5'h1B</td> <td>27 clocks</td> </tr> <tr> <td>5'h10</td> <td>16 clocks</td> <td>5'h16</td> <td>22 clocks</td> <td>5'h1C</td> <td>28 clocks</td> </tr> <tr> <td>5'h11</td> <td>17 clocks</td> <td>5'h17</td> <td>23 clocks</td> <td>5'h1D</td> <td>29 clocks</td> </tr> <tr> <td>5'h12</td> <td>18 clocks</td> <td>5'h18</td> <td>24 clocks</td> <td>5'h1E</td> <td>30 clocks</td> </tr> <tr> <td>5'h13</td> <td>19 clocks</td> <td>5'h19</td> <td>25 clocks</td> <td>5'h1F</td> <td>31 clocks</td> </tr> <tr> <td>5'h14</td> <td>20 clocks</td> <td>5'h1A</td> <td>26 clocks</td> <td></td> <td></td> </tr> </tbody> </table> FP0[3:0], BP0[3:0] FP0[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display). BP0[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of														RTN[4:0]	Clocks per line	RTN[4:0]	Clocks per line	RTN[4:0]	Clocks per line	5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks	5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks	5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks	5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks	5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks	5'h14	20 clocks	5'h1A	26 clocks		
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8.2.42. Display_Timing_Setting for Partial Mode (C2h)

C2H	Display_Timing_Setting for Partial Mode																																																																	
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																					
Command	0	1	↑	x	1	1	0	0	0	0	1	0	C2																																																					
1 st Parameter	1	1	↑	0	0	0	0	BC1	0	0	DIV1[1]	DIV1[0]	x																																																					
2 nd Parameter	1	1	↑	0	0	0	0	RTN1[4]	RTN1[3]	RTN1[2]	RTN1[1]	RTN1[0]	xx																																																					
3 rd Parameter	1	1	↑	0	FP1[3]	FP1[2]	FP1[1]	FP1[0]	BP1[3]	BP1[2]	BP1[1]	BP1[0]	xxx																																																					
Description	<p>BC1: BC1 is used to select VCOM liquid crystal drive waveform. BC1 = 0: Frame inversion waveform is selected. BC1 = 1: Line inversion waveform is selected.</p> <p>DIV1[1:0]: DIV1[1:0] is used to set division ratio of internal clock frequency. The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed. The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.</p> <table border="1"> <thead> <tr> <th>DIV1[1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>1/1</td> </tr> <tr> <td>2'h1</td> <td>1/2</td> </tr> <tr> <td>2'h2</td> <td>1/4</td> </tr> <tr> <td>2'h3</td> <td>1/8</td> </tr> </tbody> </table> <p>Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)] fosc. : internal oscillator frequency clocks per line : RTNn setting division ratio: DIVn setting Line: total driving line number BP: back porch line number FP: front porch line number</p> <p>RTN1[4:0]: RTN0[4:0] is used to set 1H (line) period.</p> <table border="1"> <thead> <tr> <th>RTN1[4:0]</th> <th>Clocks per line</th> <th>RTN1[4:0]</th> <th>Clocks per line</th> <th>RTN1[4:0]</th> <th>Clocks per line</th> </tr> </thead> <tbody> <tr> <td>5'h00~0F</td> <td>Setting prohibited</td> <td>5'h15</td> <td>21 clocks</td> <td>5'h1B</td> <td>27 clocks</td> </tr> <tr> <td>5'h10</td> <td>16 clocks</td> <td>5'h16</td> <td>22 clocks</td> <td>5'h1C</td> <td>28 clocks</td> </tr> <tr> <td>5'h11</td> <td>17 clocks</td> <td>5'h17</td> <td>23 clocks</td> <td>5'h1D</td> <td>29 clocks</td> </tr> <tr> <td>5'h12</td> <td>18 clocks</td> <td>5'h18</td> <td>24 clocks</td> <td>5'h1E</td> <td>30 clocks</td> </tr> <tr> <td>5'h13</td> <td>19 clocks</td> <td>5'h19</td> <td>25 clocks</td> <td>5'h1F</td> <td>31 clocks</td> </tr> <tr> <td>5'h14</td> <td>20 clocks</td> <td>5'h1A</td> <td>26 clocks</td> <td></td> <td></td> </tr> </tbody> </table> <p>FP1[3:0], BP1[3:0] FP1[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display). BP1[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of</p>														DIV1[1:0]	Division Ratio	2'h0	1/1	2'h1	1/2	2'h2	1/4	2'h3	1/8	RTN1[4:0]	Clocks per line	RTN1[4:0]	Clocks per line	RTN1[4:0]	Clocks per line	5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks	5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks	5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks	5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks	5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks	5'h14	20 clocks	5'h1A	26 clocks		
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RTN1[4:0]	Clocks per line	RTN1[4:0]	Clocks per line	RTN1[4:0]	Clocks per line																																																													
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8.2.43. Display_Timing_Setting for Idle Mode (C3h)

C3H	Display_Timing_Setting for Idle Mode																																																																	
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																					
Command	0	1	↑	x	1	1	0	0	0	0	1	1	C3																																																					
1 st Parameter	1	1	↑	0	0	0	0	BC2	0	0	DIV2[1]	DIV2[0]	x																																																					
2 nd Parameter	1	1	↑	0	0	0	0	RTN2[4]	RTN2[3]	RTN2[2]	RTN2[1]	RTN2[0]	xx																																																					
3 rd Parameter	1	1	↑	0	FP2[3]	FP2[2]	FP2[1]	FP2[0]	BP2[3]	BP2[2]	BP2[1]	BP2[0]	xxx																																																					
Description	<p>BC2: BC1 is used to select VCOM liquid crystal drive waveform. BC1 = 0: Frame inversion waveform is selected. BC1 = 1: Line inversion waveform is selected.</p> <p>DIV2[1:0]: DIV1[1:0] is used to set division ratio of internal clock frequency. The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed. The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.</p> <table border="1"> <thead> <tr> <th>DIV2[1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>1/1</td> </tr> <tr> <td>2'h1</td> <td>1/2</td> </tr> <tr> <td>2'h2</td> <td>1/4</td> </tr> <tr> <td>2'h3</td> <td>1/8</td> </tr> </tbody> </table> <p>Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)] fosc. : internal oscillator frequency clocks per line : RTNn setting division ratio: DIVn setting Line: total driving line number BP: back porch line number FP: front porch line number</p> <p>RTN2[4:0]: RTN0[4:0] is used to set 1H (line) period.</p> <table border="1"> <thead> <tr> <th>RTN2[4:0]</th> <th>Clocks per line</th> <th>RTN2[4:0]</th> <th>Clocks per line</th> <th>RTN2[4:0]</th> <th>Clocks per line</th> </tr> </thead> <tbody> <tr> <td>5'h00~0F</td> <td>Setting prohibited</td> <td>5'h15</td> <td>21 clocks</td> <td>5'h1B</td> <td>27 clocks</td> </tr> <tr> <td>5'h10</td> <td>16 clocks</td> <td>5'h16</td> <td>22 clocks</td> <td>5'h1C</td> <td>28 clocks</td> </tr> <tr> <td>5'h11</td> <td>17 clocks</td> <td>5'h17</td> <td>23 clocks</td> <td>5'h1D</td> <td>29 clocks</td> </tr> <tr> <td>5'h12</td> <td>18 clocks</td> <td>5'h18</td> <td>24 clocks</td> <td>5'h1E</td> <td>30 clocks</td> </tr> <tr> <td>5'h13</td> <td>19 clocks</td> <td>5'h19</td> <td>25 clocks</td> <td>5'h1F</td> <td>31 clocks</td> </tr> <tr> <td>5'h14</td> <td>20 clocks</td> <td>5'h1A</td> <td>26 clocks</td> <td></td> <td></td> </tr> </tbody> </table> <p>FP2[3:0], BP2[3:0] FP2[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display). BP2[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of</p>														DIV2[1:0]	Division Ratio	2'h0	1/1	2'h1	1/2	2'h2	1/4	2'h3	1/8	RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line	5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks	5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks	5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks	5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks	5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks	5'h14	20 clocks	5'h1A	26 clocks		
DIV2[1:0]	Division Ratio																																																																	
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2'h2	1/4																																																																	
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	<p>display).</p> <table border="1"> <thead> <tr> <th>FP2[3:0]</th><th>Front and back</th></tr> </thead> <tbody> <tr> <td>BP2[3:0]</td><td>porch period (line period)</td></tr> <tr> <td>4'h0</td><td>Setting prohibited</td></tr> <tr> <td>4'h1</td><td>Setting prohibited</td></tr> <tr> <td>4'h2</td><td>2 lines</td></tr> <tr> <td>4'h3</td><td>3 lines</td></tr> <tr> <td>4'h4</td><td>4 lines</td></tr> <tr> <td>4'h5</td><td>5 lines</td></tr> <tr> <td>4'h6</td><td>6 lines</td></tr> <tr> <td>4'h7</td><td>7 lines</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>FP2[3:0]</th><th>Front and back</th></tr> </thead> <tbody> <tr> <td>BP2[3:0]</td><td>porch period (line period)</td></tr> <tr> <td>4'h8</td><td>8 lines</td></tr> <tr> <td>4'h9</td><td>9 lines</td></tr> <tr> <td>4'hA</td><td>10 lines</td></tr> <tr> <td>4'hB</td><td>11 lines</td></tr> <tr> <td>4'hC</td><td>12 lines</td></tr> <tr> <td>4'hD</td><td>13 lines</td></tr> <tr> <td>4'hE</td><td>14 lines</td></tr> <tr> <td>4'hF</td><td>15 lines</td></tr> </tbody> </table> <p>Note to Setting BP and FP</p> <p>The condition in setting BP and FP bits are: $BP \geq 2$ lines $FP \geq 2$ lines $FP+BP \leq 16$ lines</p>	FP2[3:0]	Front and back	BP2[3:0]	porch period (line period)	4'h0	Setting prohibited	4'h1	Setting prohibited	4'h2	2 lines	4'h3	3 lines	4'h4	4 lines	4'h5	5 lines	4'h6	6 lines	4'h7	7 lines	FP2[3:0]	Front and back	BP2[3:0]	porch period (line period)	4'h8	8 lines	4'h9	9 lines	4'hA	10 lines	4'hB	11 lines	4'hC	12 lines	4'hD	13 lines	4'hE	14 lines	4'hF	15 lines
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HW Reset	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h8, BP2=4'h8																																								

8.2.44. Frame Rate and Inversion Control (C5h)

C5H	Frame Rate Control																																																		
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																						
Command	0	1	↑	1	1	1	0	0	0	1	0	1	C5																																						
1 st Parameter	1	1	↑	0	0	0	0	0	0	FRA[2]	FRA[1]	FRA[0]	-																																						
Description	Set the frame frequency of the full colors normal mode. The frame frequency needs to meet 80Hz±5% in this mode. <table border="1"> <thead> <tr> <th>FRA[2:0]</th> <th>Frame Rate (Hz)</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>125</td> </tr> <tr> <td>001</td> <td>100</td> </tr> <tr> <td>010</td> <td>85 (default)</td> </tr> <tr> <td>011</td> <td>72</td> </tr> <tr> <td>100</td> <td>56</td> </tr> <tr> <td>101</td> <td>50</td> </tr> <tr> <td>110</td> <td>45</td> </tr> <tr> <td>111</td> <td>42</td> </tr> </tbody> </table>													FRA[2:0]	Frame Rate (Hz)	000	125	001	100	010	85 (default)	011	72	100	56	101	50	110	45	111	42																				
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Status	Default Value																																																		
	FRA[3:0]																																																		
Power On Sequence	4'b0100																																																		
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	NLA	NLB	NLC																																																
Power On Sequence	0	0	1																																																
SW Reset	0	0	1																																																
HW Reset	0	0	1																																																

8.2.45. Interface Control (C6h)

C6H	Interface Control																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	0	0	0	1	1	0	C6												
1 st Parameter	1	1	↑	x	SDA_EN	0	0	VSPL	HSPL	0	EPL	DPL	xx												
Description	<p>DPL: Sets the signal polarity of the PCLK pin.</p> <p>DPL = "0" The data is input on the rising edge of PCLK.</p> <p>DPL = "1" The data is input on the falling edge of PCLK.</p> <p>EPL: Sets the signal polarity of the ENABLE pin.</p> <p>EPL = "0" The data DB[17:0] is written when ENABLE = "0".</p> <p>EPL = "1" The data DB[17:0] is written when ENABLE = "1".</p> <p>HSPL: Sets the signal polarity of the HSYNC pin.</p> <p>HSPL = "0" Low active</p> <p>HSPL = "1" High active</p> <p>VSPL: Sets the signal polarity of the VSYNC pin.</p> <p>VSPL = "0" Low active</p> <p>VSPL = "1" High active</p> <p>SDA_EN: DBI type C interface selection</p> <p>SDA_EN = "0", DIN and DOUT pins are used for DBI type C interface mode.</p> <p>SDA_EN = "1", DIN/SDA pin is used for DBI type C interface mode and DOUT pin is not used.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0, SDA_EN=1'h0																								
SW Reset	No change																								
HW Reset	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0, SDA_EN=1'h0																								

8.2.46. Gamma Setting (C8h)

C8H	Gamma Setting																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	0	0	1	0	0	0	C8												
1 st Parameter	1	1	↑	x	0	KP1[2]	KP1[1]	KP1[0]	0	KP0[2]	KP0[1]	KP0[0]	xx												
2 nd Parameter	1	1	↑	x	0	KP3[2]	KP3[1]	KP3[0]	0	KP2[2]	KP2[1]	KP2[0]	xx												
3 rd Parameter	1	1	↑	x	0	KP5[2]	KP5[1]	KP5[0]	0	KP4[2]	KP4[1]	KP4[0]	xx												
4 th Parameter	1	1	↑	x	0	RP1[2]	RP1[1]	RP1[0]	0	RP0[2]	RP0[1]	RP0[0]	xx												
5 th Parameter	1	1	↑	x	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	xx												
6th Parameter	1	1	↑	x	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	xx												
7 th Parameter	1	1	↑	x	0	KN1[2]	KN1[1]	KN1[0]	0	KN0[2]	KN0[1]	KN0[0]	xx												
8 th Parameter	1	1	↑	x	0	KN3[2]	KN3[1]	KN3[0]	0	KN2[2]	KN2[1]	KN2[0]	xx												
9 th Parameter	1	1	↑	x	0	KN5[2]	KN5[1]	KN5[0]	0	KN4[2]	KN4[1]	KN4[0]	xx												
10 th Parameter	1	1	↑	x	0	RN1[2]	RN1[1]	RN1[0]	0	RN0[2]	RN0[1]	RN0[0]	xx												
11 th Parameter	1	1	↑	x	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	xx												
12 th Parameter	1	1	↑	x	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	xx												
Description	KP5-0[2:0] : yfine adjustment register for positive polarity RP1-0[2:0] : ygradient adjustment register for positive polarity VRP1-0[4:0] : yamplitude adjustment register for positive polarity KN5-0[2:0] : yfine adjustment register for negative polarity RN1-0[2:0] : ygradient adjustment register for negative polarity VRN1-0[4:0] : yamplitude adjustment register for negative polarity																								
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Status	Default Value																								
Power On Sequence	All the parameters are 00h																								
SW Reset	No change																								
HW Reset	All the parameters are 00h																								

8.2.47. Power_Setting (D0h)

D0H	Power_Setting																																																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																			
Command	0	1	↑	x	1	1	0	1	0	0	0	0	D0																																																			
1 st Parameter	1	1	↑	x	0	0	0	0	0	VC[2]	VC[1]	VC[0]	xx																																																			
2 nd Parameter	1	1	↑	x	0	PON	0	0	0	BT[2]	BT[1]	BT[0]	xx																																																			
3 rd Parameter	1	1	↑	x	0	0	0	VCIRE	VRH[3]	VRH[2]	VRH[1]	VRH[0]	xx																																																			
Description	VC[2:0] Sets the ratio factor of Vci to generate the reference voltages Vci1. <table border="1"> <thead> <tr> <th>VC[2:0]</th> <th>Vci1 voltage</th> </tr> </thead> <tbody> <tr><td>3'h0</td><td>Stop Output</td></tr> <tr><td>3'h1</td><td>0.70 x Vci</td></tr> <tr><td>3'h2</td><td>0.75 x Vci</td></tr> <tr><td>3'h3</td><td>0.80 x Vci</td></tr> <tr><td>3'h4</td><td>0.85 x Vci</td></tr> <tr><td>3'h5</td><td>0.90 x Vci</td></tr> <tr><td>3'h6</td><td>0.95 x Vci</td></tr> <tr><td>3'h7</td><td>1.0 x Vci</td></tr> </tbody> </table> BT[2:0] Sets the Step up factor and output voltage level from the reference voltages Vci1. <table border="1"> <thead> <tr> <th>BT[2:0]</th> <th>DDVDH</th> <th>VCL</th> <th>VGH</th> <th>VGL</th> </tr> </thead> <tbody> <tr><td>3'h0</td><td>Vci1 x 2</td><td>- Vci1</td><td rowspan="3">Vci1 x 6</td><td>- Vci1 x 5</td></tr> <tr><td>3'h1</td><td rowspan="2">Vci1 x 2</td><td colspan="2" rowspan="2">- Vci1</td><td>- Vci1 x 4</td></tr> <tr><td>3'h2</td><td>- Vci1 x 3</td></tr> <tr><td>3'h3</td><td rowspan="3">Vci1 x 2</td><td rowspan="3">- Vci1</td><td rowspan="3">Vci1 x 5</td><td>- Vci1 x 5</td></tr> <tr><td>3'h4</td><td>- Vci1 x 4</td></tr> <tr><td>3'h5</td><td>- Vci1 x 3</td></tr> <tr><td>3'h6</td><td rowspan="2">Vci1 x 2</td><td rowspan="6">- Vci1</td><td rowspan="6">Vci1 x 4</td><td>- Vci1 x 4</td></tr> <tr><td>3'h7</td><td>- Vci1 x 3</td></tr> </tbody> </table> Note 1: Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages. Note 2: Set following voltages within the respective ranges: DDVDH = 6.0V (max) VGH = 18.0V (max) VGL= -12.5V (max) VCL= -3.0V (max).													VC[2:0]	Vci1 voltage	3'h0	Stop Output	3'h1	0.70 x Vci	3'h2	0.75 x Vci	3'h3	0.80 x Vci	3'h4	0.85 x Vci	3'h5	0.90 x Vci	3'h6	0.95 x Vci	3'h7	1.0 x Vci	BT[2:0]	DDVDH	VCL	VGH	VGL	3'h0	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 5	3'h1	Vci1 x 2	- Vci1		- Vci1 x 4	3'h2	- Vci1 x 3	3'h3	Vci1 x 2	- Vci1	Vci1 x 5	- Vci1 x 5	3'h4	- Vci1 x 4	3'h5	- Vci1 x 3	3'h6	Vci1 x 2	- Vci1	Vci1 x 4	- Vci1 x 4	3'h7	- Vci1 x 3
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PON is used to control the operation to generate VLOUT3. PON=0: Halts the step-up operation to generate VLOUT3. PON=1: Starts the step-up operation to generate VLOUT3.																																																																
VRH[3:0]: Sets the factor to generate VREG1OUT from VCILVL.																																																																
VCIRE: Select the external reference voltage Vci or internal reference voltage VCIR.																																																																
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	VRH3	VRH2	VRH1	VRH0	VREG1OUT	VRH3	VRH2	VRH1	VRH0	VREG1OUT
	0	0	0	0	Halt	0	0	0	0	Halt
	0	0	0	1	Vci x 1.60	0	0	0	1	2.5V x 1.60 = 4.000V
	0	0	1	0	Vci x 1.65	0	0	1	0	2.5V x 1.65 = 4.125V
	0	0	1	1	Vci x 1.70	0	0	1	1	2.5V x 1.70 = 4.250V
	0	1	0	0	Vci x 1.75	0	1	0	0	2.5V x 1.75 = 4.375V
	0	1	0	1	Vci x 1.80	0	1	0	1	2.5V x 1.80 = 4.500V
	0	1	1	0	Vci x 1.85	0	1	1	0	2.5V x 1.85 = 4.625V
	0	1	1	1	Vci x 1.90	0	1	1	1	2.5V x 1.90 = 4.750V
	1	0	0	0	Vci x 1.95	1	0	0	0	2.5V x 1.95 = 4.875V
	1	0	0	1	Vci x 2.00	1	0	0	1	2.5V x 2.00 = 5.000V
	1	0	1	0	Vci x 2.05	1	0	1	0	2.5V x 2.05 = 5.125V
	1	0	1	1	Vci x 2.10	1	0	1	1	2.5V x 2.10 = 5.250V
	1	1	0	0	Vci x 2.20	1	1	0	0	2.5V x 2.20 = 5.500V
	1	1	0	1	Vci x 2.30	1	1	0	1	2.5V x 2.30 = 5.750V
	1	1	1	0	Vci x 2.40	1	1	1	0	2.5V x 2.40 = 6.000V
	1	1	1	1	Vci x 2.40	1	1	1	1	2.5V x 2.40 = 6.000V

When VCI<2.5V, Internal reference voltage will be same as VCI.

Make sure that VC[2:0] and VRH[3:0] setting restriction: VREG1OUT \leq (DDVDH - 0.25)V.

Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	

Default	Status	Default Value
	Power On Sequence	VC[2:0]=3'h0, BT[2:0]=3'h5, VCOMG=1'h0, PON=1'h0; VRH[3:0]=4'h0, VCIRE=1'h0,
	SW Reset	No change
	HW Reset	VC[2:0]=3'h0, BT[2:0]=3'h5, VCOMG=1'h0, PON=1'h0; VRH[3:0]=4'h0, VCIRE=1'h0,

8.2.48. VCOM Control (D1h)

D1H	VCOM Control																																																																																																																																																																										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																														
Command	0	1	↑	x	1	1	0	1	0	0	0	1	D1																																																																																																																																																														
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SEL VCM	xx																																																																																																																																																														
2 nd Parameter	1	1	↑	x	0	0	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	xx																																																																																																																																																														
3 rd Parameter	1	1	↑	x	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	xx																																																																																																																																																														
Description	<p>VCM [6:0] is used to set factor to generate VCOMH voltage from the reference voltage VREG1OUT.</p> <table border="1"> <thead> <tr> <th>VCM</th> <th>VCOMH Voltage</th> </tr> </thead> <tbody> <tr><td>6'h00</td><td>VREG1OUT x 0.685</td></tr> <tr><td>6'h01</td><td>VREG1OUT x 0.690</td></tr> <tr><td>6'h02</td><td>VREG1OUT x 0.695</td></tr> <tr><td>6'h03</td><td>VREG1OUT x 0.700</td></tr> <tr><td>6'h04</td><td>VREG1OUT x 0.705</td></tr> <tr><td>6'h05</td><td>VREG1OUT x 0.710</td></tr> <tr><td>6'h06</td><td>VREG1OUT x 0.715</td></tr> <tr><td>6'h07</td><td>VREG1OUT x 0.720</td></tr> <tr><td>6'h08</td><td>VREG1OUT x 0.725</td></tr> <tr><td>6'h09</td><td>VREG1OUT x 0.730</td></tr> <tr><td>6'h0A</td><td>VREG1OUT x 0.735</td></tr> <tr><td>6'h0B</td><td>VREG1OUT x 0.740</td></tr> <tr><td>6'h0C</td><td>VREG1OUT x 0.745</td></tr> <tr><td>6'h0D</td><td>VREG1OUT x 0.750</td></tr> <tr><td>6'h0E</td><td>VREG1OUT x 0.755</td></tr> <tr><td>6'h0F</td><td>VREG1OUT x 0.760</td></tr> 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1.08</td></tr> <tr><td>5'h04</td><td>VREG1OUT x 0.78</td><td>5'h14</td><td>VREG1OUT x 1.10</td></tr> <tr><td>5'h05</td><td>VREG1OUT x 0.80</td><td>5'h15</td><td>VREG1OUT x 1.12</td></tr> </tbody> </table>													VCM	VCOMH Voltage	6'h00	VREG1OUT x 0.685	6'h01	VREG1OUT x 0.690	6'h02	VREG1OUT x 0.695	6'h03	VREG1OUT x 0.700	6'h04	VREG1OUT x 0.705	6'h05	VREG1OUT x 0.710	6'h06	VREG1OUT x 0.715	6'h07	VREG1OUT x 0.720	6'h08	VREG1OUT x 0.725	6'h09	VREG1OUT x 0.730	6'h0A	VREG1OUT x 0.735	6'h0B	VREG1OUT x 0.740	6'h0C	VREG1OUT x 0.745	6'h0D	VREG1OUT x 0.750	6'h0E	VREG1OUT x 0.755	6'h0F	VREG1OUT x 0.760	6'h10	VREG1OUT x 0.765	6'h11	VREG1OUT x 0.770	6'h12	VREG1OUT x 0.775	6'h13	VREG1OUT x 0.780	6'h14	VREG1OUT x 0.785	6'h15	VREG1OUT x 0.790	6'h16	VREG1OUT x 0.795	6'h17	VREG1OUT x 0.800	6'h18	VREG1OUT x 0.805	6'h19	VREG1OUT x 0.810	6'h1A	VREG1OUT x 0.815	6'h1B	VREG1OUT x 0.820	6'h1C	VREG1OUT x 0.825	6'h1D	VREG1OUT x 0.830	6'h1E	VREG1OUT x 0.835	6'h1F	VREG1OUT x 0.840	6'h20	VREG1OUT x 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6'h27	VREG1OUT x 0.880																																																																																																																																																																										
6'h28	VREG1OUT x 0.885																																																																																																																																																																										
6'h29	VREG1OUT x 0.890																																																																																																																																																																										
6'h2A	VREG1OUT x 0.895																																																																																																																																																																										
6'h2B	VREG1OUT x 0.900																																																																																																																																																																										
6'h2C	VREG1OUT x 0.905																																																																																																																																																																										
6'h2D	VREG1OUT x 0.910																																																																																																																																																																										
6'h2E	VREG1OUT x 0.915																																																																																																																																																																										
6'h2F	VREG1OUT x 0.920																																																																																																																																																																										
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6'h31	VREG1OUT x 0.930																																																																																																																																																																										
6'h32	VREG1OUT x 0.935																																																																																																																																																																										
6'h33	VREG1OUT x 0.940																																																																																																																																																																										
6'h34	VREG1OUT x 0.945																																																																																																																																																																										
6'h35	VREG1OUT x 0.950																																																																																																																																																																										
6'h36	VREG1OUT x 0.955																																																																																																																																																																										
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6'h3E	VREG1OUT x 0.995																																																																																																																																																																										
6'h3F	VREG1OUT x 1.000																																																																																																																																																																										
VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude																																																																																																																																																																								
5'h00	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02																																																																																																																																																																								
5'h01	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04																																																																																																																																																																								
5'h02	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06																																																																																																																																																																								
5'h03	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08																																																																																																																																																																								
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		<table border="1"> <tr><td>5'h06</td><td>VREG1OUT x 0.82</td><td>5'h16</td><td>VREG1OUT x 1.14</td></tr> <tr><td>5'h07</td><td>VREG1OUT x 0.84</td><td>5'h17</td><td>VREG1OUT x 1.16</td></tr> <tr><td>5'h08</td><td>VREG1OUT x 0.86</td><td>5'h18</td><td>VREG1OUT x 1.18</td></tr> <tr><td>5'h09</td><td>VREG1OUT x 0.88</td><td>5'h19</td><td>VREG1OUT x 1.20</td></tr> <tr><td>5'h0A</td><td>VREG1OUT x 0.90</td><td>5'h1A</td><td>VREG1OUT x 1.22</td></tr> <tr><td>5'h0B</td><td>VREG1OUT x 0.92</td><td>5'h1B</td><td>VREG1OUT x 1.24</td></tr> <tr><td>5'h0C</td><td>VREG1OUT x 0.94</td><td>5'h1C</td><td>VREG1OUT x 1.26</td></tr> <tr><td>5'h0D</td><td>VREG1OUT x 0.96</td><td>5'h1D</td><td>VREG1OUT x 1.28</td></tr> <tr><td>5'h0E</td><td>VREG1OUT x 0.98</td><td>5'h1E</td><td>VREG1OUT x 1.30</td></tr> <tr><td>5'h0F</td><td>VREG1OUT x 1.00</td><td>5'h1F</td><td>VREG1OUT x 1.32</td></tr> </table>	5'h06	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14	5'h07	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16	5'h08	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18	5'h09	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20	5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.22	5'h0B	VREG1OUT x 0.92	5'h1B	VREG1OUT x 1.24	5'h0C	VREG1OUT x 0.94	5'h1C	VREG1OUT x 1.26	5'h0D	VREG1OUT x 0.96	5'h1D	VREG1OUT x 1.28	5'h0E	VREG1OUT x 0.98	5'h1E	VREG1OUT x 1.30	5'h0F	VREG1OUT x 1.00	5'h1F	VREG1OUT x 1.32	
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Set VDV[4:0] to let VCOM amplitude less than 6V.																																											
SELVCM: Selection the VCM setting.																																											
		<table border="1"> <tr><td>SELVCM =0</td><td>Register D1h for VCM setting</td></tr> <tr><td>SELVCM =1</td><td>NV Memory selected for VCM setting</td></tr> </table>	SELVCM =0	Register D1h for VCM setting	SELVCM =1	NV Memory selected for VCM setting																																					
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Default		<table border="1"> <thead> <tr><th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>VCM[6:0]=7'h00, VDV[4:0]=5'h00, SELVCM=1'h0</td></tr> <tr><td>SW Reset</td><td>No change</td></tr> <tr><td>HW Reset</td><td>VCM[6:0]=7'h00, VDV[4:0]=5'h00, SELVCM=1'h0</td></tr> </tbody> </table> <p>Note: When the VCM NV memory had been programmed, the default value of SELVCM will be set as '1'.</p>	Status	Default Value	Power On Sequence	VCM[6:0]=7'h00, VDV[4:0]=5'h00, SELVCM=1'h0	SW Reset	No change	HW Reset	VCM[6:0]=7'h00, VDV[4:0]=5'h00, SELVCM=1'h0																																	
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8.2.49. Power_Setting for Normal Mode (D2h)

D2H	Power_Setting for Normal Mode																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	1	1	0	1	0	0	1	0	D2																										
1 st Parameter	1	1	↑	x	0	0	0	0	0	AP0[2]	AP0[1]	AP0[0]	xx																										
2 nd Parameter	1	1	↑	x	0	DC10[2]	DC10[1]	DC10[0]	0	DC00[2]	DC00[1]	DC00[0]	xx																										
Description	AP0[2:0]																																						
	AP0 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.																																						
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AP0[2:0]	Gamma Driver Amplifier	Source Driver Amplifier																																					
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DC00[1:0]	Step-up circuit 1 clock frequency (fDCDC1)																																						
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<table border="1"> <thead> <tr> <th>DC10[1:0]</th><th>Step-up circuit 2 clock frequency (fDCDC2)</th></tr> </thead> <tbody> <tr><td>2'h0</td><td>Fosc / 16</td></tr> <tr><td>2'h1</td><td>Fosc / 32</td></tr> <tr><td>2'h2</td><td>Fosc / 64</td></tr> <tr><td>2'h3</td><td>Fosc / 128</td></tr> <tr><td>2'h4</td><td>Fosc / 256</td></tr> <tr><td>2'h5</td><td>Fosc / 512</td></tr> <tr><td>2'h6</td><td>Setting inhibited</td></tr> <tr><td>2'h7</td><td>Halt step-up circuit 2</td></tr> </tbody> </table>													DC10[1:0]	Step-up circuit 2 clock frequency (fDCDC2)	2'h0	Fosc / 16	2'h1	Fosc / 32	2'h2	Fosc / 64	2'h3	Fosc / 128	2'h4	Fosc / 256	2'h5	Fosc / 512	2'h6	Setting inhibited	2'h7	Halt step-up circuit 2									
DC10[1:0]	Step-up circuit 2 clock frequency (fDCDC2)																																						
2'h0	Fosc / 16																																						
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Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>AP0[2:0]=3'h0, DC10[2:0]=3'h7, DC00[2:0]=3'h7</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>AP0[2:0]=3'h0, DC10[2:0]=3'h7, DC00[2:0]=3'h7</td></tr></tbody></table>	Status	Default Value	Power On Sequence	AP0[2:0]=3'h0, DC10[2:0]=3'h7, DC00[2:0]=3'h7	SW Reset	No change	HW Reset	AP0[2:0]=3'h0, DC10[2:0]=3'h7, DC00[2:0]=3'h7
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Power On Sequence	AP0[2:0]=3'h0, DC10[2:0]=3'h7, DC00[2:0]=3'h7								
SW Reset	No change								
HW Reset	AP0[2:0]=3'h0, DC10[2:0]=3'h7, DC00[2:0]=3'h7								

8.2.50. Power_Setting for Partial Mode (D3h)

D3H	Power_Setting for Partial Mode																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	1	1	0	1	0	0	1	1	D3																										
1 st Parameter	1	1	↑	x	0	0	0	0	0	AP1[2]	AP1[1]	AP1[0]	xx																										
2 nd Parameter	1	1	↑	x	0	DC11[2]	DC11[1]	DC11[0]	0	DC01[2]	DC01[1]	DC01[0]	xx																										
Description	AP1[2:0]																																						
	AP1 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP1=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.																																						
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2'h2	Fosc / 64																																						
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2'h4	Fosc / 256																																						
2'h5	Fosc / 512																																						
2'h6	Setting inhibited																																						
2'h7	Halt step-up circuit 2																																						
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Status	Availability																																						
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																						
Sleep In	Yes																																						

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Default	Status	Default Value
	Power On Sequence	AP1[2:0]=3'h0, DC11[2:0]=3'h7, DC01[2:0]=3'h7
	SW Reset	No change
	HW Reset	AP1[2:0]=3'h0, DC11[2:0]=3'h7, DC01[2:0]=3'h7

8.2.51. Power_Setting for Idle Mode (D4h)

D4H		Power_Setting for Idle Mode																																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	x	1	1	0	1	0	1	0	0	0	D4																											
1 st Parameter	1	1	↑	x	0	0	0	0	0	AP2[2]	AP2[1]	AP2[0]	xx																												
2 nd Parameter	1	1	↑	x	0	DC12[2]	DC12[1]	DC12[0]	0	DC02[2]	DC02[1]	DC02[0]	xx																												
Description	AP2[2:0]		AP2 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP2=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.																																						
			<table border="1"> <thead> <tr> <th>AP2[2:0]</th><th>Gamma Driver Amplifier</th><th>Source Driver Amplifier</th></tr> </thead> <tbody> <tr> <td>3'h0</td><td>Halt operation</td><td>Halt operation</td></tr> <tr> <td>3'h1</td><td>1.00</td><td>1.00</td></tr> <tr> <td>3'h2</td><td>1.00</td><td>0.75</td></tr> <tr> <td>3'h3</td><td>1.00</td><td>0.50</td></tr> <tr> <td>3'h4</td><td>0.75</td><td>1.00</td></tr> <tr> <td>3'h5</td><td>0.75</td><td>0.75</td></tr> <tr> <td>3'h6</td><td>0.75</td><td>0.50</td></tr> <tr> <td>3'h7</td><td>0.50</td><td>0.50</td></tr> </tbody> </table>													AP2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier	3'h0	Halt operation	Halt operation	3'h1	1.00	1.00	3'h2	1.00	0.75	3'h3	1.00	0.50	3'h4	0.75	1.00	3'h5	0.75	0.75	3'h6	0.75	0.50	3'h7	0.50
AP2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier																																							
3'h0	Halt operation	Halt operation																																							
3'h1	1.00	1.00																																							
3'h2	1.00	0.75																																							
3'h3	1.00	0.50																																							
3'h4	0.75	1.00																																							
3'h5	0.75	0.75																																							
3'h6	0.75	0.50																																							
3'h7	0.50	0.50																																							
DC02[2:0], DC12[2:0]		DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2.																																							
		<table border="1"> <thead> <tr> <th>DC02[1:0]</th><th>Step-up circuit 1 clock frequency (fDCDC1)</th></tr> </thead> <tbody> <tr> <td>2'h0</td><td>Fosc</td></tr> <tr> <td>2'h1</td><td>Fosc / 2</td></tr> <tr> <td>2'h2</td><td>Fosc / 4</td></tr> <tr> <td>2'h3</td><td>Fosc / 8</td></tr> <tr> <td>2'h4</td><td>Fosc / 16</td></tr> <tr> <td>2'h5</td><td>Fosc / 32</td></tr> <tr> <td>2'h6</td><td>Fosc / 64</td></tr> <tr> <td>2'h7</td><td>Halt step-up circuit 1</td></tr> </tbody> </table>												DC02[1:0]	Step-up circuit 1 clock frequency (fDCDC1)	2'h0	Fosc	2'h1	Fosc / 2	2'h2	Fosc / 4	2'h3	Fosc / 8	2'h4	Fosc / 16	2'h5	Fosc / 32	2'h6	Fosc / 64	2'h7	Halt step-up circuit 1										
DC02[1:0]	Step-up circuit 1 clock frequency (fDCDC1)																																								
2'h0	Fosc																																								
2'h1	Fosc / 2																																								
2'h2	Fosc / 4																																								
2'h3	Fosc / 8																																								
2'h4	Fosc / 16																																								
2'h5	Fosc / 32																																								
2'h6	Fosc / 64																																								
2'h7	Halt step-up circuit 1																																								
		<table border="1"> <thead> <tr> <th>DC12[1:0]</th><th>Step-up circuit 2 clock frequency (fDCDC2)</th></tr> </thead> <tbody> <tr> <td>2'h0</td><td>Fosc / 16</td></tr> <tr> <td>2'h1</td><td>Fosc / 32</td></tr> <tr> <td>2'h2</td><td>Fosc / 64</td></tr> <tr> <td>2'h3</td><td>Fosc / 128</td></tr> <tr> <td>2'h4</td><td>Fosc / 256</td></tr> <tr> <td>2'h5</td><td>Fosc / 512</td></tr> <tr> <td>2'h6</td><td>Setting inhibited</td></tr> <tr> <td>2'h7</td><td>Halt step-up circuit 2</td></tr> </tbody> </table>													DC12[1:0]	Step-up circuit 2 clock frequency (fDCDC2)	2'h0	Fosc / 16	2'h1	Fosc / 32	2'h2	Fosc / 64	2'h3	Fosc / 128	2'h4	Fosc / 256	2'h5	Fosc / 512	2'h6	Setting inhibited	2'h7	Halt step-up circuit 2									
DC12[1:0]	Step-up circuit 2 clock frequency (fDCDC2)																																								
2'h0	Fosc / 16																																								
2'h1	Fosc / 32																																								
2'h2	Fosc / 64																																								
2'h3	Fosc / 128																																								
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Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>AP2[2:0]=3'h0, DC12[2:0]=3'h7, DC02[2:0]=3'h7</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>AP2[2:0]=3'h0, DC11[2:0]=3'h7, DC02[2:0]=3'h7</td></tr></tbody></table>	Status	Default Value	Power On Sequence	AP2[2:0]=3'h0, DC12[2:0]=3'h7, DC02[2:0]=3'h7	SW Reset	No change	HW Reset	AP2[2:0]=3'h0, DC11[2:0]=3'h7, DC02[2:0]=3'h7
Status	Default Value								
Power On Sequence	AP2[2:0]=3'h0, DC12[2:0]=3'h7, DC02[2:0]=3'h7								
SW Reset	No change								
HW Reset	AP2[2:0]=3'h0, DC11[2:0]=3'h7, DC02[2:0]=3'h7								

8.2.52. NV Memory Write (E0h)

E0H		NV Memory Write																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	1	1	1	0	0	0	0	0	E0													
1 st Parameter	1	1	↑	x	VM_D [7]	VM_D [6]	VM_D [5]	VM_D [4]	VM_D [3]	VM_D [2]	VM_D [1]	VM_D [0]	xx													
Description	This command is used to program the NV memory data. VM_D[7:0]: Use to write the data (including VCM and ID code) into the NV memory data.																									
Restriction																										
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
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Sleep In	Yes																									
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>VCM_D[7:0]=8'h00</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>VCM_D[7:0]=8'h00</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	VCM_D[7:0]=8'h00	SW Reset	No change	HW Reset	VCM_D[7:0]=8'h00				
Status	Default Value																									
Power On Sequence	VCM_D[7:0]=8'h00																									
SW Reset	No change																									
HW Reset	VCM_D[7:0]=8'h00																									

8.2.53. NV Memory Control (E1h)

NV Memory Control																																						
E1H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																									
Command	0	1	↑	x	1	1	1	0	0	0	0	1	E1																									
1 st Parameter	1	1	↑	x	0	0	ID_PGM_EN	VCM_PGM_EN	0	0	ID_SEL[1]	ID_SEL[0]	xx																									
Description	This command is used to control the NV memory programming. ID_SEL[1:0]: ID NV memory selection <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>ID_SEL[1:0]</th> <th>ID OTP Selection</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>ID code 1 [15:8]</td> </tr> <tr> <td>01</td> <td>ID code 1 [7:0]</td> </tr> <tr> <td>10</td> <td>ID code 2 [15:8]</td> </tr> <tr> <td>11</td> <td>ID code 2 [7:0]</td> </tr> </tbody> </table> VCM_PGM_EN: VCM OTP programming enable. When writing the VCOMH NV memory, the bit must be set as '1'. ID_PGM_EN: ID OTP programming enable. When writing the ID code NV memory, the bit must be set as '1'. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>ID_PGM_EN</th> <th>VCM_PGM_EN</th> <th>OTP Programming Selection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>NV Memory programming disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>VCM (VCOMH) NV Memory programming enable</td> </tr> <tr> <td>1</td> <td>0</td> <td>ID code NV Memory programming enable</td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting Prohibited</td> </tr> </tbody> </table>													ID_SEL[1:0]	ID OTP Selection	00	ID code 1 [15:8]	01	ID code 1 [7:0]	10	ID code 2 [15:8]	11	ID code 2 [7:0]	ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection	0	0	NV Memory programming disabled	0	1	VCM (VCOMH) NV Memory programming enable	1	0	ID code NV Memory programming enable	1	1	Setting Prohibited
ID_SEL[1:0]	ID OTP Selection																																					
00	ID code 1 [15:8]																																					
01	ID code 1 [7:0]																																					
10	ID code 2 [15:8]																																					
11	ID code 2 [7:0]																																					
ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection																																				
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																																					
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Sleep In	Yes																																					
Default	<table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_AP[1:0]=2'h0</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_AP[1:0]=2'h0</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_AP[1:0]=2'h0	SW Reset	No change	HW Reset	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_AP[1:0]=2'h0																	
Status	Default Value																																					
Power On Sequence	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_AP[1:0]=2'h0																																					
SW Reset	No change																																					
HW Reset	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_AP[1:0]=2'h0																																					

8.2.54. NV Memory Status Read (E2h)

E2H		NV Memory Status Read																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	1	0	0	0	1	0	E2												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	x	0	0	0	0	0	0	PGM_CNT1	PGM_CNT0	xx												
3 rd Parameter	1	↑	1	x	0	0	NV_VCM[5]	NV_VCM[4]	NV_VCM[3]	NV_VCM[2]	NV_VCM[1]	NV_VCM[0]	xx												
Description	PGM_CNT[1:0]: NV memory programmed record. The bit will increase “+1” automatically when writing the NV_VCM [5:0]. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PGM_CNT[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>NV Memory clean</td> </tr> <tr> <td>01</td> <td>NV Memory programmed 1 time</td> </tr> <tr> <td>10</td> <td>NV Memory programmed 2 times</td> </tr> </tbody> </table> These bits are read only. NV_VCM [5:0]: NV memory VCM data read value. These bits are read only.													PGM_CNT[1:0]	Description	00	NV Memory clean	01	NV Memory programmed 1 time	10	NV Memory programmed 2 times				
PGM_CNT[1:0]	Description																								
00	NV Memory clean																								
01	NV Memory programmed 1 time																								
10	NV Memory programmed 2 times																								
Restriction																									
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

8.2.55. NV Memory Protection (E3h)

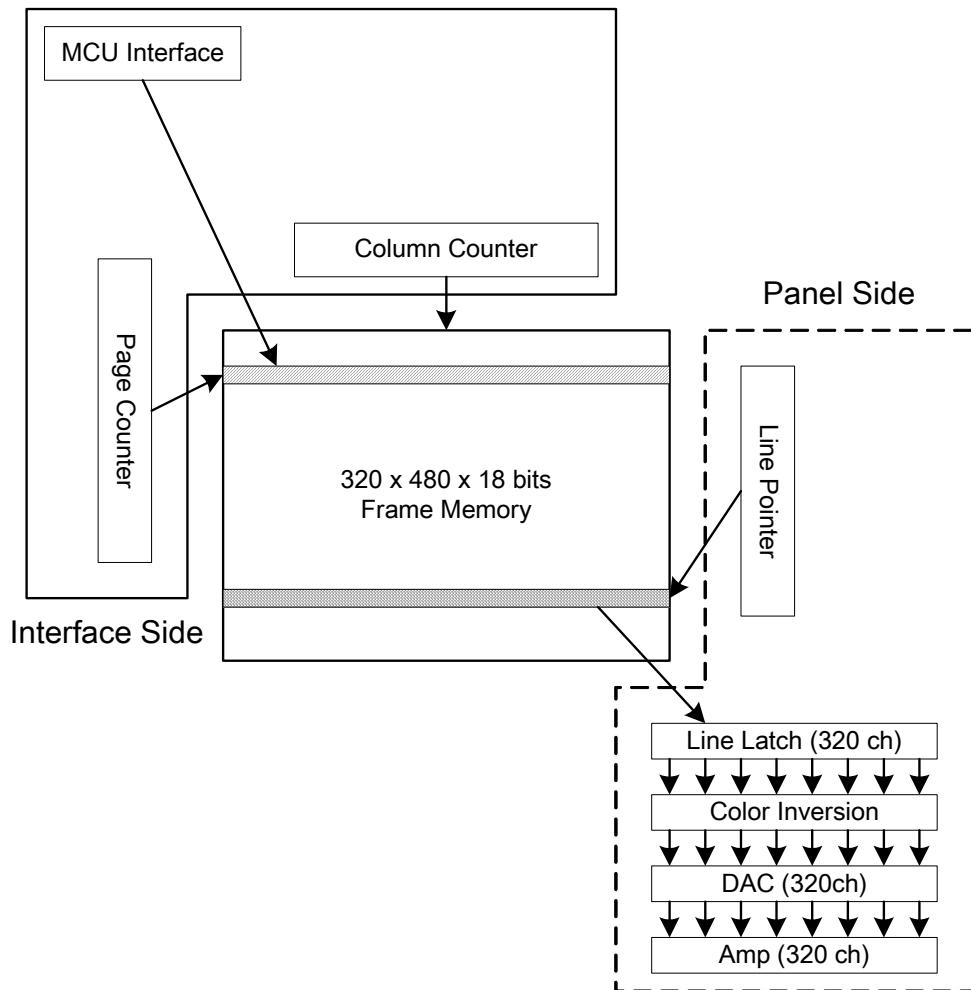
NV Memory Protection																									
E3H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	--	1	1	1	0	0	0	1	1	E3												
1 st Parameter	1	1	↑	--	KEY [15]	KEY [14]	KEY [13]	KEY [12]	KEY [11]	KEY [10]	KEY [9]	KEY [8]	xx												
2 nd Parameter	1	1	↑	--	KEY [7]	KEY [6]	KEY [5]	KEY [4]	KEY [3]	KEY [2]	KEY [1]	KEY [0]	xx												
Description	KEY[15:0]: NV memory programming protection key. When writing OTP data C8h, this register must be set as 0xAA55 to enable OTP programming. If C8h register is not written with 0xAA55, NV Memory programming will fail.																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>KEY[15:0]=16'h0000</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>KEY[15:0]=16'h0000</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	KEY[15:0]=16'h0000	SW Reset	No change	HW Reset	KEY[15:0]=16'h0000				
Status	Default Value																								
Power On Sequence	KEY[15:0]=16'h0000																								
SW Reset	No change																								
HW Reset	KEY[15:0]=16'h0000																								

9. Display Data RAM

9.1. Configuration

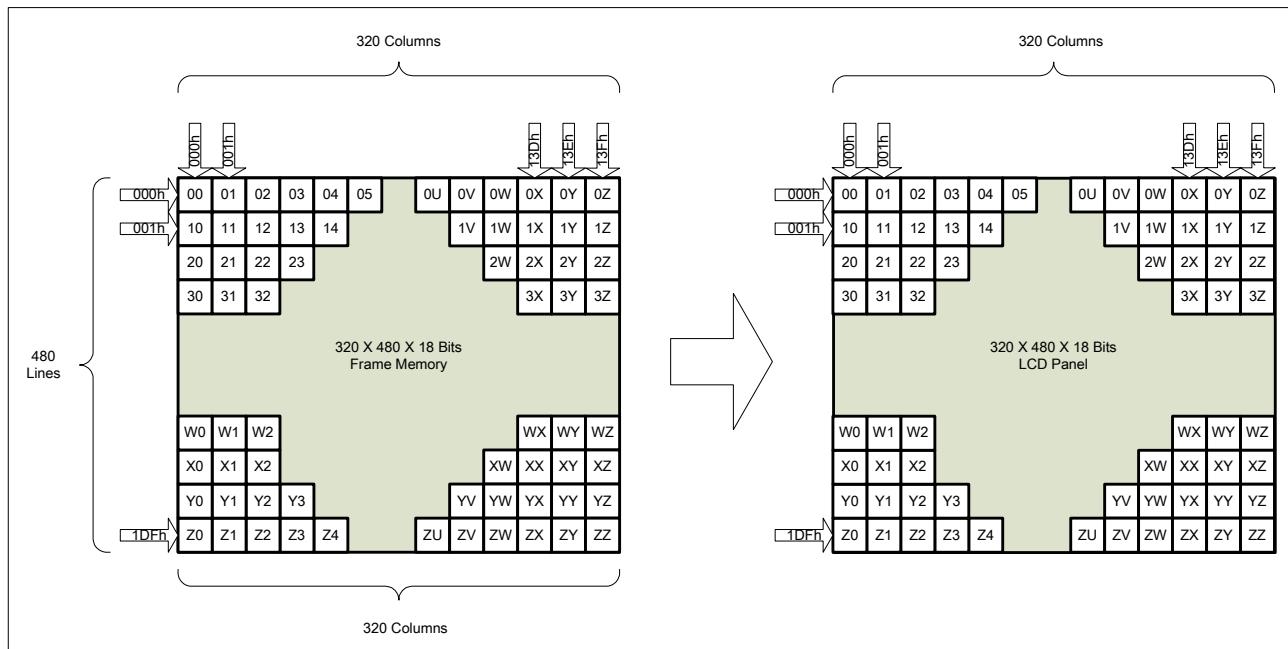
The display data RAM stores display dots and consists of 2,764,800bits (320 x 18 x 480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the frame memory.



9.2. Memory to Display Address Mapping

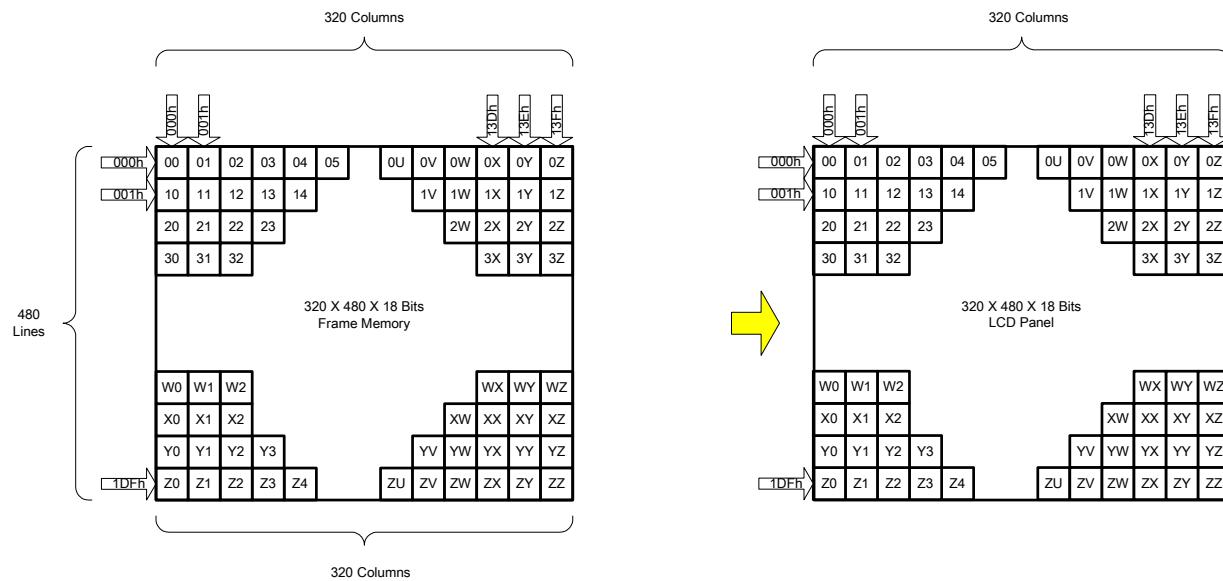
In this mode, content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer 0000h to 01DFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).



9.3. Vertical Scroll Mode

There is a vertical scrolling mode, which is described by the commands “set_scroll_area”(33h) and “set_scroll_start”(37h).

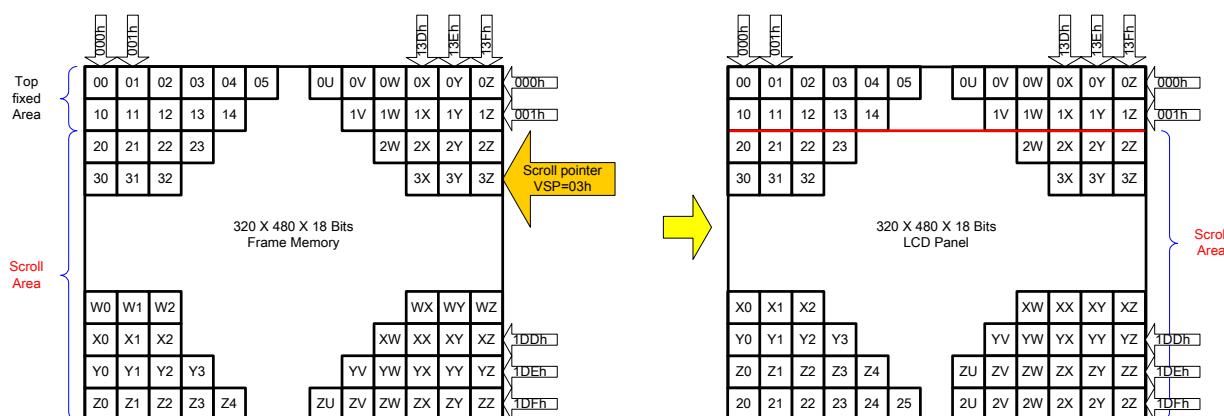
(1)Normal Display On or Partial Mode On, Vertical Scroll Off



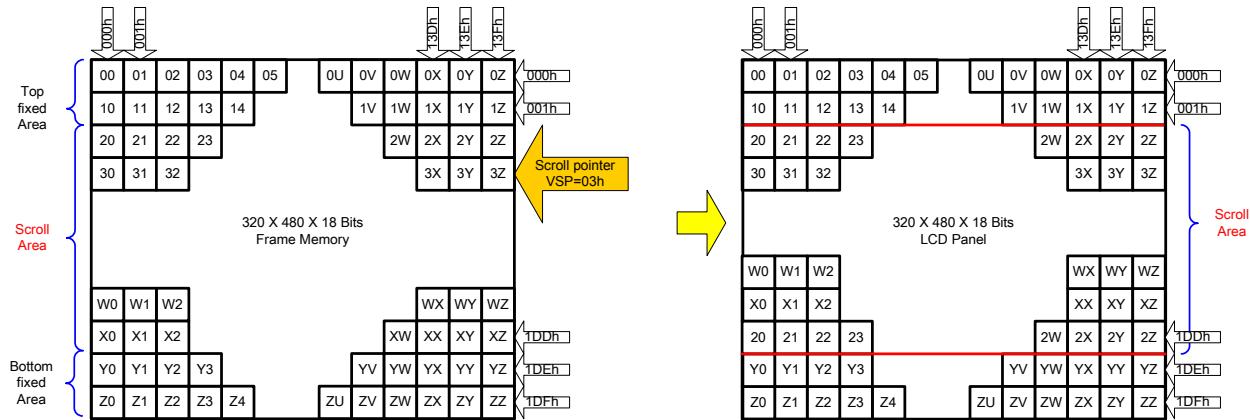
(2) Vertical Scroll Mode

“set_scroll_area(33h)”and “set_scroll_start(37h)” setting define the scroll area.

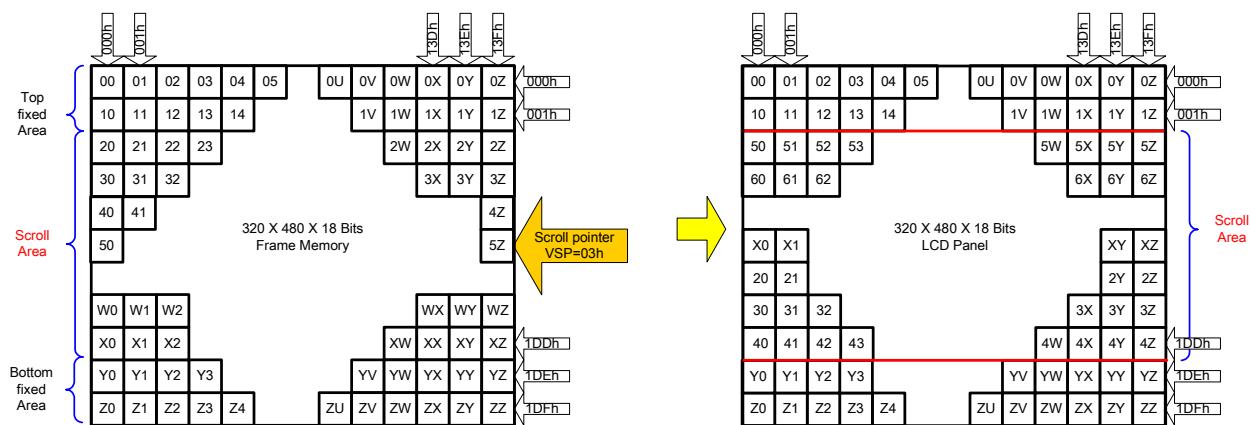
Example1: TFA=2, VSA=478, BFA=0 (set_address_mode(36h) B4=0), VSP=3



Example2: TFA=2,VSA=476,BFA=2 (set_address_mode(36h) B4=0), VSP=3



Example3: TFA=2,VSA=476,BFA=2 (set_address_mode(36h) B4=0), VSP=5



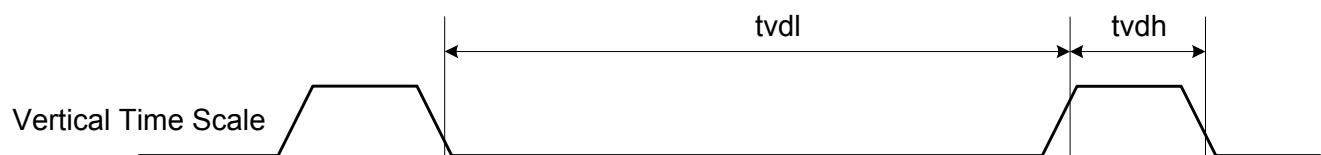
10. Tearing Effect Output

The tearing effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

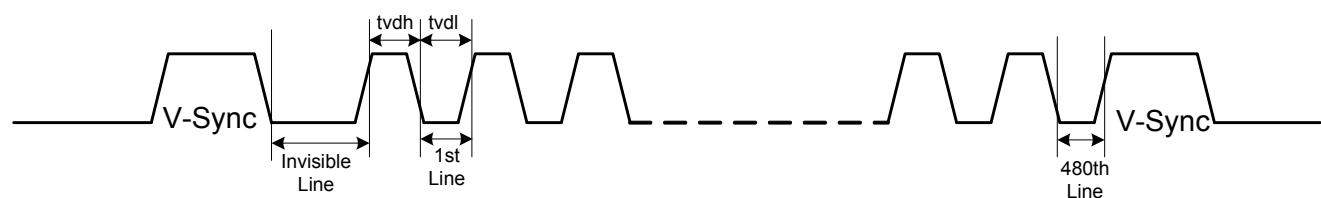
Mode 1 (set_tear_on, TELOM=0), the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

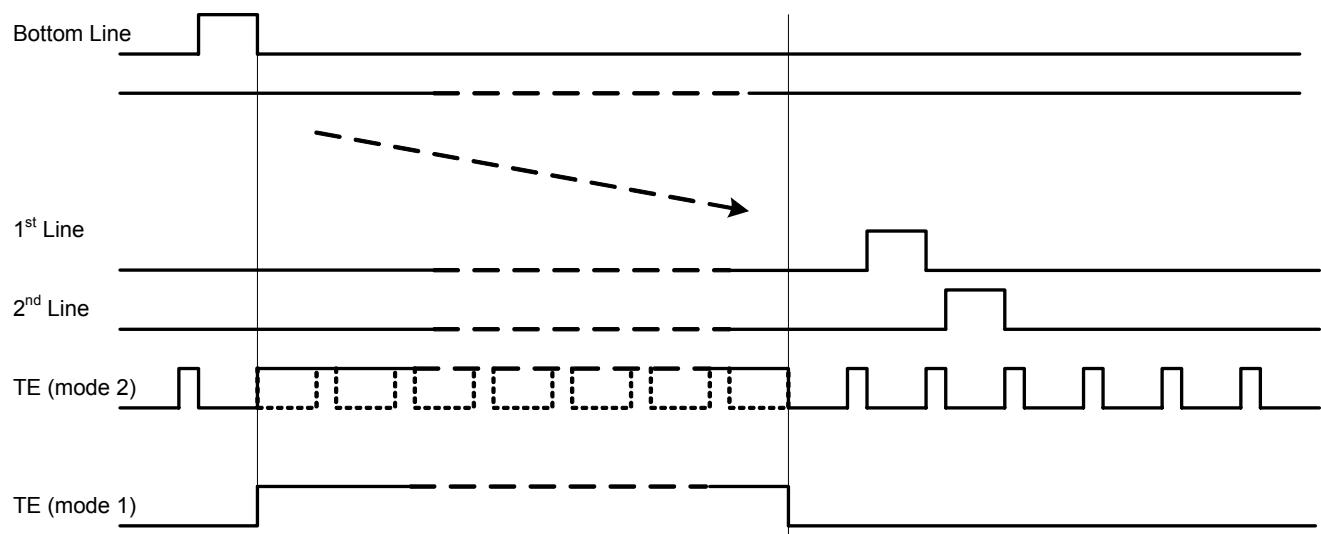
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2 (set_tear_on, TELOM=1), the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 480 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

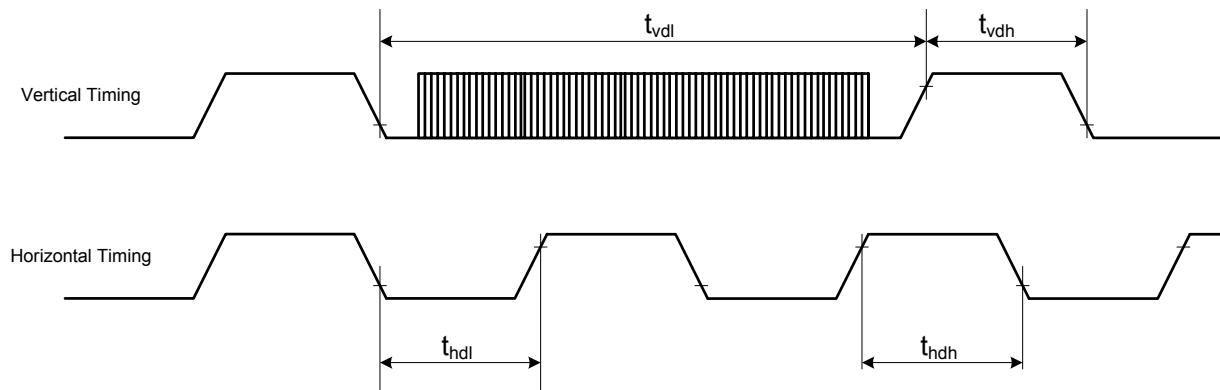
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

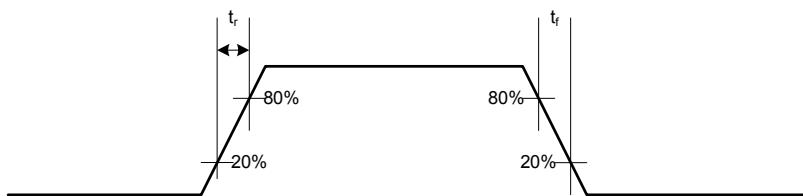


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdI}	Vertical timing low duration	TBD		ms	
t_{vdH}	Vertical timing high duration	TBD		us	
t_{hdl}	Horizontal timing low duration	TBD		us	
t_{hdH}	Horizontal timing high duration	TBD		us	

Notes:

1. The timings in Table 8.3.1 apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

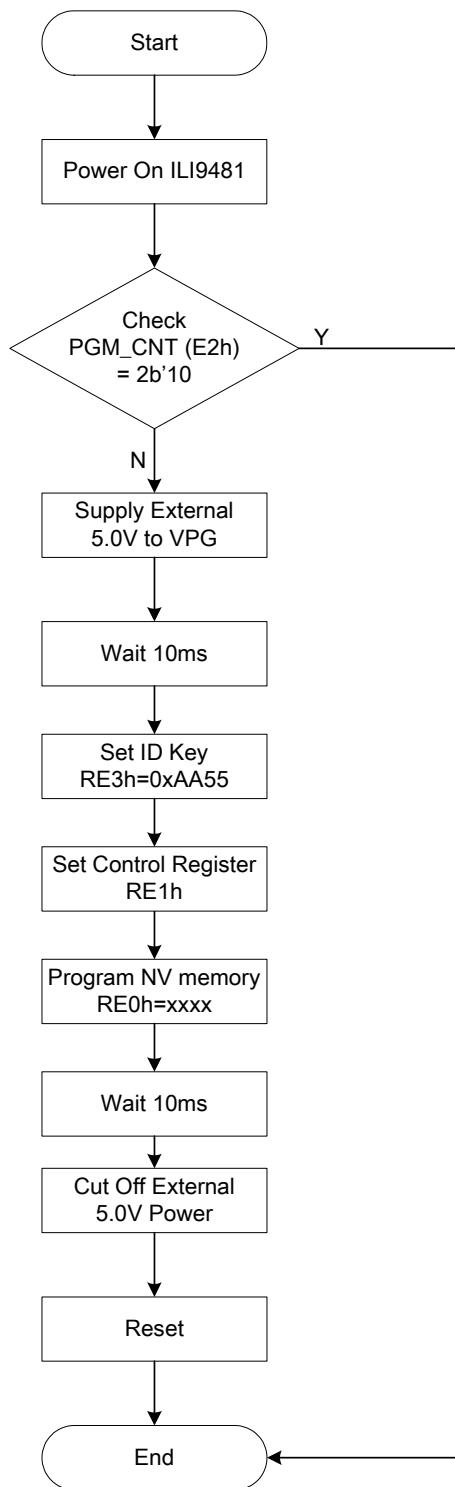


The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect:

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

TEON (35h)	TELOM (35h, 1 st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

11. NV Memory Programming Flow



12. Gamma Correction

ILI9481 incorporates the γ -correction function to display 262,144 colors for the LCD panel. The γ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9481 available with liquid crystal panels of various characteristics.

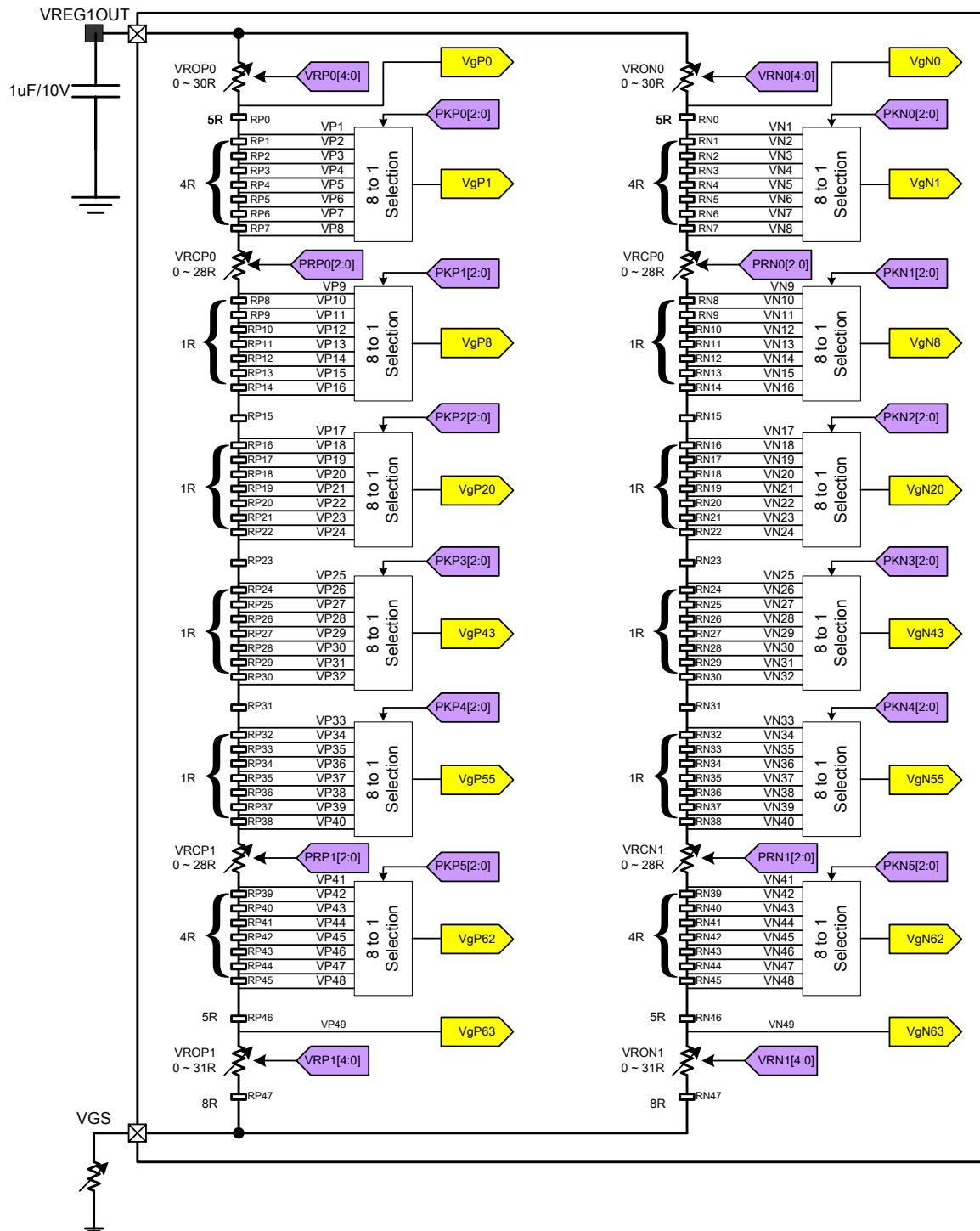


Figure 1 Grayscale Voltage Adjustment

13. Electrical Characteristics

13.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9481 is used out of the absolute maximum ratings, the ILI9481 may be permanently damaged. To use the ILI9481 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9481 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	VCC, IOVCC	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI - GND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	DDVDH - GND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	GND - VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	DDVDH - VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH - GND	V	-0.3 ~ + 18.5	1, 5
Power supply voltage (1)	GND - VGL	V	-0.3 ~ + 18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:

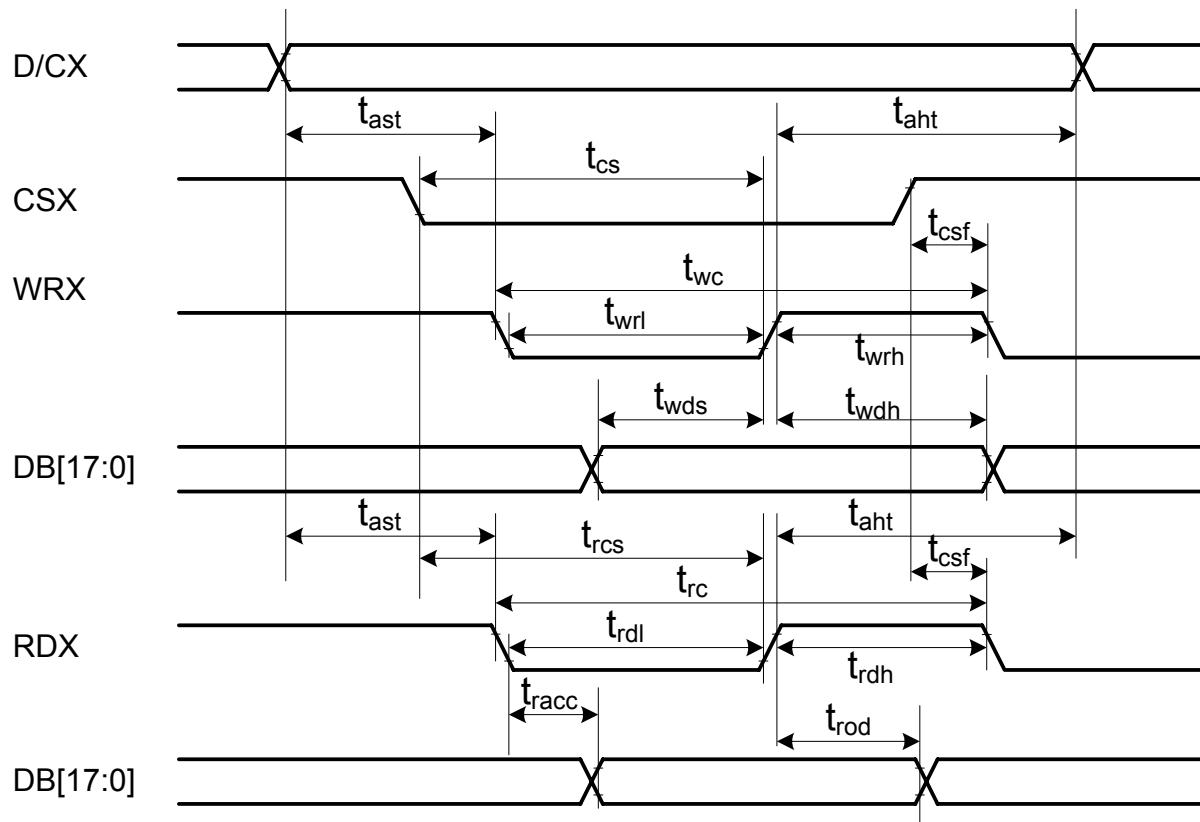
1. VCC,DGND must be maintained
2. (High) (VCC = VCC) \geq DGND (Low), (High) IOVCC \geq DGND (Low).
3. Make sure (High) VCI \geq DGND (Low).
4. Make sure (High) DDVDH \geq ASSD (Low).
5. Make sure (High) DDVDH \geq VCL (Low).
6. Make sure (High) VGH \geq ASSD (Low).
7. Make sure (High) ASSD \geq VGL (Low).
8. For die and wafer products, specified up to 85°C.
9. This temperature specifications apply to the TCP package

13.2. DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply Voltage	V _{CI}	Analog Operation Voltage	2.5	2.8	3.3	V
I/O pin Power Supply Voltage	IOVCC	I/O pin Operation Voltage	1.7	2.8	3.3	V
Logic High level input voltage	V _{IH}		0.7*IOVCC	-	IOVCC	V
Logic Low level input voltage	V _{IL}		0.0	-	0.3*IOVCC	V
Logic High level Output voltage	V _{IH}	Iout = -1 mA	0.8*IOVCC	-	IOVCC	V
Logic Low level Output voltage	V _{IL}	Iout = +1 mA	0.0	-	0.2*IOVCC	V
Logic High level input current	IIHD	D[17:0]			10	uA
Logic Low level input current	IILD	D[17:0]	-10			uA

13.3. AC Characteristics

13.3.1. DBI Type B (18/16/9/8 bit) Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	t _{ast}	Address setup time	0	-	ns	
	t _{taht}	Address hold time (Write/Read)	10	-	ns	
	t _{tcs}	Chip Select setup time (Write)	20	-	ns	
CSX	t _{trcs}	Chip Select setup time (Read)	170	-	ns	
	t _{tcsf}	Chip Select Wait time (Write/Read)	20	-	ns	
WRX	t _{tw}	Write cycle	80	-	ns	
	t _{twrh}	Write Control pulse H duration	35	-	ns	
	t _{wrl}	Write Control pulse L duration	35	-	ns	
RDX	t _{rc}	Read cycle	450	-	ns	

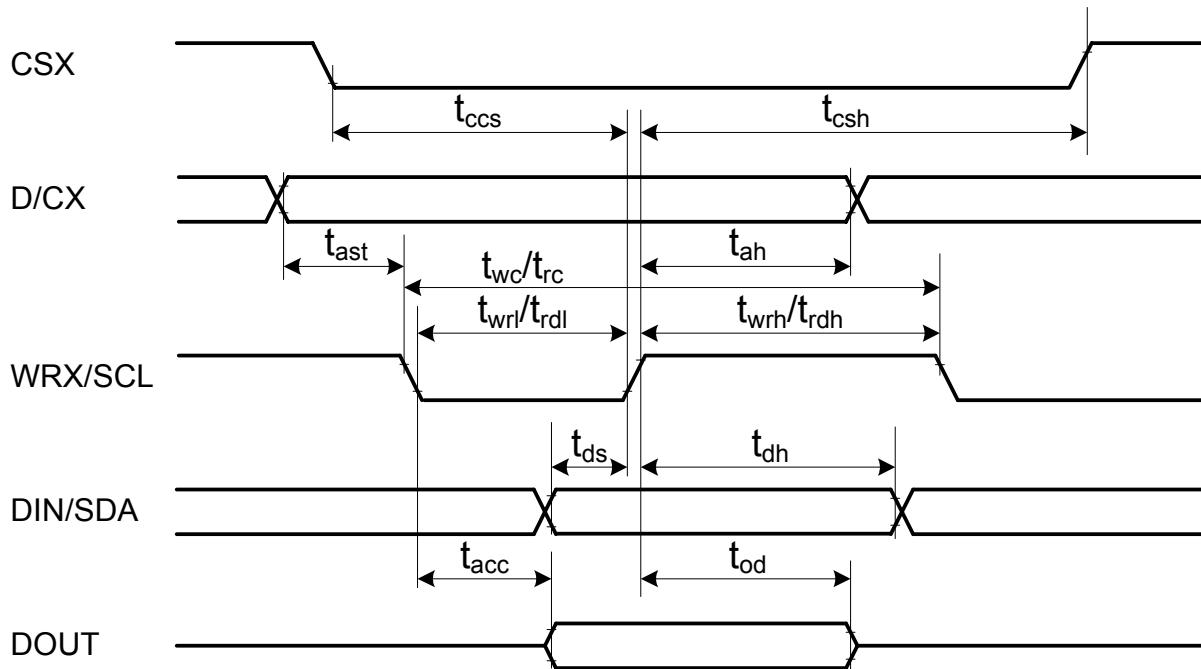
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	trdh	Read Control pulse H duration	250	-	ns	
	trdl	Read Control pulse L duration	170	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	twds	Write data setup time	15	-	ns	For maximum CL=30pF
	twdh	Write data hold time	25	-	ns	
	tracc	Read access time	10	340	ns	For minimum CL=8pF
	trod	Read output disable time	10	-	ns	

Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

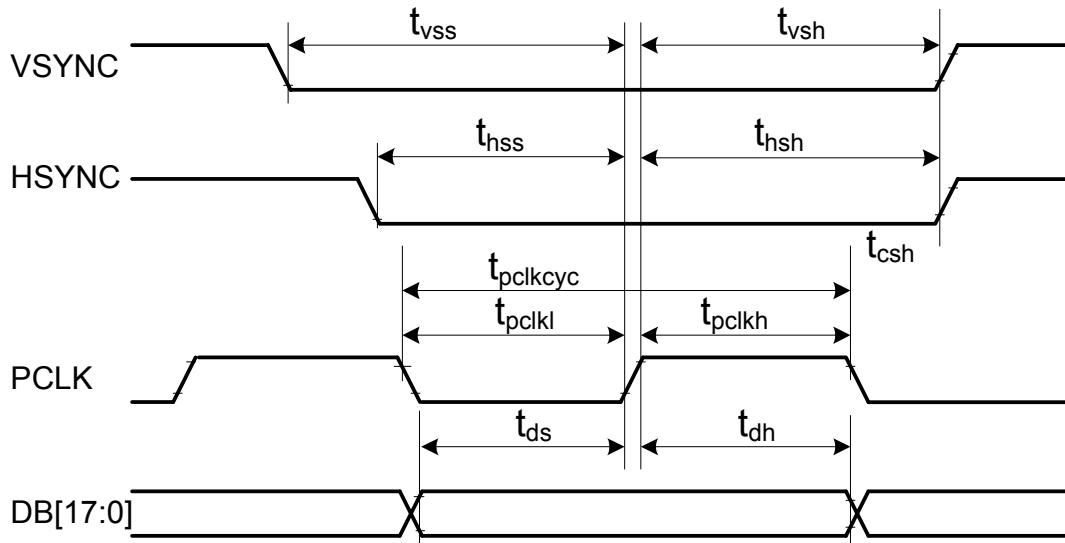
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VDD=2.5V to 3.0V, GND=0V

13.3.2. DBI Type C Interface Timing Characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{css}	Chip select setup time (Write)	40	-	ns	
	t_{csh}	Chip select hold time (Write)	40	-	ns	
D/CX	t_{as}	Address setup time	10		ns	
	t_{ah}	Address hold time (Write/Read)	10		ns	
WRX/SCL (Write)	t_{wc}	Write cycle	100		ns	
	t_{wrh}	SCL High duration (write)	40		ns	
	t_{wrl}	SCL Low duration (write)	40		ns	
WRX/SCL (Read)	t_{rc}	Read cycle	300		ns	
	t_{rdh}	SCL High duration (read)	120		ns	
	t_{rdl}	SCL Low duration (read)	120		ns	
DIN/SDA (Driver IC)	t_{ds}	Data setup time	30		ns	
	t_{dh}	Data hold time	30		ns	
DOUT (Driver IC)	t_{acc}	Access time	-	110	ns	
	t_{od}	Output disable time	10		ns	

13.3.3. DPI Interface Timing Characteristics



Parameter	Symbol	Condition	Min.	Max.	Unit
Vsync Setup Time	t_{vss}		15	-	ns
Vsync Hold Time	t_{vsh}		15	-	ns
Hsync Setup Time	t_{hss}		15	-	ns
Hsync Hold Time	t_{hsh}		15	-	ns
Pixel Clock Duty Cycle	$t_{pclkcyc}$		33	67	%
Pixel Clock Low Duration	t_{pclkli}		15	-	ns
Pixel Clock High Duration	t_{pclkhi}		15	-	ns
Data Setup Time	t_{ds}		15	-	ns
Data Hold Time	t_{dh}		15	-	ns

14. Revision History

Version No.	Date	Page	Description
V.01	2006/4/17		New Created