Data Sheet

S6D0129

Preliminary

240 RGB X 320 DOT 1-CHIP DRIVER IC WITH INTERNAL GRAM
FOR 262,144 Colors TFT-LCD

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Ver. 0.4

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Preliminary

CONTENTS

Preliminary

Preliminary

INTRODUCTION

The S6D0129 is 1-chip solution for TFT-LCD panel: source driver with built-in memory, gate driver, power IC are integrated on one chip. This IC can display to a maximum of 240-RGB x 320 dot graphics on 260k-color TFT panel.

The S6D0129 also supports 18-/16-/9-/8-bits high-speed bus interface, high-speed RAM-write functions that enable efficient data transfer, and high-speed rewriting of data to the internal GRAM.

There is an external interface. In case of display data, the S6D0129 offers a flexible 18-/16-/6-bits bus of RGB interface for transferring the 260k colors display data.

The motion picture area can be specified in internal GRAM by window function. The specified window area can be updated selectively, so that motion picture can be displayed simultaneously independent of still picture area.

The S6D0129 has various functions for reducing the power consumption of a LCD system: operating at low voltage (1.8V), register-controlled power-save mode, low-current mode, partial display mode and so on. The IC has internal GRAM to store 240-RGB x 320 dot 260k-color image and internal booster that generates the LCD driving voltage, breeder resistance and the voltage follower circuit for LCD driver.

This LSI is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities, such as digital cellular phones supporting a web browser, bi-directional pagers, and small PDAs.

Preliminary

FEATURES

- **240-RGB x 320 dot TFT-LCD display controller/driver IC for 262,144 colors (720 channel-source driver/ 320 channel-gate driver)**
- **18-/16-/9-/8-bit high-speed parallel bus interface (80- and 68- system) and serial peripheral interface (SPI)**
- **18-/16-/6-bit RGB interface and VSYNC interface**
- **Writing to a window-RAM address area by using a window-address function**
- **Various color-display control functions**
  - 262,144 colors can be displayed at the same time (including gamma adjust)
  - Vertical scroll display function in raster-row units
- **Internal RAM capacity: 240 x 18 x 320 = 1,382,000 bits**
- **Low-power operation supports:**
  - Power-save mode: standby mode, sleep mode
  - Partial display of two screens in any position
  - Maximum 6-times step-up circuit for generating driving voltage
  - Voltage followers to decrease direct current flow in the LCD drive breeder-resistors
  - Charge sharing function for the switching performance of step-up circuits and operational amplifiers
- **1-raster row inversion drive (Reverse the polarity of driving voltage in every selected raster row)**
- **Internal oscillation circuit and external hardware reset**
- **Structure for TFT-display retention volume (only for Cst)**
- **Alternating functions for TFT-LCD counter-electrode power**
  - Line alternating drive of Vcom.
- **Internal power supply circuit**
  - Step-up circuit: four to six times positive-polarity, three to five times negative-polarity
  - Adjustment of Vcom amplitude: internal 64-level digital potentiometer
- **Operating voltage**

• Apply voltage
  - VDD to VSS = 1.8 ± 0.15V (non-regulating) (logic voltage range – non-regulated)
    Refer to Voltage Regulation Function.
    * 0.15V is tolerance voltage
  - VDD3 to VSS = 1.8 to 3.3 V (regulating) (logic voltage range – regulated)
    Refer to Voltage Regulation Function.
  - VCI to VSS = 2.5 to 3.3 V (internal reference power-supply voltage)

• Generate voltage
  - For the source driver: AVDD to VSS = 3.5 to 5.5V (power supply for driving circuits)
    GVDD to VSS = 3.0 to 5.0V (reference power supply for grayscale voltages)
  - For the gate driver: VGH to VGL = 14 to 30 V, VGH to VSS = +10.0 to +16.5 V,
    VGL to VSS = -13.5 to -8.0 V.
  - For the step up circuit: VCI1 to VSS = 1.75 to 2.75 V (refer to Instruction Description)
  - For the TFT-LCD counter electrode: Vcom amplitude (max) = 6V,
    VcomH to VSS = 3.0 to 5.0V,
    VcomL to VSS = -2.0 to 0.0V

Preliminary

BLOCK DIAGRAM

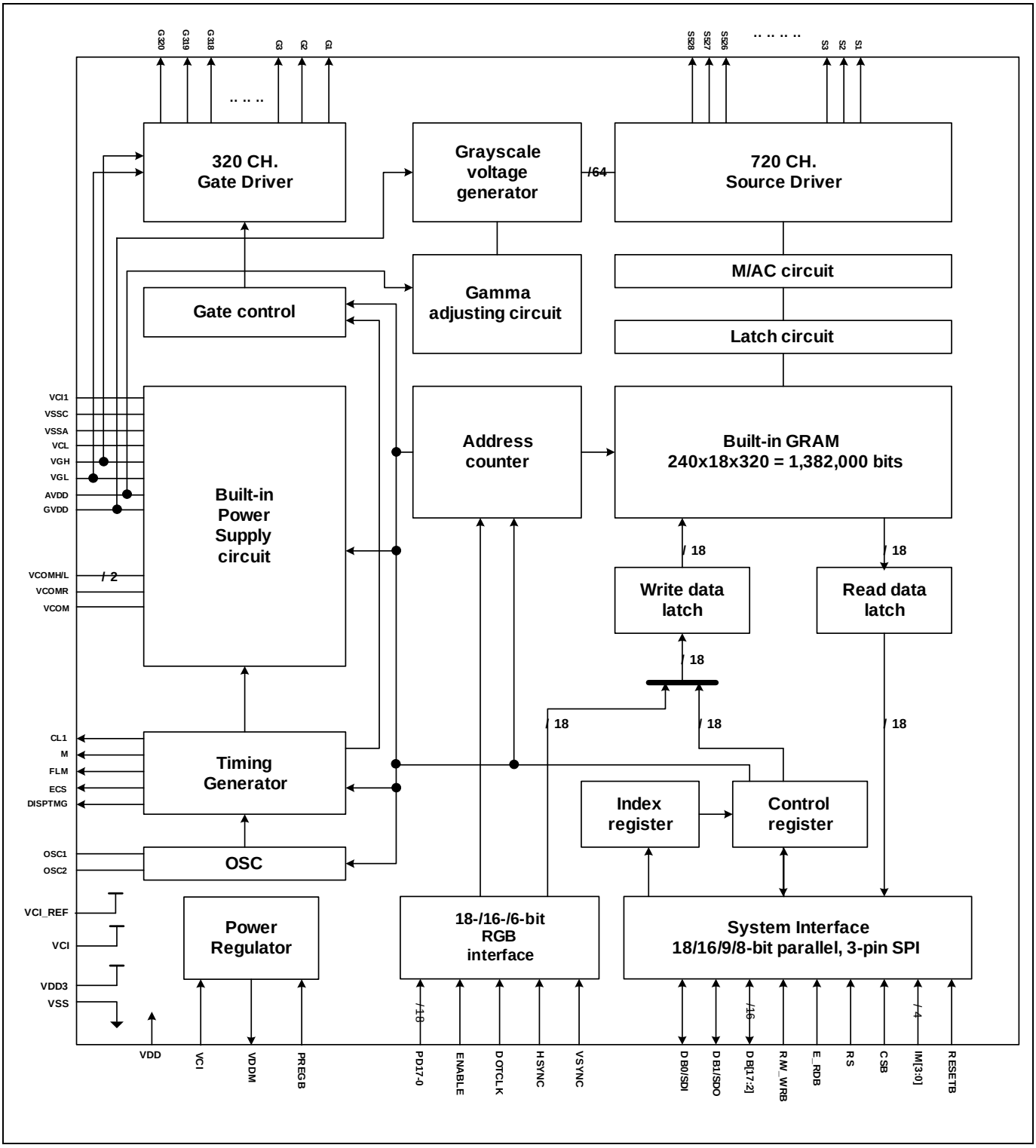

Figure1. S6D0129 Block Diagram

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Preliminary

PAD CONFIGURATION

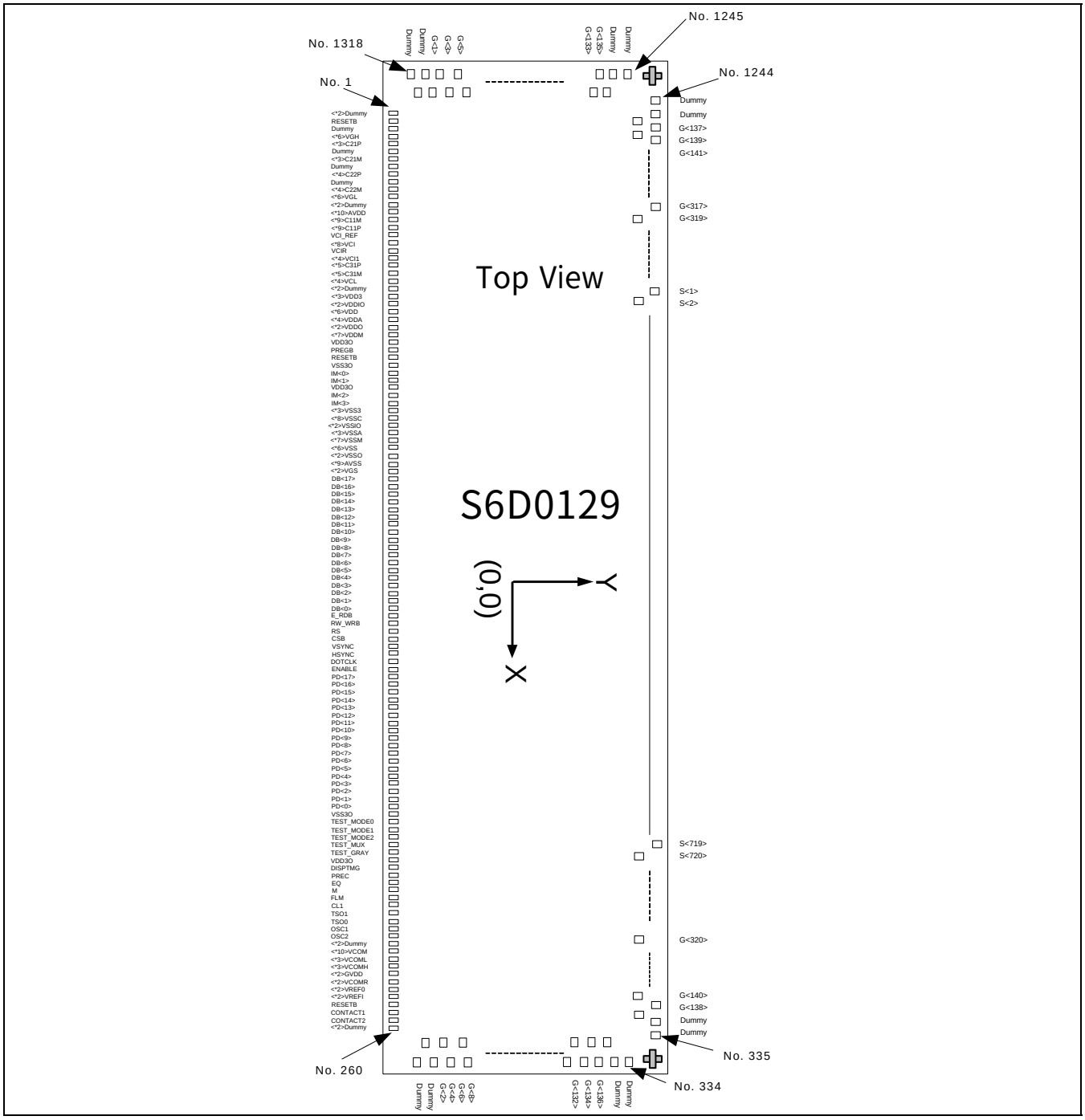


Figure 2. Pad Configuration

Preliminary

Table 1. S6D0129 Pad Dimensions

Items	Pad name.	Size		Unit
		X	Y	
Chip size[1)]	-	22,908	2,336	um
Bumped Pad size	Input Pad	55	104	
	Output Pad	22	100	
Bumped Pad Height	All Pad	17 (typ.) ±3	17 (typ.) ±3	

NOTES:

1) Scribe line included in this chip size (Scribe lane: 100um)

Preliminary

ALIGN KEY CONFIGURATION AND COORDINATE

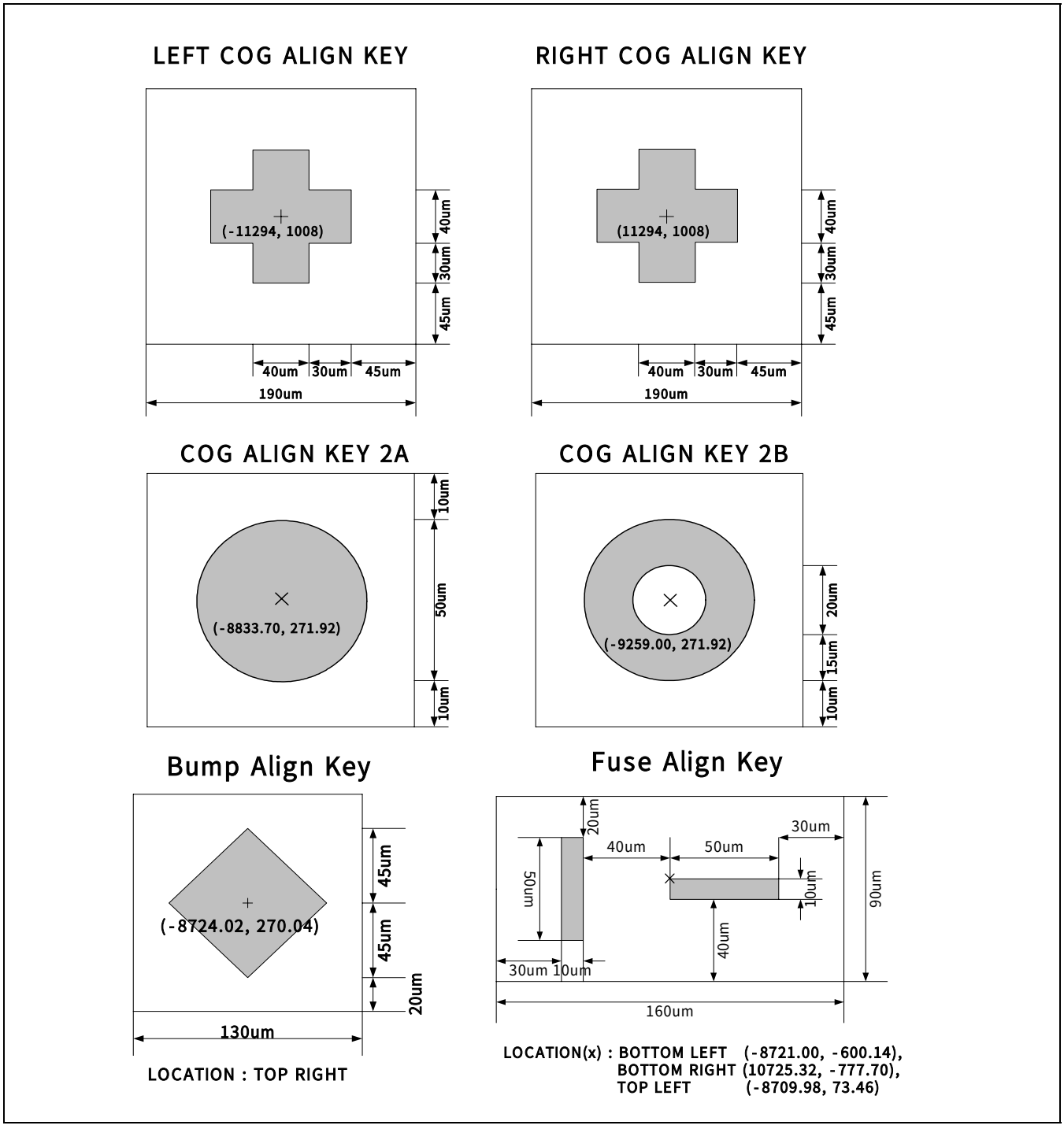


Figure 3. COG and BUMP align key

Preliminary

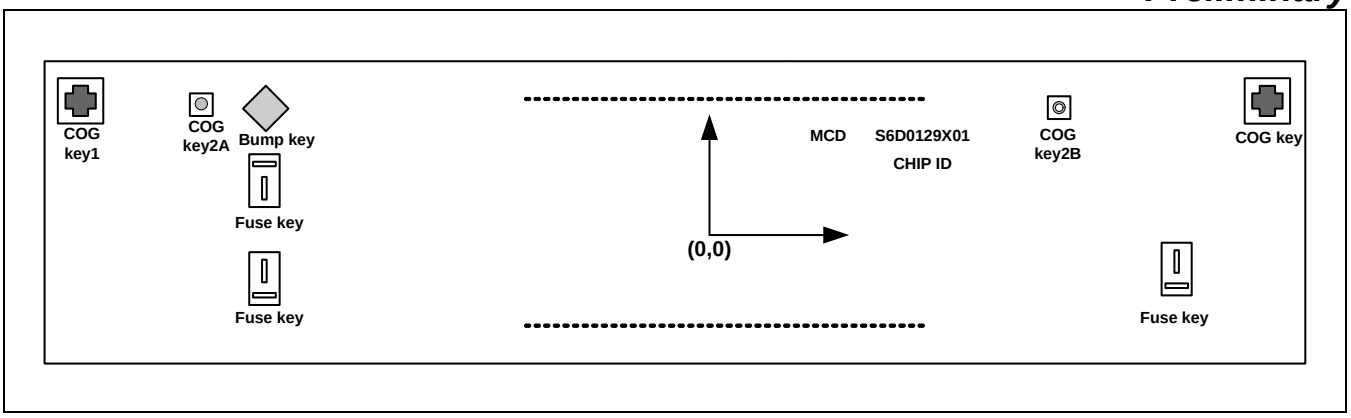


Figure 4. Align key configuration

NOTES:

1. Gold bump height: 17 ± 3 um (typical)
2. **Wafer thickness: 470um**

Preliminary

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
1	-10540	-1049	DUMMY<1>	65	-5420	-1049	VCI	129	-300	-1049	VSS3:G	193	5180	-1049	DOTCLK
2	-10460	-1049	DUMMY<2>	66	-5340	-1049	VCI	130	-220	-1049	VSSC	194	5260	-1049	ENABLE
3	-10380	-1049	RESETB	67	-5260	-1049	VCI	131	-140	-1049	VSSC	195	5340	-1049	PD<17>
4	-10300	-1049	DUMMY<3>	68	-5180	-1049	VCI	132	-60	-1049	VSSC	196	5420	-1049	PD<16>
5	-10220	-1049	VGH	69	-5100	-1049	VCI	133	20	-1049	VSSC	197	5500	-1049	PD<15>
6	-10140	-1049	VGH	70	-5020	-1049	VCI	134	100	-1049	VSSC	198	5580	-1049	PD<14>
7	-10060	-1049	VGH	71	-4940	-1049	VCI	135	180	-1049	VSSC	199	5660	-1049	PD<13>
8	-9980	-1049	VGH	72	-4860	-1049	VCI	136	260	-1049	VSSC	200	5740	-1049	PD<12>
9	-9900	-1049	VGH	73	-4780	-1049	VCIR	137	340	-1049	VSSC	201	5820	-1049	PD<11>
10	-9820	-1049	VGH	74	-4700	-1049	VCI1	138	420	-1049	VSSIO:G	202	5900	-1049	PD<10>
11	-9740	-1049	C21P	75	-4620	-1049	VCI1	139	500	-1049	VSSIO:G	203	5980	-1049	PD<9>
12	-9660	-1049	C21P	76	-4540	-1049	VCI1	140	580	-1049	VSSA:G	204	6060	-1049	PD<8>
13	-9580	-1049	C21P	77	-4460	-1049	VCI1	141	660	-1049	VSSA:G	205	6140	-1049	PD<7>
14	-9500	-1049	DUMMY<4>	78	-4380	-1049	C31P	142	740	-1049	VSSA:G	206	6220	-1049	PD<6>
15	-9420	-1049	C21M	79	-4300	-1049	C31P	143	820	-1049	VSSM:G	207	6300	-1049	PD<5>
16	-9340	-1049	C21M	80	-4220	-1049	C31P	144	900	-1049	VSSM:G	208	6380	-1049	PD<4>
17	-9260	-1049	C21M	81	-4140	-1049	C31P	145	980	-1049	VSSM:G	209	6460	-1049	PD<3>
18	-9180	-1049	DUMMY<5>	82	-4060	-1049	C31P	146	1060	-1049	VSSM:G	210	6540	-1049	PD<2>
19	-9100	-1049	C22P	83	-3980	-1049	C31M	147	1140	-1049	VSSM:G	211	6620	-1049	PD<1>
20	-9020	-1049	C22P	84	-3900	-1049	C31M	148	1220	-1049	VSSM:G	212	6700	-1049	PD<0>
21	-8940	-1049	C22P	85	-3820	-1049	C31M	149	1300	-1049	VSSM:G	213	6780	-1049	VSS3O
22	-8860	-1049	C22P	86	-3740	-1049	C31M	150	1380	-1049	VSS:G	214	6860	-1049	TEST_MODE<0>
23	-8780	-1049	DUMMY<6>	87	-3660	-1049	C31M	151	1460	-1049	VSS:G	215	6940	-1049	TEST_MODE<1>
24	-8700	-1049	C22M	88	-3580	-1049	VCL	152	1540	-1049	VSS:G	216	7020	-1049	TEST_MODE<2>
25	-8620	-1049	C22M	89	-3500	-1049	VCL	153	1620	-1049	VSS:G	217	7100	-1049	TEST_MUX
26	-8540	-1049	C22M	90	-3420	-1049	VCL	154	1700	-1049	VSS:G	218	7180	-1049	TEST_GRAY
27	-8460	-1049	C22M	91	-3340	-1049	VCL	155	1780	-1049	VSS:G	219	7260	-1049	VDD3O
28	-8380	-1049	VGL	92	-3260	-1049	DUMMY<9>	156	1860	-1049	VSSO	220	7340	-1049	DISPTMG
29	-8300	-1049	VGL	93	-3180	-1049	DUMMY<10>	157	1940	-1049	VSSO	221	7420	-1049	PREC
30	-8220	-1049	VGL	94	-3100	-1049	VDD3:P	158	2020	-1049	AVSS:G	222	7500	-1049	EQ
31	-8140	-1049	VGL	95	-3020	-1049	VDD3:P	159	2100	-1049	AVSS:G	223	7580	-1049	M
32	-8060	-1049	VGL	96	-2940	-1049	VDD3:P	160	2180	-1049	AVSS:G	224	7660	-1049	FLM
33	-7980	-1049	VGL	97	-2860	-1049	VDDIO	161	2260	-1049	AVSS:G	225	7740	-1049	CL1
34	-7900	-1049	DUMMY<7>	98	-2780	-1049	VDDIO	162	2340	-1049	AVSS:G	226	7820	-1049	TSO<1>
35	-7820	-1049	DUMMY<8>	99	-2700	-1049	VDD:P	163	2420	-1049	AVSS:G	227	7900	-1049	TSO<0>
36	-7740	-1049	AVDD:P	100	-2620	-1049	VDD:P	164	2500	-1049	AVSS:G	228	7980	-1049	OSC1
37	-7660	-1049	AVDD:P	101	-2540	-1049	VDD:P	165	2580	-1049	AVSS:G	229	8060	-1049	OSC2
38	-7580	-1049	AVDD:P	102	-2460	-1049	VDD:P	166	2660	-1049	AVSS:G	230	8140	-1049	DUMMY<11>
39	-7500	-1049	AVDD:P	103	-2380	-1049	VDD:P	167	2740	-1049	VGS	231	8220	-1049	DUMMY<12>
40	-7420	-1049	AVDD:P	104	-2300	-1049	VDD:P	168	2820	-1049	VGS	232	8300	-1049	VCOM
41	-7340	-1049	AVDD:P	105	-2220	-1049	VDDA:P	169	2900	-1049	DB<17>	233	8380	-1049	VCOM
42	-7260	-1049	AVDD:P	106	-2140	-1049	VDDA:P	170	3000	-1049	DB<16>	234	8460	-1049	VCOM
43	-7180	-1049	AVDD:P	107	-2060	-1049	VDDA:P	171	3100	-1049	DB<15>	235	8540	-1049	VCOM
44	-7100	-1049	AVDD:P	108	-1980	-1049	VDDA:P	172	3200	-1049	DB<14>	236	8620	-1049	VCOM
45	-7020	-1049	AVDD:P	109	-1900	-1049	VDDO	173	3300	-1049	DB<13>	237	8700	-1049	VCOM
46	-6940	-1049	C11M	110	-1820	-1049	VDDO	174	3400	-1049	DB<12>	238	8780	-1049	VCOM
47	-6860	-1049	C11M	111	-1740	-1049	VDDM	175	3500	-1049	DB<11>	239	8860	-1049	VCOM
48	-6780	-1049	C11M	112	-1660	-1049	VDDM	176	3600	-1049	DB<10>	240	8940	-1049	VCOM
49	-6700	-1049	C11M	113	-1580	-1049	VDDM	177	3700	-1049	DB<9>	241	9020	-1049	VCOM
50	-6620	-1049	C11M	114	-1500	-1049	VDDM	178	3800	-1049	DB<8>	242	9100	-1049	VCOML
51	-6540	-1049	C11M	115	-1420	-1049	VDDM	179	3900	-1049	DB<7>	243	9180	-1049	VCOML
52	-6460	-1049	C11M	116	-1340	-1049	VDDM	180	4000	-1049	DB<6>	244	9260	-1049	VCOML
53	-6380	-1049	C11M	117	-1260	-1049	VDDM	181	4100	-1049	DB<5>	245	9340	-1049	VCOMH
54	-6300	-1049	C11M	118	-1180	-1049	VDD3O	182	4200	-1049	DB<4>	246	9420	-1049	VCOMH
55	-6220	-1049	C11P	119	-1100	-1049	PREGB	183	4300	-1049	DB<3>	247	9500	-1049	VCOMH
56	-6140	-1049	C11P	120	-1020	-1049	RESETB	184	4400	-1049	DB<2>	248	9580	-1049	GVDD
57	-6060	-1049	C11P	121	-940	-1049	VSS3O	185	4500	-1049	DB<1>	249	9660	-1049	GVDD
58	-5980	-1049	C11P	122	-860	-1049	IM<0>	186	4600	-1049	DB<0>	250	9740	-1049	VCOMR
59	-5900	-1049	C11P	123	-780	-1049	IM<1>	187	4700	-1049	E_RDB	251	9820	-1049	VCOMR
60	-5820	-1049	C11P	124	-700	-1049	VDD3O	188	4780	-1049	RW_WRB	252	9900	-1049	VREFO
61	-5740	-1049	C11P	125	-620	-1049	IM<2>	189	4860	-1049	RS	253	9980	-1049	VREFO
62	-5660	-1049	C11P	126	-540	-1049	IM<3>	190	4940	-1049	CSB	254	10060	-1049	VREFI
63	-5580	-1049	C11P	127	-460	-1049	VSS3:G	191	5020	-1049	VSYNC	255	10140	-1049	VREFI
64	-5500	-1049	VCI_REF	128	-380	-1049	VSS3:G	192	5100	-1049	HSYNC	256	10220	-1049	RESETB

Preliminary

Table 3. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
257	10300	-1049	COMTACT<1>	321	11337	466	G<116>	385	9864	911	D<232>	449	8160	1051	S<701>
258	10380	-1049	COMTACT<2>	322	11197	490	G<118>	386	9840	1051	D<234>	450	8136	911	S<700>
259	10460	-1049	DUMMY<13>	323	11337	514	G<120>	387	9816	911	D<236>	451	8112	1051	S<699>
260	10540	-1049	DUMMY<14>	324	11197	538	G<122>	388	9792	1051	D<238>	452	8088	911	S<698>
261	11337	-974	DUMMY<15>	325	11337	562	G<124>	389	9768	911	D<240>	453	8064	1051	S<697>
262	11197	-950	DUMMY<16>	326	11197	586	G<126>	390	9744	1051	D<242>	454	8040	911	S<696>
263	11337	-926	DUMMY<17>	327	11337	610	G<128>	391	9720	911	D<244>	455	8016	1051	S<695>
264	11197	-902	G<2>	328	11197	634	G<130>	392	9696	1051	G<246>	456	7992	911	S<694>
265	11337	-878	G<4>	329	11337	658	G<132>	393	9672	911	G<248>	457	7968	1051	S<693>
266	11197	-854	G<6>	330	11197	682	G<134>	394	9648	1051	G<250>	458	7944	911	S<692>
267	11337	-830	G<8>	331	11337	706	G<136>	395	9624	911	G<252>	459	7920	1051	S<691>
268	11197	-806	G<10>	332	11197	730	DUMMY<18>	396	9600	1051	G<254>	460	7896	911	S<690>
269	11337	-782	G<12>	333	11337	754	DUMMY<19>	397	9576	911	G<256>	461	7872	1051	S<689>
270	11197	-758	G<14>	334	11337	802	DUMMY<20>	398	9552	1051	G<258>	462	7848	911	S<688>
271	11337	-734	G<16>	335	11088	1051	DUMMY<21>	399	9528	911	G<260>	463	7824	1051	S<687>
272	11197	-710	G<18>	336	11040	1051	DUMMY<22>	400	9504	1051	G<262>	464	7800	911	S<686>
273	11337	-686	G<20>	337	11016	911	DUMMY<23>	401	9480	911	G<264>	465	7776	1051	S<685>
274	11197	-662	G<22>	338	10992	1051	G<138>	402	9456	1051	G<266>	466	7752	911	S<684>
275	11337	-638	G<24>	339	10968	911	G<140>	403	9432	911	G<268>	467	7728	1051	S<683>
276	11197	-614	G<26>	340	10944	1051	G<142>	404	9408	1051	G<270>	468	7704	911	S<682>
277	11337	-590	G<28>	341	10920	911	G<144>	405	9384	911	G<272>	469	7680	1051	S<681>
278	11197	-566	G<30>	342	10896	1051	G<146>	406	9360	1051	G<274>	470	7656	911	S<680>
279	11337	-542	G<32>	343	10872	911	G<148>	407	9336	911	G<276>	471	7632	1051	S<679>
280	11197	-518	G<34>	344	10848	1051	G<150>	408	9312	1051	G<278>	472	7608	911	S<678>
281	11337	-494	G<36>	345	10824	911	G<152>	409	9288	911	G<280>	473	7584	1051	S<677>
282	11197	-470	G<38>	346	10800	1051	G<154>	410	9264	1051	G<282>	474	7560	911	S<676>
283	11337	-446	G<40>	347	10776	911	G<156>	411	9240	911	G<284>	475	7536	1051	S<675>
284	11197	-422	G<42>	348	10752	1051	G<158>	412	9216	1051	G<286>	476	7512	911	S<674>
285	11337	-398	G<44>	349	10728	911	G<160>	413	9192	911	G<288>	477	7488	1051	S<673>
286	11197	-374	G<46>	350	10704	1051	G<162>	414	9168	1051	G<290>	478	7464	911	S<672>
287	11337	-350	G<48>	351	10680	911	G<164>	415	9144	911	G<292>	479	7440	1051	S<671>
288	11197	-326	G<50>	352	10656	1051	G<166>	416	9120	1051	G<294>	480	7416	911	S<670>
289	11337	-302	G<52>	353	10632	911	G<168>	417	9096	911	G<296>	481	7392	1051	S<669>
290	11197	-278	G<54>	354	10608	1051	G<170>	418	9072	1051	G<298>	482	7368	911	S<668>
291	11337	-254	G<56>	355	10584	911	G<172>	419	9048	911	G<300>	483	7344	1051	S<667>
292	11197	-230	G<58>	356	10560	1051	G<174>	420	9024	1051	G<302>	484	7320	911	S<666>
293	11337	-206	G<60>	357	10536	911	G<176>	421	9000	911	G<304>	485	7296	1051	S<665>
294	11197	-182	G<62>	358	10512	1051	G<178>	422	8976	1051	G<306>	486	7272	911	S<664>
295	11337	-158	G<64>	359	10488	911	G<180>	423	8952	911	G<308>	487	7248	1051	S<663>
296	11197	-134	G<66>	360	10464	1051	G<182>	424	8928	1051	G<310>	488	7224	911	S<662>
297	11337	-110	G<68>	361	10440	911	G<184>	425	8904	911	G<312>	489	7200	1051	S<661>
298	11197	-86	G<70>	362	10416	1051	G<186>	426	8880	1051	G<314>	490	7176	911	S<660>
299	11337	-62	G<72>	363	10392	911	G<188>	427	8856	911	G<316>	491	7152	1051	S<659>
300	11197	-38	G<74>	364	10368	1051	G<190>	428	8832	1051	G<318>	492	7128	911	S<658>
301	11337	-14	G<76>	365	10344	911	G<192>	429	8808	911	G<320>	493	7104	1051	S<657>
302	11197	10	G<78>	366	10320	1051	G<194>	430	8616	911	S<720>	494	7080	911	S<656>
303	11337	34	G<80>	367	10296	911	G<196>	431	8592	1051	S<719>	495	7056	1051	S<655>
304	11197	58	G<82>	368	10272	1051	G<198>	432	8568	911	S<718>	496	7032	911	S<654>
305	11337	82	G<84>	369	10248	911	G<200>	433	8544	1051	S<717>	497	7008	1051	S<653>
306	11197	106	G<86>	370	10224	1051	G<202>	434	8520	911	S<716>	498	6984	911	S<652>
307	11337	130	G<88>	371	10200	911	G<204>	435	8496	1051	S<715>	499	6960	1051	S<651>
308	11197	154	G<90>	372	10176	1051	G<206>	436	8472	911	S<714>	500	6936	911	S<650>
309	11337	178	G<92>	373	10152	911	G<208>	437	8448	1051	S<713>	501	6912	1051	S<649>
310	11197	202	G<94>	374	10128	1051	G<210>	438	8424	911	S<712>	502	6888	911	S<648>
311	11337	226	G<96>	375	10104	911	G<212>	439	8400	1051	S<711>	503	6864	1051	S<647>
312	11197	250	G<98>	376	10080	1051	G<214>	440	8376	911	S<710>	504	6840	911	S<646>
313	11337	274	G<100>	377	10056	911	G<216>	441	8352	1051	S<709>	505	6816	1051	S<645>
314	11197	298	G<102>	378	10032	1051	G<218>	442	8328	911	S<708>	506	6792	911	S<644>
315	11337	322	G<104>	379	10008	911	G<220>	443	8304	1051	S<707>	507	6768	1051	S<643>
316	11197	346	G<106>	380	9984	1051	G<222>	444	8280	911	S<706>	508	6744	911	S<642>
317	11337	370	G<108>	381	9960	911	G<224>	445	8256	1051	S<705>	509	6720	1051	S<641>
318	11197	394	G<110>	382	9936	1051	G<226>	446	8232	911	S<704>	510	6696	911	S<640>
319	11337	418	G<112>	383	9912	911	G<228>	447	8208	1051	S<703>	511	6672	1051	S<639>
320	11197	442	G<114>	384	9888	1051	G<230>	448	8184	911	S<702>	512	6648	911	S<638>

SAMSUNG ELECTRONICS

Preliminary

Table 4. Pad Center Coordinates(continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
513	6624	1051	S<637>	577	5088	1051	S<573>	641	3552	1051	S<509>	705	2016	1051	S<445>
514	6600	911	S<636>	578	5064	911	S<572>	642	3528	911	S<508>	706	1992	911	S<444>
515	6576	1051	S<635>	579	5040	1051	S<571>	643	3504	1051	S<507>	707	1968	1051	S<443>
516	6552	911	S<634>	580	5016	911	S<570>	644	3480	911	S<506>	708	1944	911	S<442>
517	6528	1051	S<633>	581	4992	1051	S<569>	645	3456	1051	S<505>	709	1920	1051	S<441>
518	6504	911	S<632>	582	4968	911	S<568>	646	3432	911	S<504>	710	1896	911	S<440>
519	6480	1051	S<631>	583	4944	1051	S<567>	647	3408	1051	S<503>	711	1872	1051	S<439>
520	6456	911	S<630>	584	4920	911	S<566>	648	3384	911	S<502>	712	1848	911	S<438>
521	6432	1051	S<629>	585	4896	1051	S<565>	649	3360	1051	S<501>	713	1824	1051	S<437>
522	6408	911	S<628>	586	4872	911	S<564>	650	3336	911	S<500>	714	1800	911	S<436>
523	6384	1051	S<627>	587	4848	1051	S<563>	651	3312	1051	S<499>	715	1776	1051	S<435>
524	6360	911	S<626>	588	4824	911	S<562>	652	3288	911	S<498>	716	1752	911	S<434>
525	6336	1051	S<625>	589	4800	1051	S<561>	653	3264	1051	S<497>	717	1728	1051	S<433>
526	6312	911	S<624>	590	4776	911	S<560>	654	3240	911	S<496>	718	1704	911	S<432>
527	6288	1051	S<623>	591	4752	1051	S<559>	655	3216	1051	S<495>	719	1680	1051	S<431>
528	6264	911	S<622>	592	4728	911	S<558>	656	3192	911	S<494>	720	1656	911	S<430>
529	6240	1051	S<621>	593	4704	1051	S<557>	657	3168	1051	S<493>	721	1632	1051	S<429>
530	6216	911	S<620>	594	4680	911	S<556>	658	3144	911	S<492>	722	1608	911	S<428>
531	6192	1051	S<619>	595	4656	1051	S<555>	659	3120	1051	S<491>	723	1584	1051	S<427>
532	6168	911	S<618>	596	4632	911	S<554>	660	3096	911	S<490>	724	1560	911	S<426>
533	6144	1051	S<617>	597	4608	1051	S<553>	661	3072	1051	S<489>	725	1536	1051	S<425>
534	6120	911	S<616>	598	4584	911	S<552>	662	3048	911	S<488>	726	1512	911	S<424>
535	6096	1051	S<615>	599	4560	1051	S<551>	663	3024	1051	S<487>	727	1488	1051	S<423>
536	6072	911	S<614>	600	4536	911	S<550>	664	3000	911	S<486>	728	1464	911	S<422>
537	6048	1051	S<613>	601	4512	1051	S<549>	665	2976	1051	S<485>	729	1440	1051	S<421>
538	6024	911	S<612>	602	4488	911	S<548>	666	2952	911	S<484>	730	1416	911	S<420>
539	6000	1051	S<611>	603	4464	1051	S<547>	667	2928	1051	S<483>	731	1392	1051	S<419>
540	5976	911	S<610>	604	4440	911	S<546>	668	2904	911	S<482>	732	1368	911	S<418>
541	5952	1051	S<609>	605	4416	1051	S<545>	669	2880	1051	S<481>	733	1344	1051	S<417>
542	5928	911	S<608>	606	4392	911	S<544>	670	2856	911	S<480>	734	1320	911	S<416>
543	5904	1051	S<607>	607	4368	1051	S<543>	671	2832	1051	S<479>	735	1296	1051	S<415>
544	5880	911	S<606>	608	4344	911	S<542>	672	2808	911	S<478>	736	1272	911	S<414>
545	5856	1051	S<605>	609	4320	1051	S<541>	673	2784	1051	S<477>	737	1248	1051	S<413>
546	5832	911	S<604>	610	4296	911	S<540>	674	2760	911	S<476>	738	1224	911	S<412>
547	5808	1051	S<603>	611	4272	1051	S<539>	675	2736	1051	S<475>	739	1200	1051	S<411>
548	5784	911	S<602>	612	4248	911	S<538>	676	2712	911	S<474>	740	1176	911	S<410>
549	5760	1051	S<601>	613	4224	1051	S<537>	677	2688	1051	S<473>	741	1152	1051	S<409>
550	5736	911	S<600>	614	4200	911	S<536>	678	2664	911	S<472>	742	1128	911	S<408>
551	5712	1051	S<599>	615	4176	1051	S<535>	679	2640	1051	S<471>	743	1104	1051	S<407>
552	5688	911	S<598>	616	4152	911	S<534>	680	2616	911	S<470>	744	1080	911	S<406>
553	5664	1051	S<597>	617	4128	1051	S<533>	681	2592	1051	S<469>	745	1056	1051	S<405>
554	5640	911	S<596>	618	4104	911	S<532>	682	2568	911	S<468>	746	1032	911	S<404>
555	5616	1051	S<595>	619	4080	1051	S<531>	683	2544	1051	S<467>	747	1008	1051	S<403>
556	5592	911	S<594>	620	4056	911	S<530>	684	2520	911	S<466>	748	984	911	S<402>
557	5568	1051	S<593>	621	4032	1051	S<529>	685	2496	1051	S<465>	749	960	1051	S<401>
558	5544	911	S<592>	622	4008	911	S<528>	686	2472	911	S<464>	750	936	911	S<400>
559	5520	1051	S<591>	623	3984	1051	S<527>	687	2448	1051	S<463>	751	912	1051	S<399>
560	5496	911	S<590>	624	3960	911	S<526>	688	2424	911	S<462>	752	888	911	S<398>
561	5472	1051	S<589>	625	3936	1051	S<525>	689	2400	1051	S<461>	753	864	1051	S<397>
562	5448	911	S<588>	626	3912	911	S<524>	690	2376	911	S<460>	754	840	911	S<396>
563	5424	1051	S<587>	627	3888	1051	S<523>	691	2352	1051	S<459>	755	816	1051	S<395>
564	5400	911	S<586>	628	3864	911	S<522>	692	2328	911	S<458>	756	792	911	S<394>
565	5376	1051	S<585>	629	3840	1051	S<521>	693	2304	1051	S<457>	757	768	1051	S<393>
566	5352	911	S<584>	630	3816	911	S<520>	694	2280	911	S<456>	758	744	911	S<392>
567	5328	1051	S<583>	631	3792	1051	S<519>	695	2256	1051	S<455>	759	720	1051	S<391>
568	5304	911	S<582>	632	3768	911	S<518>	696	2232	911	S<454>	760	696	911	S<390>
569	5280	1051	S<581>	633	3744	1051	S<517>	697	2208	1051	S<453>	761	672	1051	S<389>
570	5256	911	S<580>	634	3720	911	S<516>	698	2184	911	S<452>	762	648	911	S<388>
571	5232	1051	S<579>	635	3696	1051	S<515>	699	2160	1051	S<451>	763	624	1051	S<387>
572	5208	911	S<578>	636	3672	911	S<514>	700	2136	911	S<450>	764	600	911	S<386>
573	5184	1051	S<577>	637	3648	1051	S<513>	701	2112	1051	S<449>	765	576	1051	S<385>
574	5160	911	S<576>	638	3624	911	S<512>	702	2088	911	S<448>	766	552	911	S<384>
575	5136	1051	S<575>	639	3600	1051	S<511>	703	2064	1051	S<447>	767	528	1051	S<383>
576	5112	911	S<574>	640	3576	911	S<510>	704	2040	911	S<446>	768	504	911	S<382>

Preliminary

Table 5. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
769	480	1051	S<381>	833	-1056	1051	S<317>	897	-2592	1051	S<253>	961	-4128	1051	S<189>
770	456	911	S<380>	834	-1080	911	S<316>	898	-2616	911	S<252>	962	-4152	911	S<188>
771	432	1051	S<379>	835	-1104	1051	S<315>	899	-2640	1051	S<251>	963	-4176	1051	S<187>
772	408	911	S<378>	836	-1128	911	S<314>	900	-2664	911	S<250>	964	-4200	911	S<186>
773	384	1051	S<377>	837	-1152	1051	S<313>	901	-2688	1051	S<249>	965	-4224	1051	S<185>
774	360	911	S<376>	838	-1176	911	S<312>	902	-2712	911	S<248>	966	-4248	911	S<184>
775	336	1051	S<375>	839	-1200	1051	S<311>	903	-2736	1051	S<247>	967	-4272	1051	S<183>
776	312	911	S<374>	840	-1224	911	S<310>	904	-2760	911	S<246>	968	-4296	911	S<182>
777	288	1051	S<373>	841	-1248	1051	S<309>	905	-2784	1051	S<245>	969	-4320	1051	S<181>
778	264	911	S<372>	842	-1272	911	S<308>	906	-2808	911	S<244>	970	-4344	911	S<180>
779	240	1051	S<371>	843	-1296	1051	S<307>	907	-2832	1051	S<243>	971	-4368	1051	S<179>
780	216	911	S<370>	844	-1320	911	S<306>	908	-2856	911	S<242>	972	-4392	911	S<178>
781	192	1051	S<369>	845	-1344	1051	S<305>	909	-2880	1051	S<241>	973	-4416	1051	S<177>
782	168	911	S<368>	846	-1368	911	S<304>	910	-2904	911	S<240>	974	-4440	911	S<176>
783	144	1051	S<367>	847	-1392	1051	S<303>	911	-2928	1051	S<239>	975	-4464	1051	S<175>
784	120	911	S<366>	848	-1416	911	S<302>	912	-2952	911	S<238>	976	-4488	911	S<174>
785	96	1051	S<365>	849	-1440	1051	S<301>	913	-2976	1051	S<237>	977	-4512	1051	S<173>
786	72	911	S<364>	850	-1464	911	S<300>	914	-3000	911	S<236>	978	-4536	911	S<172>
787	48	1051	S<363>	851	-1488	1051	S<299>	915	-3024	1051	S<235>	979	-4560	1051	S<171>
788	24	911	S<362>	852	-1512	911	S<298>	916	-3048	911	S<234>	980	-4584	911	S<170>
789	0	1051	S<361>	853	-1536	1051	S<297>	917	-3072	1051	S<233>	981	-4608	1051	S<169>
790	-24	911	S<360>	854	-1560	911	S<296>	918	-3096	911	S<232>	982	-4632	911	S<168>
791	-48	1051	S<359>	855	-1584	1051	S<295>	919	-3120	1051	S<231>	983	-4656	1051	S<167>
792	-72	911	S<358>	856	-1608	911	S<294>	920	-3144	911	S<230>	984	-4680	911	S<166>
793	-96	1051	S<357>	857	-1632	1051	S<293>	921	-3168	1051	S<229>	985	-4704	1051	S<165>
794	-120	911	S<356>	858	-1656	911	S<292>	922	-3192	911	S<228>	986	-4728	911	S<164>
795	-144	1051	S<355>	859	-1680	1051	S<291>	923	-3216	1051	S<227>	987	-4752	1051	S<163>
796	-168	911	S<354>	860	-1704	911	S<290>	924	-3240	911	S<226>	988	-4776	911	S<162>
797	-192	1051	S<353>	861	-1728	1051	S<289>	925	-3264	1051	S<225>	989	-4800	1051	S<161>
798	-216	911	S<352>	862	-1752	911	S<288>	926	-3288	911	S<224>	990	-4824	911	S<160>
799	-240	1051	S<351>	863	-1776	1051	S<287>	927	-3312	1051	S<223>	991	-4848	1051	S<159>
800	-264	911	S<350>	864	-1800	911	S<286>	928	-3336	911	S<222>	992	-4872	911	S<158>
801	-288	1051	S<349>	865	-1824	1051	S<285>	929	-3360	1051	S<221>	993	-4896	1051	S<157>
802	-312	911	S<348>	866	-1848	911	S<284>	930	-3384	911	S<220>	994	-4920	911	S<156>
803	-336	1051	S<347>	867	-1872	1051	S<283>	931	-3408	1051	S<219>	995	-4944	1051	S<155>
804	-360	911	S<346>	868	-1896	911	S<282>	932	-3432	911	S<218>	996	-4968	911	S<154>
805	-384	1051	S<345>	869	-1920	1051	S<281>	933	-3456	1051	S<217>	997	-4992	1051	S<153>
806	-408	911	S<344>	870	-1944	911	S<280>	934	-3480	911	S<216>	998	-5016	911	S<152>
807	-432	1051	S<343>	871	-1968	1051	S<279>	935	-3504	1051	S<215>	999	-5040	1051	S<151>
808	-456	911	S<342>	872	-1992	911	S<278>	936	-3528	911	S<214>	1000	-5064	911	S<150>
809	-480	1051	S<341>	873	-2016	1051	S<277>	937	-3552	1051	S<213>	1001	-5088	1051	S<149>
810	-504	911	S<340>	874	-2040	911	S<276>	938	-3576	911	S<212>	1002	-5112	911	S<148>
811	-528	1051	S<339>	875	-2064	1051	S<275>	939	-3600	1051	S<211>	1003	-5136	1051	S<147>
812	-552	911	S<338>	876	-2088	911	S<274>	940	-3624	911	S<210>	1004	-5160	911	S<146>
813	-576	1051	S<337>	877	-2112	1051	S<273>	941	-3648	1051	S<209>	1005	-5184	1051	S<145>
814	-600	911	S<336>	878	-2136	911	S<272>	942	-3672	911	S<208>	1006	-5208	911	S<144>
815	-624	1051	S<335>	879	-2160	1051	S<271>	943	-3696	1051	S<207>	1007	-5232	1051	S<143>
816	-648	911	S<334>	880	-2184	911	S<270>	944	-3720	911	S<206>	1008	-5256	911	S<142>
817	-672	1051	S<333>	881	-2208	1051	S<269>	945	-3744	1051	S<205>	1009	-5280	1051	S<141>
818	-696	911	S<332>	882	-2232	911	S<268>	946	-3768	911	S<204>	1010	-5304	911	S<140>
819	-720	1051	S<331>	883	-2256	1051	S<267>	947	-3792	1051	S<203>	1011	-5328	1051	S<139>
820	-744	911	S<330>	884	-2280	911	S<266>	948	-3816	911	S<202>	1012	-5352	911	S<138>
821	-768	1051	S<329>	885	-2304	1051	S<265>	949	-3840	1051	S<201>	1013	-5376	1051	S<137>
822	-792	911	S<328>	886	-2328	911	S<264>	950	-3864	911	S<200>	1014	-5400	911	S<136>
823	-816	1051	S<327>	887	-2352	1051	S<263>	951	-3888	1051	S<199>	1015	-5424	1051	S<135>
824	-840	911	S<326>	888	-2376	911	S<262>	952	-3912	911	S<198>	1016	-5448	911	S<134>
825	-864	1051	S<325>	889	-2400	1051	S<261>	953	-3936	1051	S<197>	1017	-5472	1051	S<133>
826	-888	911	S<324>	890	-2424	911	S<260>	954	-3960	911	S<196>	1018	-5496	911	S<132>
827	-912	1051	S<323>	891	-2448	1051	S<259>	955	-3984	1051	S<195>	1019	-5520	1051	S<131>
828	-936	911	S<322>	892	-2472	911	S<258>	956	-4008	911	S<194>	1020	-5544	911	S<130>
829	-960	1051	S<321>	893	-2496	1051	S<257>	957	-4032	1051	S<193>	1021	-5568	1051	S<129>
830	-984	911	S<320>	894	-2520	911	S<256>	958	-4056	911	S<192>	1022	-5592	911	S<128>
831	-1008	1051	S<319>	895	-2544	1051	S<255>	959	-4080	1051	S<191>	1023	-5616	1051	S<127>
832	-1032	911	S<318>	896	-2568	911	S<254>	960	-4104	911	S<190>	1024	-5640	911	S<126>

Table 6. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
1025	-5664	1051	S<125>	1089	-7200	1051	S<61>	1153	-8880	1051	G<313>	1217	-10416	1051	G<185>
1026	-5688	911	S<124>	1090	-7224	911	S<60>	1154	-8904	911	G<311>	1218	-10440	911	G<183>
1027	-5712	1051	S<123>	1091	-7248	1051	S<59>	1155	-8928	1051	G<309>	1219	-10464	1051	G<181>
1028	-5736	911	S<122>	1092	-7272	911	S<58>	1156	-8952	911	G<307>	1220	-10488	911	G<179>
1029	-5760	1051	S<121>	1093	-7296	1051	S<57>	1157	-8976	1051	G<305>	1221	-10512	1051	G<177>
1030	-5784	911	S<120>	1094	-7320	911	S<56>	1158	-9000	911	G<303>	1222	-10536	911	G<175>
1031	-5808	1051	S<119>	1095	-7344	1051	S<55>	1159	-9024	1051	G<301>	1223	-10560	1051	G<173>
1032	-5832	911	S<118>	1096	-7368	911	S<54>	1160	-9048	911	G<299>	1224	-10584	911	G<171>
1033	-5856	1051	S<117>	1097	-7392	1051	S<53>	1161	-9072	1051	G<297>	1225	-10608	1051	G<169>
1034	-5880	911	S<116>	1098	-7416	911	S<52>	1162	-9096	911	G<295>	1226	-10632	911	G<167>
1035	-5904	1051	S<115>	1099	-7440	1051	S<51>	1163	-9120	1051	G<293>	1227	-10656	1051	G<165>
1036	-5928	911	S<114>	1100	-7464	911	S<50>	1164	-9144	911	G<291>	1228	-10680	911	G<163>
1037	-5952	1051	S<113>	1101	-7488	1051	S<49>	1165	-9168	1051	G<289>	1229	-10704	1051	G<161>
1038	-5976	911	S<112>	1102	-7512	911	S<48>	1166	-9192	911	G<287>	1230	-10728	911	G<159>
1039	-6000	1051	S<111>	1103	-7536	1051	S<47>	1167	-9216	1051	G<285>	1231	-10752	1051	G<157>
1040	-6024	911	S<110>	1104	-7560	911	S<46>	1168	-9240	911	G<283>	1232	-10776	911	G<155>
1041	-6048	1051	S<109>	1105	-7584	1051	S<45>	1169	-9264	1051	G<281>	1233	-10800	1051	G<153>
1042	-6072	911	S<108>	1106	-7608	911	S<44>	1170	-9288	911	G<279>	1234	-10824	911	G<151>
1043	-6096	1051	S<107>	1107	-7632	1051	S<43>	1171	-9312	1051	G<277>	1235	-10848	1051	G<149>
1044	-6120	911	S<106>	1108	-7656	911	S<42>	1172	-9336	911	G<275>	1236	-10872	911	G<147>
1045	-6144	1051	S<105>	1109	-7680	1051	S<41>	1173	-9360	1051	G<273>	1237	-10896	1051	G<145>
1046	-6168	911	S<104>	1110	-7704	911	S<40>	1174	-9384	911	G<271>	1238	-10920	911	G<143>
1047	-6192	1051	S<103>	1111	-7728	1051	S<39>	1175	-9408	1051	G<269>	1239	-10944	1051	G<141>
1048	-6216	911	S<102>	1112	-7752	911	S<38>	1176	-9432	911	G<267>	1240	-10968	911	G<139>
1049	-6240	1051	S<101>	1113	-7776	1051	S<37>	1177	-9456	1051	G<265>	1241	-10992	1051	G<137>
1050	-6264	911	S<100>	1114	-7800	911	S<36>	1178	-9480	911	G<263>	1242	-11016	911	DUMMY<24>
1051	-6288	1051	S<99>	1115	-7824	1051	S<35>	1179	-9504	1051	G<261>	1243	-11040	1051	DUMMY<25>
1052	-6312	911	S<98>	1116	-7848	911	S<34>	1180	-9528	911	G<259>	1244	-11088	1051	DUMMY<26>
1053	-6336	1051	S<97>	1117	-7872	1051	S<33>	1181	-9552	1051	G<257>	1245	-11337	802	DUMMY<27>
1054	-6360	911	S<96>	1118	-7896	911	S<32>	1182	-9576	911	G<255>	1246	-11337	754	DUMMY<28>
1055	-6384	1051	S<95>	1119	-7920	1051	S<31>	1183	-9600	1051	G<253>	1247	-11197	730	DUMMY<29>
1056	-6408	911	S<94>	1120	-7944	911	S<30>	1184	-9624	911	G<251>	1248	-11337	706	G<135>
1057	-6432	1051	S<93>	1121	-7968	1051	S<29>	1185	-9648	1051	G<249>	1249	-11197	682	G<133>
1058	-6456	911	S<92>	1122	-7992	911	S<28>	1186	-9672	911	G<247>	1250	-11337	658	G<131>
1059	-6480	1051	S<91>	1123	-8016	1051	S<27>	1187	-9696	1051	G<245>	1251	-11197	634	G<129>
1060	-6504	911	S<90>	1124	-8040	911	S<26>	1188	-9720	911	G<243>	1252	-11337	610	G<127>
1061	-6528	1051	S<89>	1125	-8064	1051	S<25>	1189	-9744	1051	G<241>	1253	-11197	586	G<125>
1062	-6552	911	S<88>	1126	-8088	911	S<24>	1190	-9768	911	G<239>	1254	-11337	562	G<123>
1063	-6576	1051	S<87>	1127	-8112	1051	S<23>	1191	-9792	1051	G<237>	1255	-11197	538	G<121>
1064	-6600	911	S<86>	1128	-8136	911	S<22>	1192	-9816	911	G<235>	1256	-11337	514	G<119>
1065	-6624	1051	S<85>	1129	-8160	1051	S<21>	1193	-9840	1051	G<233>	1257	-11197	490	G<117>
1066	-6648	911	S<84>	1130	-8184	911	S<20>	1194	-9864	911	G<231>	1258	-11337	466	G<115>
1067	-6672	1051	S<83>	1131	-8208	1051	S<19>	1195	-9888	1051	G<229>	1259	-11197	442	G<113>
1068	-6696	911	S<82>	1132	-8232	911	S<18>	1196	-9912	911	G<227>	1260	-11337	418	G<111>
1069	-6720	1051	S<81>	1133	-8256	1051	S<17>	1197	-9936	1051	G<225>	1261	-11197	394	G<109>
1070	-6744	911	S<80>	1134	-8280	911	S<16>	1198	-9960	911	G<223>	1262	-11337	370	G<107>
1071	-6768	1051	S<79>	1135	-8304	1051	S<15>	1199	-9984	1051	G<221>	1263	-11197	346	G<105>
1072	-6792	911	S<78>	1136	-8328	911	S<14>	1200	-10008	911	G<219>	1264	-11337	322	G<103>
1073	-6816	1051	S<77>	1137	-8352	1051	S<13>	1201	-10032	1051	G<217>	1265	-11197	298	G<101>
1074	-6840	911	S<76>	1138	-8376	911	S<12>	1202	-10056	911	G<215>	1266	-11337	274	G<99>
1075	-6864	1051	S<75>	1139	-8400	1051	S<11>	1203	-10080	1051	G<213>	1267	-11197	250	G<97>
1076	-6888	911	S<74>	1140	-8424	911	S<10>	1204	-10104	911	G<211>	1268	-11337	226	G<95>
1077	-6912	1051	S<73>	1141	-8448	1051	S<9>	1205	-10128	1051	G<209>	1269	-11197	202	G<93>
1078	-6936	911	S<72>	1142	-8472	911	S<8>	1206	-10152	911	G<207>	1270	-11337	178	G<91>
1079	-6960	1051	S<71>	1143	-8496	1051	S<7>	1207	-10176	1051	G<205>	1271	-11197	154	G<89>
1080	-6984	911	S<70>	1144	-8520	911	S<6>	1208	-10200	911	G<203>	1272	-11337	130	G<87>
1081	-7008	1051	S<69>	1145	-8544	1051	S<5>	1209	-10224	1051	G<201>	1273	-11197	106	G<85>
1082	-7032	911	S<68>	1146	-8568	911	S<4>	1210	-10248	911	G<199>	1274	-11337	82	G<83>
1083	-7056	1051	S<67>	1147	-8592	1051	S<3>	1211	-10272	1051	G<197>	1275	-11197	58	G<81>
1084	-7080	911	S<66>	1148	-8616	911	S<2>	1212	-10296	911	G<195>	1276	-11337	34	G<79>
1085	-7104	1051	S<65>	1149	-8640	1051	S<1>	1213	-10320	1051	G<193>	1277	-11197	10	G<77>
1086	-7128	911	S<64>	1150	-8808	911	G<319>	1214	-10344	911	G<191>	1278	-11337	-14	G<75>
1087	-7152	1051	S<63>	1151	-8832	1051	G<317>	1215	-10368	1051	G<189>	1279	-11197	-38	G<73>
1088	-7176	911	S<62>	1152	-8856	911	G<315>	1216	-10392	911	G<187>	1280	-11337	-62	G<71>

Preliminary

Table 7. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
1281	-11197	-86	G<69>												
1282	-11337	-110	G<67>												
1283	-11197	-134	G<65>												
1284	-11337	-158	G<63>												
1285	-11197	-182	G<61>												
1286	-11337	-206	G<59>												
1287	-11197	-230	G<57>												
1288	-11337	-254	G<55>												
1289	-11197	-278	G<53>												
1290	-11337	-302	G<51>												
1291	-11197	-326	G<49>												
1292	-11337	-350	G<47>												
1293	-11197	-374	G<45>												
1294	-11337	-398	G<43>												
1295	-11197	-422	G<41>												
1296	-11337	-446	G<39>												
1297	-11197	-470	G<37>												
1298	-11337	-494	G<35>												
1299	-11197	-518	G<33>												
1300	-11337	-542	G<31>												
1301	-11197	-566	G<29>												
1302	-11337	-590	G<27>												
1303	-11197	-614	G<25>												
1304	-11337	-638	G<23>												
1305	-11197	-662	G<21>												
1306	-11337	-686	G<19>												
1307	-11197	-710	G<17>												

Preliminary

PIN DESCRIPTION

POWER SUPPLY PIN

Table 8. Power supply pin description

Symbol	I/O	Description
VDD	I / Power	System power supply. As S6D0129 has internal regulator, VDD range varies with each mode. Non-regulated mode (PREGB = 1): 1.8 ± 0.15 V (Connected to VDD3) Regulated mode (PREGB = 0) : 1.8 V
VDDM	I / Power	Power supply for internal RAM. Regulated power.
VDDIO	I / Power	I/O power supply for internal interface.
VDDA	I / Power	Power supply for analog circuit block.
VDDO	I / Power	Power supply for oscillator circuit.
PREGB	I	Internal power regulator control input pin. When the internal regulated power is used as VDD, PREGB is fixed to “low” level. When the external logic power (VDD3) is used as VDD, PREGB is fixed to “high” level.
VDD3	I / Power	I/O power supply for external interface. (VDD3: +1.8 ~ +3.3 V)
AVDD	O / Power	A power output pin for source driver block that is generated from power block. Connect a capacitor for stabilization. (AVDD: +3.5 ~ +5.5 V)
GVDD	O / Power	A standard level for grayscale voltage generator. Connect a capacitor for stabilization. When internal GVDD generator is not used, connect an external power supply. (AVDD – 0.5 V)
VCI	I / Power	Analog power supply (VCI : 2.5 ~ 3.3V)
VCI_REF	I / Power	A Reference voltage for VCI. Must connect to VCI at FPC
VSS	I / Power	System ground. (0V)
VSS3	I / Power	System ground level for I/O.
VSSC	I / Power	System ground level for step up circuit block.

Preliminary

Table 9. Power supply pin description (continued)

Symbol	I/O	Description
VSSA	I / Power	System ground level for analog circuit block.
VSSM	I / Power	System ground level for internal RAM.
VSSO	I / Power	System ground level for oscillator circuit.
AVSS	I / Power	System ground level for source driver block.
VGS	I / Power	Gamma ground level.
VCI1	O/ Power	A reference voltage in step-up circuit 1. Connect a capacitor for stabilization. VCI1 can not exceed 2.75 V.
VCL	O/ Power	A power supply pin for generating VcomL. Connect a capacitor for stabilization.
VREFO	O	A reference voltage for GVDD, VCOMH, VCOML.
VREFI	I	A reference voltage for GVDD, VCOMH, VCOML.
Vcom	O	A power supply for the TFT-display counter electrode. The M pin can set the alternating cycle. Connect this pin to the TFT-display counter electrode. This pin is also used as VCI recycling function: When VCIR = “High” period, outputs (S1 to S720) of all source driver are short to VCI level
VcomR	I/O	A reference voltage of VcomH. When VcomH is externally adjusted, halt the internal adjuster of VcomH by setting the register and insert a variable resistor between GVDD and VSS. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.
VcomH	O	This pin indicates a high level of Vcom that is generated from driving the Vcom alternation. Connect this pin to the capacitor for stabilization.
VcomL	O	When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization.
VGH	O/ Power	A positive power output pin for gate driver, internal step-up circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization.

Preliminary

Table 10. Power supply pin description (continued)

Symbol	I/O	Description
VGL	O/ Power	A Negative power output pin for gate driver, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. When internal VGL generator is not used, connect an external-voltage power supply higher than –13.75 V. To protect IC against Latch up, connect the cathode of the schottky diode to the VSS pad. And the anode of the schottky diode to the VGL pad. Refer to application circuit. Connect a capacitor for stabilization.
OSC1, OSC2	I/O	Connect an external resistor for R-C oscillation. When input the clock from outside, input to OSC1, and open OSC2. When use DOTCLK, connect OSC1 pin to VSS3.
C11M, C11P	-	Connect the step-up capacitor for generating the AVDD level.
C21M, C21P C22M, C22P	-	Connect a step-up capacitor for generating the VGH, VGL level.
C31M, C31P	-	Connect a step-up capacitor for generating the VCL level.

Preliminary

SYSTEM/EXTERANL INTERFACE PIN

Table 11. System interface pin description

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM3-1,
IM0/ID</td><td>I</td><td>Selects the MPU interface mode:
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU interface mode</th><th>DB PIN assign</th></tr>
<tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>68-system 16-bit bus interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VDD3</td><td>68-system 8-bit bus interface</td><td>DB17-10</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VDD3</td><td>VSS</td><td>80-system 16-bit bus interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VDD3</td><td>VDD3</td><td>80-system 8-bit bus interface</td><td>DB17-10</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VSS</td><td>ID</td><td>Serial peripheral interface (SPI)</td><td>DB1-0</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VDD3</td><td>*</td><td>Non-selecting</td><td>-</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VSS</td><td>VSS</td><td>68-system 18-bit bus interface</td><td>DB17-0</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VSS</td><td>VDD3</td><td>68-system 9-bit bus interface</td><td>DB17-9</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VDD3</td><td>VSS</td><td>80-system 18-bit bus interface</td><td>DB17-0</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VDD3</td><td>VDD3</td><td>80-system 9-bit bus interface</td><td>DB17-9</td></tr>
<tr><td>VDD3</td><td>VDD3</td><td>*</td><td>*</td><td>Non-selecting</td><td>-</td></tr>
</table>
When a SPI mode is selected, the IM0 pin is used as ID setting bit for a device code.</td></tr>
<tr><td>CSB</td><td>I</td><td>Input pin for chip selection signal.
Low: S6D0129 is selected and can be accessed.
High: S6D0129 is not selected, and cannot be accessed.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select pin.
Low: Index/status, High: Control
Must be fixed at VSS level, when this signal is not used.</td></tr>
<tr><td>RW_WRB/
SCL</td><td>I</td><td>
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>Pin function</th><th>MPU type</th><th>Pin description</th></tr>
<tr><td>*</td><td>VSS</td><td>VSS</td><td>RW</td><td>68-system</td><td>Read/Write operation selection pin.
Low: Write, High: Read</td></tr>
<tr><td>*</td><td>VSS</td><td>VDD3</td><td>WRB</td><td>80-system</td><td>Write strobe signal. (Input pin)
Data is fetched at the rising edge.</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VSS</td><td>SCL</td><td>Serial Peripheral Interface (SPI)</td><td>The synchronous clock signal.
(Input pin)</td></tr>
</table>
</td></tr>
<tr><td>E_RDB</td><td>I</td><td>
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>Pin function</th><th>MPU type</th><th>Pin description</th></tr>
<tr><td>*</td><td>VSS</td><td>VSS</td><td>E</td><td>68-system</td><td>Read/Write operation enable pin.</td></tr>
<tr><td>*</td><td>VSS</td><td>VDD3</td><td>RDB</td><td>80-system</td><td>Read strobe signal. (Input pin)
Read out data at the low level.</td></tr>
</table>
When SPI mode is selected, fix this pin at VSS level.</td></tr>
<tr><td>DB0/SDI</td><td>I/O</td><td>Bi-directional data bus.
18-bit interface: DB 17-0
16-bit interface: DB 17-10, DB 8-1
9-bit interface: DB 17-9
8-bit interface: DB 17-10
Fix DB0 to the VDD3 or VSS level, if the pin is not in use.
For a serial peripheral interface (SPI), input data is fetched at the rising edge of SCL signal.</td></tr>
<tr><td>RESETB</td><td>I</td><td>Reset pin. Initializes the IC, when this signal is low. Must be reset after power-on.</td></tr>
</table>

Preliminary

Table 12. System interface pin description (Continued)

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>DB1/SDO</td><td>I/O</td><td>Bi-directional data bus.
18-bit interface: DB 17-0
16-bit interface: DB 17-10, DB 8-1
9-bit interface: DB 17-9
8-bit interface: DB 17-10
Fix DB1 to the VDD3 or VSS level, if the pin is not in use.
For a serial peripheral interface (SPI), serves as the serial data output pin (SDO). Successive bits are output at the falling edge of the SCL signal.</td></tr>
<tr><td>DB17-DB2</td><td>I/O</td><td>Bi-directional data bus.
18-bit interface: DB 17-0
16-bit interface: DB 17-10, DB 8-1
9-bit interface: DB 17-9
8-bit interface: DB 17-10
Fix unused pin to the VDD3 or VSS level.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>Data enable signal pin for RGB interface.
EPL=”0”: Only in case of ENABLE=”Low”, the IC can be access via RGB interface.
EPL=”1”: Only in case of ENABLE=”High”, the IC can be access via RGB interface.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>GRAM write</th><th>GRAM address</th></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>0</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>1</td><td>Valid</td><td>Updated</td></tr>
</table>
Fix ENABLE pin at VDD3 or VSS level, if the pin is not used.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Synchronous signal of frame.
VSPL= “0”: Low active, VSPL=”1”: High active
Fix this pin at VDD3 or VSS level, if the pin is not used.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>Synchronous signal of line.
HSPL=”0”: Low active, HSPL=”1”: High active
Fix this pin at VDD3 or VSS level, if the pin is not used.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>Input pin for clock signal of external interface: dot clock.
DPL=”0”: Display data is fetched at rising edge of DOTCLK.
DPL=”1”: Display data is fetched at falling edge of DOTCLK.
Fix this pin at VDD3 or VSS level, if the pin is not used.</td></tr>
<tr><td>PD17-PD0</td><td>I</td><td>RGB data input bus.
18-bit interface: PD 17-0
16-bit interface: PD 17-13, PD 11-1
6-bit interface: PD 17-12
Fix unused pin to the VDD3 or VSS level.</td></tr>
</table>

Preliminary

DISPLAY PIN

Table 13. Display pin description

Symbol	I/O	Description
S1 – S720	O	Source driver output pins. The SS bit can change the shift direction of the source signal. Example] If SS = 0, gray data of S1 is read from RAM address 0000h. If SS = 1, contents of RAM address 0000h is out from S720. S1, S4, S7, ... S (3n-1): display Red (R) (BGR = 0) S2, S5, S8, ... S (3n-2): display Green (G) (BGR = 0) S3, S6, S9, ... S (3n): display Blue (B) (BGR = 0)
G1 – G320	O	Gate driver output pins. The output of driving circuit is whether VGH or VGL. VGH: gate-ON level VGL: gate-OFF level

MISCELLANEOUS PIN

Table 14. Oscillator and internal power regulator pin description

Symbol	I/O	Description
TEST_MODE0 TEST_MODE1 TEST_MODE2 TEST_MUX/ TEST_GRAY	I	Input pin for test. In normal operation, connect this pin to VSS3.
NDTREE_OUT/ DISPTMG/ PREC/ M/ CL1/ ESC/ FLM/ TSO1/ TSO0	O	Output pin for test. In normal operation, leave this pin open.
DUMMY	-	Dummy pin. Open or connect VSS3.

Preliminary

FUNCTIONAL DESCRIPTION

SYSTEM INTERFACE

The S6D0129 has nine high-speed system interfaces: an 80-system 18-/16-/9-/8-bit bus, a 68-system 18-/16-/9-/8-bit bus, and a serial interface (SPI: Serial Peripheral Interface). The IM3-0 pins select the interface mode.
The S6D0129 has three 18-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR is a register to store index information from each control register. The WDR is a register that temporarily stores data to be written into each control register and GRAM. The RDR is a register to temporarily store data to be read data from GRAM. The data to be written to GRAM from MPU is once written to the WDR and then automatically written to GRAM by internal operation. Since data are read through the RDR from GRAM, the data read out first are invalid and the ensuring data are read out normally.

Table 15. Register Selection (18-/16-/9-/8- Parallel Interface)

SYSTEM	RW_WRB	E_RDB	RS	Operations
68	0	1	0	Write index to IR
	1	1	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	1	1	Read from GRAM through RDR
80	0	1	0	Write index to IR
	1	0	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	0	1	Read from GRAM through RDR

Table 16. CSB signal (GRAM update control)

CSB	Operation
0	Data is written to GRAM, GRAM address is updated
1	Data is not written to GRAM, GRAM address is not updated

Table 17. Register Selection (Serial Peripheral Interface)

R/W bit	RS bit	Operation
0	0	Write index to IR
1	0	Read internal status
0	1	Write data to control register and GRAM through WDR
1	1	Read data from GRAM through RDR

Preliminary

EXTERNAL INTERFACE (RGB-I/F, VSYNC-I/F)

The S6D0129 incorporates RGB and VSYNC interface as external interface for motion picture display.
When the RGB interface is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for display. The RGB data for display (PD17-0) are written according to enable signal (ENABLE) and data valid signal (VLD) in synchronization with VSYNC, HSYNC, and DOTCLK signal. This allows flicker-free updating of the screen.
When the VSYNC interface is selected, internal operation is normally synchronized with internal clock except operation related to frame synchronization: It is synchronized with the VSYNC signal. The data for display are written to GRAM via conventional system interface. There are some limitations on the timing and methods for writing to GRAM in VSYNC interface. See the section on the EXTERNAL DISPLAY INTERFACE.

ADDRESS COUNTER (AC)

The address counter (AC) assigns address to GRAM. When an address-set-instruction is written to the IR, the address information is sent from IR to AC. After writing to the GRAM, the address value of AC is automatically increased/ decreased by 1 according to ID1-0 bit of control register. After reading data from GRAM, the AC is not updated. A window address function allows data to be written only to a window area specified by GRAM.

GRAPHICS RAM (GRAM)

The graphics RAM (GRAM) has 18-bits/pixel and stores the bit-pattern data for 240-RGB x 320 dot display.

GRAYSCALE VOLTAGE GENERATOR

The grayscale voltage circuit generates a certain voltage level that is specified by the grayscale Υ-adjusting resistor for LCD driver circuit. By use of the generator, 262,144 colors can be displayed at the same time. For details, see the GAMMA-ADJUSTING RESISTOR section.

TIMING GENERATOR

The timing generator generates timing signals for the operation of internal circuits such as GRAM.
The GRAM read timing for display and the internal operation timing for MPU access is generated separately to avoid interference with one another. Several important timing signals can be monitored via signal monitoring pin (M, FLM, CL1, VCIR, DISPTMG).

OSCILLATION CIRCUIT (OSC)

The S6D0129 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pin. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulse can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the OSCILLATION CIRCUIT section.

Preliminary

SOURCE DRIVER CIRCUIT

The liquid crystal display source driver circuit consists of 720 drivers (S1 to S720).
Display pattern data is latched when 720-channel data has arrived. The latched data then enables the source drivers to generate drive waveform outputs. The SS bit can change the shift direction of 720-channel data by selecting an appropriate direction for the device-mounted configuration.

GATE DRIVER CIRCUIT

The liquid crystal display gate driver circuit consists of 320 gate drivers (G1 to G320).
The VGH or VGL level is output by the signal from the gate control circuit.

Preliminary

SYSTEM/RGB INTERFACE AND GRAM ADDRESS SETTING

GRAM ADDRESS SETTING (SS="0")

When SS bit is 0 (source output shift direction: right) and BGR bit is 0 (RGB sequence: right) that can be set in R01h register, GRAM address is set as follows:

Table 18. GRAM address (SS="0")

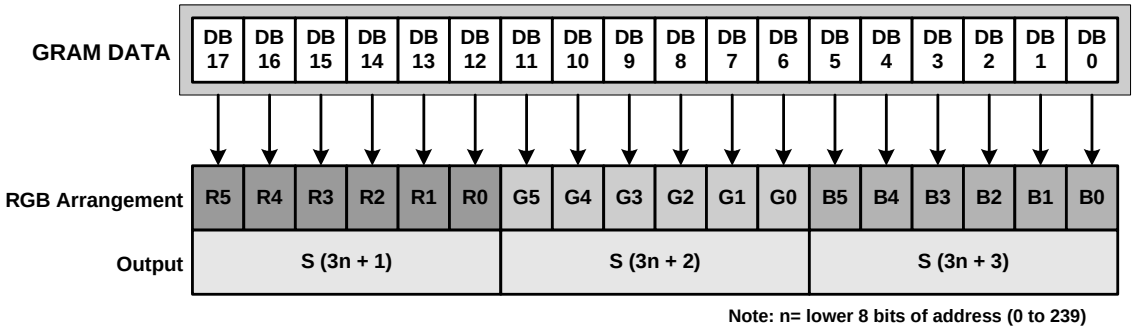
S/G Output		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB 17 ..... DB 0			DB 17 ..... DB 0			DB 17 ..... DB 0			DB 17 ..... DB 0				DB 17 ..... DB 0			DB 17 ..... DB 0			DB 17 ..... DB 0			DB 17 ..... DB 0		
G1	G320	"0000"H			"0001"H			"0002"H			"0003"H			.....	"00EC"H			"00ED"H			"00EE"H			"00EF"H		
G2	G319	"0100"H			"0101"H			"0102"H			"0103"H			.....	"01EC"H			"01ED"H			"01EE"H			"01EF"H		
G3	G318	"0200"H			"0201"H			"0202"H			"0203"H			.....	"02EC"H			"02ED"H			"02EE"H			"02EF"H		
G4	G317	"0300"H			"0301"H			"0302"H			"0303"H			.....	"03EC"H			"03ED"H			"03EE"H			"03EF"H		
G5	G316	"0400"H			"0401"H			"0402"H			"0403"H			.....	"04EC"H			"04ED"H			"04EE"H			"04EF"H		
G6	G315	"0500"H			"0501"H			"0502"H			"0503"H			.....	"05EC"H			"05ED"H			"05EE"H			"05EF"H		
G7	G314	"0600"H			"0601"H			"0602"H			"0603"H			.....	"06EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G313	"0700"H			"0701"H			"0702"H			"0703"H			.....	"07EC"H			"07ED"H			"07EE"H			"07EF"H		
G9	G312	"0800"H			"0801"H			"0802"H			"0803"H			.....	"08EC"H			"08ED"H			"08EE"H			"08EF"H		
G10	G311	"0900"H			"0901"H			"0902"H			"0903"H			.....	"09EC"H			"09ED"H			"09EE"H			"09EF"H		
G11	G310	"0A00"H			"0A01"H			"0A02"H			"0A03"H			.....	"0AEC"H			"0AED"H			"0AEE"H			"0EEF"H		
G12	G309	"0B00"H			"0B01"H			"0B02"H			"0B03"H			.....	"0BEC"H			"0BED"H			"0BEE"H			"0BEF"H		
G13	G308	"0C00"H			"0C01"H			"0C02"H			"0C03"H			.....	"0CEC"H			"0CED"H			"0CEE"H			"0CEF"H		
G14	G307	"0D00"H			"0D01"H			"0D02"H			"0D03"H			.....	"0DEC"H			"0DED"H			"0DEE"H			"0DEF"H		
G15	G306	"0E00"H			"0E01"H			"0E02"H			"0E03"H			.....	"0EEC"H			"0EED"H			"0EEE"H			"0EEF"H		
G16	G305	"0F00"H			"0F01"H			"0F02"H			"0F03"H			.....	"0FEC"H			"0FED"H			"0FEE"H			"0FEF"H		
G17	G304	"1000"H			"1001"H			"1002"H			"1003"H			.....	"10EC"H			"10ED"H			"10EE"H			"10EF"H		
G18	G303	"1100"H			"1101"H			"1102"H			"1103"H			.....	"11EC"H			"11ED"H			"11EE"H			"11EF"H		
G19	G302	"1200"H			"1201"H			"1202"H			"1203"H			.....	"12EC"H			"12ED"H			"12EE"H			"12EF"H		
G20	G301	"1300"H			"1301"H			"1302"H			"1303"H			.....	"13EC"H			"13ED"H			"13EE"H			"13EF"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G313	G8	"13800"H			"13801"H			"13802"H			"13803"H			.....	"138EC"H			"138ED"H			"138EE"H			"138EF"H		
G314	G7	"13900"H			"13901"H			"13902"H			"13903"H			.....	"139EC"H			"139ED"H			"139EE"H			"139EF"H		
G315	G6	"13A00"H			"13A01"H			"13A02"H			"13A03"H			.....	"13AEC"H			"13AED"H			"13AEE"H			"13AEF"H		
G316	G5	"13B00"H			"13B01"H			"13B02"H			"13B03"H			.....	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			.....	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			.....	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			.....	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			.....	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		

Data fetch from GRAM for display when SS=0 is shown in the following figure.

Preliminary

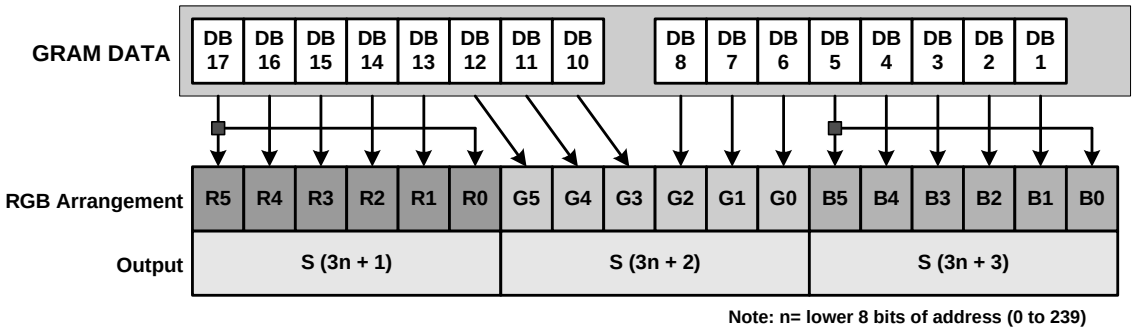
SYSTEM INTERFACE

68/80-system 18-bit interface



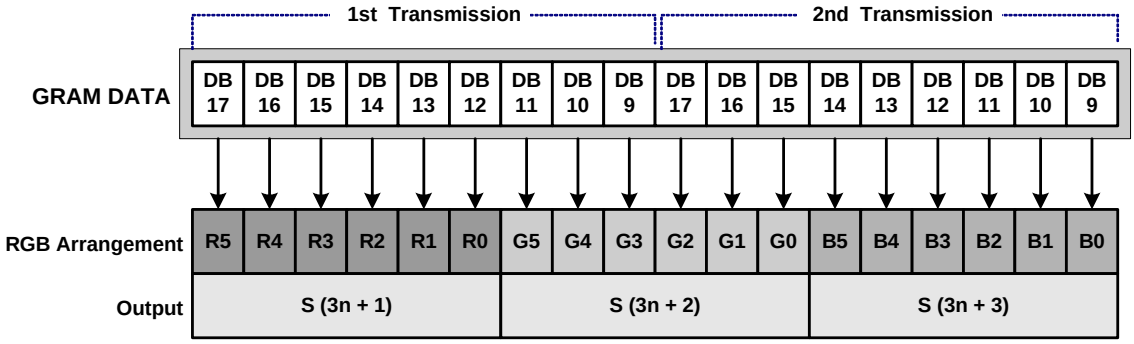
Note: n= lower 8 bits of address (0 to 239)

68/80-system 16-bit interface



Note: n= lower 8 bits of address (0 to 239)

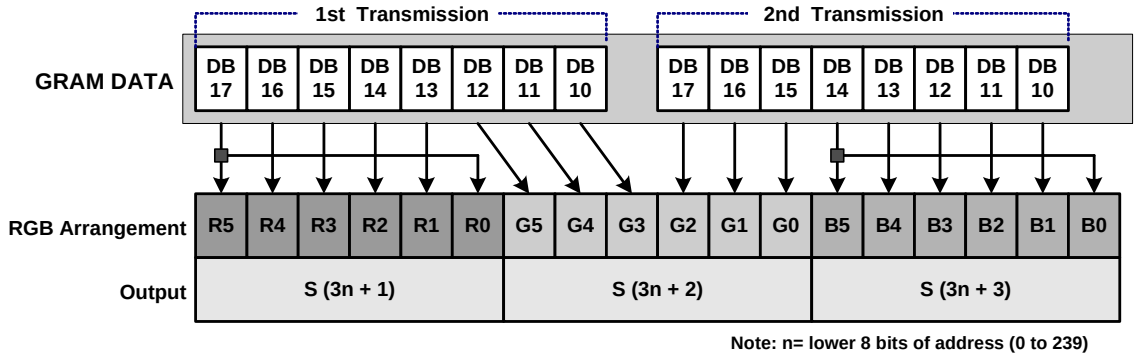
68/80-system 9-bit interface



Note: n= lower 8 bits of address (0 to 239)

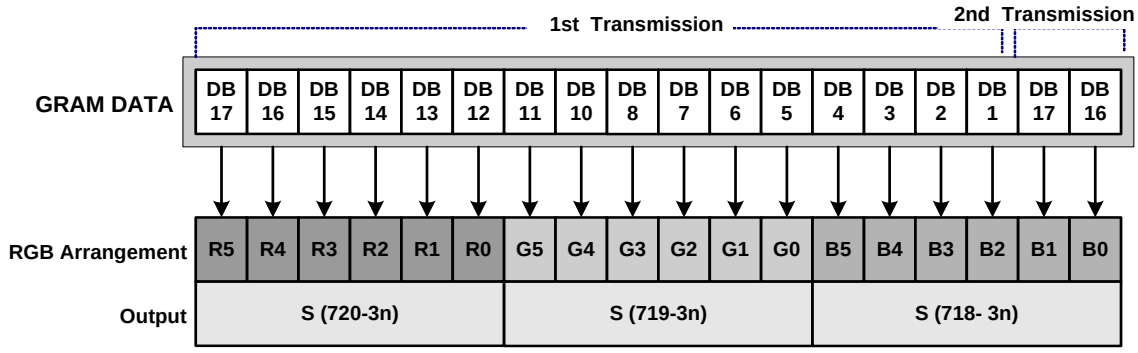
Preliminary

68/80-system 8-bit interface (TRI=0, DFM=0)



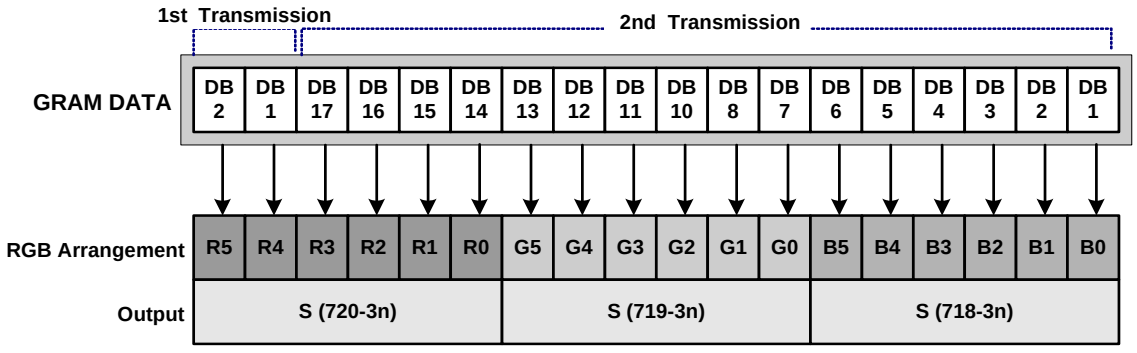
Note: n= lower 8 bits of address (0 to 239)

80-system 16-bit interface (TRI=1, DFM=0): 2 times transmission (262 K color)



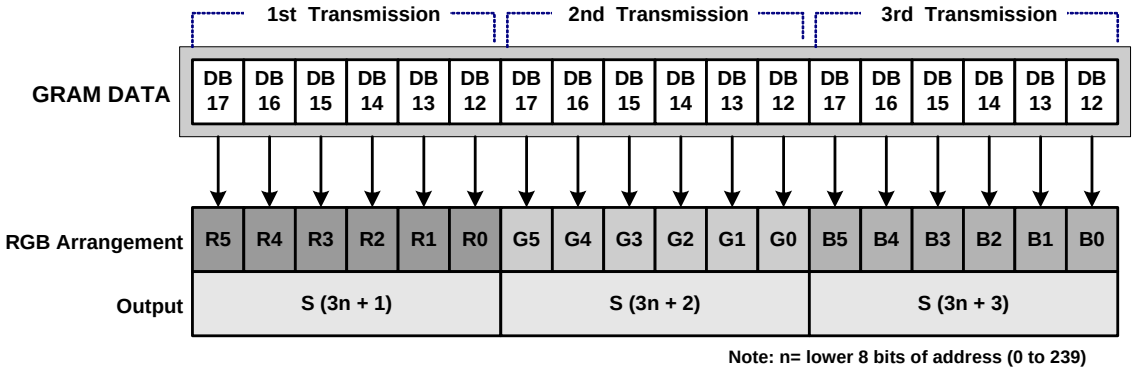
Note: n= lower 8 bits of address (0 to 239)

80-system 16-bit interface (TRI=1, DFM=1): 2 times transmission (262 K color)



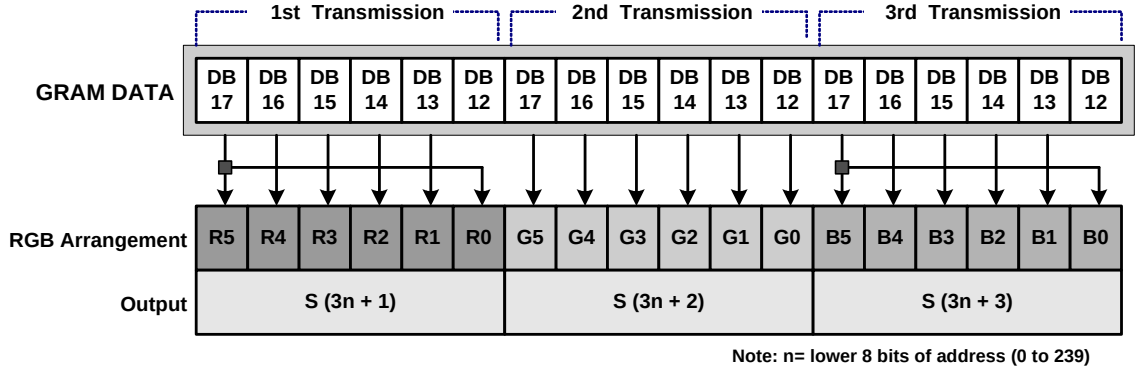
Note: n= lower 8 bits of address (0 to 239)

80-system 8-bit interface (TRI=1, DFM=0)



Note: n= lower 8 bits of address (0 to 239)

80-system 8-bit interface (TRI=1, DFM=1)

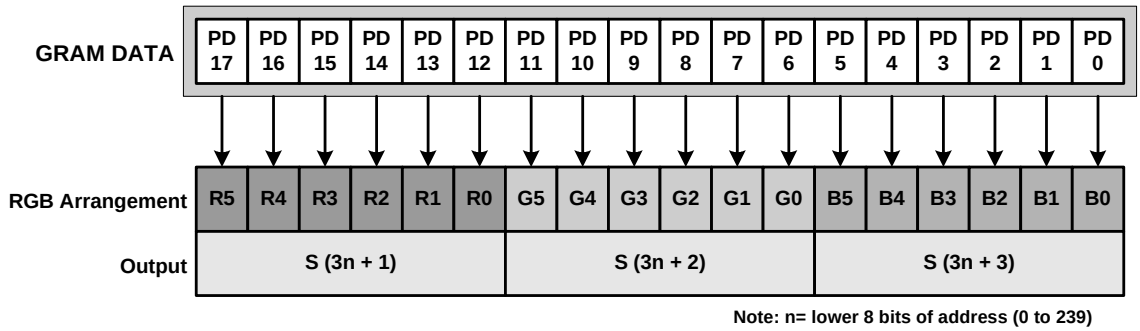


Note: n= lower 8 bits of address (0 to 239)

Preliminary

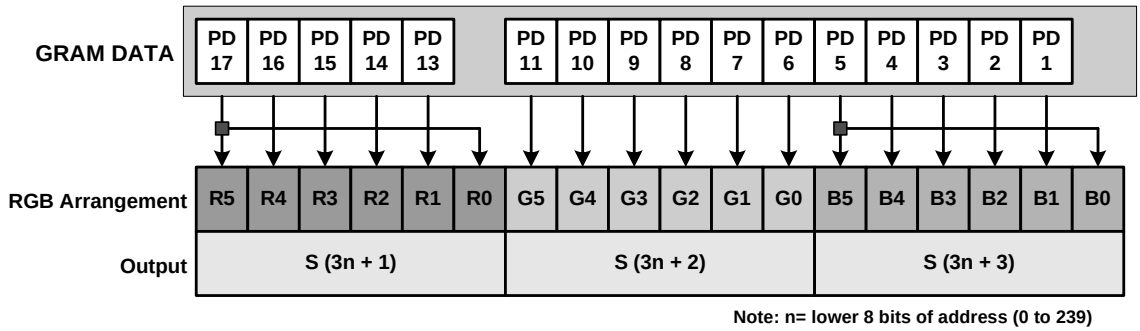
RGB INTERFACE

18-bit RGB interface



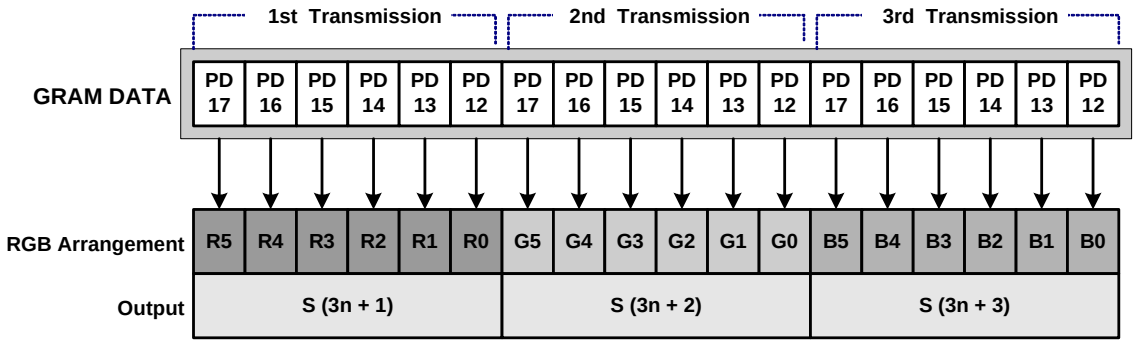
Note: n= lower 8 bits of address (0 to 239)

16-bit RGB interface



Note: n= lower 8 bits of address (0 to 239)

6-bit RGB interface



Note: n= lower 8 bits of address (0 to 239)

Preliminary

GRAM ADDRESS SETTING (SS="1")

When SS bit is 1 (source output shift direction: reversed) and BGR bit is 1 (RGB sequence: reversed) that can be set in R01h register, GRAM address is set as follows:

Table 19. GRAM address (SS="1")

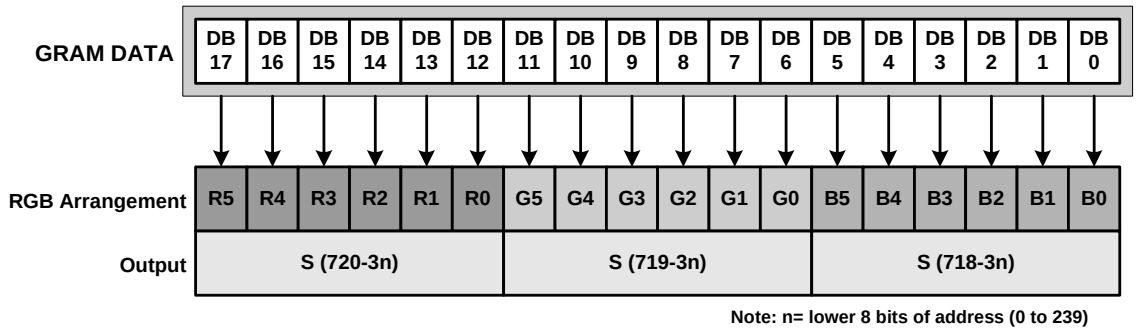
S/G Output		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB 0 ..... DB 17			DB 0 ..... DB 17			DB 0 ..... DB 17			DB 0 ..... DB 17				DB 0 ..... DB 17			DB 0 ..... DB 17			DB 0 ..... DB 17			DB 0 ..... DB 17		
G1	G320	"00EF"H			"00EE"H			"00ED"H			"00EC"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G319	"01EF"H			"01EE"H			"01ED"H			"01EC"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G318	"02EF"H			"02EE"H			"02ED"H			"02EC"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G317	"03EF"H			"03EE"H			"03ED"H			"03EC"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G316	"04EF"H			"04EE"H			"04ED"H			"04EC"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G315	"05EF"H			"05EE"H			"05ED"H			"05EC"H			.....	"0503"H			"0502"H			"0501"H			"0500"H		
G7	G314	"06EF"H			"06EE"H			"06ED"H			"06EC"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G313	"07EF"H			"07EE"H			"07ED"H			"07EC"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G312	"08EF"H			"08EE"H			"08ED"H			"08EC"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G311	"09EF"H			"09EE"H			"09ED"H			"09EC"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G310	"0EEF"H			"0AEE"H			"0AED"H			"0AEC"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G309	"0BEF"H			"0BEE"H			"0BED"H			"0BEC"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G308	"0CEF"H			"0CEE"H			"0CED"H			"0CEC"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G307	"0DEF"H			"0DEE"H			"0DED"H			"0DEC"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G306	"0EEF"H			"0EEE"H			"0EED"H			"0EEC"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G305	"0FEF"H			"0FEE"H			"0FED"H			"0FEC"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G304	"10EF"H			"10EE"H			"10ED"H			"10EC"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G303	"11EF"H			"11EE"H			"11ED"H			"11EC"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G302	"12EF"H			"12EE"H			"12ED"H			"12EC"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G301	"13EF"H			"13EE"H			"13ED"H			"13EC"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G313	G8	"138EF"H			"138EE"H			"138ED"H			"138EC"H			.....	"13803"H			"13802"H			"13801"H			"13800"H		
G314	G7	"139EF"H			"139EE"H			"139ED"H			"139EC"H			.....	"13903"H			"13902"H			"13901"H			"13900"H		
G315	G6	"13AEF"H			"13AEE"H			"13AED"H			"13AEC"H			.....	"13A03"H			"13A02"H			"13A01"H			"13A00"H		
G316	G5	"13BEF"H			"13BEE"H			"13BED"H			"13BEC"H			.....	"13B03"H			"13B02"H			"13B01"H			"13B00"H		
G317	G4	"13CEF"H			"13CEE"H			"13CED"H			"13CEC"H			.....	"13C03"H			"13C02"H			"13C01"H			"13C00"H		
G318	G3	"13DEF"H			"13DEE"H			"13DED"H			"13DEC"H			.....	"13D03"H			"13D02"H			"13D01"H			"13D00"H		
G319	G2	"13EEF"H			"13EEE"H			"13EED"H			"13EEC"H			.....	"13E03"H			"13E02"H			"13E01"H			"13E00"H		
G320	G1	"13FEF"H			"13FEE"H			"13FED"H			"13FEC"H			.....	"13F03"H			"13F02"H			"13F01"H			"13F00"H		

Data fetch from GRAM for display when SS=1 is shown in the following figure.

Preliminary

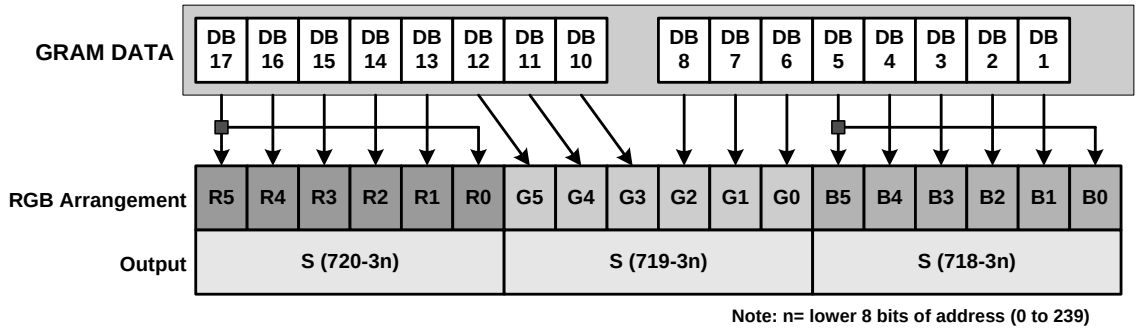
SYSTEM INTERFACE

68/80-system 18-bit interface



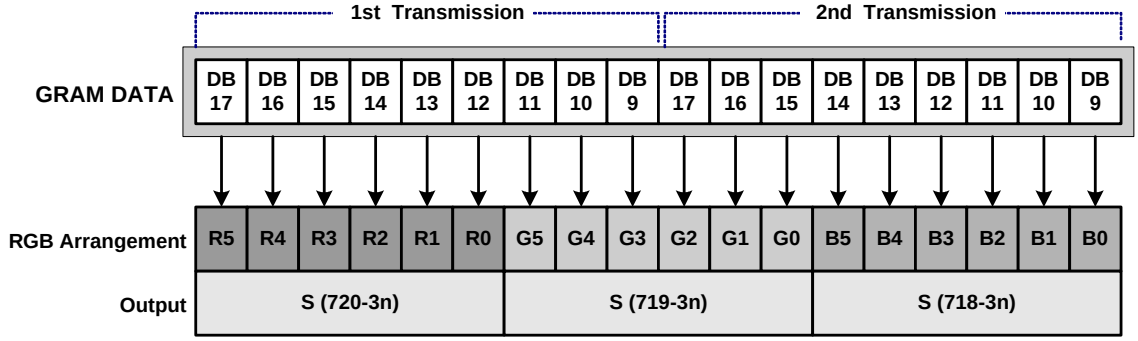
Note: n= lower 8 bits of address (0 to 239)

68/80-system 16-bit interface



Note: n= lower 8 bits of address (0 to 239)

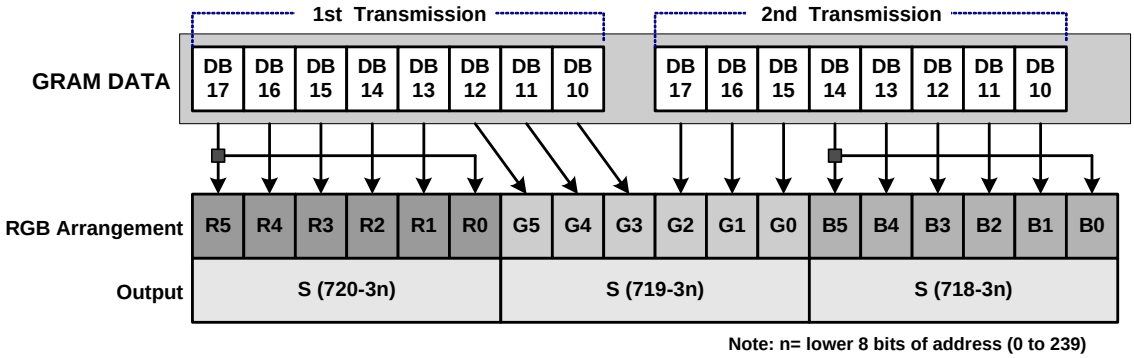
68/80-system 9-bit interface



Note: n= lower 8 bits of address (0 to 239)

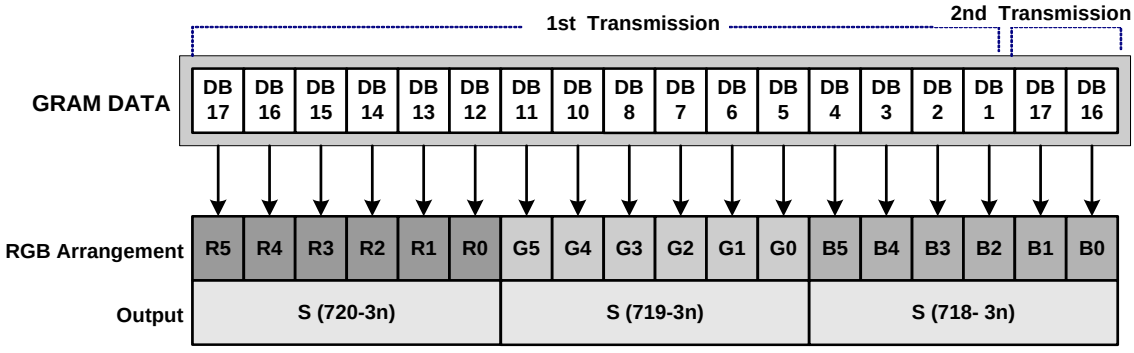
Preliminary

68/80-system 8-bit interface (TRI=0, DFM=0)



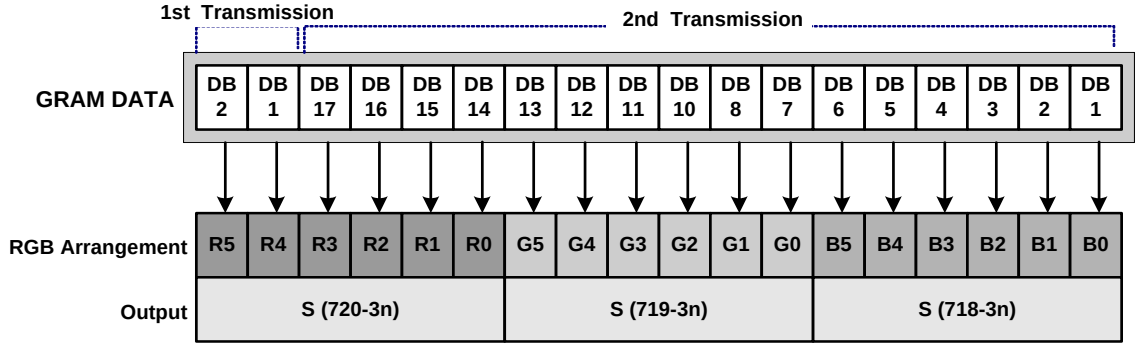
Note: n= lower 8 bits of address (0 to 239)

80-system 16-bit interface (TRI=1, DFM=0): 2 times transmission (262 K color)



Note: n= lower 8 bits of address (0 to 239)

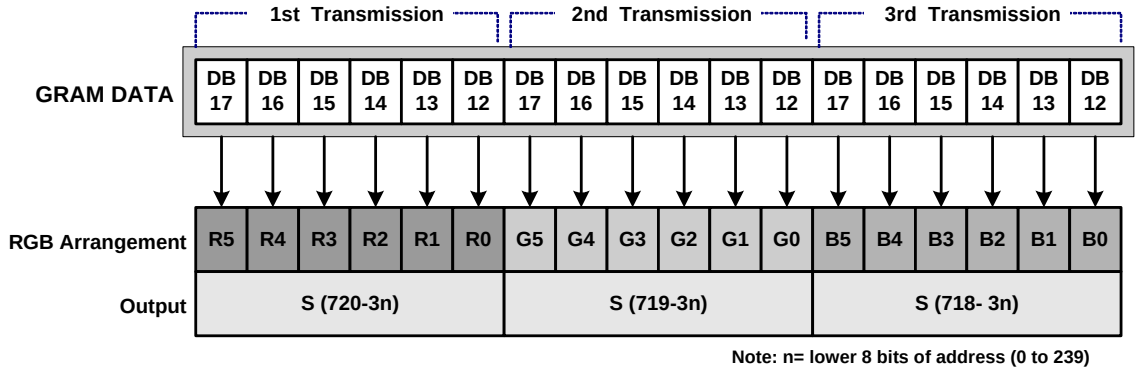
80-system 16-bit interface (TRI=1, DFM=1): 2 times transmission (262 K color)



Note: n= lower 8 bits of address (0 to 239)

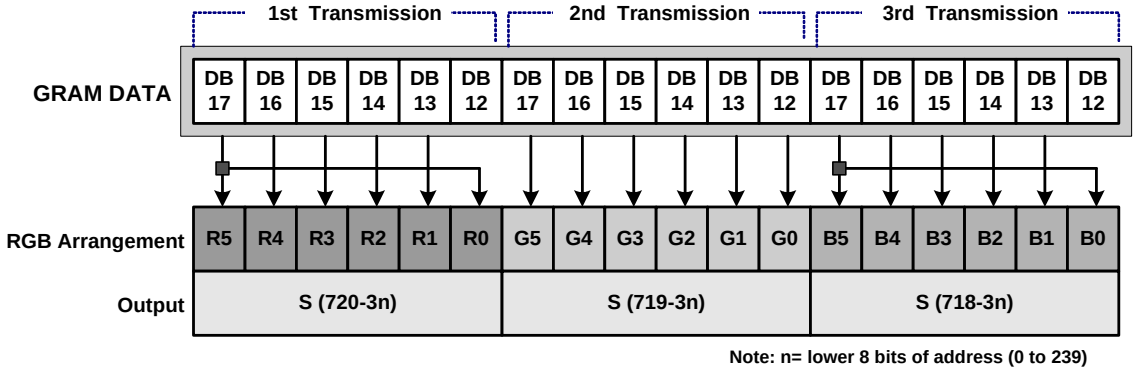
Preliminary

80-system 8-bit interface (TRI=1, DFM=0): 3 times transmission (262 K color)



Note: n= lower 8 bits of address (0 to 239)

80-system 8-bit interface (TRI=1, DFM=1): 3 times transmission (65 K color)

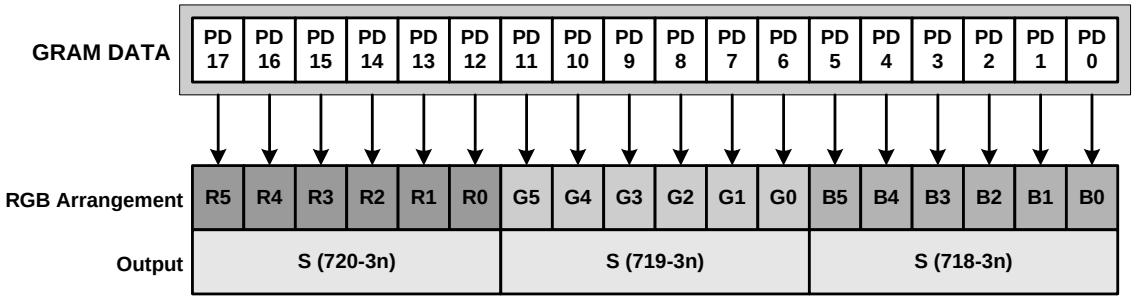


Note: n= lower 8 bits of address (0 to 239)

Preliminary

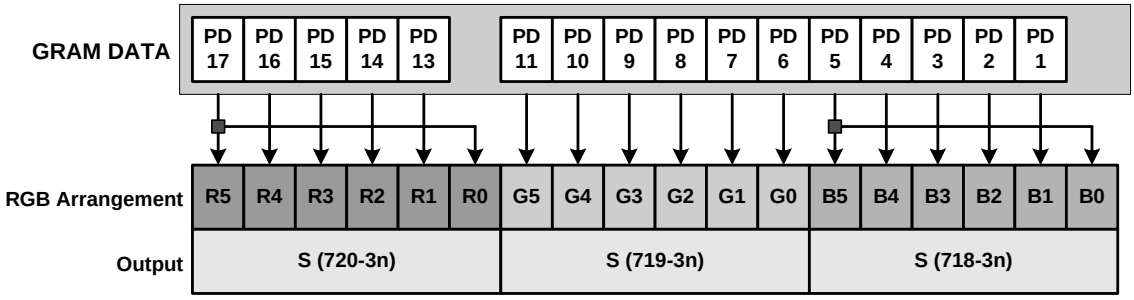
RGB INTERFACE

18-bit interface



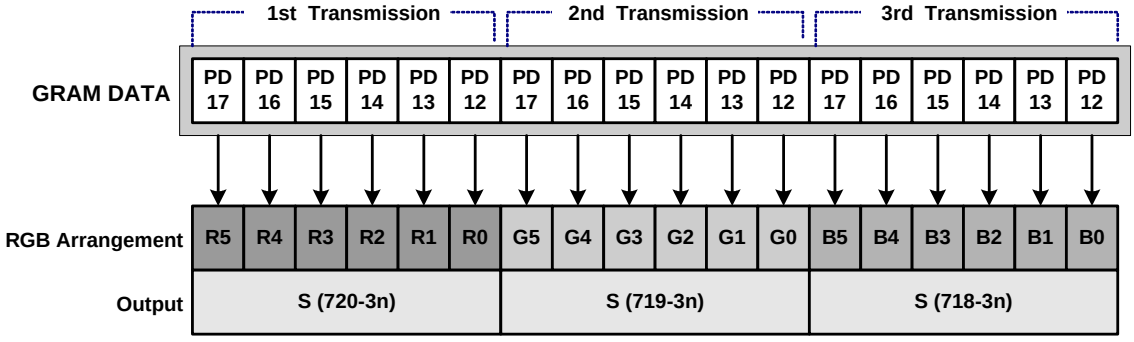
Note: n= lower 8 bits of address (0 to 239)

16-bit interface



Note: n= lower 8 bits of address (0 to 239)

6-bit interface



Note: n= lower 8 bits of address (0 to 239)

Preliminary

INSTRUCTIONS

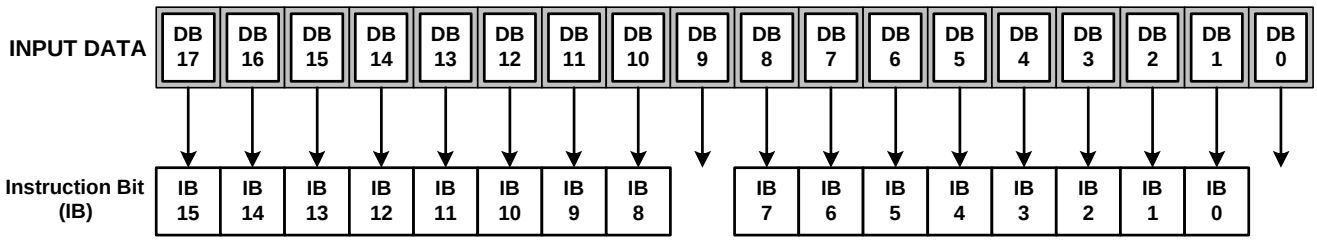
The S6D0129 uses the 18-bit bus architecture. Before the internal operation of the S6D0129 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the S6D0129 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB17 to DB0), make up the S6D0129 instructions.
There are nine categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table
- Interface with the gate driver and power supply IC

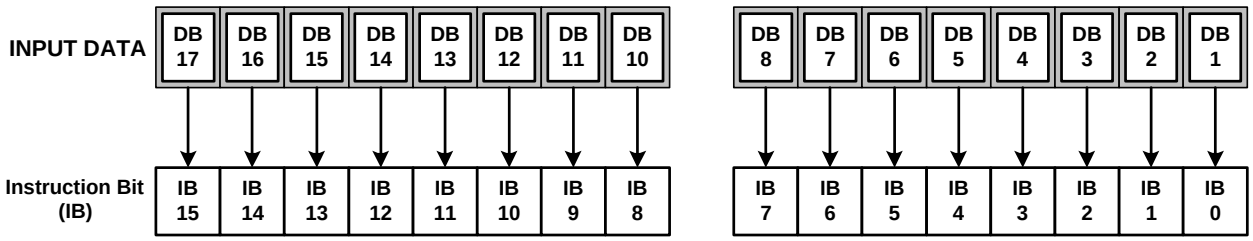
Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. As instructions are executed in 0 cycles, they can be written in succession.

The 16-bit instruction assignment differs from interface-setup (18-/16-/9-/8-/SPI), so instructions should be fetched according to the data format shown below:

80-system 18-bit Interface

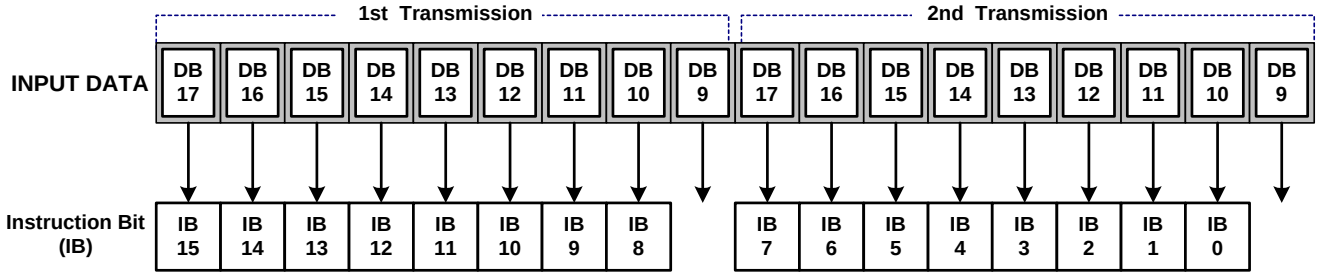


80-system 16-bit Interface

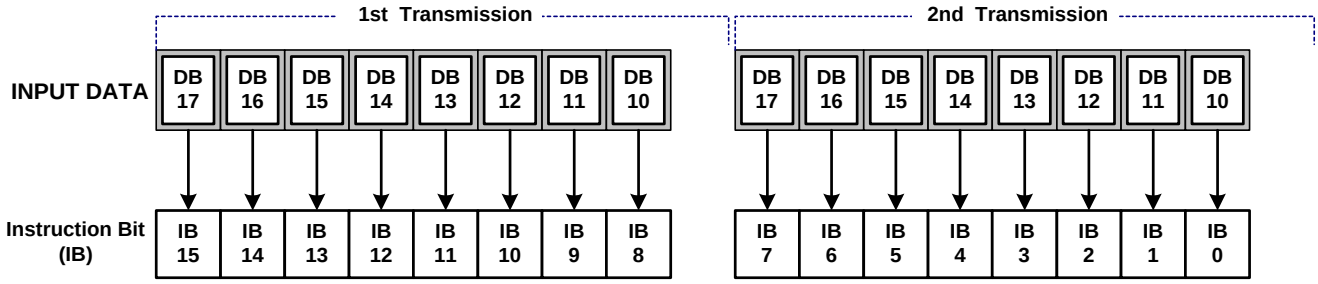


Preliminary

80-system 9-bit Interface



80-system 8-bit Interface/SPI



Preliminary

INSTRUCTION TABLE

Table 20. Instruction Table

Reg. No	R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	Register Name / Description
IR	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**Index /** Sets the index register value
SR	1	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0	**Status read /** Reads the internal status of the S6D0129
R00h	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	**Start oscillation(R00H) /** Starts the oscillation circuit
	1	1	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	**Device code read /** Read 0129H
R01h	0	1	0	VSPL	HSPL	DPL	EPL	0	GS	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0	**Driver output control(R01H) /** VSPL: set polarity of VSYNC pin. HSPL: set polarity of HSYNC pin. DPL: set polarity of DOTCLK pin. EPL: set polarity of ENABLE pin GS: gate driver shift direction SS: source driver shift direction NL5-0: number of driving lines
R02h	0	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	**LCD-Driving-waveform control (R02H)/** FLD1-0: number of interlaced field B/C: LCD drive AC waveform EOR: Exclusive OR-ing the AC waveform NW5-0: n raster row inversion
R03h	0	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	0	0	0	**Entry mode(R03H) /** TRI: 8-bit interface mode DFM: defines color depth for the IC BGR: RGB swap control I/D1-0: address counter Increment / Decrement control AM: horizontal / vertical RAM update
R07h	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	0	GON	CL	REV	D1	D0	**Display control (R07H) /** PT1-0: Non-display area source output control VLE2-1: 1^{st} /2^{nd} partial vertical scroll SPT: 1^{st} /2^{nd} partial display enable GON: gate on/off control CL: 8-color display mode enable REV: display area inversion drive D1-0: source output control
R08h	0	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0	**Blank period control 1 (R08H)/** FP3-0: Front porch setting BP3-0: Back porch setting
R09h	0	1	0	0	0	0	0	0	0	0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0	**Gate non display area control (R09H)** PTG1-0: Non-display area gate output control. ISC3-0: Non-display area gate interval scan control
R0Bh	0	1	NO1	NO0	SDT1	SDT0	VCIR 2	VCIR 1	VCIR 0	DIV1	DIV0	0	DCR_ EX	DCR2	DCR1	DCR0	RTN1	RTN0	**Frame cycle control (R0BH)/** NO1-0: specify the amount of non-overlap SDT1-0: set amount of source delay VCIR2-0: VCI recycling period setting DIV1-0: division ratio of internal clock setting DCR_EX: Input signal selection. DCR2-0:Set clock cycle for step-up circuit. RTN10: set the 1-H period
R0Ch	0	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0	**External interface control(R0CH) /** RM: specify the interface for RAM access DM1-0: specify display operation mode RIM1-0: specify RGB-I/F mode
R10h	0	1	0	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	0	0	0	SLP	STB	**Power control 1 (R10H) /** SAP2-0:Adjust fixed current BT2-0:Adjust scale factor DC2-0:Adjust the frequency SLP: sleep mode control STB: standby mode control
R11h	0	1	0	0	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0	0	0	0	0	0	VC2	VC1	VC0	**Power control 2 (R11H)/** GVD5-0:set GVDD voltage VC2-0:set VCI1 voltage

Preliminary

Table 21. Instruction Table (Continued)

Reg. No	R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	Register Name / Description
R13h	0	1	0	0	0	0	0	0	0	0	0	PON	PON1	AON	0	0	0	0	**Power control 3 (R13H)/** PON: booster circuit control PON1: booster circuit control AON: operationt start bit for the amplifer.
R14h	0	1	0	VCMR	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VML5	VML4	VML3	VML2	VML1	VML0	**Power control 4 (R14H)/** VCMR: VCOMH control VCM5-0:set the VCOMH voltage VML5-0:set the amplitude of VCOM voltage
R20h	0	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	**RAM address set (R20H&R21H)/** AD16-0:set GRAM address.
R21h	0	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	
R22h	0	1	**WD17-0 : Pin assignment varies according to the interface method**																**Write data to GRAM (R22H)/** WD17-0:Input data for GRAM
	1	1	**RD17-0 : Pin assignment varies according to the interface method**																**Read data from GRAM (R22H)/** RD17-0:Read data from GRAM
R30h	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00	**Gamma control 1 (R30H)/** Adjust Gamma voltage
R31h	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20	**Gamma control 2 (R31H)/** Adjust Gamma voltage
R32h	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40	**Gamma control 3 (R32H)/** Adjust Gamma voltage
R33h	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00	**Gamma control 4 (R33H)/** Adjust Gamma voltage
R34h	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00	**Gamma control 5 (R34H)/** Adjust Gamma voltage
R35h	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20	**Gamma control 6 (R35H)/** Adjust Gamma voltage
R36h	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40	**Gamma control 7 (R36H)/** Adjust Gamma voltage
R37h	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00	**Gamma control 8 (R37H)/** Adjust Gamma voltage
R38h	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00	**Gamma control 9 (R38H)/** Adjust Amplitude voltage
R39h	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00	**Gamma control 10 (R39H)/** Adjust Amplitude voltage
R40h	0	1	0	0	0	0	0	0	0	0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	**Gate scan position (R40H)/** SCN5-0: scan starting position of gate
R41h	0	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	**Vertical scroll control (R41H)/** VL8-0:
R42h	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	**1st screen driving position (R42H, R43H)** SE18-10: 1st screen end position SS18-10: 1st screen start position
R43h	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	
R44h	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	**2nd screen driving position (R44H, R45H)** SE28-20: 2nd screen end position SS28-20: 2nd screen start position
R45h	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	
R46h	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	**Horizontal window address (R46H)** HSA7-0: Horizontal window address start position HEA7-0: Horizontal window address end position
R47h	0	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	**Vertical window Address (R47H, R48H)** VEA8-0: Vertical window address end position VSA8-0: Vertical window address start position
R48h	0	1	0	0	0	0	0	0		VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
R71h	0	1	Test command1																**Don't use this command**
R72h	0	1	Test command2																**Don't use this command**

INSTRUCTION DESCRIPTIONS

Index

The index instruction specifies the RAM control indexes (R00h to R7Fh). It sets the register number in the range of 000000 to 1111111 in binary form. However, R71h to R72h are used for test registers.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Status Read

The status read instruction read out the internal status of the IC.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0

L8–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1

The start oscillation instruction restarts the oscillator from the Halt State in the standby mode. After this instruction, wait at least 10 ms for oscillation to stabilize before giving the next instruction.
(See the Power Control 1 Register (R10h))

If this register is read forcibly, *0129h is read.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VSPL	HSPL	DPL	EPL	0	GS	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0

VSPL: reverses the polarity of the VSYNC signal.
VSPL= “0”: VSYNC is low active.
VSPL= “1”: VSYNC is high active.

HSPL: reverses the polarity of the HSYNC signal.
HSPL= “0”: HSYNC is low active.
HSPL= “1”: HSYNC is high active.

DPL: reverses the polarity of the DOTCLK signal.
DPL= “0”: Display data is fetched on the rising edge of DOTCLK.
DPL= “1”: Display data is fetched on the falling edge of DOTCLK.

EPL: Set the polarity of ENABLE pin while using RGB interface.

EPL = “0”: ENABLE = ”Low” / write data of PD17-0
ENABLE = ”High” / don’t write data of PD17-0
EPL = “1”: ENABLE = ”High” / write data of PD17-0
ENABLE = ”Low” / don’t write data of PD17-0

Table 22. Relationship between EPL, ENABLE and RAM access

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
0	1	Invalid	Held
1	1	Valid	Updated
1	0	Invalid	Held

GS: Selects the output shift direction of the gate driver. When GS = 0, G1 shifts to G320. When GS = 1, G320 shifts to G1.

SS: Selects the output shift direction of the source driver. When SS = 0, S1 shifts to S720. When SS = 1, S720 shifts to S1. In addition, SS and BGR bits should be specified in case of the RGB order is changed. When SS = 0 and BGR = 0, <R><G><B> are assigned in order from S1 pin. When SS = 1 and BGR = 1, <R><G><B> are assigned in order from S720. Re-write data to GRAM whenever SS and BGR bit are changed.

NL5–0: Specify the number of raster-rows to be driven. The number of raster-row can be adjusted in units of eight. The address mapping of GRAM is independent of this setting. The set value should be higher than the panel size.

Table 23. NL bit and Drive Duty (SCN5-0=00_0000)

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	LCD Raster Rows	Gate- Lines Used
0	0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	0	1	240RGB X 16	16	G1 to G16
0	0	0	0	1	0	240RGB X 24	24	G1 to G24
0	0	0	0	1	1	240RGB X 32	32	G1 to G32
0	0	0	1	0	0	240RGB X 40	40	G1 to G40
0	0	0	1	0	1	240RGB X 48	48	G1 to G48
0	0	0	1	1	0	240RGB X 56	56	G1 to G56
0	0	0	1	1	1	240RGB X 64	64	G1 to G64
0	0	1	0	0	0	240RGB X 72	72	G1 to G72
0	0	1	0	0	1	240RGB X 80	80	G1 to G80
0	0	1	0	1	0	240RGB X 88	88	G1 to G88
0	0	1	0	1	1	240RGB X 96	96	G1 to G96
0	0	1	1	0	0	240RGB X 104	104	G1 to G104
0	0	1	1	0	1	240RGB X 112	112	G1 to G112
0	0	1	1	1	0	240RGB X 120	120	G1 to G120
0	0	1	1	1	1	240RGB X 128	128	G1 to G128
0	1	0	0	0	0	240RGB X 136	136	G1 to G136
0	1	0	0	0	1	240RGB X 144	144	G1 to G144
0	1	0	0	1	0	240RGB X 152	152	G1 to G152
0	1	0	0	1	1	240RGB X 160	160	G1 to G160
0	1	0	1	0	0	240RGB X 168	168	G1 to G168
0	1	0	1	0	1	240RGB X 176	176	G1 to G176
0	1	0	1	1	0	240RGB X 184	184	G1 to G184
0	1	0	1	1	1	240RGB X 192	192	G1 to G192
0	1	1	0	0	0	240RGB X 200	200	G1 to G200
0	1	1	0	0	1	240RGB X 208	208	G1 to G208
0	1	1	0	1	0	240RGB X 216	216	G1 to G216
0	1	1	0	1	1	240RGB X 224	224	G1 to G224
0	1	1	1	0	0	240RGB X 232	232	G1 to G232
0	1	1	1	0	1	240RGB X 240	240	G1 to G240
0	1	1	1	1	0	240RGB X 248	248	G1 to G248
0	1	1	1	1	1	240RGB X 256	256	G1 to G256
1	0	0	0	0	0	240RGB X 264	264	G1 to G264
1	0	0	0	0	1	240RGB X 272	272	G1 to G272
1	0	0	0	1	0	240RGB X 280	280	G1 to G280
1	0	0	0	1	1	240RGB X 288	288	G1 to G288
1	0	0	1	0	0	240RGB X 296	296	G1 to G296
1	0	0	1	0	1	240RGB X 304	304	G1 to G304
1	0	0	1	1	0	240RGB X 312	312	G1 to G312
1	0	0	1	1	1	240RGB X 320	320	G1 to G320

NOTE: A FP (front porch) and BP (back porch) period will be inserted as blanking period (All gates output VGL level) before / after the driver scan through all of the scans.

LCD-Driving-Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

FLD1-0: These bits are for the set up of the interlaced driver's n raster-row. See the following table and figure for the set up value and field raster-row and scanning method.

Table 24. Association chart for scanning FLD1-0 and n raster-row

FLD1	FLD0	Scanning method
0	0	1 field
0	1	1 field
1	0	1 field
1	1	3 field (interlaced)

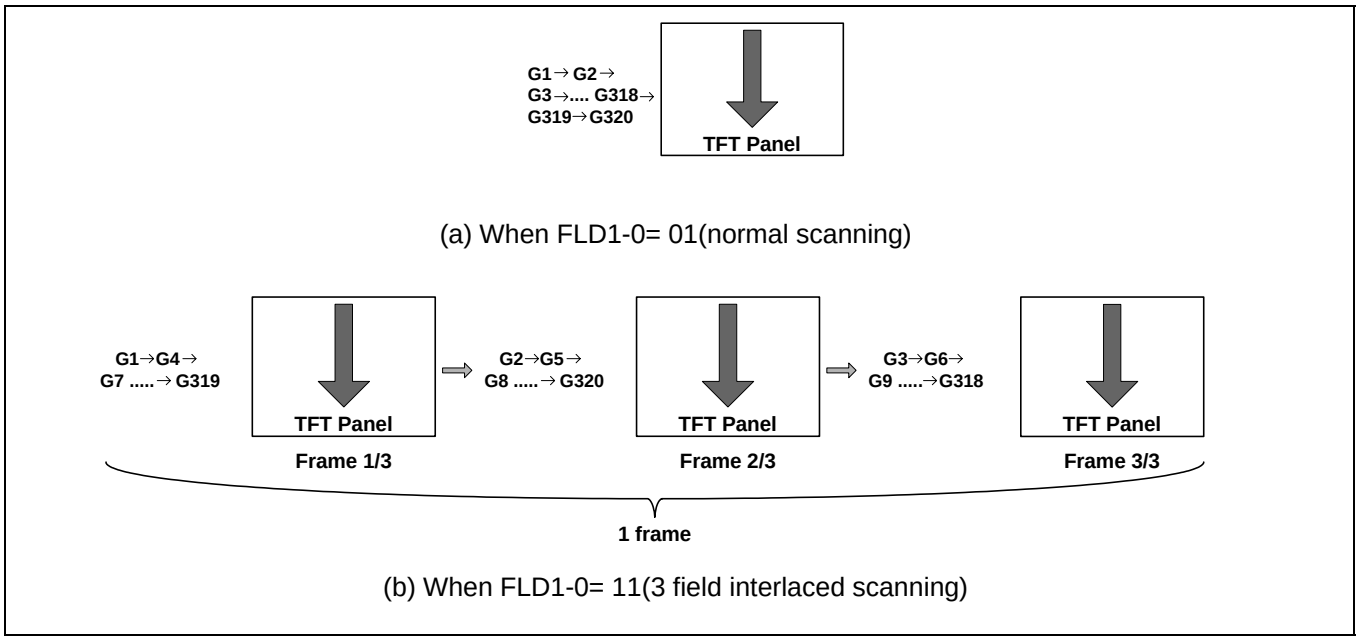


Figure 5. Interlaced scanning method

B/C: When B/C = 0, a frame inversion waveform is generated and alternates at every frame. When B/C = 1, an n raster-row AC waveform is generated and alternates in each raster-row specified by bits EOR in the LCD-driving-waveform control register (R02h). For details, see the N-RASTER-ROW REVERSED AC DRIVE section.

EOR: When the line inversion waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals. And the n-raster-row reversed signals are being EOR (Exclusive-OR) for alternating drive. When the EOR is used, the number of the LCD drive raster-row and the n raster-row alternates the LCD. For details, see the ONE-RASTER-ROW REVERSED AC DRIVE section.

NW5–0: Specify the number of raster-rows that will alternate in the line inversion waveform setting (B/C = 1). NW5–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected. For details, refer to N-RASTER ROW REVERSED AC DRIVE section

Preliminary

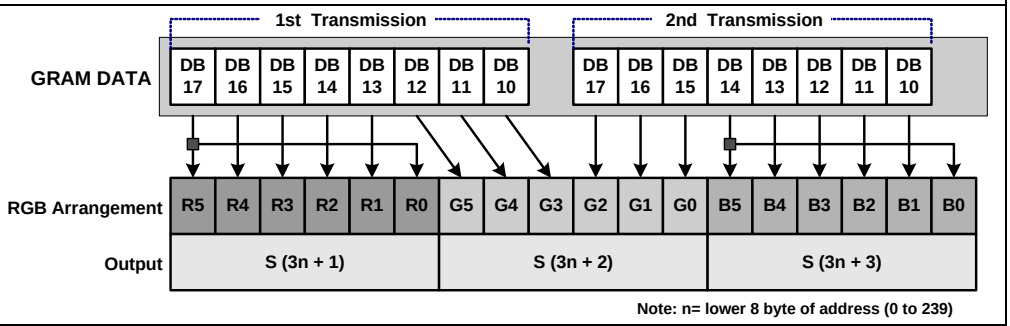
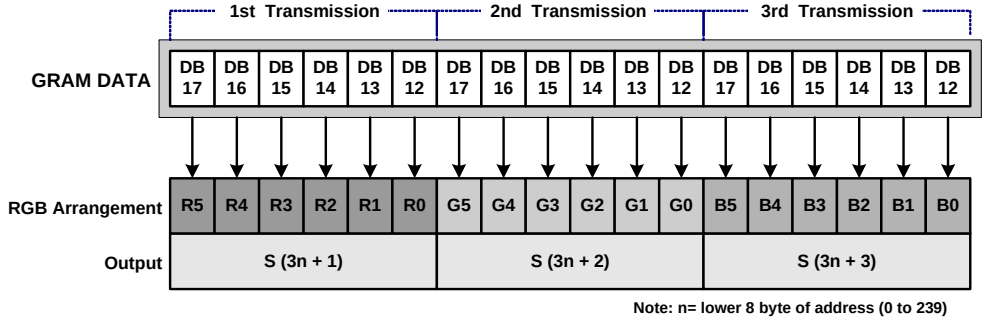
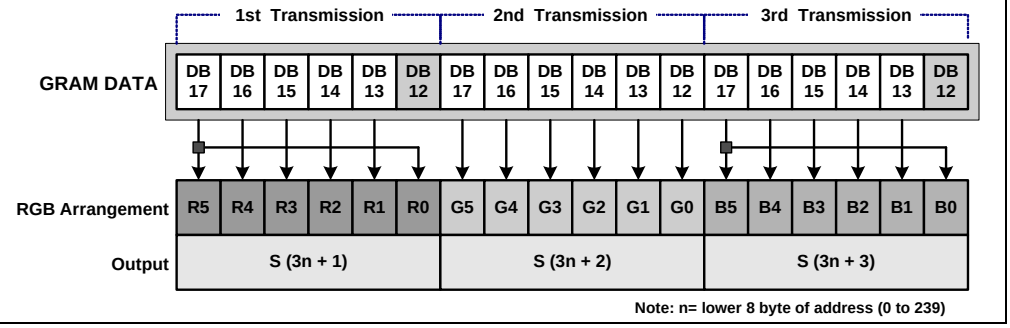
Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	0	0	0

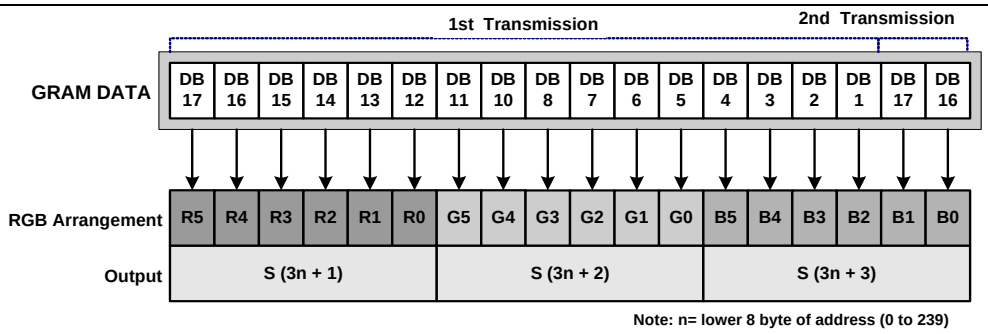
TRI: This bit is active on the 80-system of 8-bit bus interface, the data for 1-pixel is transported to the memory for 3 write cycles. And, this bit is on the 80-system of 16-bit interface, the data for 1-pixel is transported to the memory for 2 write cycles. When the 80-system interface mode is not set the 8-bit or16-bit mode, set TRI bit to be "0".

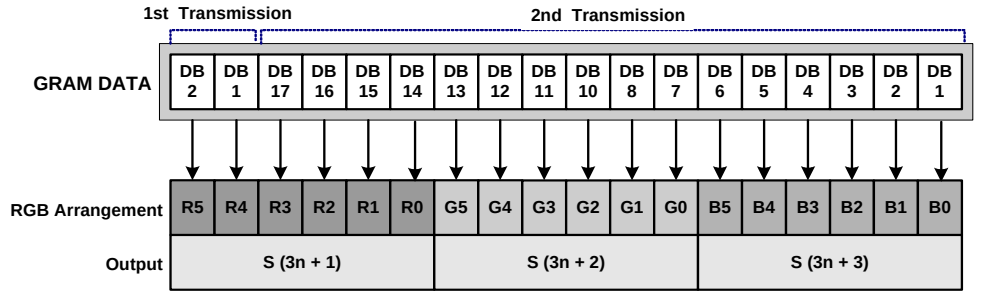
DFM: When 8-bit or16-bit 80 interface mode and TRI bit =1, DFM defines color depth for the IC.
8-bit (80-system), DFM = 0: 262k-color mode (3 times of 6-bit data transfer to GRAM)
8-bit (80-system), DFM = 1: 65k-color mode (5-bit, 6-bit, 5-bit data transfer to GRAM)

16-bit (80-system), DFM = 0: 262k-color mode (16-bit, 2-bit data transfer to GRAM)
16-bit (80-system), DFM = 1: 262k-color mode (2-bit, 16-bit data transfer to GRAM)

TRI	DFM	Interface Mode	Write data to GRAM
0	0	*	
1	0	80-system 8-bit	
	1	80-system 8-bit	

Preliminary

<table>
<tr><th>TRI</th><th>DFM</th><th>Interface Mode</th><th>Write data to GRAM</th></tr>
<tr><td rowspan="2">1</td><td>0</td><td>80-system 16-bit</td><td> 

Note: n= lower 8 byte of address (0 to 239)</td></tr>
<tr><td>1</td><td>80-system 16-bit</td><td> 

Note: n= lower 8 byte of address (0 to 239)</td></tr>
</table>

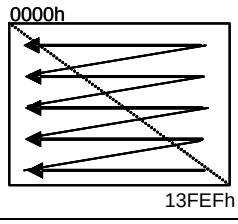
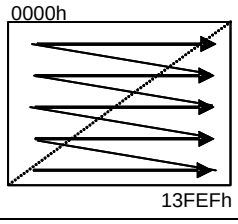
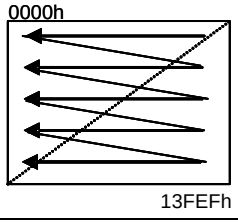
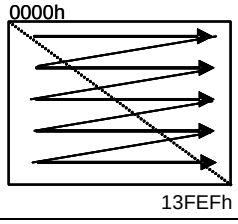
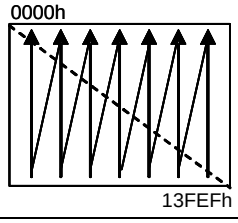
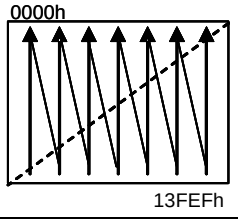
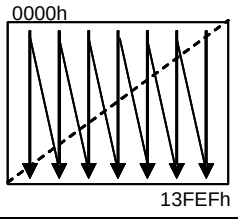
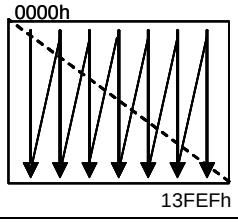
SAMSUNG ELECTRONICS

Preliminary

I/D1-0: When I/D1-0 = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decreased by 1 after the data is written to the GRAM. Automatic address counter updating is not performed when reading data from GRAM. The increment/decrement setting of the address counter by I/D1-0 bits is performed independently for the upper (AD15-8) and lower (AD7-0) addresses. The AM bit sets the direction of moving through the addresses when the GRAM is written.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

Table 25. Address Direction Setting

	I/D1-0=”00” H: decrement V: decrement	I/D1-0=”01” H: increment V: decrement	I/D1-0=”10” H: decrement V: increment	I/D1-0=”11” H: increment V: increment
AM=0 Horizontal				
AM=1 Vertical				

BGR: About writing 18-bit data to GRAM, it is changed <R><G><B> into <B><G><R>.

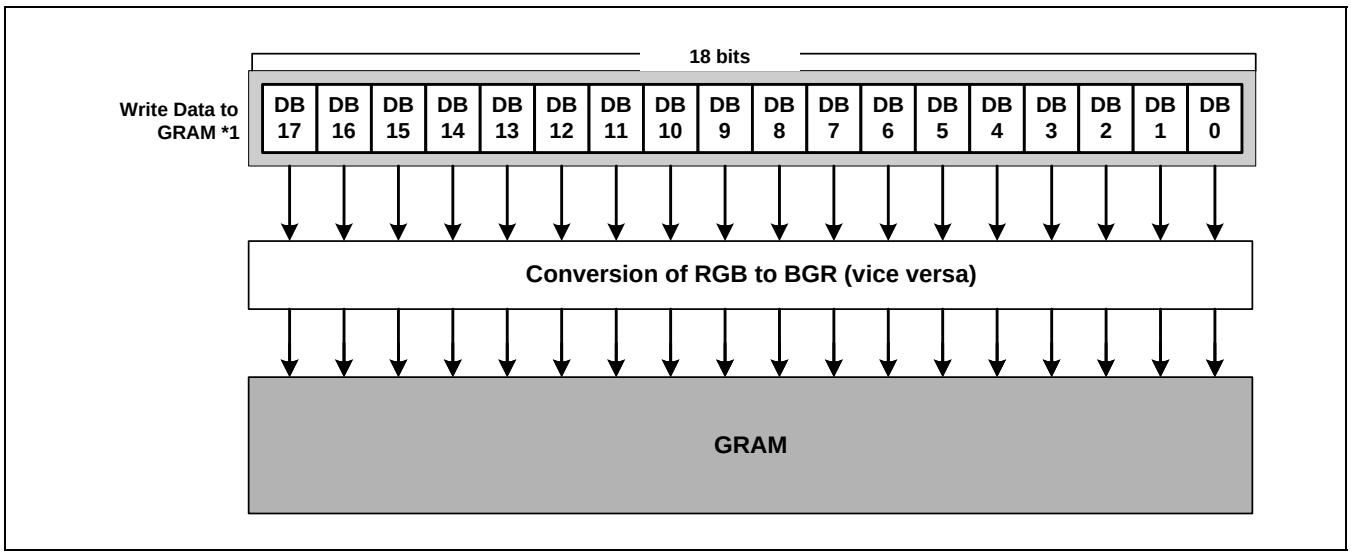


Figure 6. Write data to GRAM via RGB swapping block

Preliminary

Display Control (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	0	GON	CL	REV	D1	D0

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

PT1	PT0	Source Output on Non-display Area		VCOM Output on Non-display Area		Gate Output for Non-display Area
		Positive	Negative	Positive	Negative	
0	0	AVSS	AVSS	AVSS	AVSS	Refer to PTG setting
0	1	AVSS	GVDD	VCOML	VCOMH	Refer to PTG setting
1	0	GVDD	AVSS	VCOML	VCOMH	Refer to PTG setting
1	1	Hi-z	Hi-z	AVSS	AVSS	Refer to PTG setting

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens cannot be controlled at the same time.

VLE2	VLE1	2nd Screen	1st Screen
0	0	Fixed display	Fixed display
0	1	Fixed display	Scroll
1	0	Scroll	Fixed display
1	1	Setting disabled	Setting disabled

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

Note: this function is not available when the external display interface (i.e. RGB interface or VSYNC interface) is in use.

GON: Gate on/off control signal. All gate output is set to be gate off level when GON = 0.
When GON = 1, gate driver is working: G1 to G320 output is either VGH or VGL level. See the Instruction set up flow for further description on the display on/off flow.

GON	Gate Output
0	All gate off (All gates output are set to VGL)
1	Gate on(VGH / VGL)

CL: CL = 1 selects 8-color display mode. For details, see the section on 8-COLOR DISPLAY MODE.

CL	Number of display colors
0	262,144 colors
1	8 colors

REV: When the REV = 1, all character and graphics display sections display with reversal. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

REV	GRAM Data	Display Area	
		Positive	**Negative**
0	18'h00000 : 18'h3FFFF	V63 : V0	V0 : V63
1	18'h00000 : 18'h3FFFF	V0 : V63	V63 : V0

D1–0: When D1 is 1, display is on. And, when D1 is 0, display is off. When display is off, the display data remains in the GRAM, and can be re-displayed instantly by setting "D1 = 1". When D1 is 0, the display is off with the entire source outputs set to the VSS level. Because of this, the S6D0129 can control the charging current for the LCD with AC driving. Control the display on/off while control GON. For details, see the Instruction set up flow.

When D1–0 = 01, the internal display of the S6D0129 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	GON	Source output	Gate Output	VCOM Output	Internal display operation
0	0	0	AVSS	VGL	AVSS	Halt
0	1	1	AVSS	Operate	AVSS	Operate
1	0	1	Blank Display	Operate	Operate	Operate
1	1	1	Normal Display	Operate	Operate	Operate

Notes:

1. Writing from MCU to GRAM is independent of D1–0.
2. In sleep and standby mode, D1–0 = 00. However, the register contents of D1–0 are not modified.
3. When source output is the same phase with VCOM, white screen is displayed at normally white LCD panel

Display control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

The blanking period in the front and end of the display area can be defined using this register.
When N-raster-row is driving, a blank period is inserted after all screens are drawn. Front and Back porch can be adjusted using FP3-0 and BP3-0 bits (R08h).

FP3-0/BP3-0: Set the periods of blanking (the front and back porch), which are placed at the beginning and end of the display. FP3-0 is for a front porch and BP3-0 is for a back porch. When front and back porches are set, the settings should meet the following conditions.

BP + FP ≤ 16 raster-rows

FP ≥ 2 raster-rows
BP ≥ 2 raster-rows

When the external display interface is in use, the front porch (FP) will start on the falling edge of the VSYNC signal and display operation commences at the end of the front-porch period. The back porch (BP) will start when data for the number of raster-rows specified by the NL bits has been displayed. During the period between the completion of the back-porch period and the next VSYNC signal, the display will remain blank.

NOTE: In the interlace drive mode, FP and BP setting is ignored: total sum of blanking period between 3 frame are automatically set to be 16 raster-rows.

Table 26. Front/Back Porch

FP3 BP3	FP2 BP2	FP1 BP1	FP0 BP0	# of Raster Periods In the Front Porch # of Raster Periods In the Back Porch
0	0	0	0	Setting Disabled
0	0	0	1	Setting Disabled
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
. . .	. . .	. . .	. . .	. . .
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	Setting Disabled

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	PTG1	PTG0	ISC 3	ISC 2	ISC 1	ISC 0

PTG1-0: set the gate scan mode at Non-display area.

PTG1	PTG0	Non-display area Gate driver output	Non-display area Source driver output	VCOM output
0	0	Normal scan	PT setting	
0	1	Fixed to VGL	PT setting	
1	0	Interval scan mode	PT setting	
1	1	Setting disabled	-	

ISC3-0: when non-display area gate scan mode is set to be Interval scan mode, gate scan occurs every frame that is defined by ISC3-0 bit (R09h).

ISC3	ISC2	ISC1	ISC0	Interval period	fFLM (in 60hz)
0	0	0	0	0 frame	-
0	0	0	1	3 frame	50ms
0	0	1	0	5 frame	84ms
0	0	1	1	7 frame	117ms
0	1	0	0	9 frame	150ms
0	1	0	1	11 frame	184ms
0	1	1	0	13 frame	217ms
0	1	1	1	15 frame	251ms
1	0	0	0	17 frame	284ms
1	0	0	1	19 frame	317ms
1	0	1	0	21 frame	351ms
1	0	1	1	23 frame	384ms
1	1	0	0	25 frame	418ms
1	1	0	1	27 frame	451ms
1	1	1	0	29 frame	484ms
1	1	1	1	31 frame	518ms

Preliminary

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	VCIR 2	VCIR 1	VCIR 0	DI V1	DIV 0	0	DCR _EX	DCR 2	DCR 1	DCR 0	RTN1	RTN0

NO1-0: Set amount of non-overlay for the gate output.

NO1	NO0	Amount of non-overlap	
		Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	2 clock cycle	16 clock cycle
0	1	4 clock cycle	32 clock cycle
1	0	6 clock cycle	48 clock cycle
1	1	8 clock cycle	64 clock cycle

Note: The amount of non-overlap time is defined from the falling edge of the CL1

SDT1-0: Set delay amount from gate edge (end) to source output.

SDT1	SDT0	Delay amount of the source output	
		Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	1 clock cycle	8 clock cycle
0	1	2 clock cycle	16 clock cycle
1	0	3 clock cycle	24 clock cycle
1	1	4 clock cycle	32 clock cycle

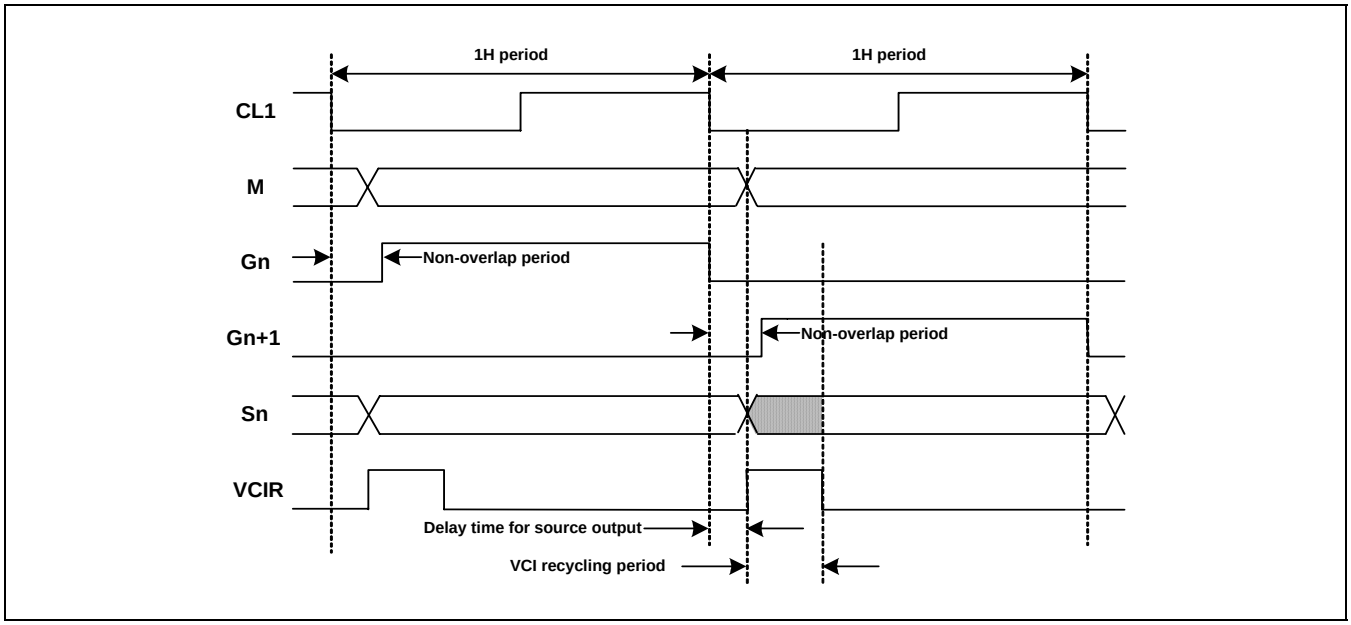


Figure 7. Set Delay from Gate Output to Source Output and VCIR signal

Note: The values specified by the bits of VCIR, SDT1-0 and NO1-0 vary in a reference clock for each interface mode.

Internal operation mode: Internal R-C oscillation clock
RGB-I/F mode : DOTCLK
VSYNC-I/F : Internal R-C oscillation clock

VCIR2-0: VCIR period is sustained for the number of clock cycle which is set on VCIR2-0.

VCIR2	VCIR1	VCIR0	VCIR period	
			Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	0	0	0
0	0	1	2 clock cycle	8 clock cycle
0	1	0	4 clock cycle	16 clock cycle
0	1	1	6 clock cycle	24 clock cycle
1	0	0	8 clock cycle	32 clock cycle
1	0	1	12 clock cycle	48 clock cycle
1	1	0	14 clock cycle	56 clock cycle
1	1	1	Setting disabled	Setting disabled

Preliminary

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks, which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the 1H period (RTN3-0). When changing number of the drive cycle, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

DIV1	DIV0	Division Ratio	Internal operation clock frequency(INCLK)
0	0	1	fosc/1
0	1	2	fosc/2
1	0	4	fosc/4
1	1	8	fosc/8

*fosc = R-C oscillation frequency

$$\text{Frame Frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row x division ratio x (Line+B)}} \text{ [Hz]}$$

f_{osc}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
B: Blank period(Back porch + Front Porch)

Figure 8. Formula for the frame frequency

DCR_EX: Input signal selection signal for external interface mode. (0: internal operation clock, 1: External clock) Set DCR_EX bit to 1 for external clock. The external clock is the DCCLK (clock cycle for step-up circuit) source, when external interface mode is in use (DM[1:0]=”01” or “11”).

DCR 2-0: Set clock cycle for step-up circuit in external interface mode. Please set DCR_EX bit to “1” and DCR1-0 value when external interface is in use. In this case, DOTCLK must be input periodically and continuously.

DCR2	DCR1	DCR0	Clock cycle for step-up circuits (DCCLK) in external interface mode
0	0	0	DOTCLK/32
0	0	1	DOTCLK/64
0	1	0	DOTCLK/128
0	1	1	DOTCLK/256
1	*	*	DOTCLK/512

Note: If external input clock cycle is variable or discontinuous, clock cycle for step-up circuit must be generated internally (DCR_EX=0).

RTN1-0: Set the 1H period (1 raster-row).

RTN1	RTN0	Horizontal clock frequency(CL1)	Clock frequency for step-up circuits(DCCLK)
0	0	INCLK/16	fosc/8
0	1	INCLK/20	fosc/10
1	0	INCLK/24	fosc/12
1	1	INCLK/28	fosc/14

Preliminary

External Display Interface Control (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RM: Specifies the interface for RAM accesses. When the display data is written via the RGB interface, RM bit should be set (RM = 1). This bit and the DM bits can be set independently. The display data can be written via the system interface by clearing this bit while the RGB interface is used.

RM	Interface for RAM Access
0	System interface / VSYNC interface
1	RGB interface

DM1-0: Specify the display operation mode. The interface operation is based on the bits of DM1-0. This setting enables switching interface between internal operation and the external display interface. Switching among two external display interfaces (RGB and VSYNC interface) should not be done.

DM1	DM0	Display Operation Mode
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disable

RIM1-0: Specify the RGB interface mode when the RGB interface is used. Specifically, this setting specifies the mode when the bits of DM and RM are set to RGB interface. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)
0	1	16-bit RGB interface (one transfer /pixel)
1	0	6-bit RGB interface (three transfers /pixel)
1	1	Setting disable

Depending on the external display interface setting, various interfaces can be specified to match the display state. While displaying motion pictures (RGB /VSYNC interface), the data for display can be written in high-speed write mode, which achieves both low power consumption and high-speed access.

Table 27. Display State and Interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1-0)
Still Pictures	Internal Clock	System interface (RM=0)	Internal clock (DM1-0=00)
Motion Pictures	RGB interface (1)	RGB interface(RM=1)	RGB interface (DM1-0=01)
Rewrite still picture area while displaying motion pictures	RGB interface (2)	System interface (RM=0)	RGB interface (DM1-0=01)
Motion Picture Display	VSYNC interface	System interface (RM=0)	VSYNC interface (DM1-0=10)

NOTE: 1) The instruction register can only be set through the system interface.
2) Switching among RGB and VSYNC interface cannot be done.
3) RGB interface modes should not be set during operation.
4) For the transition flow for each operation mode, see the External Display Interface section.

Internal Clock Mode

All display operation is controlled by signals that are generated by the internal clock in internal clock mode. All inputs through the external display interface are invalid. The internal RAM can be accessed only via the system interface.

RGB Interface Mode (1)

The display operations are controlled by the frame synchronization clock (VSYNC), raster-row synchronization signal (HSYNC), and dot clock (DOTCLK) in RGB interface mode. These signals should be supplied during display operation in this mode.

The display data is transferred to the internal RAM via PD17-0 for each pixel. Combining the function of the high-speed write mode and the window address enables display of both the motion picture area and the internal RAM area simultaneously. In this method, data is only transferred when the screen is updated, which reduces the amount of data transferred.

The periods of the front (FP), back (BP) porch, and the display are automatically generated in the S6D0129 by counting the raster-row synchronization signal (HSYNC) based on the frame synchronization signal (VSYNC).

RGB Interface Mode (2)

When RGB interface is in use, data can be written to RAM via the system interface. This write operation should be performed while data for display is not being transferred via RGB interface (ENABLE = active). Before the next data transfer for display via RGB interface, the setting above should be changed, and then the address and index (R22h) should be set.

VSYNC Interface Mode

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When data is written to the internal RAM with the required speed after the falling edge of VSYNC, motion pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

In VSYNC interface mode. Only the VSYNC input pin is valid. The other input signals for the external display interface are invalid.

The periods of the front and back porch and display period are automatically generated by the frame synchronization signal (VSYNC) according to the setting of the S6D0129 registers.

Preliminary

Power Control 1 (R10h)
Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	0	0	0	SLP	STB
W	1	0	0	GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GVD 0	0	0	0	0	0	VC2	VC1	VC0

SAP2-0: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver. When the amount of fixed current is large, LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During non-display, when SAP2-0 = “000”, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SAP2	SAP1	SAP0	Amount of Current in Operational Amplifier
0	0	0	Operation of the operational amplifier stops.
0	0	1	Small
0	1	0	Medium Low
0	1	1	Medium
1	0	0	Medium High
1	0	1	Large
1	1	0	Setting disabled
1	1	1	Setting disabled

BT2–0: The output factor of step-up is switched. You can adjust scale factor of the step-up circuit according to the used voltage value. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. You should adjust the frequency that is considering on the display quality and the current consumption.

BT2	BT1	BT0	VGH	VGL	Notes*	
0	0	0	4 X Vci1	-3X Vci1	11V	-8.25V
0	0	1	4 X Vci1	-4X Vci1	11V	-11V
0	1	0	5 X Vci1	-3X Vci1	13.75V	-8.25V
0	1	1	5 X Vci1	-4X Vci1	13.75V	-11V
1	0	0	5 X Vci1	-5X Vci1	13.75V	-13.75V
1	0	1	6 X Vci1	-3X Vci1	16.5V	-8.25V
1	1	0	6 X Vci1	-4X Vci1	16.5V	-11V
1	1	1	6 X Vci1	-5X Vci1	16.5V	-13.75V

Note : The value is maximum by register setting

DC2-0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

DC2	DC1	DC0	Step-up Cycle in Step-up Circuit 1, 3	Step-up Cycle in Step-up Circuit 2
0	0	0	DCCLK / 1	DCCLK / 1
0	0	1	DCCLK / 1	DCCLK / 2
0	1	0	DCCLK / 1	DCCLK / 4
0	1	1	DCCLK / 2	DCCLK / 2
1	0	0	DCCLK / 2	DCCLK / 4
1	0	1	DCCLK / 4	DCCLK / 4
1	1	0	DCCLK / 4	DCCLK / 8
1	1	1	DCCLK / 4	DCCLK / 16

Note: DCCLK is Clock frequency for step-up circuits

SLP: When SLP is high, the S6D0129 enters the sleep mode. The internal display operations are halted except for the R-C oscillator for reducing current consumption. Only the following instructions can be executed during the sleep mode. During the sleep mode, the other GRAM data cannot be updated. Register set-up is maintained.

STB: When STB is high, the S6D0129 enters the standby mode, where display operation completely stops. This mode can halt all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Level	Condition
VCOM	AVSS
Gate	VGL
Source	AVSS

GVD5-0: Set the amplified factor of the GVDD voltage (the voltage for the Gamma voltage). It allows to amplify from 3.0v to 5.0v

GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GV D 0	GVDD Voltage	GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GVD 0	GVDD Voltage
0	0	0	0	0	0	3.00V	1	0	0	0	0	0	4.01V
0	0	0	0	0	1	3.03V	1	0	0	0	0	1	4.05V
0	0	0	0	1	0	3.06V	1	0	0	0	1	0	4.08V
0	0	0	0	1	1	3.09V	1	0	0	0	1	1	4.11V
0	0	0	1	0	0	3.12V	1	0	0	1	0	0	4.14V
0	0	0	1	0	1	3.16V	1	0	0	1	0	1	4.17V
0	0	0	1	1	0	3.19V	1	0	0	1	1	0	4.21V
0	0	0	1	1	1	3.22V	1	0	0	1	1	1	4.24V
0	0	1	0	0	0	3.25V	1	0	1	0	0	0	4.27V
0	0	1	0	0	1	3.28V	1	0	1	0	0	1	4.30V

Preliminary

GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GV D 0	GVDD Voltage	GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GVD 0	GVDD Voltage
0	0	1	0	1	0	3.31V	1	0	1	0	1	0	4.33V
0	0	1	0	1	1	3.35V	1	0	1	0	1	1	4.36V
0	0	1	1	0	0	3.38V	1	0	1	1	0	0	4.40V
0	0	1	1	0	1	3.41V	1	0	1	1	0	1	4.43V
0	0	1	1	1	0	3.44V	1	0	1	1	1	0	4.46V
0	0	1	1	1	1	3.47V	1	0	1	1	1	1	4.49V
0	1	0	0	0	0	3.51V	1	1	0	0	0	0	4.52V
0	1	0	0	0	1	3.54V	1	1	0	0	0	1	4.56V
0	1	0	0	1	0	3.57V	1	1	0	0	1	0	4.59V
0	1	0	0	1	1	3.60V	1	1	0	0	1	1	4.62V
0	1	0	1	0	0	3.63V	1	1	0	1	0	0	4.65V
0	1	0	1	0	1	3.66V	1	1	0	1	0	1	4.68V
0	1	0	1	1	0	3.70V	1	1	0	1	1	0	4.71V
0	1	0	1	1	1	3.73V	1	1	0	1	1	1	4.75V
0	1	1	0	0	0	3.76V	1	1	1	0	0	0	4.78V
0	1	1	0	0	1	3.79V	1	1	1	0	0	1	4.81V
0	1	1	0	1	0	3.82V	1	1	1	0	1	0	4.84V
0	1	1	0	1	1	3.86V	1	1	1	0	1	1	4.87V
0	1	1	1	0	0	3.89V	1	1	1	1	0	0	4.91V
0	1	1	1	0	1	3.92V	1	1	1	1	0	1	4.94V
0	1	1	1	1	0	3.95V	1	1	1	1	1	0	4.97V
0	1	1	1	1	1	3.98V	1	1	1	1	1	1	5.00V

VC2-0: Set the VCI1 voltage. These bits set the VCI1 voltage from 0.68 to 1 times of the VCI_REF voltage

VC2	VC1	VC0	VCI1
0	0	0	0.68 X VCI_REF
0	0	1	0.73 X VCI_REF
0	1	0	0.83 X VCI_REF
0	1	1	0.92 X VCI_REF
1	0	0	1.00 X VCI_REF

Note: Don't set any higher VCI1 level than 2.75V

Preliminary

Power Control 4 (R13h)
Power Control 5 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	PON	PON1	AON	0	0	0	0
W	1	0	VCMR	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VML5	VML4	VML3	VML2	VML1	VML0

PON: This is an operation-starting bit for the booster circuit1, 3. In case of PON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON = 1, please refer to the SET UP FLOW OF POWER SUPPLY.

PON1: This is an operation-starting bit for the booster circuit 2. In case of PON1 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON1= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

AON: This is an operation-starting bit for the Amplifier. In case of AON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the AON= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

VCMR: In case of VCMR is LOW, VCOMH is adjusted by VCM5-0 Register and VCOMR pin is used to monitor the input current of the AMP which output the VCOMH voltage.
In case of VCMR is HIGH, VCM5-0 register is ignored and VCOMH voltage is adjusted by VCOMR voltage. VCOMR voltage is externally supplied. The relationship between VCOMH and VCOMR is given as VCOMH=2.5xVCOMR.

Preliminary

VCM5-0: Set the VCOMH voltage.

VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0	VCOMH Voltage	VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0	VCOMH Voltage
0	0	0	0	0	0	3.00V	1	0	0	0	0	0	4.01V
0	0	0	0	0	1	3.03V	1	0	0	0	0	1	4.05V
0	0	0	0	1	0	3.06V	1	0	0	0	1	0	4.08V
0	0	0	0	1	1	3.09V	1	0	0	0	1	1	4.11V
0	0	0	1	0	0	3.12V	1	0	0	1	0	0	4.14V
0	0	0	1	0	1	3.16V	1	0	0	1	0	1	4.17V
0	0	0	1	1	0	3.19V	1	0	0	1	1	0	4.21V
0	0	0	1	1	1	3.22V	1	0	0	1	1	1	4.24V
0	0	1	0	0	0	3.25V	1	0	1	0	0	0	4.27V
0	0	1	0	0	1	3.28V	1	0	1	0	0	1	4.30V
0	0	1	0	1	0	3.31V	1	0	1	0	1	0	4.33V
0	0	1	0	1	1	3.35V	1	0	1	0	1	1	4.36V
0	0	1	1	0	0	3.38V	1	0	1	1	0	0	4.40V
0	0	1	1	0	1	3.41V	1	0	1	1	0	1	4.43V
0	0	1	1	1	0	3.44V	1	0	1	1	1	0	4.46V
0	0	1	1	1	1	3.47V	1	0	1	1	1	1	4.49V
0	1	0	0	0	0	3.51V	1	1	0	0	0	0	4.52V
0	1	0	0	0	1	3.54V	1	1	0	0	0	1	4.56V
0	1	0	0	1	0	3.57V	1	1	0	0	1	0	4.59V
0	1	0	0	1	1	3.60V	1	1	0	0	1	1	4.62V
0	1	0	1	0	0	3.63V	1	1	0	1	0	0	4.65V
0	1	0	1	0	1	3.66V	1	1	0	1	0	1	4.68V
0	1	0	1	1	0	3.70V	1	1	0	1	1	0	4.71V
0	1	0	1	1	1	3.73V	1	1	0	1	1	1	4.75V
0	1	1	0	0	0	3.76V	1	1	1	0	0	0	4.78V
0	1	1	0	0	1	3.79V	1	1	1	0	0	1	4.81V
0	1	1	0	1	0	3.82V	1	1	1	0	1	0	4.84V
0	1	1	0	1	1	3.86V	1	1	1	0	1	1	4.87V
0	1	1	1	0	0	3.89V	1	1	1	1	0	0	4.91V
0	1	1	1	0	1	3.92V	1	1	1	1	0	1	4.94V
0	1	1	1	1	0	3.95V	1	1	1	1	1	0	4.97V
0	1	1	1	1	1	3.98V	1	1	1	1	1	1	5.00V

Preliminary

VML5-0: Set the Amplitude of the VCOM voltage.
VCOML is automatically adjusted by setting the Amplitude of VCOM voltage.

VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	Amplitude of VCOM	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	Amplitude of VCOM
0	0	0	0	0	0	3.592	1	0	0	0	0	0	4.815
0	0	0	0	0	1	3.631	1	0	0	0	0	1	4.854
0	0	0	0	1	0	3.669	1	0	0	0	1	0	4.892
0	0	0	0	1	1	3.707	1	0	0	0	1	1	4.930
0	0	0	1	0	0	3.745	1	0	0	1	0	0	4.968
0	0	0	1	0	1	3.783	1	0	0	1	0	1	5.006
0	0	0	1	1	0	3.822	1	0	0	1	1	0	5.045
0	0	0	1	1	1	3.860	1	0	0	1	1	1	5.083
0	0	1	0	0	0	3.898	1	0	1	0	0	0	5.121
0	0	1	0	0	1	3.936	1	0	1	0	0	1	5.159
0	0	1	0	1	0	3.975	1	0	1	0	1	0	5.197
0	0	1	0	1	1	4.013	1	0	1	0	1	1	5.236
0	0	1	1	0	0	4.051	1	0	1	1	0	0	5.274
0	0	1	1	0	1	4.089	1	0	1	1	0	1	5.312
0	0	1	1	1	0	4.127	1	0	1	1	1	0	5.350
0	0	1	1	1	1	4.166	1	0	1	1	1	1	5.389
0	1	0	0	0	0	4.204	1	1	0	0	0	0	5.427
0	1	0	0	0	1	4.242	1	1	0	0	0	1	5.465
0	1	0	0	1	0	4.280	1	1	0	0	1	0	5.503
0	1	0	0	1	1	4.318	1	1	0	0	1	1	5.541
0	1	0	1	0	0	4.357	1	1	0	1	0	0	5.580
0	1	0	1	0	1	4.395	1	1	0	1	0	1	5.618
0	1	0	1	1	0	4.433	1	1	0	1	1	0	5.656
0	1	0	1	1	1	4.471	1	1	0	1	1	1	5.694
0	1	1	0	0	0	4.510	1	1	1	0	0	0	5.732
0	1	1	0	0	1	4.548	1	1	1	0	0	1	5.771
0	1	1	0	1	0	4.586	1	1	1	0	1	0	5.809
0	1	1	0	1	1	4.624	1	1	1	0	1	1	5.847
0	1	1	1	0	0	4.662	1	1	1	1	0	0	5.885
0	1	1	1	0	1	4.701	1	1	1	1	0	1	5.924
0	1	1	1	1	0	4.739	1	1	1	1	1	0	5.962
0	1	1	1	1	1	4.777	1	1	1	1	1	1	6.000

NOTES: Set VCOML range from -2V to 0V

Preliminary

RAM Address Set (R20h/R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting address. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address
When RGB interface is in use (RM1-0=10), AD16-0 will be set at the falling edge of the VSYNC signal.
When the internal clock operation and VSYNC interface (RM=0X) are in use, AD16-0 will be set upon execution of an instruction.

AD16 to AD0	GRAM setting
“00000”H to “000EF”H	Bitmap data for G1
“00100”H to “001EF”H	Bitmap data for G2
“00200”H to “002EF”H	Bitmap data for G3
“00300”H to “003EF”H	Bitmap data for G4
: : :	: : :
“13C00”H to “13CEF”H	Bitmap data for G317
“13D00”H to “13DEF”H	Bitmap data for G318
“13E00”H to “13EEF”H	Bitmap data for G319
“13F00”H to “13FEF”H	Bitmap data for G320

Write Data to Gram (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	RAM write data (WD17-0): Pin assignment varies according to the interface method. (see the following figure for more information)															
W	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
		When RGB-interface															

WD17-0: Input data for GRAM can be expanded to 18 bits. The expansion format varies according to the interface method. The input data selects the grayscale level. After a write, the address is automatically updated according to AM and I/D bit settings. The GRAM cannot be accessed in standby mode. When 16- or 8-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the <R><B> data to its LSB.

When written data to GRAM are used by RGB interface via the system interface, please make sure that writing data do not occur conflicts.

When the 18-bit RGB interface is in use, 18-bit data is written to RAM via PD17-0. This interface is available on the 262,144-colors. When the 16-bit RGB interface is in use, the MSB is written to its LSB. This interface is available on the 65,536-colors.

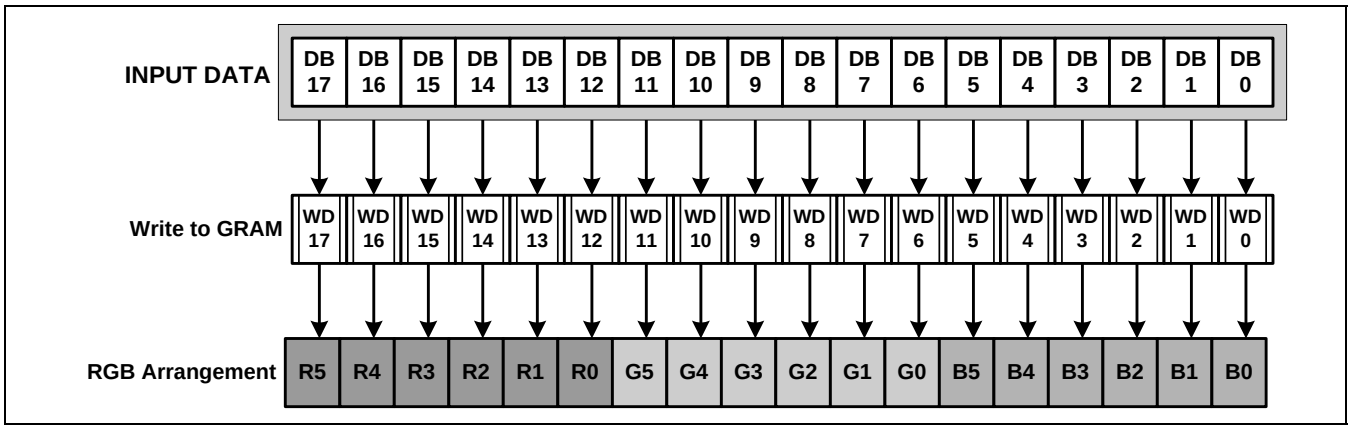


Figure 9. 18-bit System interface (260K-color)

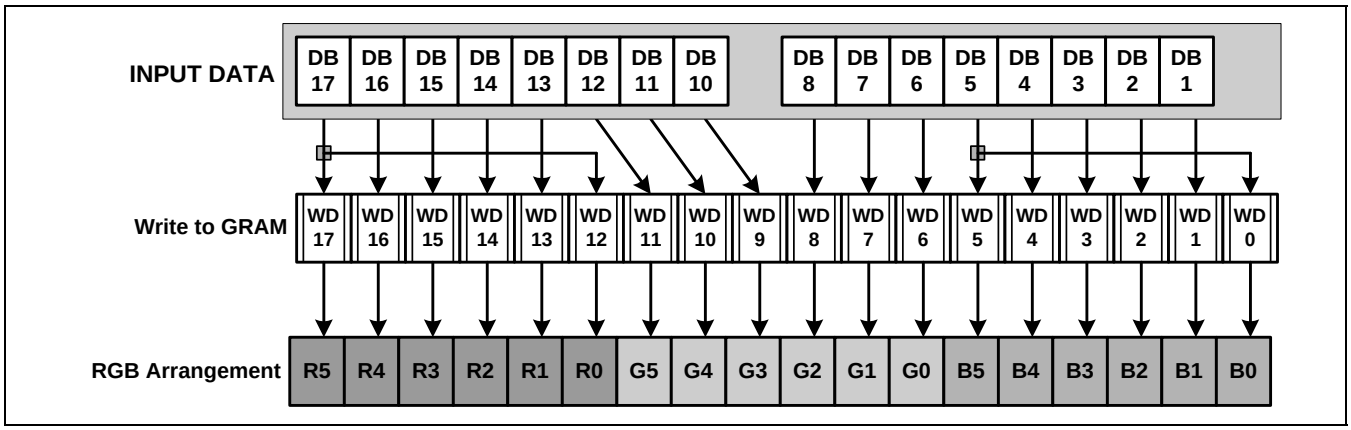


Figure 10. 16-bit System interface (65K-color)

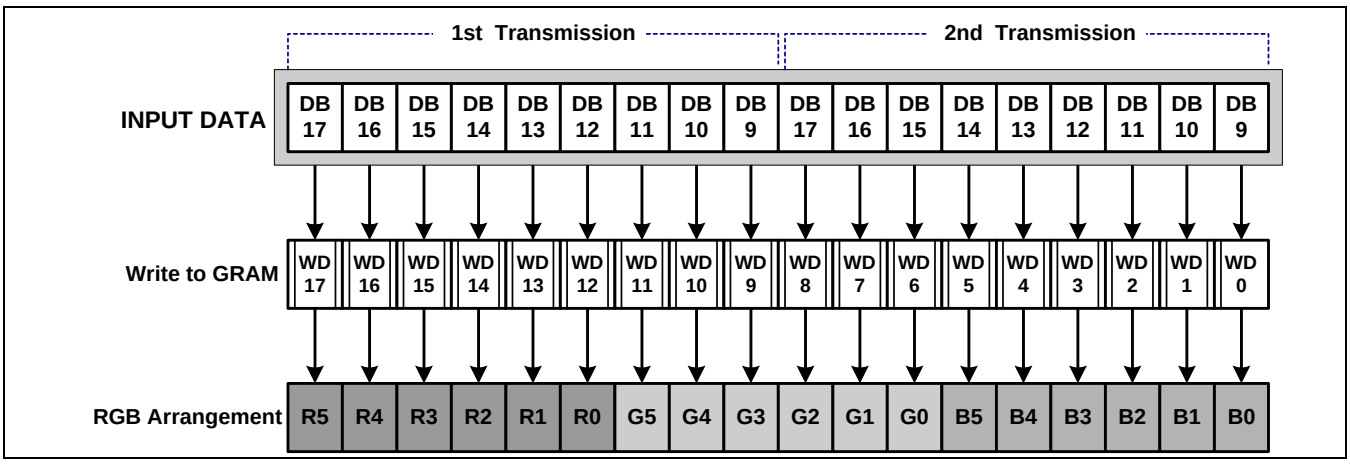


Figure 11. 9-bit System interface (260K-color)

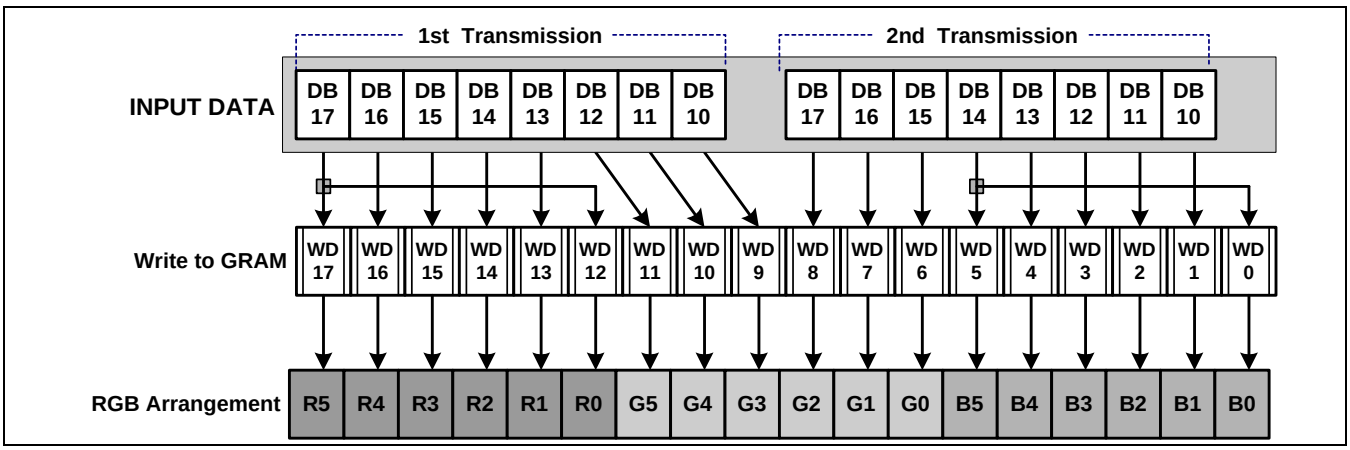


Figure 12. 8-bit System interface (65K-color) TRI=0, DFM=0

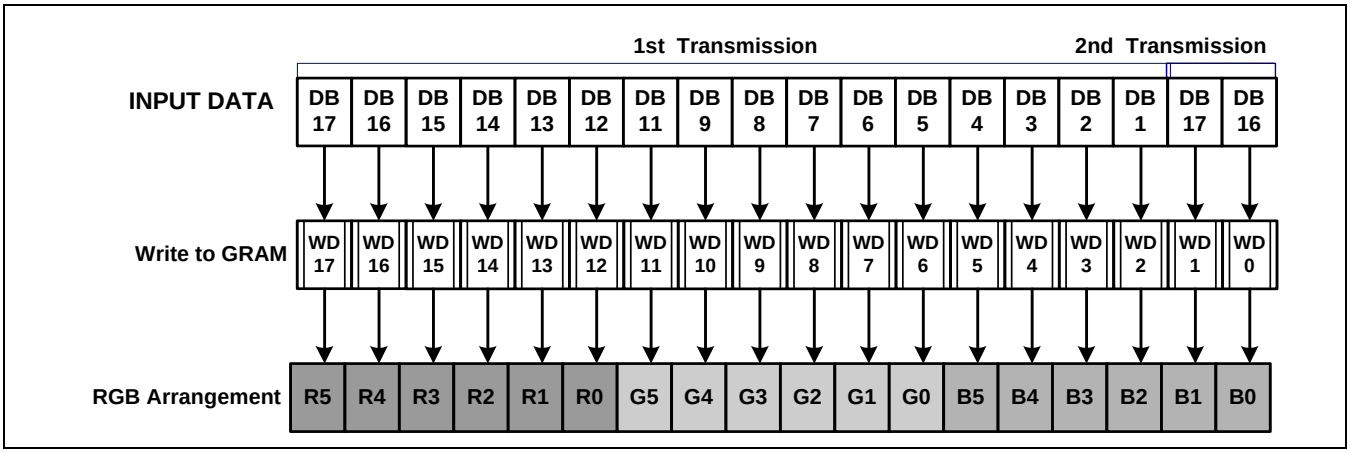


Figure 13. 16-bit System interface (260K-color) TRI=1, DFM=0

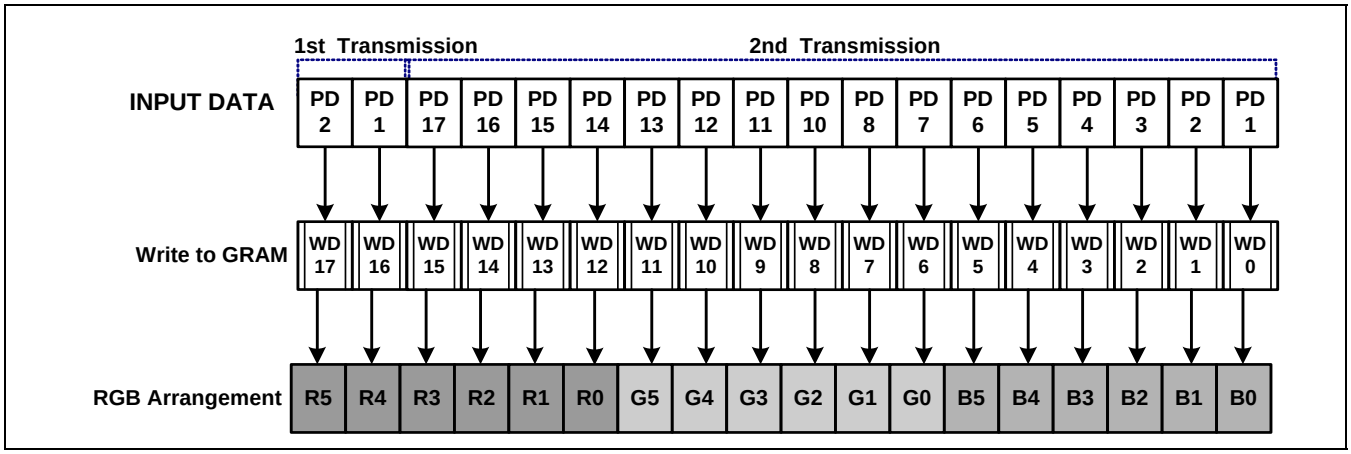


Figure 14. 8-bit System interface (65K-color) TRI=1, DFM=1

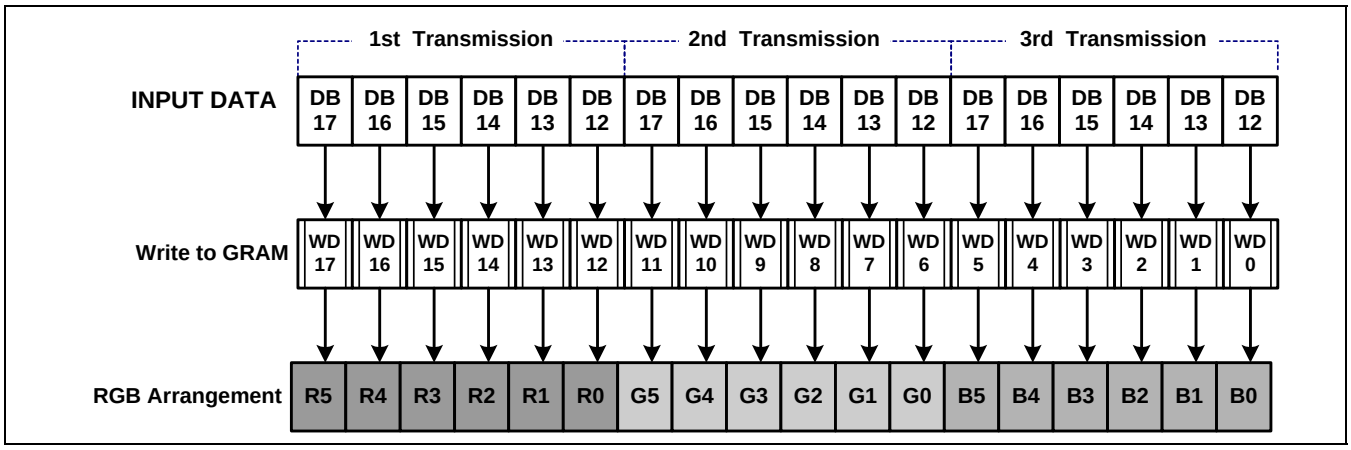


Figure 15. 8-bit System interface (260K-color) TRI=1, DFM=0

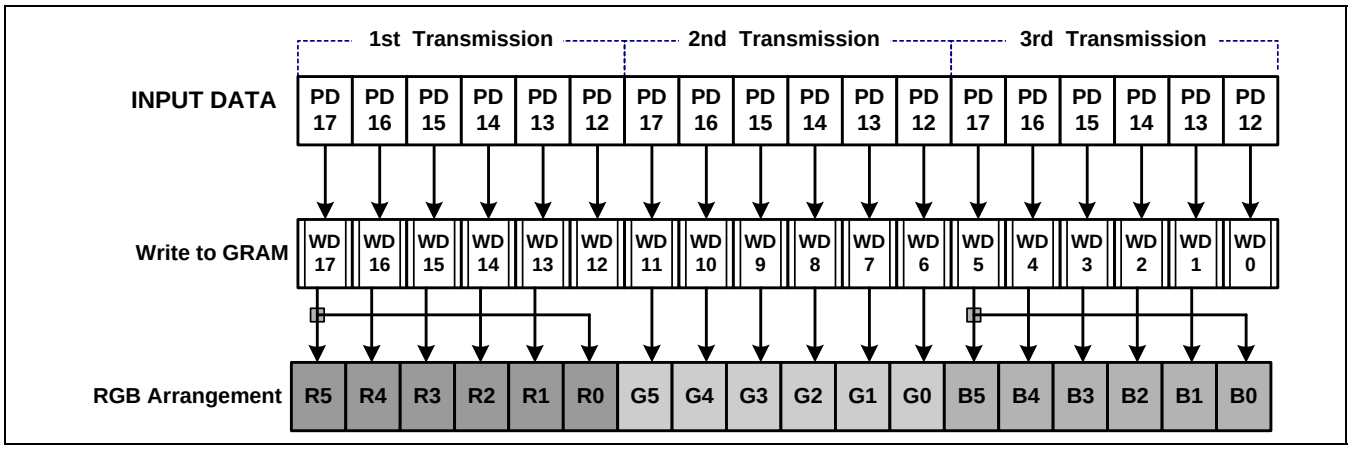


Figure 16. 8-bit System interface (65K-color) TRI=1, DFM=1

Preliminary

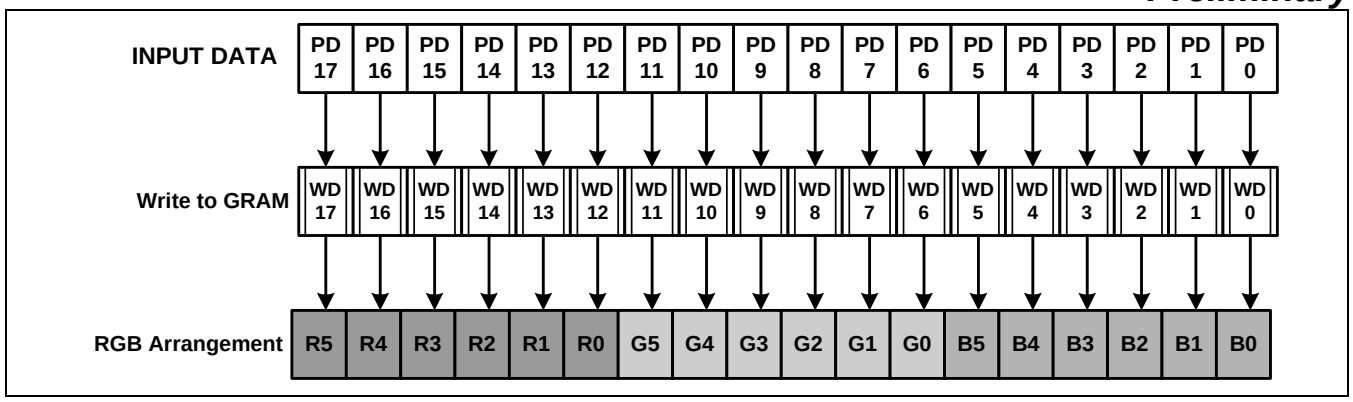


Figure 17. 18-bit RGB interface (260K-color)

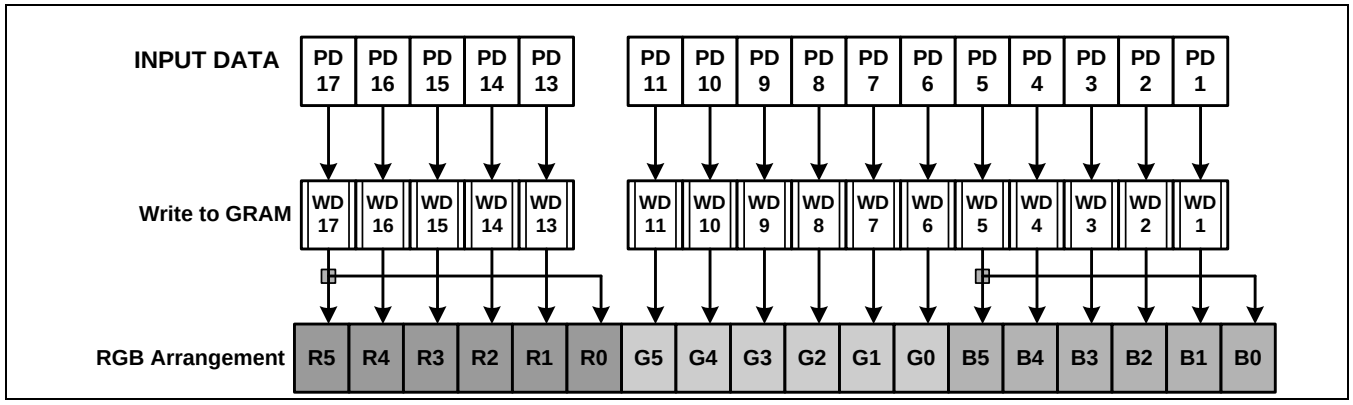


Figure 18. 16-bit RGB interface (65K-color)

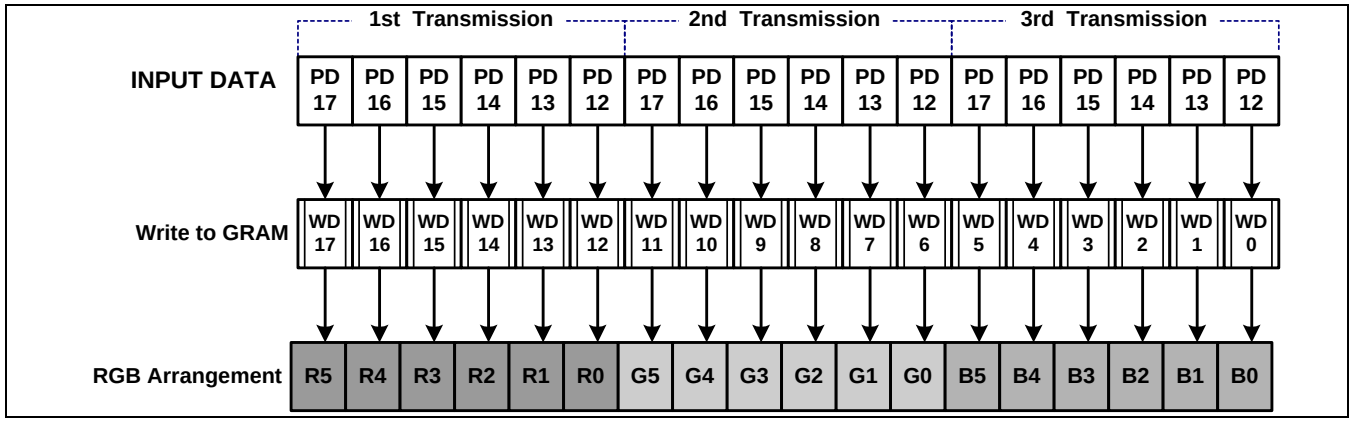


Figure 19. 6-bit RGB interface (260K-color)

Preliminary

Table 28. GRAM Data and Grayscale Level

GRAM data	Grayscale Polarity		GRAM Data	Grayscale Polarity		GRAM Data	Grayscale Polarity		GRAM Data	Grayscale Polarity	
RGB	N	P	RGB	N	P	RGB	N	P	RGB	N	P
000000	V0	V63	010000	V16	V47	100000	V32	V31	110000	V48	V15
000001	V1	V62	010001	V17	V46	100001	V33	V30	110001	V49	V14
000010	V2	V61	010010	V18	V45	100010	V34	V29	110010	V50	V13
000011	V3	V60	010011	V19	V44	100011	V35	V28	110011	V51	V12
000100	V4	V59	010100	V20	V43	100100	V36	V27	110100	V52	V11
000101	V5	V58	010101	V21	V42	100101	V37	V26	110101	V53	V10
000110	V6	V57	010110	V22	V41	100110	V38	V25	110110	V54	V9
000111	V7	V56	010111	V23	V40	100111	V39	V24	110111	V55	V8
001000	V8	V55	011000	V24	V39	101000	V40	V23	111000	V56	V7
001001	V9	V54	011001	V25	V38	101001	V41	V22	111001	V57	V6
001010	V10	V53	011010	V26	V37	101010	V42	V21	111010	V58	V5
001011	V11	V52	011011	V27	V36	101011	V43	V20	111011	V59	V4
001100	V12	V51	011100	V28	V35	101100	V44	V19	111100	V60	V3
001101	V13	V50	011101	V29	V34	101101	V45	V18	111101	V61	V2
001100	V14	V49	011110	V30	V33	101100	V46	V17	111110	V62	V1
001101	V15	V48	011111	V31	V32	101101	V47	V16	111111	V63	V0

Preliminary

RAM ACCESS via RGB INTERFACE & SYSTEM INTERFACE

All the data for display is written to the internal RAM in the S6D0129 when RGB interface is in use. In this method, data, including that in both the motion picture area and the screen update frame, can only be transferred via RGB interface. Data for display that is not in the motion picture area or the screen update frame can be written via the system interface.

RAM can be accessed via the system interface when RGB interface is in use. When data is written to RAM during RGB interface mode, the ENABLE bit should be low to stop data writing via RGB interface, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is high. After this RAM access via the system interface, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB interface. When a RAM write conflict occurs, data writing is not guaranteed.

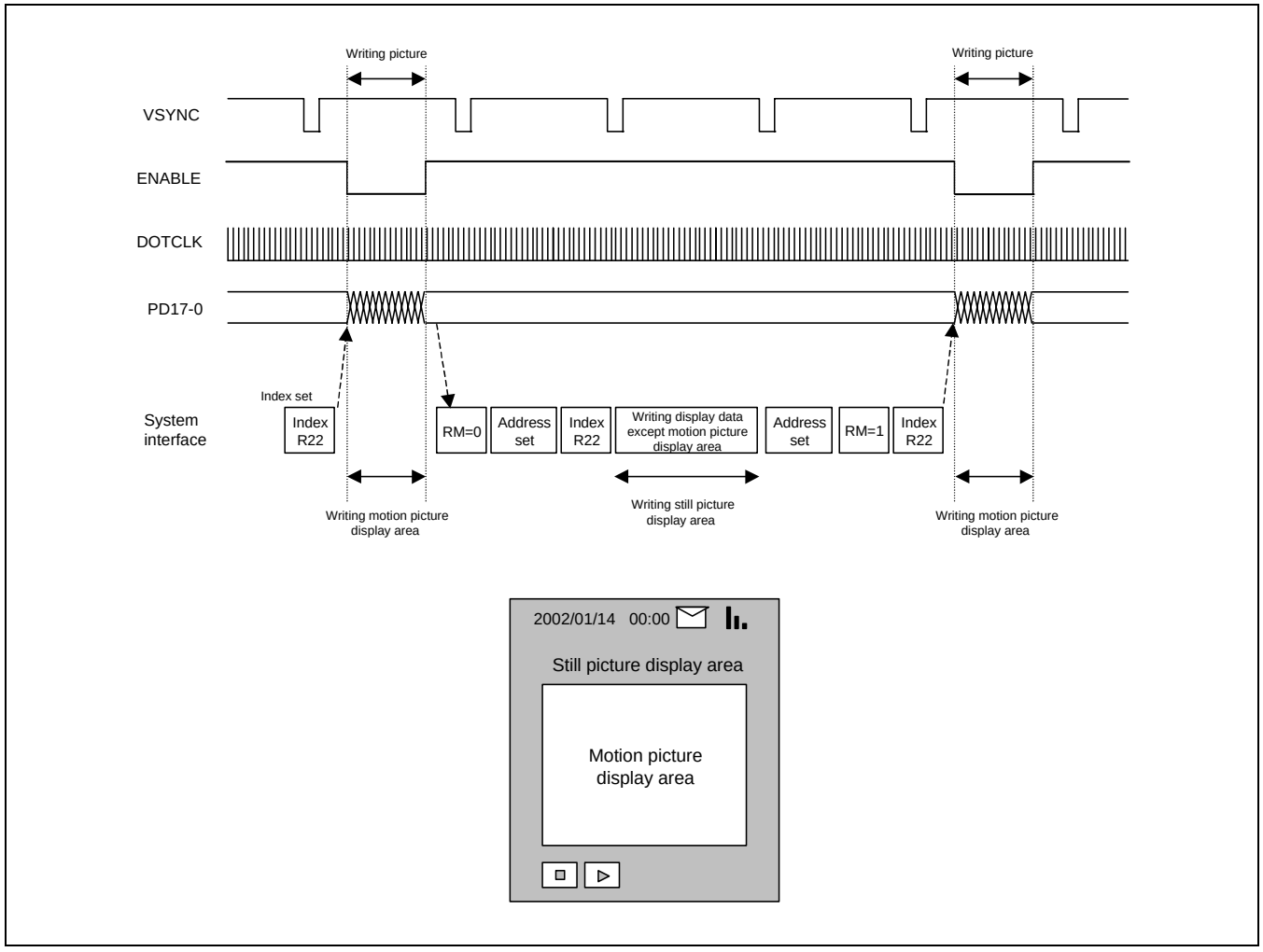


Figure 20. RAM access via RGB Interface & System Interface

SAMSUNG ELECTRONICS

Read Data from GRAM (R22h)

R/W	RS	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	1	RAM Read data (RD17-0): Pin assignment varies according to the interface method. (see the following figure for more information)																	

RD17–0: Read 18-bit data from the GRAM. When the data is read to the MCU, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

In case of 16-/8-bit interface, the LSB of <R><B> color data will not be read.

This function is not available in RGB interface mode.

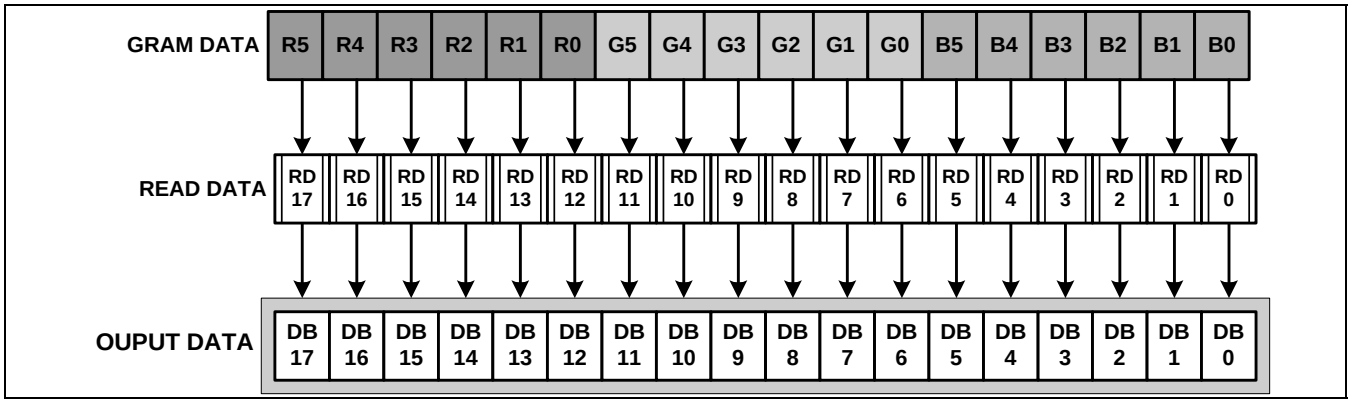


Figure 21. 18-bit System Interface for GRAM read

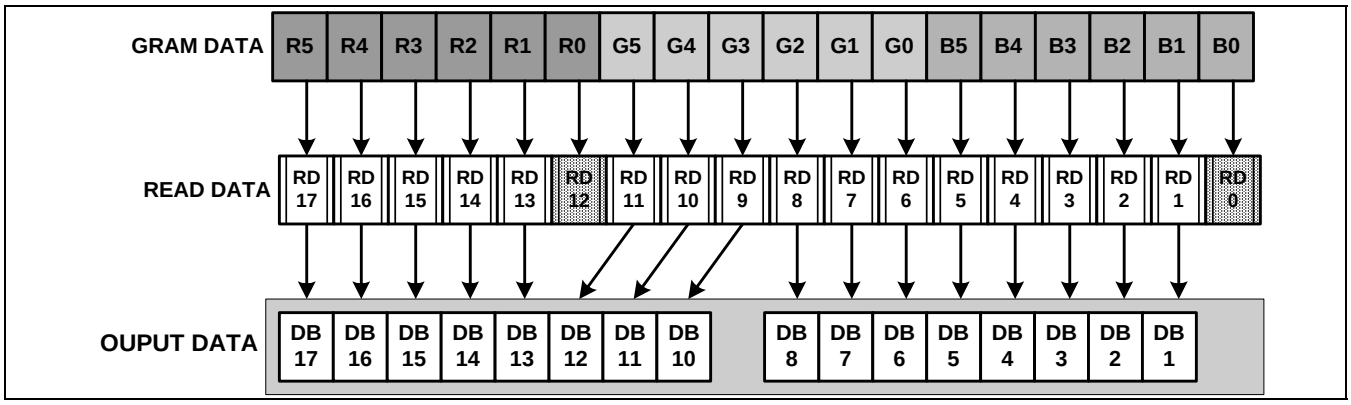


Figure 22. 16-bit System Interface for GRAM read

Preliminary

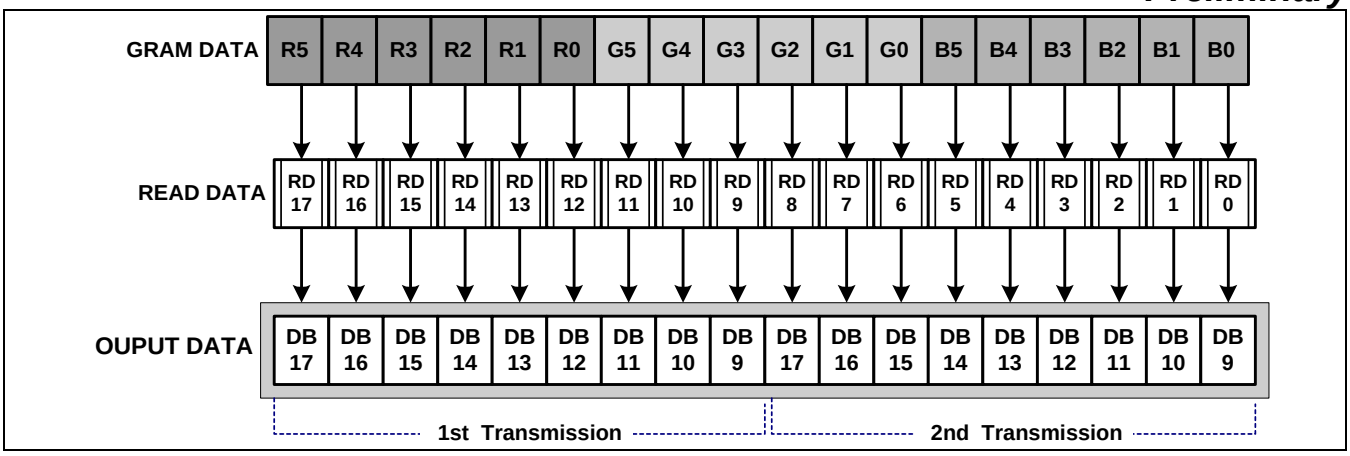


Figure 23. 9-bit System Interface for GRAM read

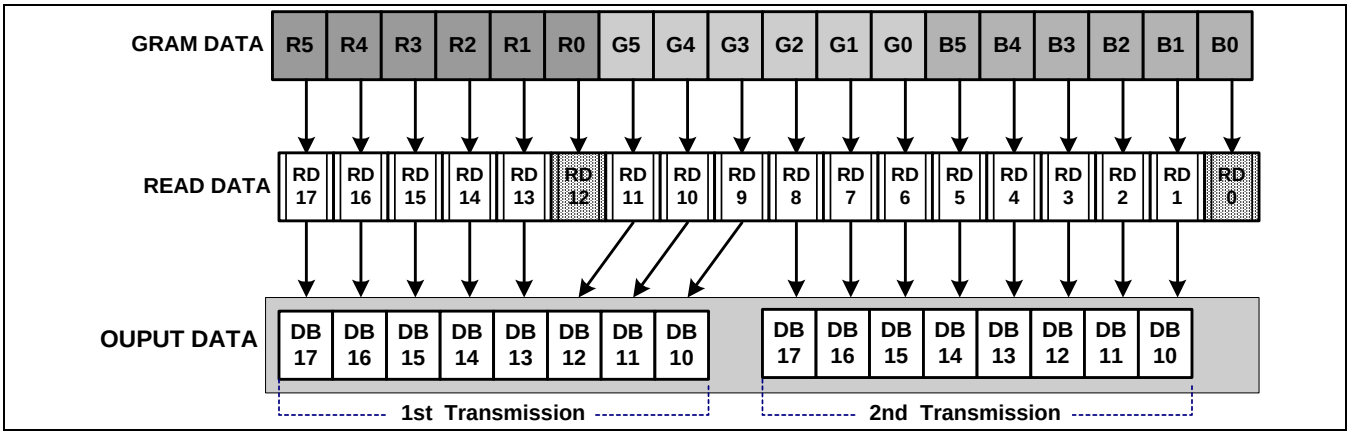


Figure 24. 8-bit System Interface for GRAM read

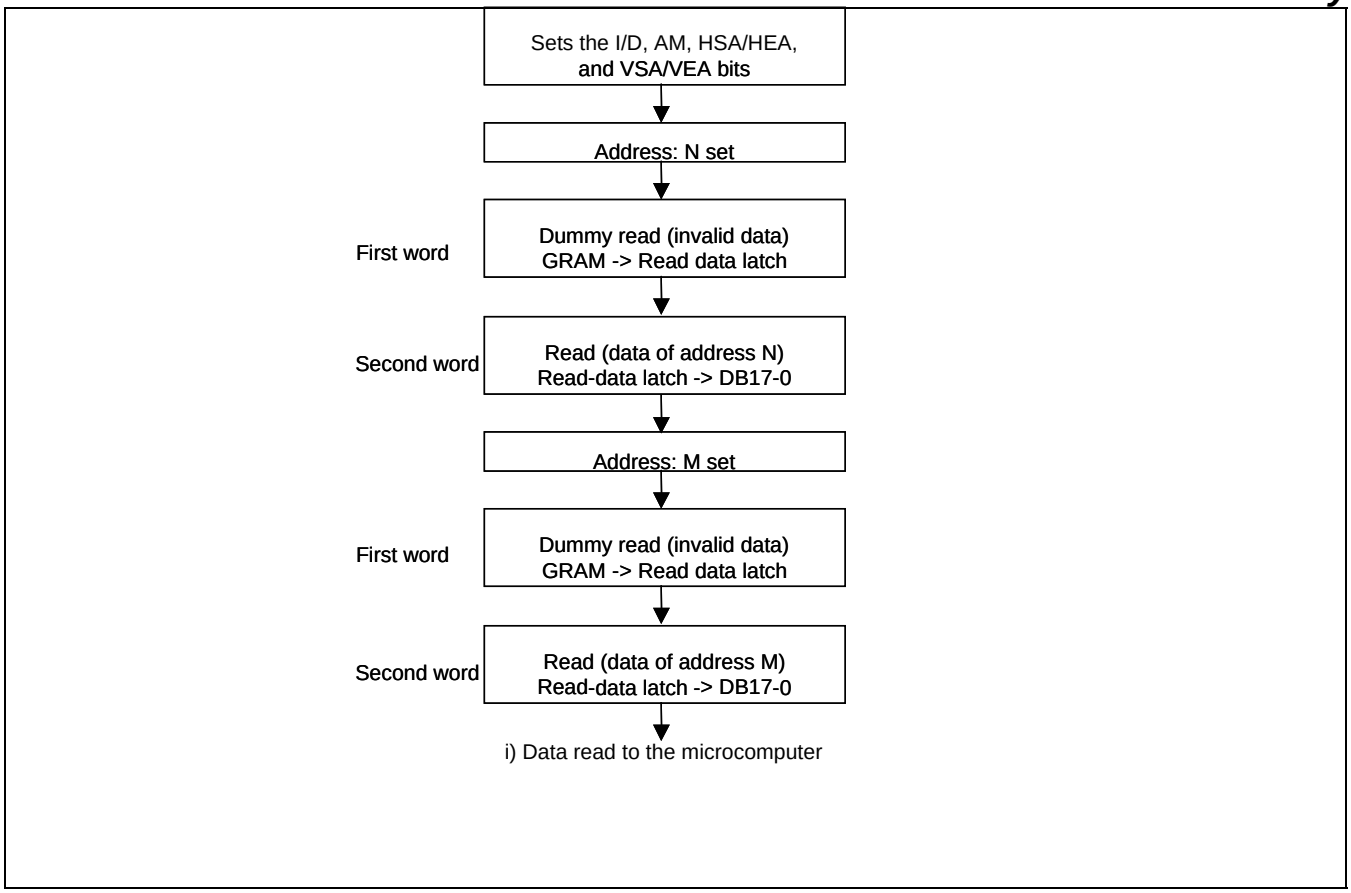


Figure 25. GRAM read sequence

Preliminary

Gamma Control (R30h to R39h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

PKP52–00: The gamma fine adjustment register for the positive polarity output

PRP12-00: The gradient adjustment register for the positive polarity output

PKN52-00: The gamma fine adjustment register for the negative polarity output

PRN12-00: The gradient adjustment register for the negative polarity output

VRP14-00: The amplitude adjustment register for the positive polarity output

VRN14-00: The amplitude adjustment register for the negative polarity output

For details, see the GAMMA ADJUSTMENT FUNCTION.

Gate Scan Position (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN5-0: Set the scanning starting position of the gate driver.

SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	Scanning start position	
						GS=0	GS=1
0	0	0	0	0	0	G1	G320
0	0	0	0	0	1	G9	G312
0	0	0	0	1	0	G17	G304
:	:	:	:	:	:	:	:
1	0	0	1	0	0	G289	G32
1	0	0	1	0	1	G297	G24
1	0	0	1	1	0	G305	G16

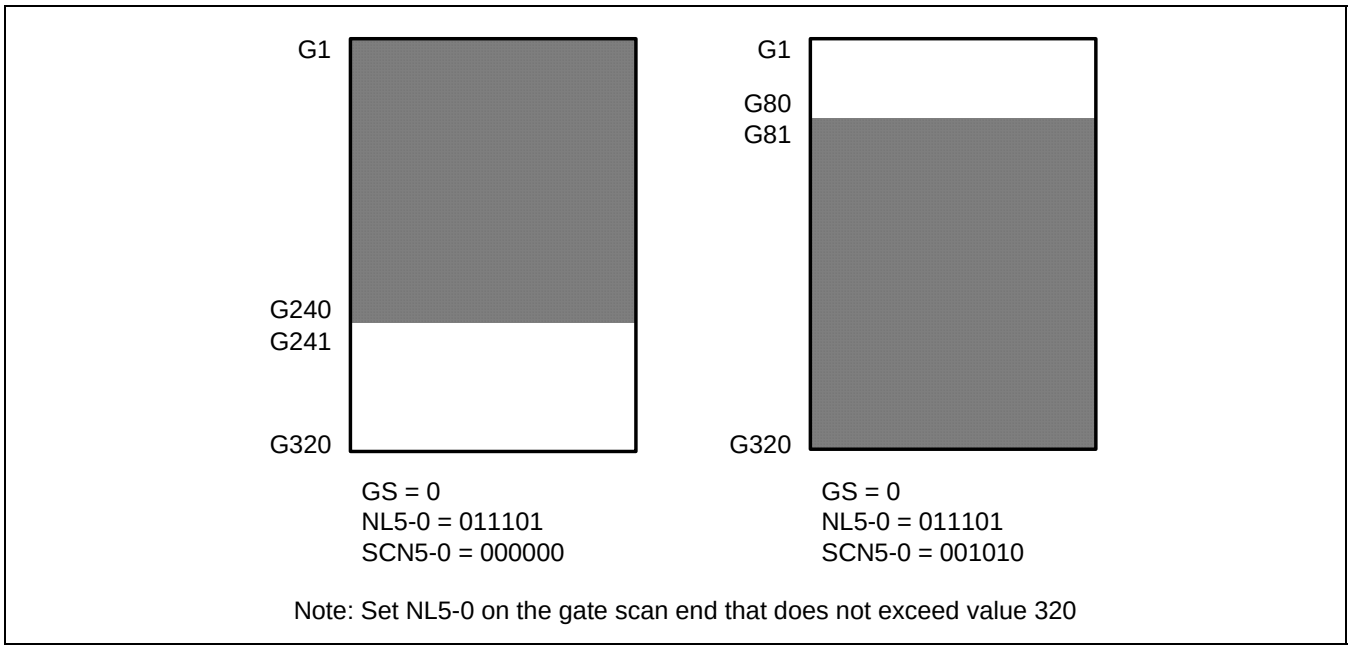


Figure 26. Relationship between NL and SCN set up value

Preliminary

Vertical Scroll Control (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL7-0: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the 1st to 320th can be scrolled for the number of the raster-row. After 320th raster-row is displayed, the display restarts from the first raster-row. The scroll length (VL8-0) is valid when VLE1 = 1 or VLE2 = 1. The raster-row display is fixed when VLE2-1 = 00.

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scroll Length
0	0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
. . .									. . .
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

Note: Don't set any higher raster-row than 319 ("13F"H)

1st Screen Driving Position (R42h/R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
W	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

2nd Screen Driving Position (R44h/R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
W	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS18–10: Specify the drive starting position for the first screen in a line unit. The LCD driving starts from the 'set value +1' gate driver.

SE18–10: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SS18–10 = 07h and SE18–10 = 10h are set, the LCD driving is performed from G8 to G17, and non-display driving is performed for G1 to G7, G18, and others. Ensure that SS18–10 ≤ SE18–10 ≤ 13Fh. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

SS28–20: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' of the gate driver. The second screen is driven when SPT = 1.

SE28–20: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' of the gate driver. For instance, when SPT = 1, SS28–20 = 20h, and SE28–20 = 13Fh are set, the LCD driving is performed from G33 to G320. Ensure that SS18–10 ≤ SE18–10 ≤ SS28–20 ≤ SE28–20 ≤ 13Fh. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

Horizontal RAM Address Position (R46h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0

Vertical RAM Address Position (R47h/R48h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VEA 8	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0
W	1	0	0	0	0	0	0	0	VSA 8	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM. The written data are from the address specified by HSA7-0 to the address specified by HEA 7-0. Note that an address must be set before RAM data are written. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ EFh.

VSA8-0/VEA8-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM. The written data are from the address specified by VSA8-0 to the address specified by VEA8-0. Note that an address must be set before RAM data are written. Ensure 000h ≤ VSA8-0 ≤ VEA8-0 ≤ 13Fh.

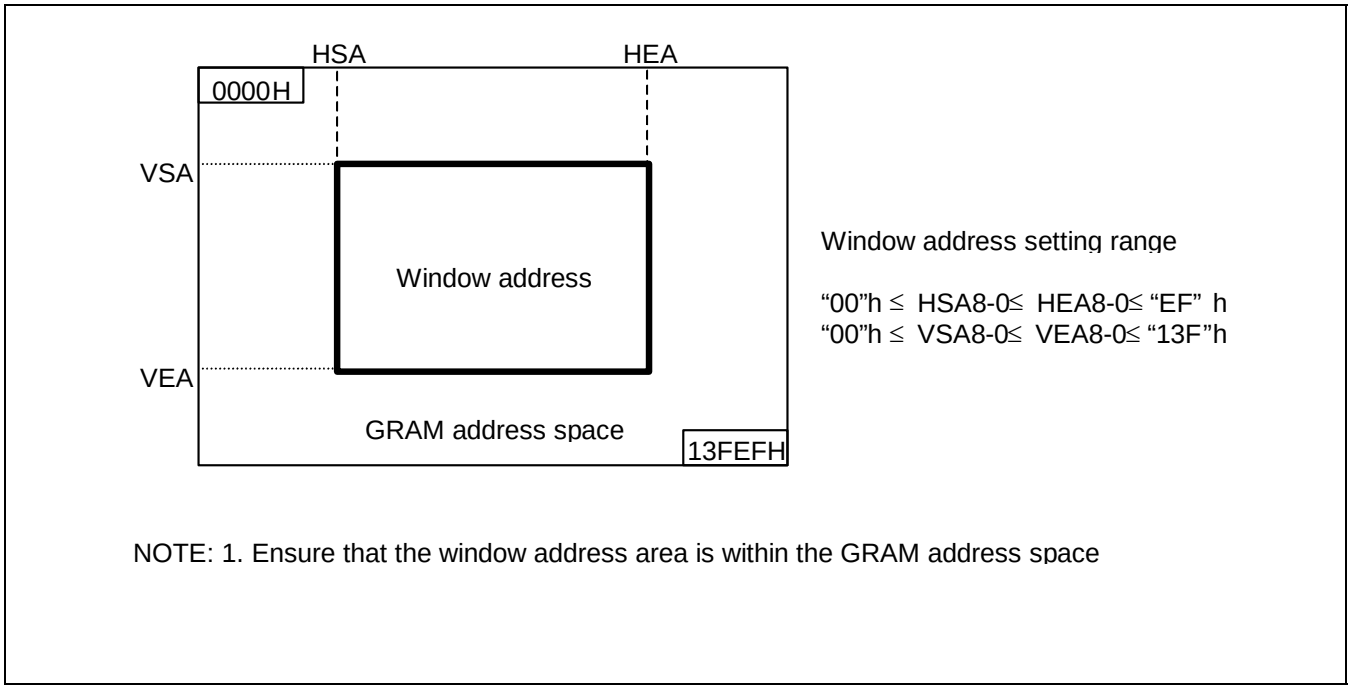


Figure 27. Window address setting range

Preliminary

RESET FUNCTION

The S6D0129 is internally initialized by RESET input. The reset input must be held for at least 1 ms. Do not access the GRAM nor initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization

1. Start oscillation executed (OSC = 1)
2. Driver output control (NL5–0 = 100111, SS = 0, GS = 0, EPL=0, VSPL=0, HSPL=0, DPL=0)
3. LCD driving AC control (FLD1-0 = 01, B/C = 0, EOR = 0)
4. Entry mode set (TRI = 0, DFM = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, BGR=0)
5. Display control 1 (PT1-0 = 00, VLE2–1 = 00: No vertical scroll, SPT = 0, GON = 0, CL = 0: 260K-color mode, REV = 0, D1–0 = 00: Display off)
6. Display control 2 (FP3-0 = 1000, BP3-0 = 1000)
7. Display control 3 (PTG1-0= 00, ISC3-0 = 0000)
8. Frame cycle control (NO1-0 = 00, SDT1-0 = 00, VCIR1-0 = 00: no charge sharing, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clock cycle in 1H period)
9. External display interface (RIM1-0=00:18-bit RGB interface, DM1-0=00: operated by internal clock, RM=0: system interface)
10. Power control 1 (SAP2-0 = 000, BT2-0 = 000, DC2–0 = 011, SLP = 0, STB = 0: Standby mode off)
11. Power control 2 (GVD5-0 = 000000, VC2-0 = 000)
12. Power control 3 (PON = 0, PON1 = 0, AON = 0)
13. Power control 4 (VCMR = 0, VCM5-0 = 000000, VML5-0 = 000000)
14. RAM address set (AD16–0 = 00000h)
15. Gamma control
    (PKP02–00 = 000, PKP12–10 = 000, PKP22–20 = 000, PKP32–30 = 000,
    PK42–40 = 000, PKP52–50 = 000, PRP02–00 = 000, PRP12–10 = 000)
    (PKN02–00 = 000, PKN12–10 = 000, PKN22–20 = 000, PKN32–30 = 000,
    PKN42–40 = 000, PKN52–50 = 000, PRN02–00 = 000, PRN12–10 = 000)
    VRP14–00 = 00000, VRP03–00 = 0000, VRN14–00 = 00000, VRN03–00 = 0000)
16. Gate scanning starting position (SCN5-0 = 000000)
17. Vertical scroll (VL8–0 = 00000000)
18. 1st screen division (SE18-10 = 100111111, SS18-10 = 00000000)
19. 2nd screen division (SE28-20 = 100111111, SS27-20 = 00000000)
20. Horizontal RAM address position (HEA7-0 = 11101111, HSA7-0 = 00000000)
21. Vertical RAM address position (VEA8-0 = 100111111, VSA8-0 = 00000000)

GRAM Data Initialization

GRAM is not automatically initialized by reset input but must be initialized by software while display is off (D1-0 = 00).

Output Pin Initialization

1. LCD driver output pins (Source output) : Output VSS level
   (Gate output) : Output VGL level
2. Oscillator output pin (OSC2): Outputs oscillation sign

Preliminary

POWER SUPPLY CIRCUIT

The following figure shows a configuration of the voltage generation circuit for S6D0129. The step-up circuits consist of step-up circuits 1 to 3. Step-up circuit1 doubles or triples the voltage supplied to VCI1 for AVDD level. Step-up circuit2 make 2, 2.5 or 3times AVDD level for VGH level, and make -1.5, -2 or -3 times AVDD level for VGL level. Step-up circuit3 reverses the VCI1 level with reference to VSS or VBS and generates the VCL level. These step-up circuits generate power supplies AVDD, GVDD, VGH, VGL, VCL, and VCOM. Reference voltages GVDD, VCOM, and VGL for the grayscale voltage are amplified from the voltage adjustment circuit. Connect VCOM to the TFT panel.

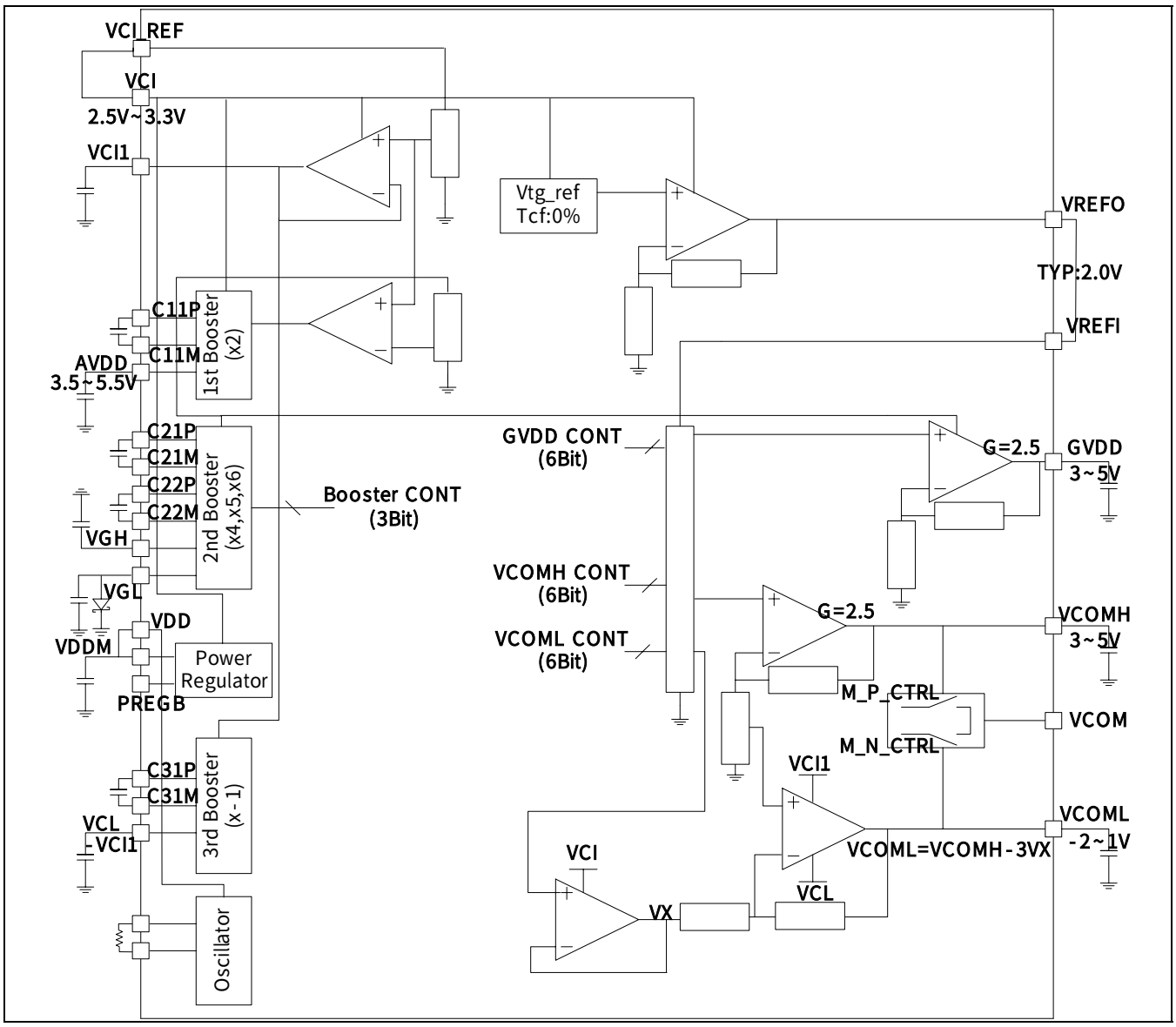


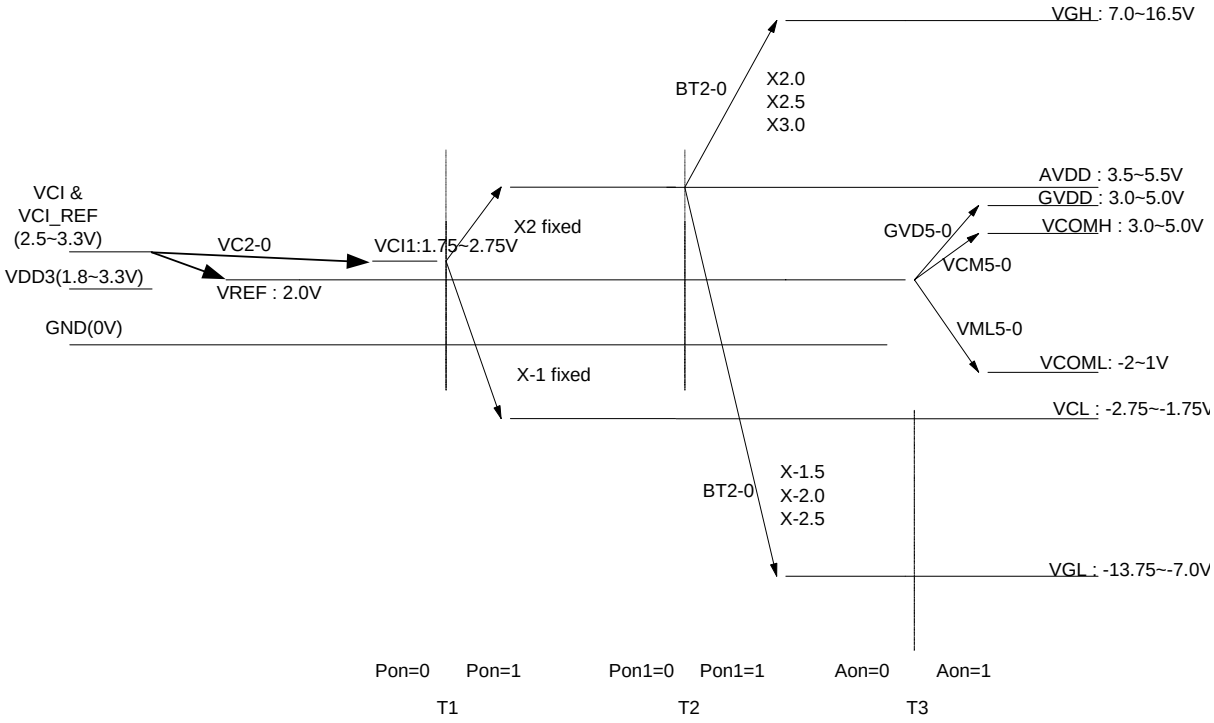
Figure 28. Configuration of the Internal Power-Supply Circuit

Notes:

Use the 1uF capacitor.

PATTERN DIAGRAMS FOR VOLTAGE SETTING

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.



Note:
Adjust the conditions of AVDD-GVDD>0.5V with loads because they differ depending on the display load to be driven. In addition, Vci can be directly input to Vci1.

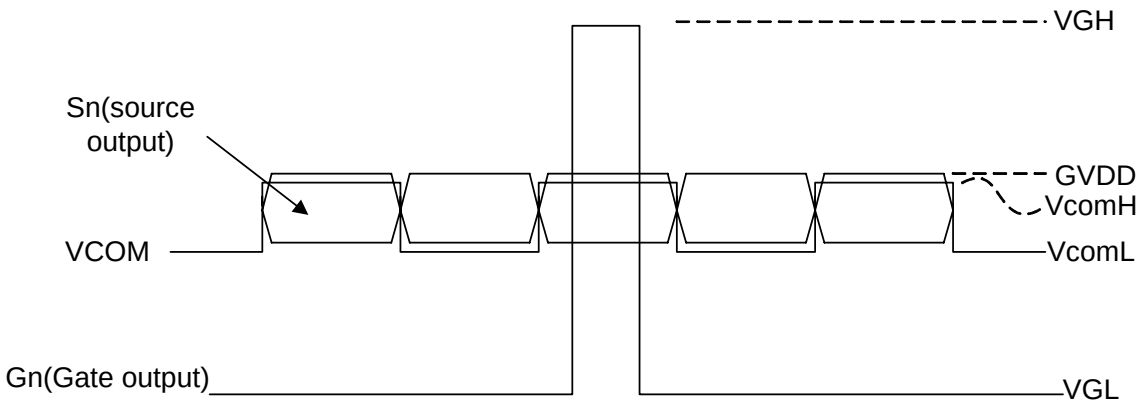


Figure 29. Pattern diagram and an example of waveforms

Preliminary

SET UP FLOW OF POWER SUPPLY

Apply the power in a sequence as shown in the following figure. The stable time of the oscillation circuit, step-up circuit, and operational amplifier depend on the external resistor or capacitance.

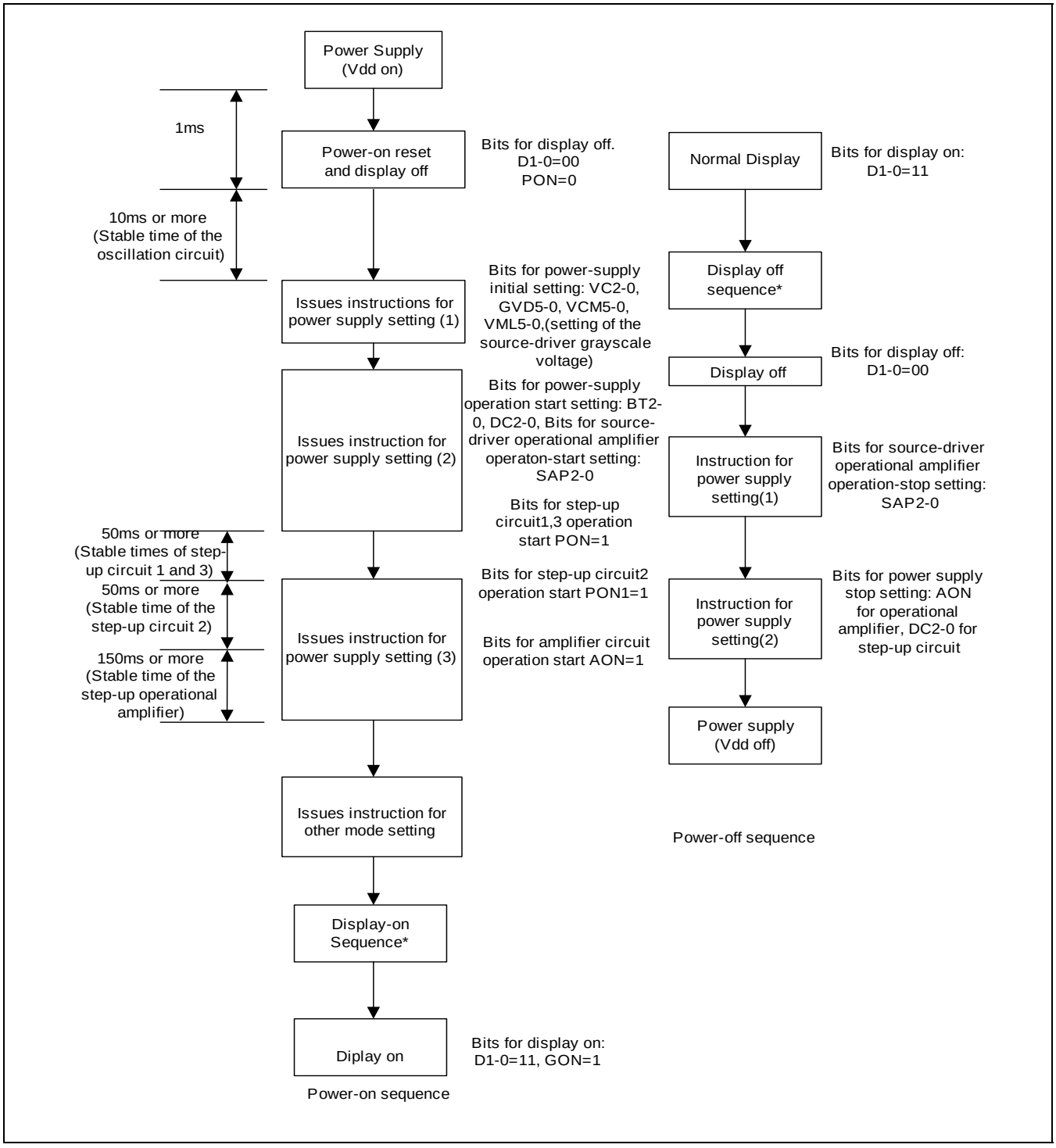
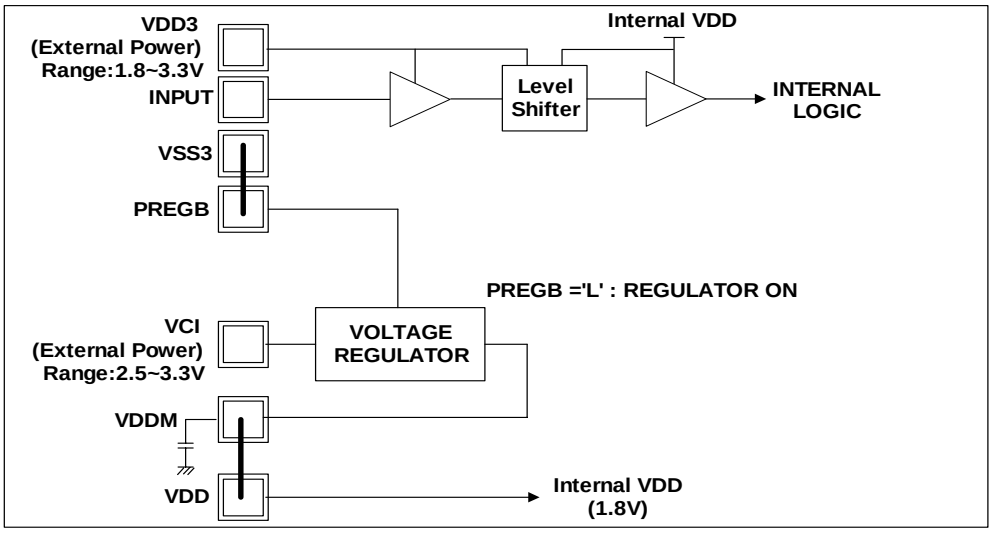


Figure 30. Set up Flow of Power Supply

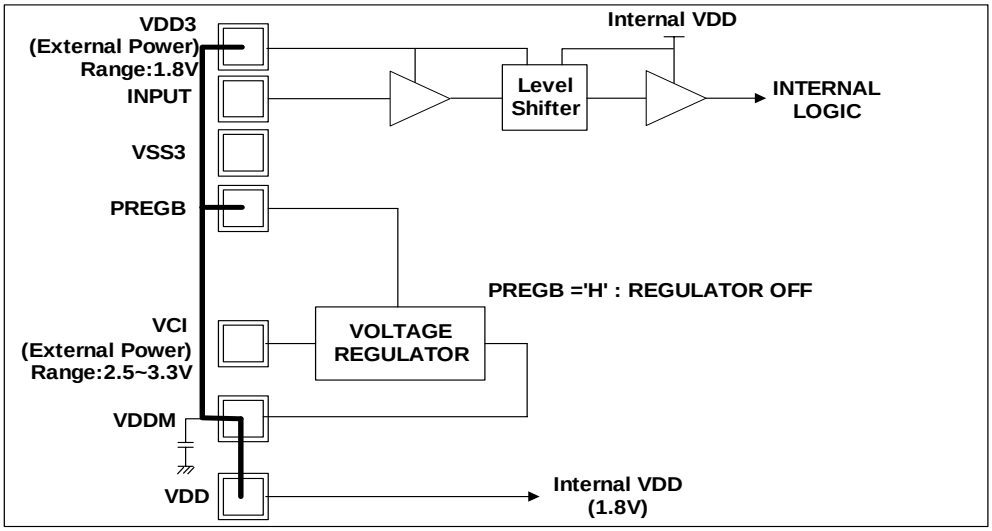
Preliminary

VOLTAGE REGULATION FUNCTION

The S6D0129 have internal voltage regulator. Voltage regulation function is controlled by PREGB pin.
If PREGB= “H”, voltage regulation is stopped. PREGB= “L” enables internal voltage regulation function.
By use of this function, internal logic circuit damage can be prohibited. Furthermore, power consumption also be obtained. Detailed function description and application setup is described in the following diagram.



(a) Voltage regulation function enabled



(b) Voltage regulation function disabled

Figure 31. Voltage regulation function

Preliminary

INTERFACE SPECIFICATION

The S6D0129 incorporates a system interface, which is used to set instructions, and an external display interface, which is used to display motion pictures. Selecting these interfaces to match the screen data (motion picture or still picture) enables efficient transfer of data for display.

The external display interface includes RGB and VSYNC interface. This allows flicker-free screen update.
When RGB interface is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for use in operating the display. The data for display (PD17-0) is written according to the values of the data enable signal (ENABLE) in synchronization with the VSYNC, HSYNC, and DOTCLK signals. In addition, using the window address function enables rewriting only to the internal RAM area to display motion pictures. Using this function also enables simultaneously display of the motion picture area and the RAM data that was written.

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When writing to the internal RAM is done within the required time after the falling edge of VSYNC, motion pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

The S6D0129 has four operation modes for each display state. These settings are specified by control instructions for external display interface. Transitions between modes should follow the transition flow.

Table 29. Display Operation Mode and RAM Access Selection

Operation Mode	RAM Access Selection (RM)	Display Operation Mode (DM1-0)
Internal Clock Operation (Displaying still picture)	System interface (RM=0)	Internal clock operation (DM1-0=00)
RGB interface (1) (Displaying motion picture)	RGB interface (RM=1)	RGB interface (DM1-0=01)
RGB interface (2) (Rewriting still picture while displaying motion pictures)	System interface (RM=0)	RGB interface (DM1-0=01)
VSYNC interface (Displaying motion Pictures)	System interface (RM=0)	VSYNC interface (DM1-0=10)

NOTES: 1) Instruction registers can only be set via system interface.
2) RGB interface and VSYNC interface cannot be used at the same time.
3) RGB interface mode cannot be set during operations.
4) For mode transitions, see the section on the external display interface.

Preliminary

SYSTEM INTERFACE

S6D0129 is enabling to set instruction and access to RAM by selecting IM3/2/1/0 pin in the system interface mode.

Table 30. IM Bits and System Interface

IM3	IM2	IM1	IM0	System Interface	DB Pin
0	0	0	0	68-system 16-bit interface	DB17 to10, 8 to1
0	0	0	1	68-system 8-bit interface	DB17 to10
0	0	1	0	80-system 16-bit interface	DB17 to10, 8 to1
0	0	1	1	80-system 8-bit interface	DB17 to10
0	1	0	*	Serial peripheral interface (SPI)	DB1 to 0
0	1	1	*	Setting disabled	-
1	0	0	0	68-system 18-bit interface	DB17 to 0
1	0	0	1	68-system 9-bit interface	DB17 to 9
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	*	*	Setting disabled	-

68/80-SYSTEM 18-BIT BUS INTERFACE

When you set the IM3/2/1/0 (interface mode) to the VDD3/VSS/VSS/VSS level, the S6D0129 allows 68-system 18-bit parallel data transfer. When you set the IM3/2/1/0 to the VDD3/VSS/VDD3/VSS level, the S6D0129 allows 80-system 18-bit parallel data transfer.

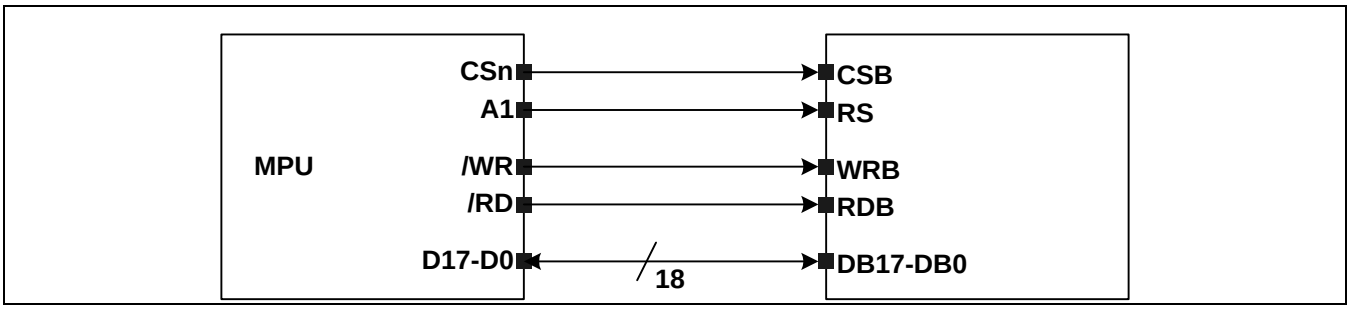


Figure 32. Interface with the 18-bit Microcomputer

68/80-SYSTEM 18-bit interface data FORMAT

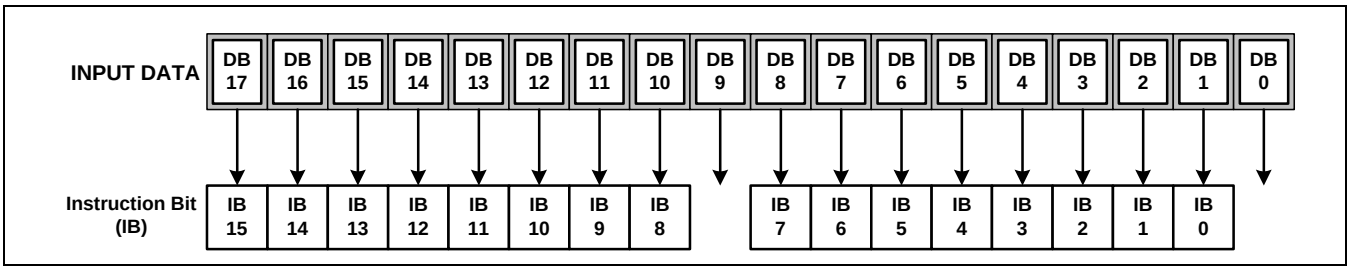


Figure 33. Instruction format for 18-bit Interface

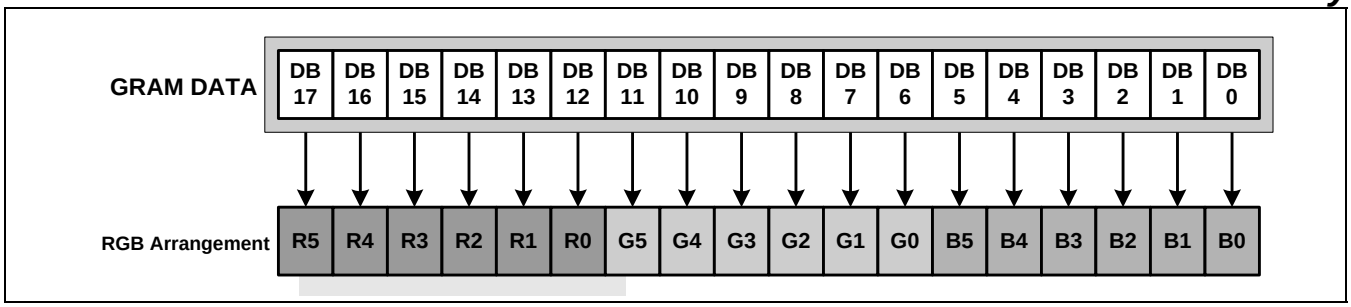


Figure 34. RAM Data Write format for 18-bit Interface

68/80-SYSTEM 16-BIT BUS INTERFACE

When you set the IM3/2/1/0 (interface mode) to the VSS/VSS/VSS/VSS level, the S6D0129 allows 68-system 16-bit parallel data transfer. When you set the IM3/2/1/0 to the VSS/VSS/VDD3/VSS level, the S6D0129 allows 80-system 16-bit parallel data transfer.

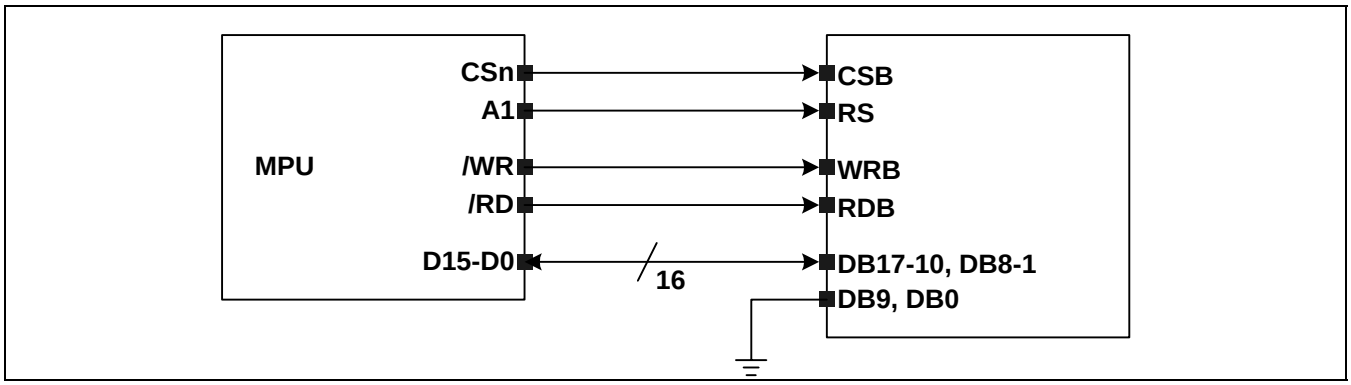


Figure 35. Interface with the 16-bit Microcomputer

68/80-SYSTEM 16-bit interface data FORMAT

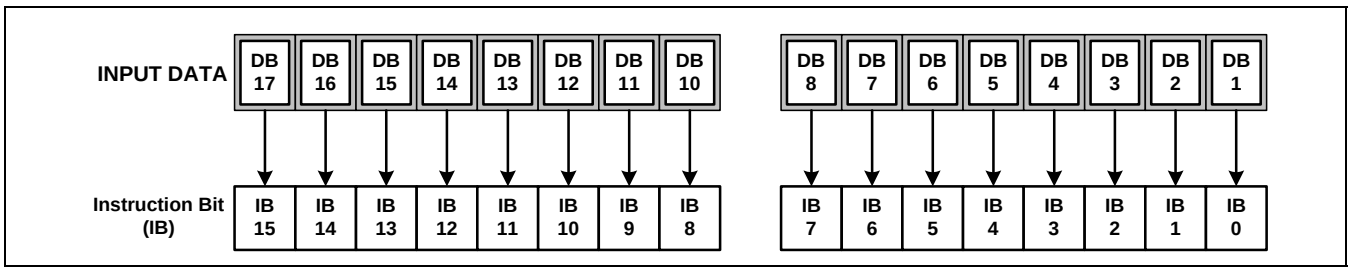


Figure 36. Instruction format for 16-bit Interface

Preliminary

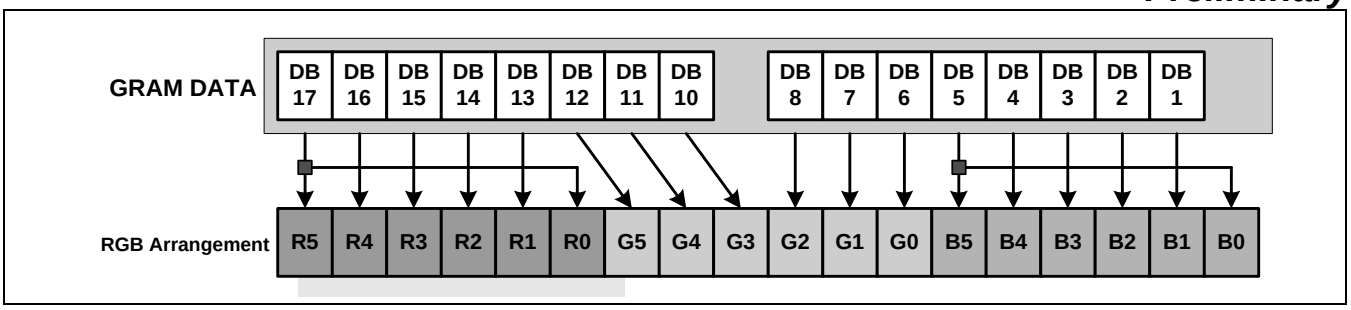


Figure 37. RAM Data Write format for 16-bit Interface

Preliminary

68/80-SYSTEM 9-BIT BUS INTERFACE

When you set the IM3/2/1/0 (interface mode) to the VDD3/VSS/VSS/VDD3 level, the S6D0129 allows 68-system 9-bit parallel data transfer using pins DB17–DB9. And, when you set the IM3/2/1/0 to be VDD3/VSS/VDD3/VDD3 level, the S6D0129 allows 80-system 9-bit parallel data transfer. The 16-bit instructions and RAM data are divided into nine upper/lower bits and the transfer starts from the upper nine bits. Fix unused pins DB8–DB0 to the VDD 3 or VSS level. Note that the upper bytes must also be written when the index register is written.

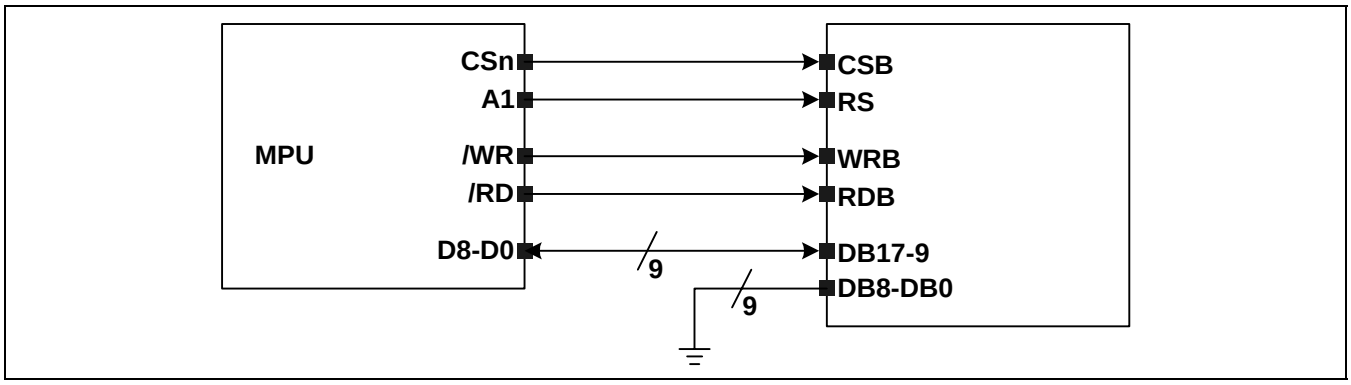


Figure 38. Interface to 9-bit Microcomputer

68/80-SYSTEM 9-bit interface data FORMAT

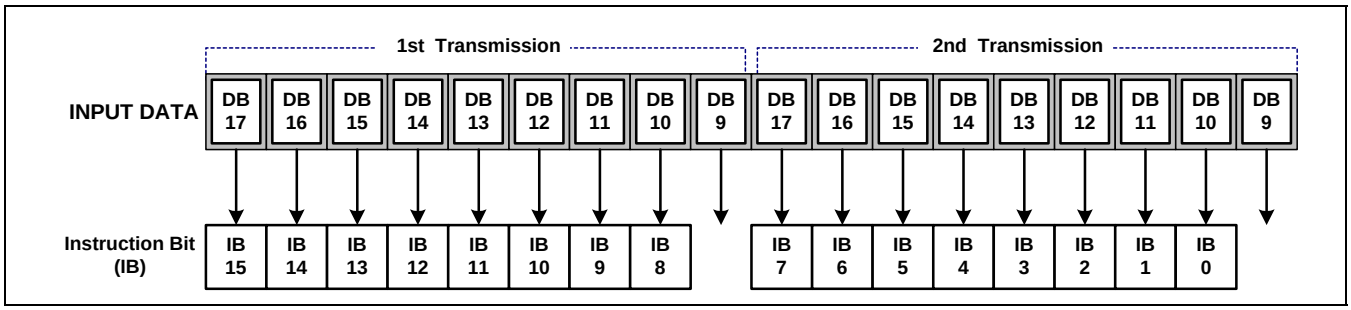


Figure 39. Instruction format for 9-bit Interface

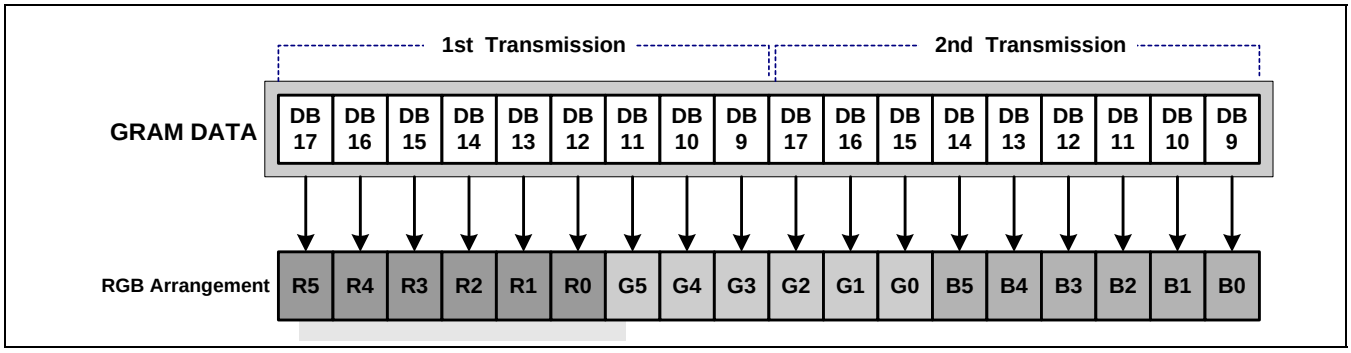


Figure 40. RAM Data Write format for 9-bit Interface

NOTE: Transfer synchronization function for a 9-bit bus interface

The S6D0129 supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 9-bit data transfer in the 9-bit bus interface. Noise causing transfer mismatch between the nine upper and lower bits can be corrected by a reset triggered by consecutively writing a “00”H instruction four times. The next transfer starts from the upper nine bits. Executing synchronization function periodically can recover any runaway in the display system.

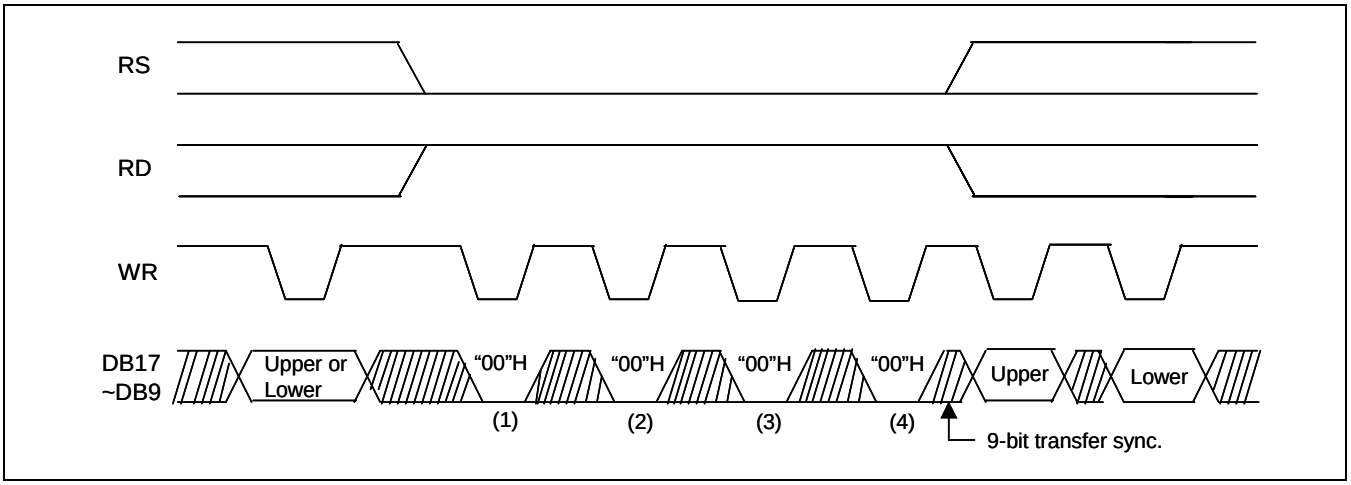


Figure 41. 9-bit Transfer Synchronization

68/80-SYSTEM 8-BIT BUS INTERFACE

When you set the IM3/2/1/0 (interface mode) to the VSS/VSS/VSS/VDD3 level, the S6D0129 allows 68-system 8-bit parallel data transfer. When you set the IM3/2/1/0 to the VSS/VSS/VDD3/VDD3 level, the S6D0129 allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB9–DB0 to the VDD3 or VSS level. Note that the upper bytes must also be written when the index register is written.

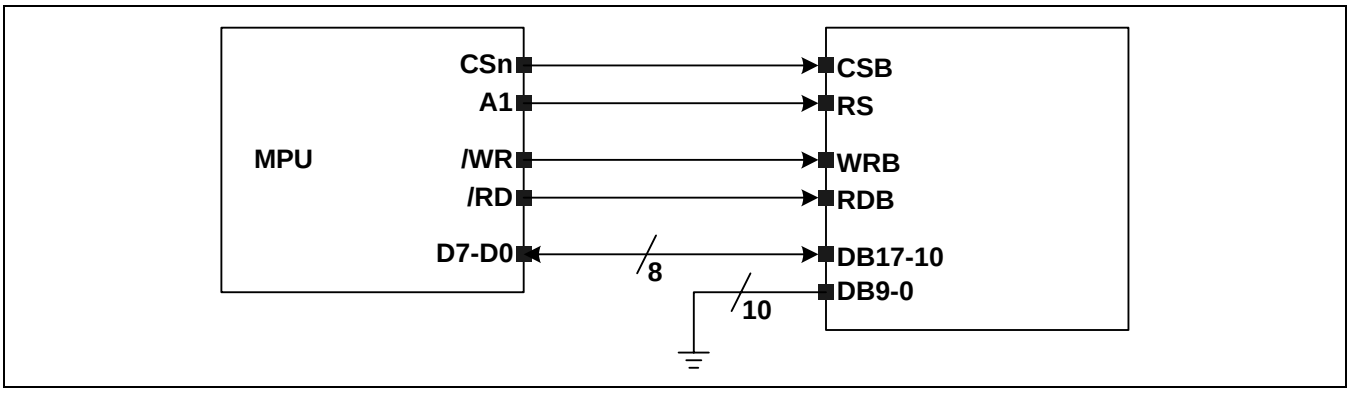


Figure 42. Interface with the 8-bit Microcomputer

Preliminary

68/80-SYSTEM 8-bit interface data FORMAT

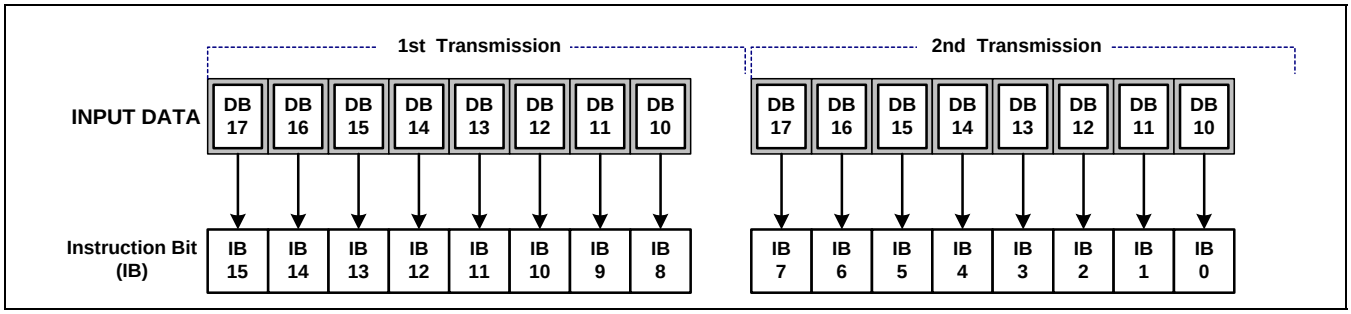


Figure 43. Instruction format for 8-bit Interface

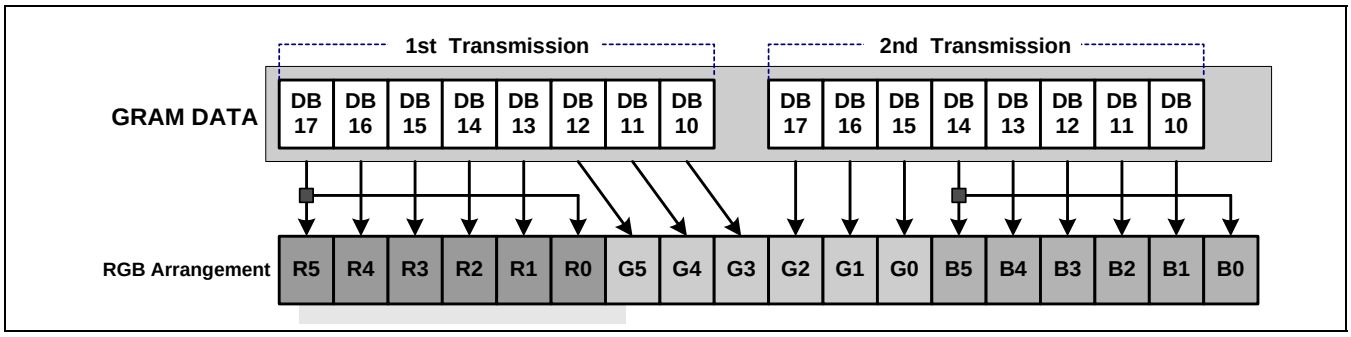


Figure 44. RAM Data Write format for 8-bit Interface

NOTE: Transfer synchronization function for an 8-bit bus interface

The S6D0129 supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a “00”H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

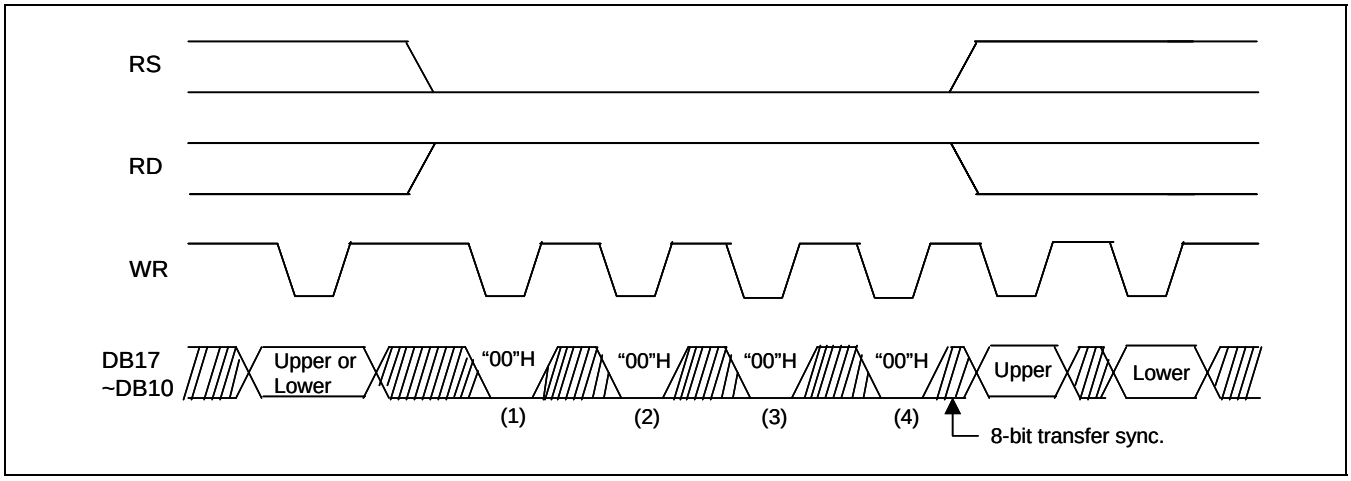


Figure 45. 8-bit Transfer Synchronization

Preliminary

SERIAL DATA TRANSFER

When you set the IM3 pin to the VSS level, the S6D0129 allows serial peripheral interface (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB17-2 pins are not used and the pins must be fixed at VDD3 or VSS. The S6D0129 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input. The S6D0129 is selected when the 6-bit chip address in the start byte matches the 6-bit device identification code that is assigned to the S6D0129. When selected, the S6D0129 receives the subsequent data string. The ID pin can determine the LSB of the identification code. The five upper bits must be 01110. Two different chip addresses must be assigned to a single S6D0129 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.
After receiving the start byte, the S6D0129 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All S6D0129 instructions are 16 bits. Two bytes are received with the MSB first (DB17 to 0), and the instructions are internally executed. After the start byte has been received, the next bytes are consisted of the first byte is fetched as the upper eight bits of the instruction and the second byte is fetched as the lower eight bits of the instruction. Four bytes of RAM read data after the start byte are invalid. The S6D0129 starts to read correct RAM data from the fifth byte.

Table 31. Start Byte Format

Transfer bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

NOTE: ID bit is selected by the IM0/ID pin.

Table 32. RS and R/W Bit Function

RS	RW	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

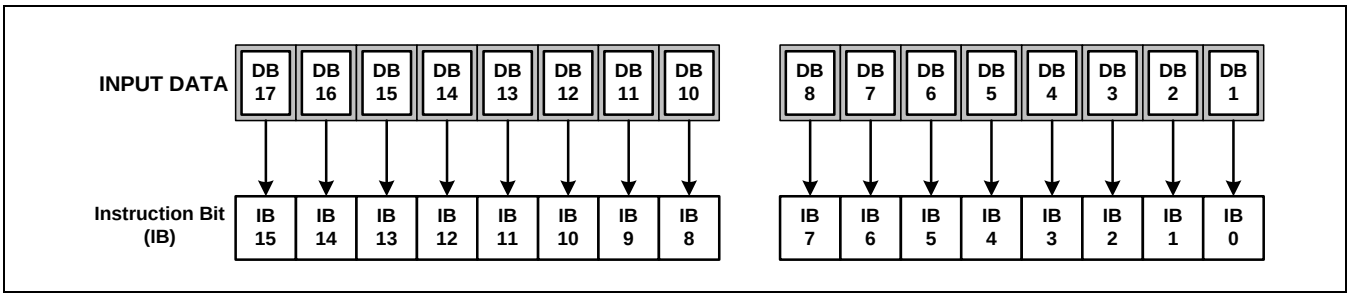


Figure 46. Instruction format for Serial Data Transfer

Preliminary

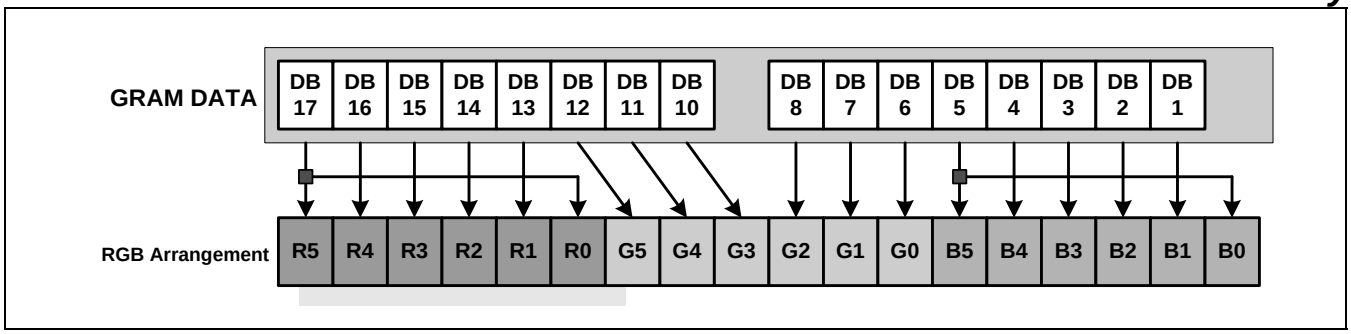


Figure 47. RAM Data Write format for Serial Data Transfer

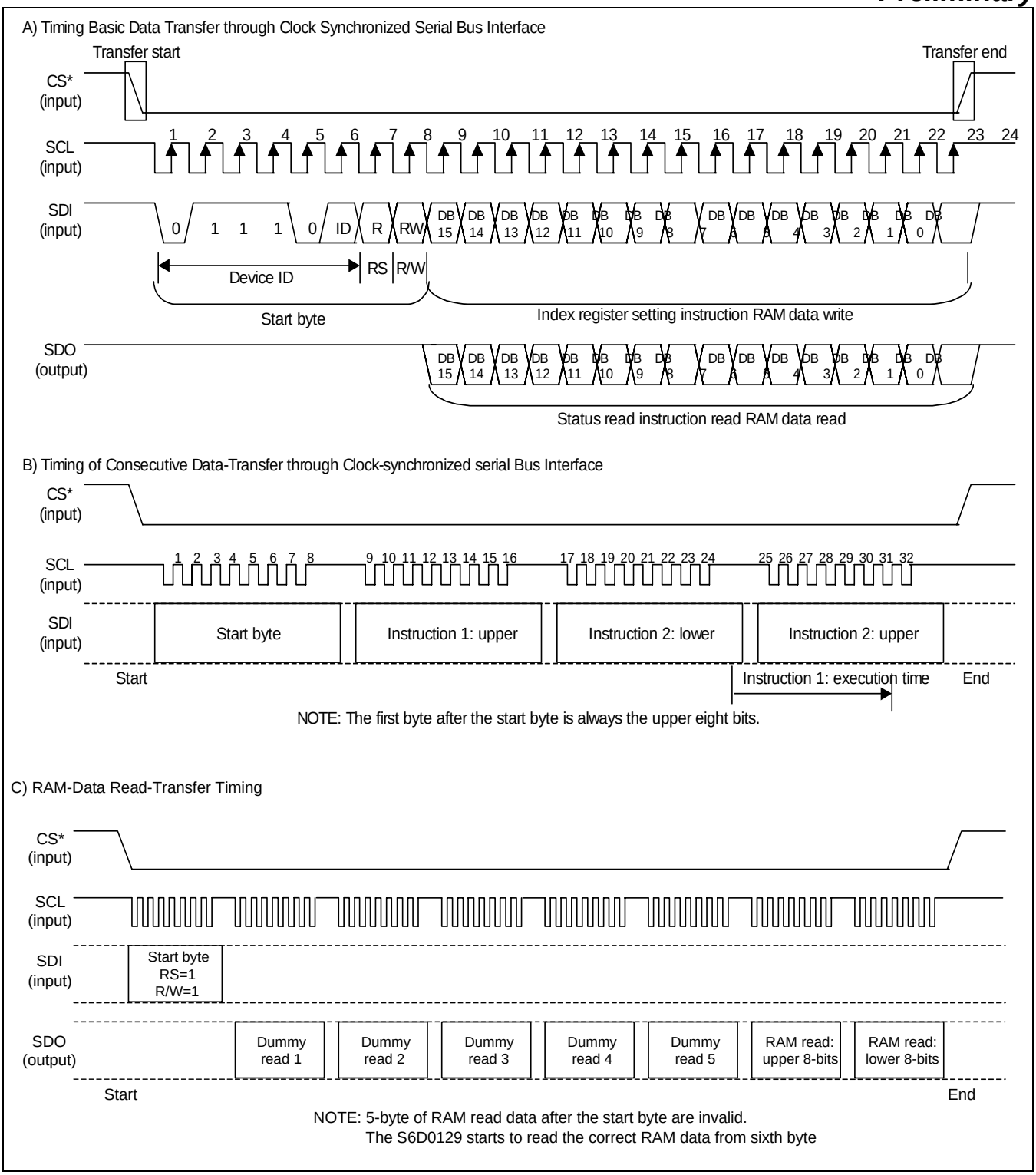


Figure 48. Procedure for transfer on clock synchronized serial bus interface

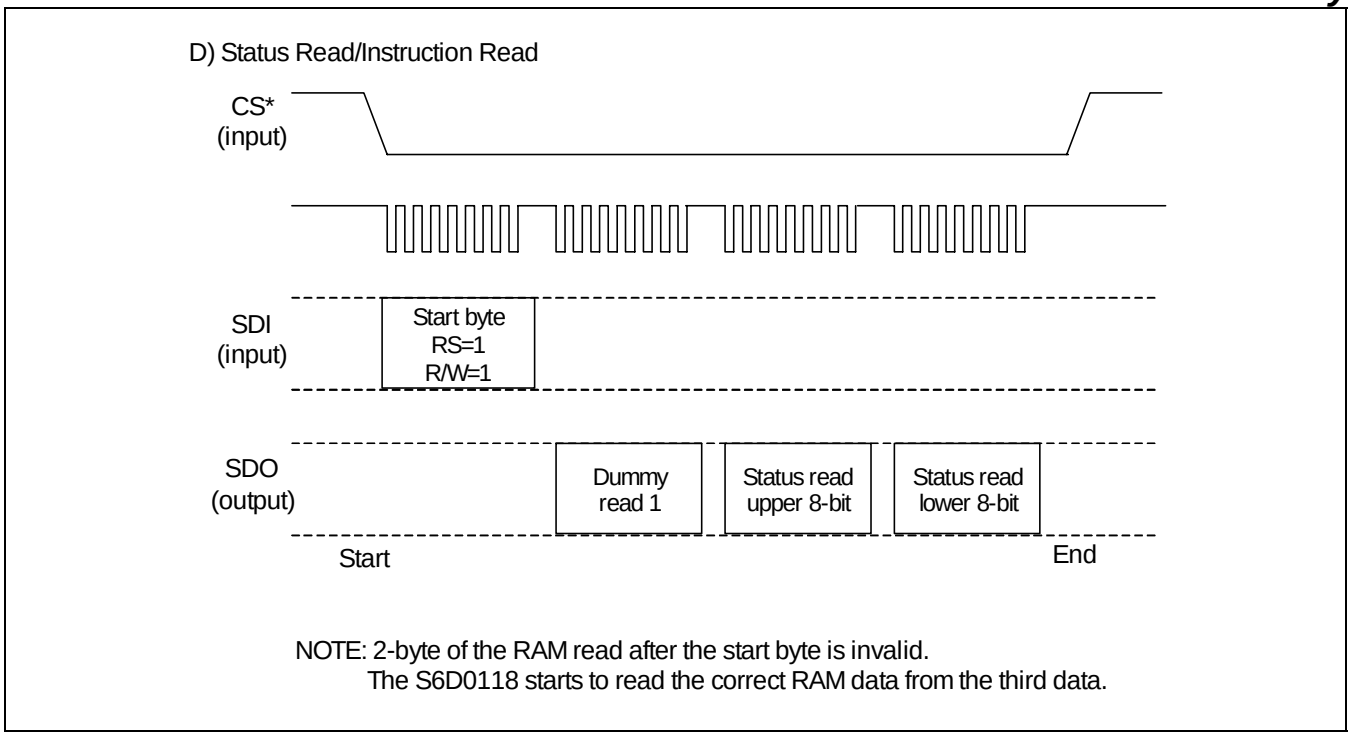


Figure 49. Procedure for transfer on clock synchronized serial bus interface (continued)

Preliminary

VSYNC INTERFACE

The S6D0129 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

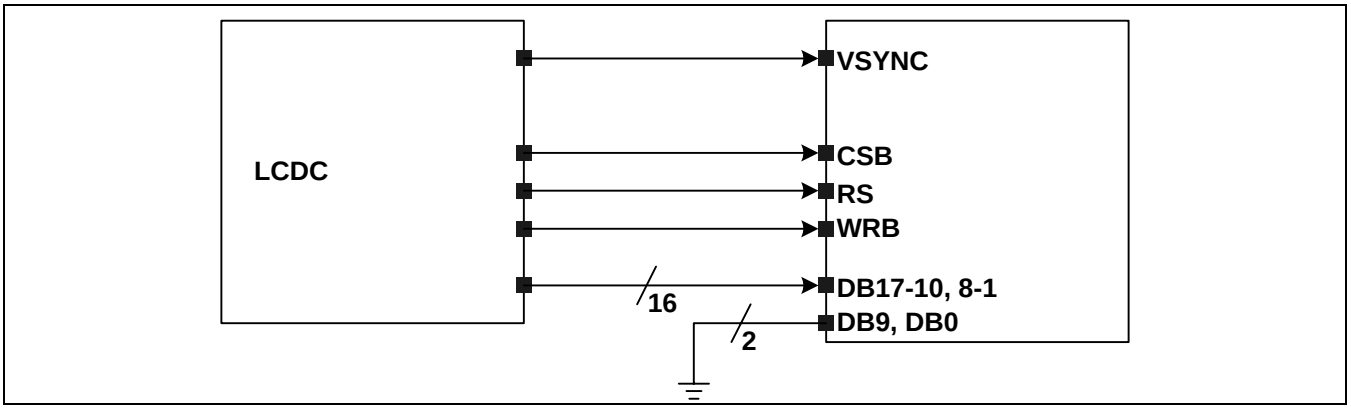


Figure 50. VSYNC Interface

When DM1-0=”10” and RM=”0”, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of motion pictures with the conventional interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

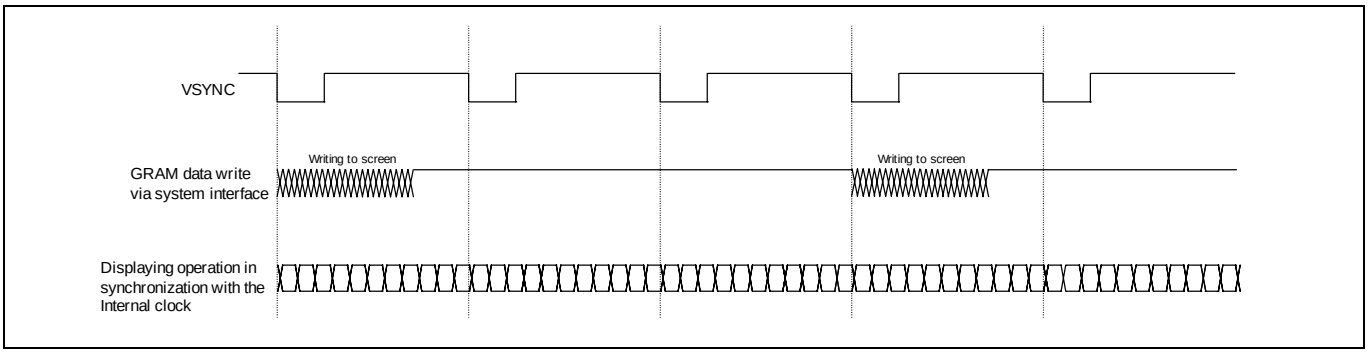


Figure 51. Motion Picture Data Transfer via VSYNC Interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below. The internal memory writing address counter is reset by VSYNC. So, insure interval time between VSYNC falling and GRAM data writing.

Internal clock frequency (fosc) [Hz] = Frame freq. × (Display raster-row (NL) + Front porch (FP) + Back porch (BP)) × 16-Clock × Fluctuation

Minimum speed for RAM writing [Hz] > 240 × Display raster-row (NL) / {((Back porch (BP) + Display raster-row (NL) – Margin) × 16 Clock) / fosc}

NOTE: When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

An example is shown below.

Example

Display size	240RGB × 320 raster-rows
Display line number	320 raster-row (NL=100111)
Back/Front porch	14 lines/2 lines (BP=1110/FP=0010)
Frame Frequency	60Hz

Internal clock frequency (fosc) [Hz]= 60 Hz × (320 + 2 + 14) lines× 16 clock × 1.1 / 0.9 = 394 kHz

NOTES: 1. Calculating the internal clock frequency requires considering the fluctuation. In the above case a 10% Fluctuation within the VSYNC period is assumed.

2. The fluctuation includes LSI production variation and air temperature fluctuation. Other fluctuations, including those for the external resistors and the supplied power, are not included in this example. Please keep in mind that a margin for these factors is also needed.

Minimum speed for RAM writing [Hz] > 240 × 320 / {((14 + 320 – 2) lines × 16 clock) / 394kHz} = 5.7 MHz

NOTES: 3. In this case RAM writing starts immediately after the falling edge of VSYNC.

4. The margin for display raster-row should be two raster-rows or more at the completion of RAM writing for one frame.

Therefore, when RAM writing starting immediately after the falling edge of VSYNC is performed at 5.7 MHz or more, the data for display can be rewritten before display operation starts. This means that flicker-free display operation is achieved.

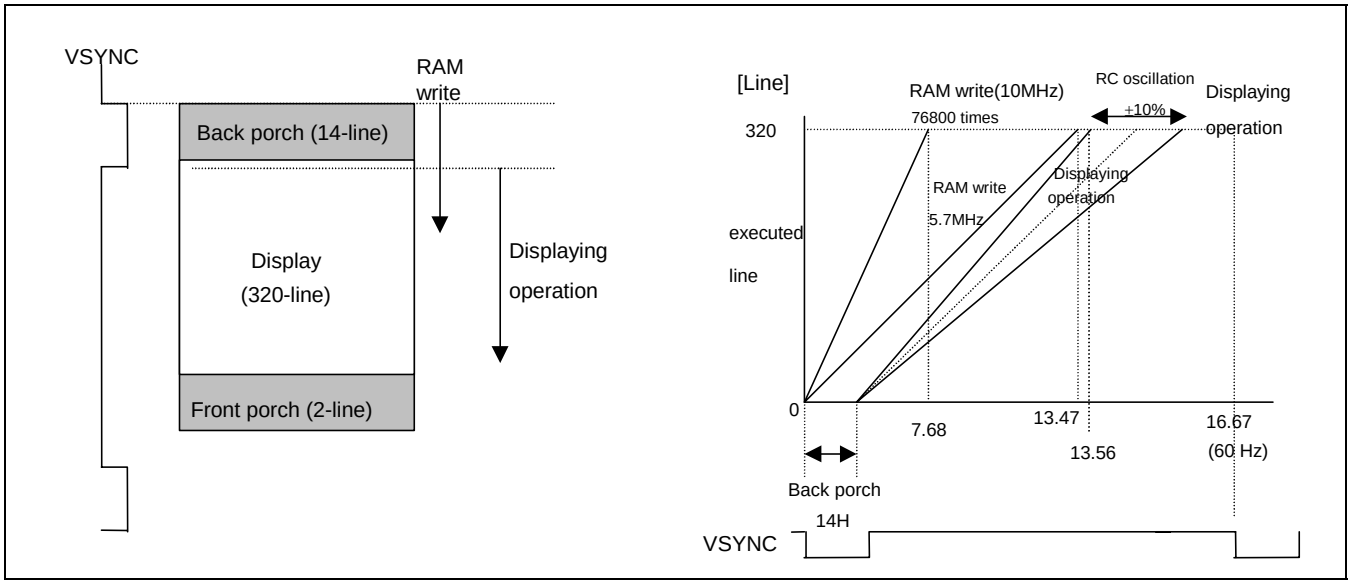


Figure 52. Operation for VSYNC Interface

Preliminary

Usage on VSYNC interface

1. The Example above is a calculated value. Please keep in mind that a margin for these factors is also needed. Because production variation of the internal oscillator requires consideration.
2. The Example above is a calculated value of rewriting the whole screen. A limitation of the motion picture area generates a margin for the RAM write speed.

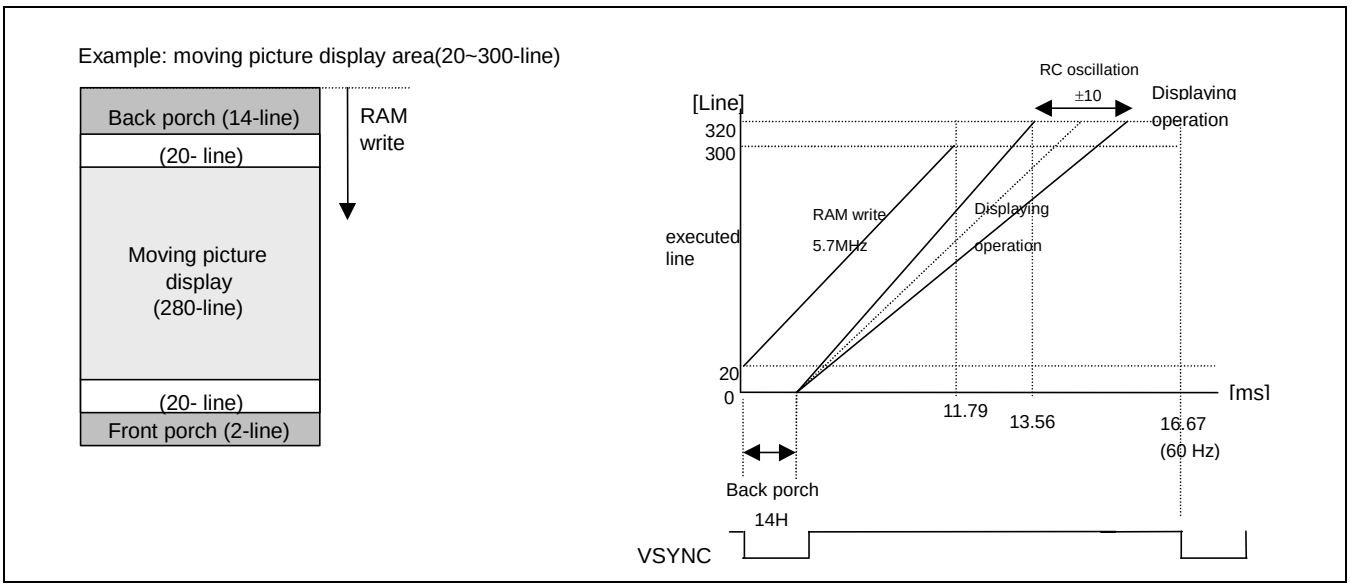


Figure 53. Limitation of Motion picture Area

3. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.
4. Transition between the internal operating clock mode (DM1-0=”00”) and VSYNC interface mode will be valid after the completion of the screen, which is displayed when the instruction is set.

Preliminary

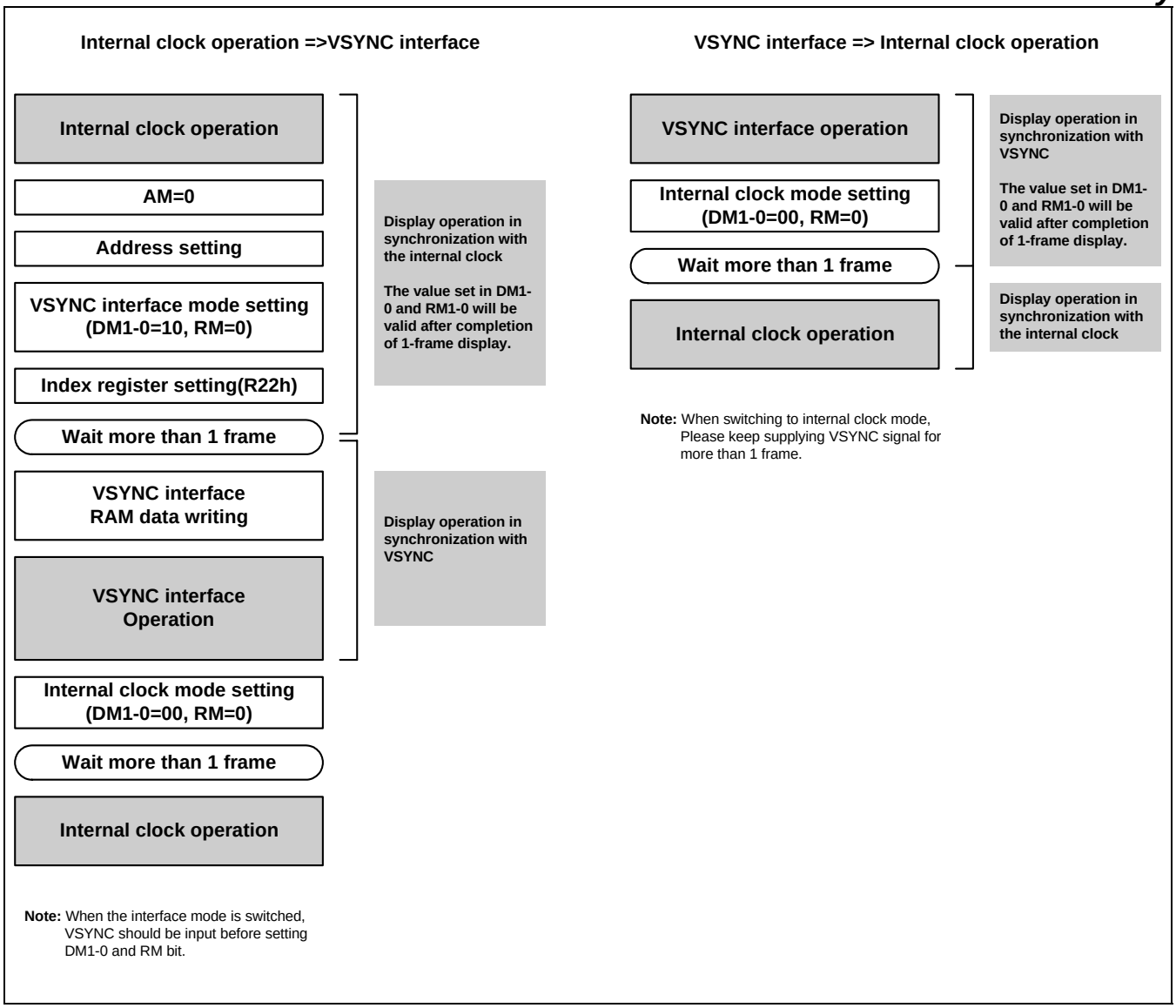


Figure 54. Transition between the Internal Operating Clock Mode and VSYNC Interface Mode

5. Partial display, vertical scroll, and interlaced driving functions are not available on VSYNC interface mode.
6. The flow of above method performs the VSYNC interface mode. And, the AM bit should be 0.

Preliminary

EXTERNAL DISPLAY INTERFACE

The following interfaces are available as external display interface. It is determined by bit setting of DM1-0.

Table 33. DM Bits

DM1	DM0	Display Operation Mode
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RGB INTERFACE

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK. Combining the function of the high-speed write mode and the window address enables transfer only the screen to be updated and reduce the power consumption.

Table 34. RIM Bits

RIM1	RIM0	RGB Interface	PD Pin
0	0	18-bit RGB interface	PD17 to 0
0	1	16-bit RGB interface	PD17 to13, 11 to 1
1	0	6-bit RGB interface	PD17 to12
1	1	Setting disabled	

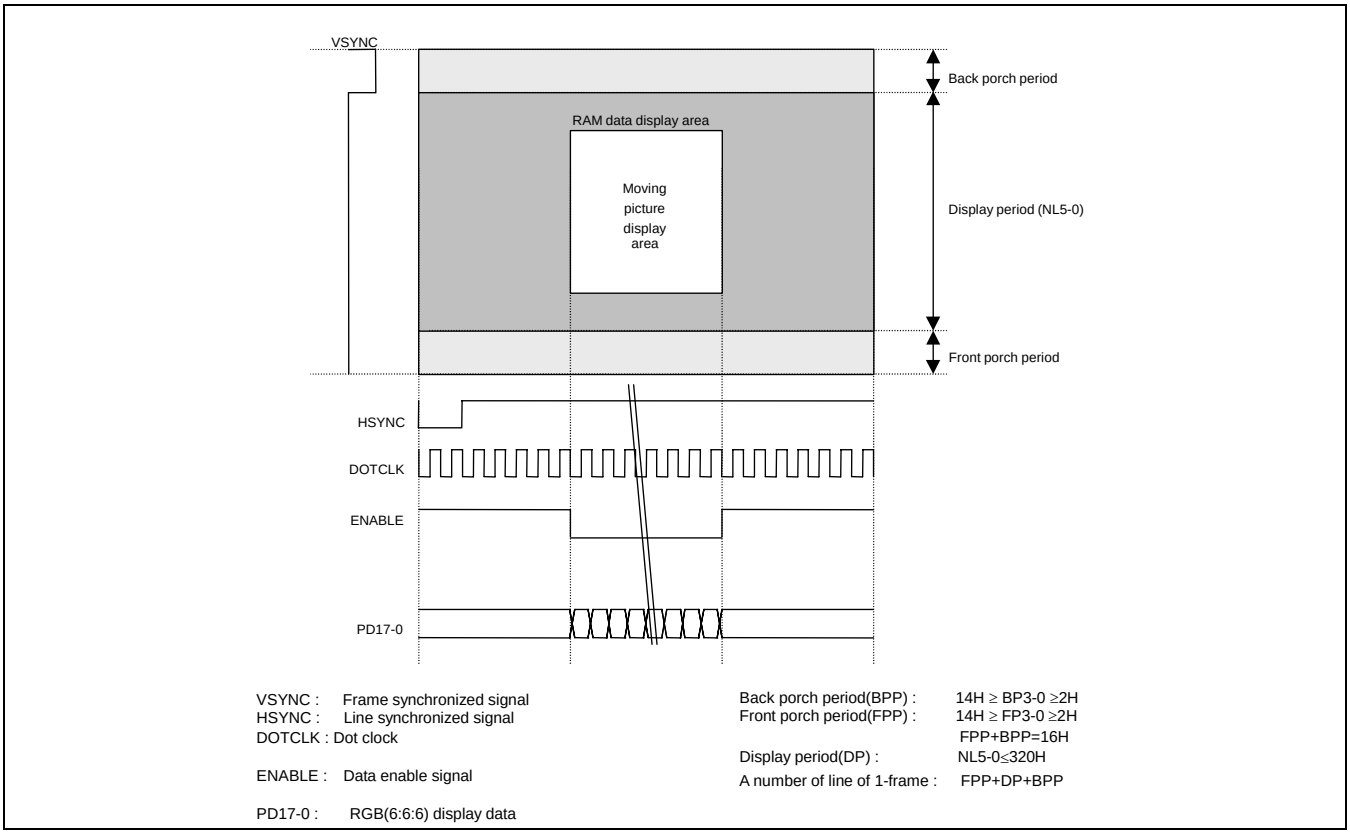


Figure 55. RGB Interface

SAMSUNG ELECTRONICS

Preliminary

ENABLE SIGNALS

The relationship between EPL and ENABLE signals is shown below. When ENABLE is not active, the address is not updates. When ENABLE is active, the address is updated.

Table 35. Relationship between EPL and ENABLE

EPL	ENABLE	RAM WRITE	RAM ADDRESS
0	0	Valid	Updated
0	1	Invalid	Hold
1	0	Invalid	Hold
1	1	Valid	Update

Preliminary

RGB INTERFACE TIMING

Time chart for RGB interface is shown below. (In case of EPL = 0)

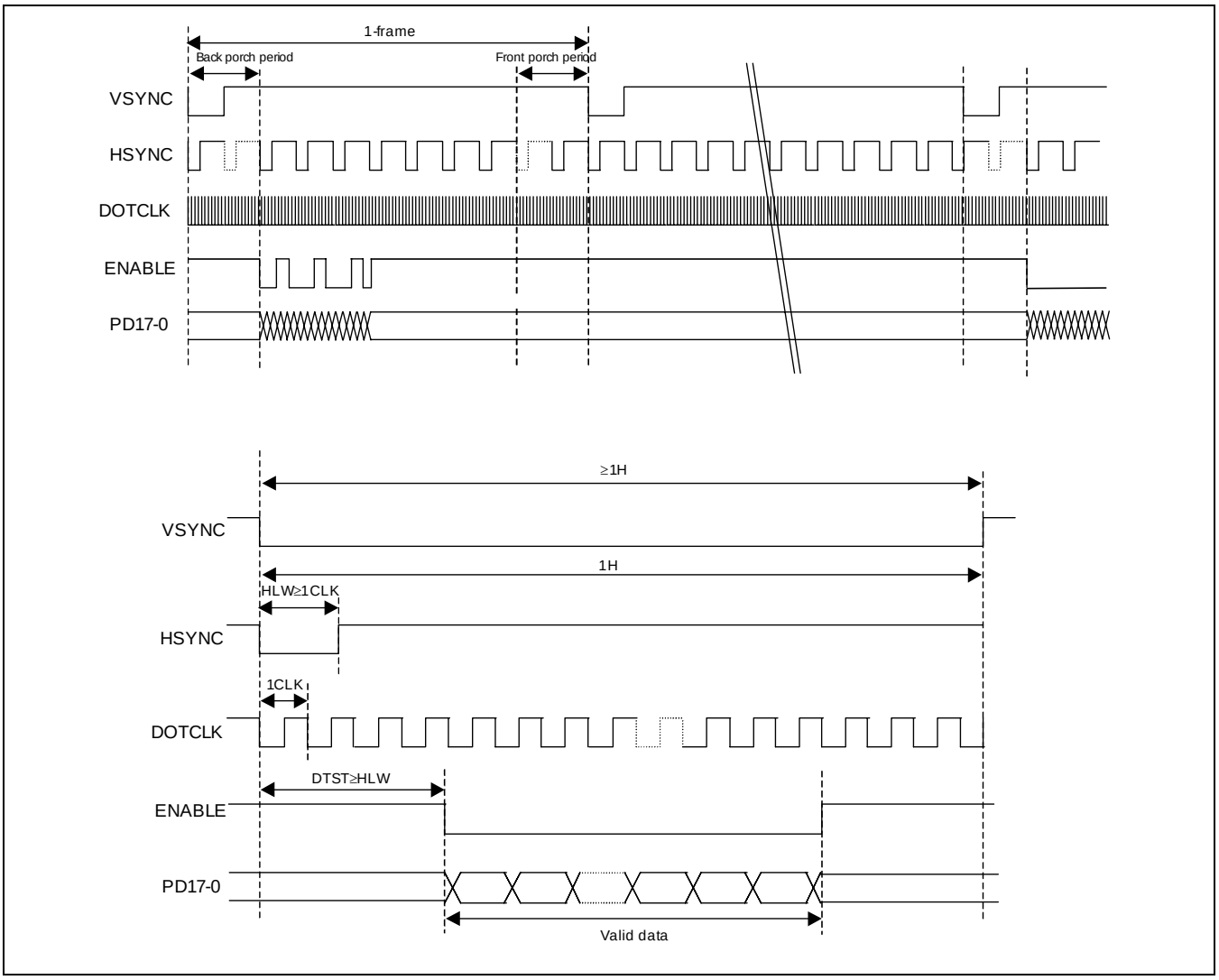


Figure 56. 16-/18-bit RGB Interface Timing (In case of EPL = 0, DPL = 0, VSPL = 0, HSPL = 0)

VLW: The period in which VSYNC is “Low” level
HLW: The period in which HSYNC is “Low” level
DTST: Set up time of data transfer

SAMSUNG ELECTRONICS

Preliminary

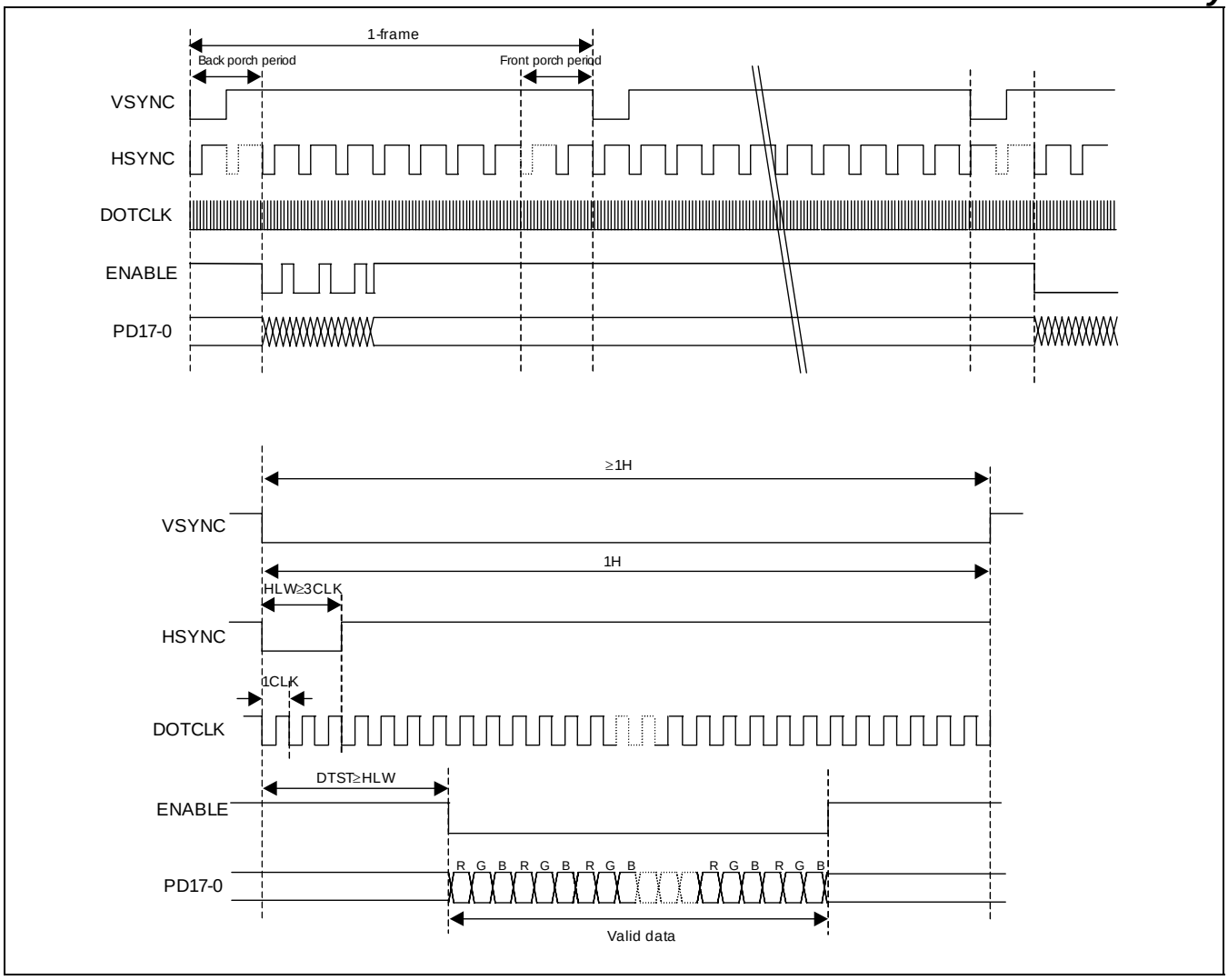


Figure 57. 6-bit RGB Interface Timing (In case of EPL = 0, DPL = 0, VSPL = 0, HSPL = 0)

VLW: The period in which VSYNC is “Low” level
HLW: The period in which HSYNC is “Low” level
DTST: Set up time of data transfer

NOTES: 1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.
2. VSYNC, HSYNC, ENABLE, DOTCLK and PD17-2 should be transferred in units of three clocks.

Preliminary

MOTION PICTURE DISPLAY

The S6D0129 incorporates RGB interface to display motion pictures and RAM to store data for display.
For displaying motion pictures, the S6D0129 has the following features.
- Motion picture area can only be transferred by the window address function.
- Motion picture area to be rewritten can only be transferred.
- Reducing the amount of data transferred enables reduce the power consumption to the whole system.
- Still picture area, such as an icon, can be updated while displaying motion pictures combining with the system interface.

RAM ACCESS VIA RGB INTERFACE AND SYSTEM INTERFACE

RAM can be accessed via the system interface when RGB interface is in use. When data is written to RAM during RGB interface mode, the ENABLE bit should be low to stop data writing via RGB interface, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is high. After this RAM access via the system interface, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB interface. When a RAM write conflict occurs, data writing is not guaranteed.
Example of display motion picture via RGB-I/F and updating still picture via the system interface are shown below.

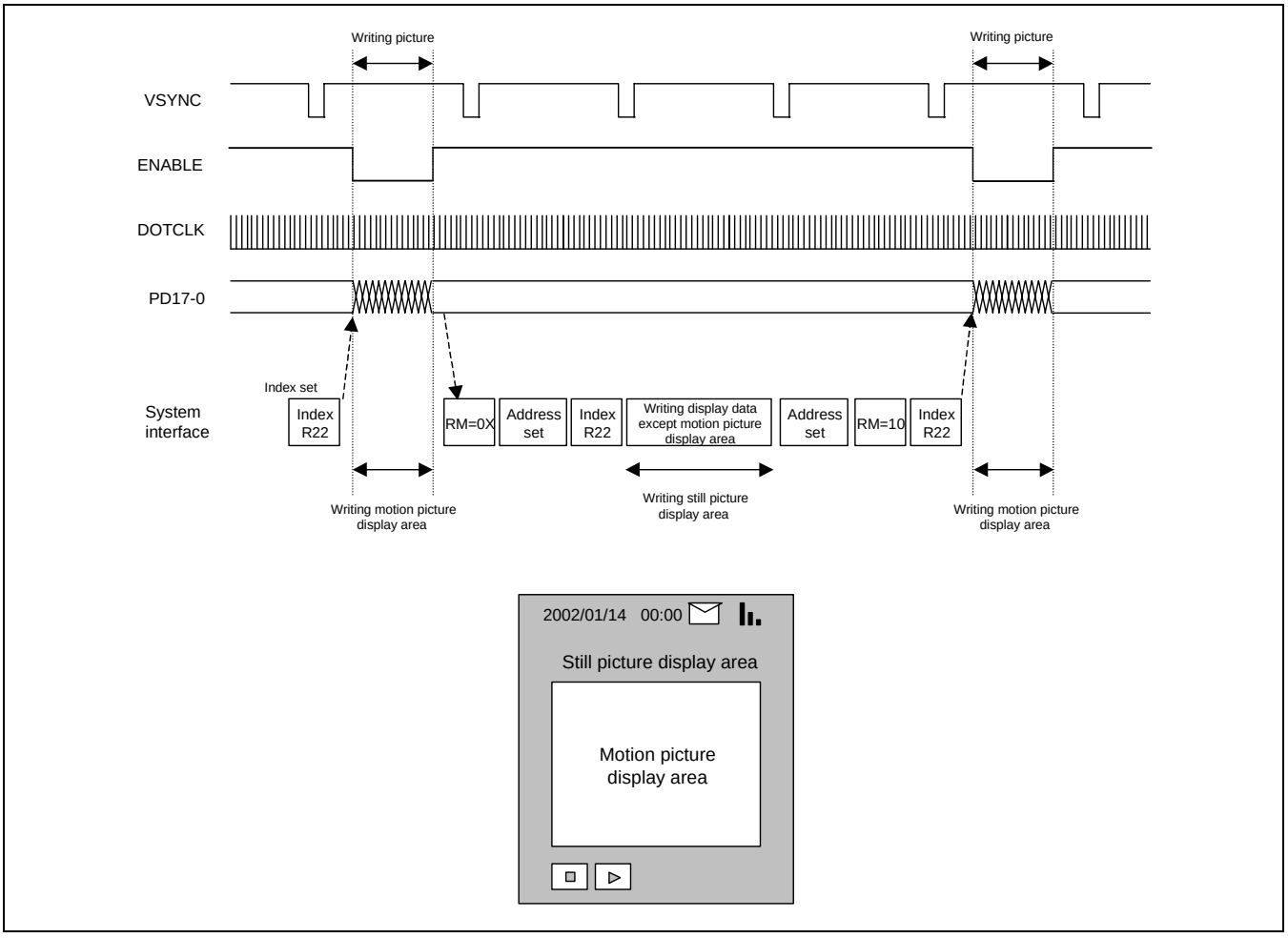


Figure 58. Example of Updating Still Picture Area during Displaying Motion Picture (In case of EPL = 0, VSPL = 0)

SAMSUNG ELECTRONICS

Preliminary

6-BIT RGB INTERFACE

6-bit RGB interface can be used by setting RIM1-0 pins to “00”. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (PD17 to 12), the data valid signal (VLD), and the data enable signal (ENABLE). Unused pins must be fixed to the VDD3 or GND level.

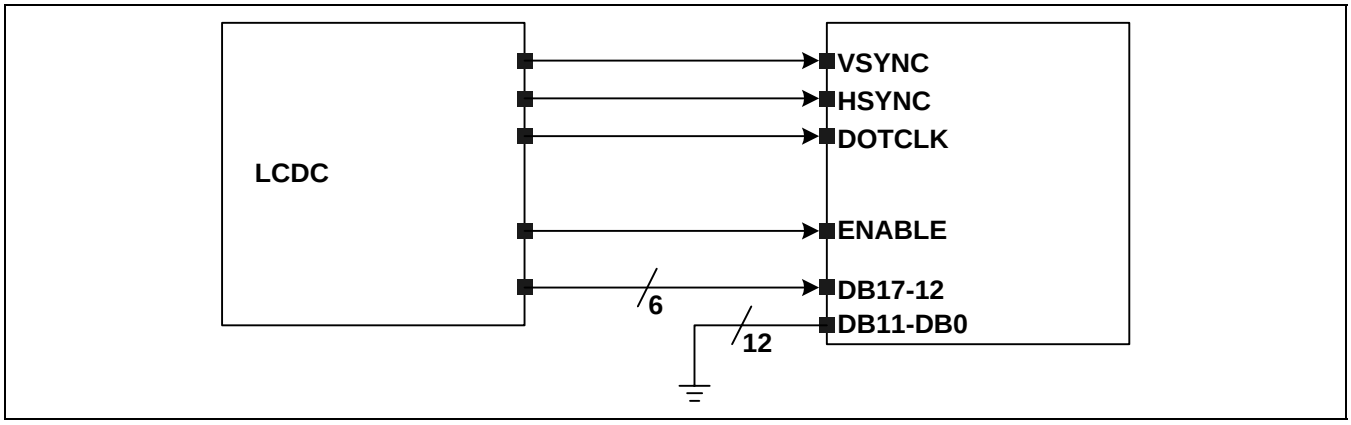


Figure 59. 6-bit RGB Interface

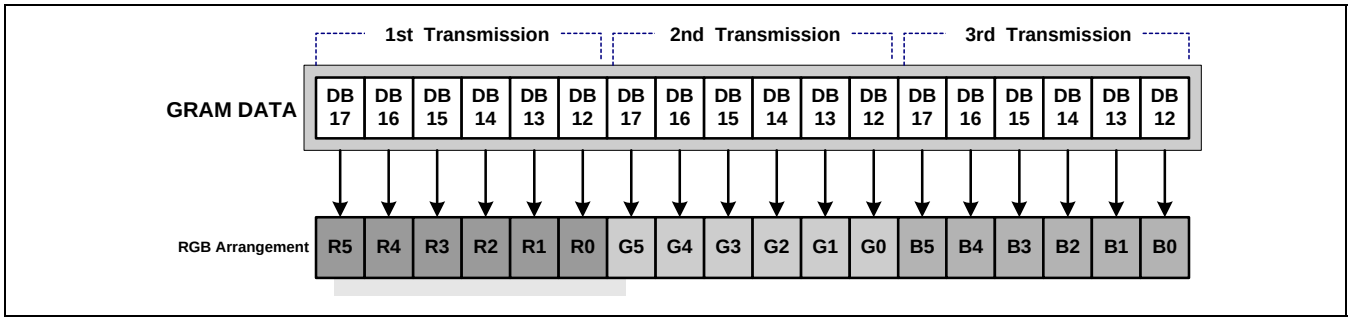


Figure 60. GRAM Write Data format for 6-bit RGB Interface Mode

NOTE: Transfer synchronization function for an 6-bit bus interface. The S6D0129 has the transfer counter to count 1st, 2nd and 3rd data transfer in the 6-bit bus interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected transfer restarts correctly. In this method, when data is consecutively transferred such as displaying motion pictures, the effect of transfer mismatch will be reduced and recover normal operation.

NOTE: The internal display is operated in units of three DOTCLK. When the DOTCLK is not input in units of pixels, click mismatch occurs and the frame, which is operated, and the next frame are not display correctly.

Preliminary

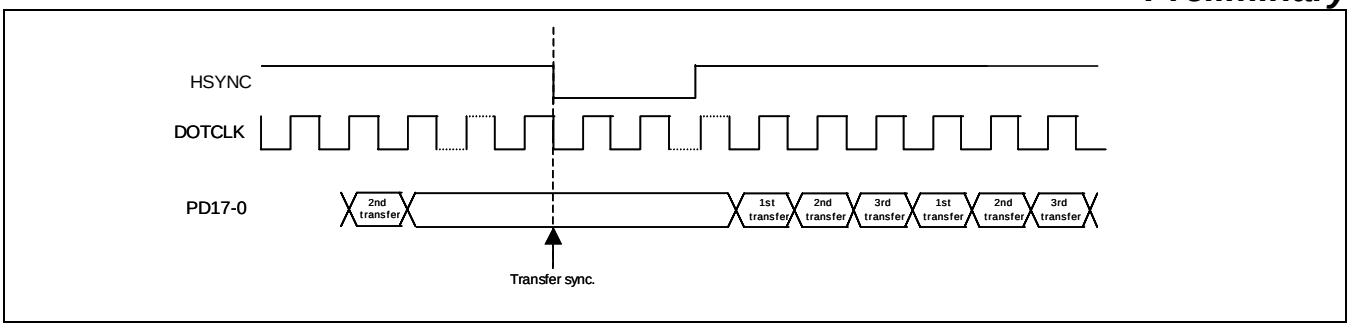


Figure 61. Transfer Synchronization Function when 6-bit RGB Interface

16-BIT RGB INTERFACE

The 16-bit RGB interface can be used by setting RIM1-0 pins to 01. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (PD17-13 and 11-1). Instruction should be set via the system interface.

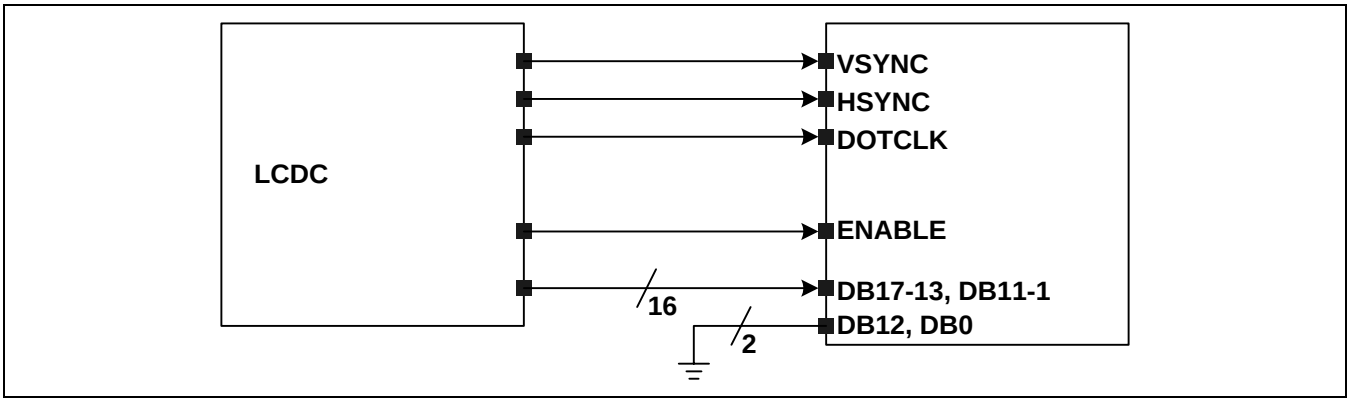


Figure 62. 16-bit RGB Interface to System

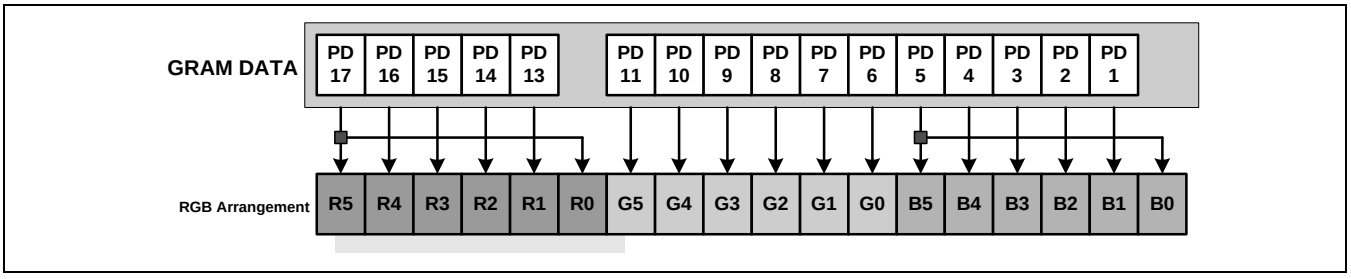


Figure 63. GRAM Write Data in the 16-bit RGB Interface Mode

Preliminary

18-BIT RGB INTERFACE

The 18-bit RGB interface can be used by setting MIF1-0 pins to 01. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (PD17-0).

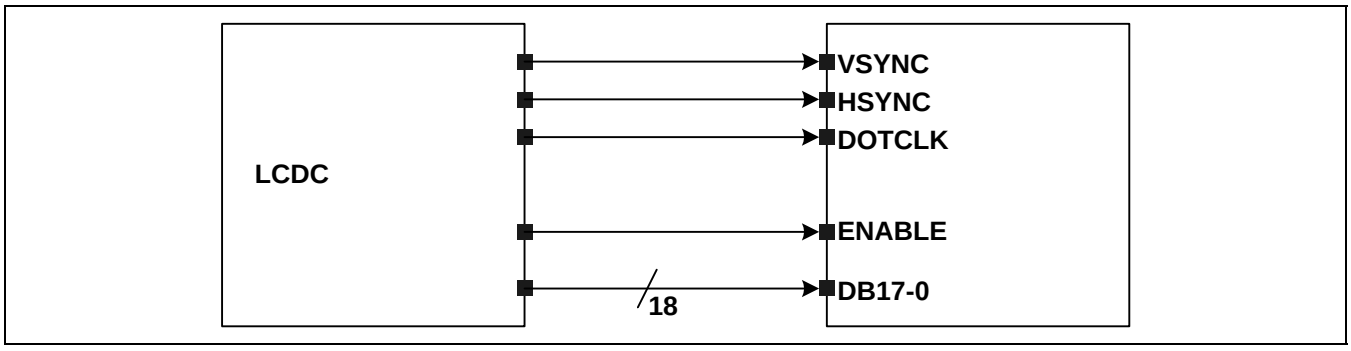


Figure 64. 18-bit RGB Interface to System

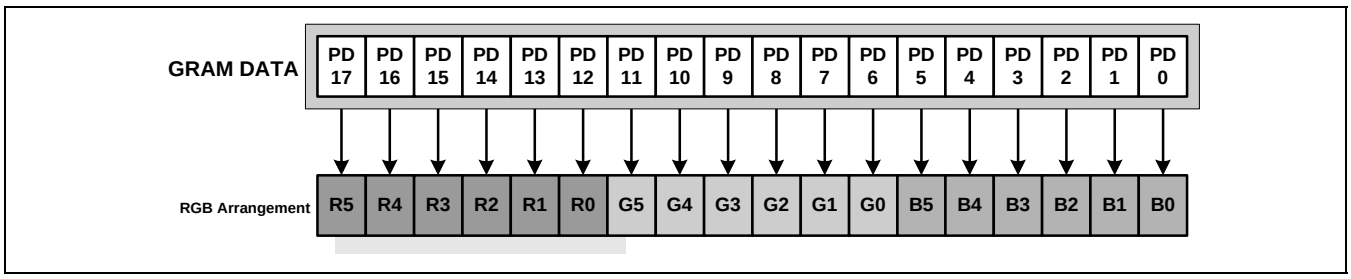


Figure 65. GRAM Write Data format for 18-bit RGB Interface Mode

Preliminary

USAGE ON EXTERNAL DISPLAY INTERFACE

1. When external display interface is in use, the following functions are not available.

Table 36. External Display Interface and Internal Display Operation

Function	External Display Interface	Internal Display Operation
Partial Display	Cannot be used	Can be used
Scroll Function	Cannot be used	Can be used
Interlaced Driving	Cannot be used	Can be used

2. VSYNC, HSYNC, and DOTCLK signals should be supplied during display operation via RGB interface.

3. Please make sure that when setting bits of NO1-0, SDT1-0, and VCIR2-0 in RGB interface, the clock on which operations are based changes from the internal operating clock to DOTCLK.

4. RGB data are transferred for three clock cycles in 6-bit RGB interface. Data transferred, therefore, should be transferred in units of RGB.

5. Interface signals, VSYNC, HSYNC, DOTCLK, ENABLE and PD17-0 should be set in units of RGB (pixels) to match RGB transfer.

6. Transitions between internal operation mode and external display interface should follow the mode transition sequence shown below.

7. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.

8. An address set is done on the falling edge of VSYNC every frame in RGB interface.

Preliminary

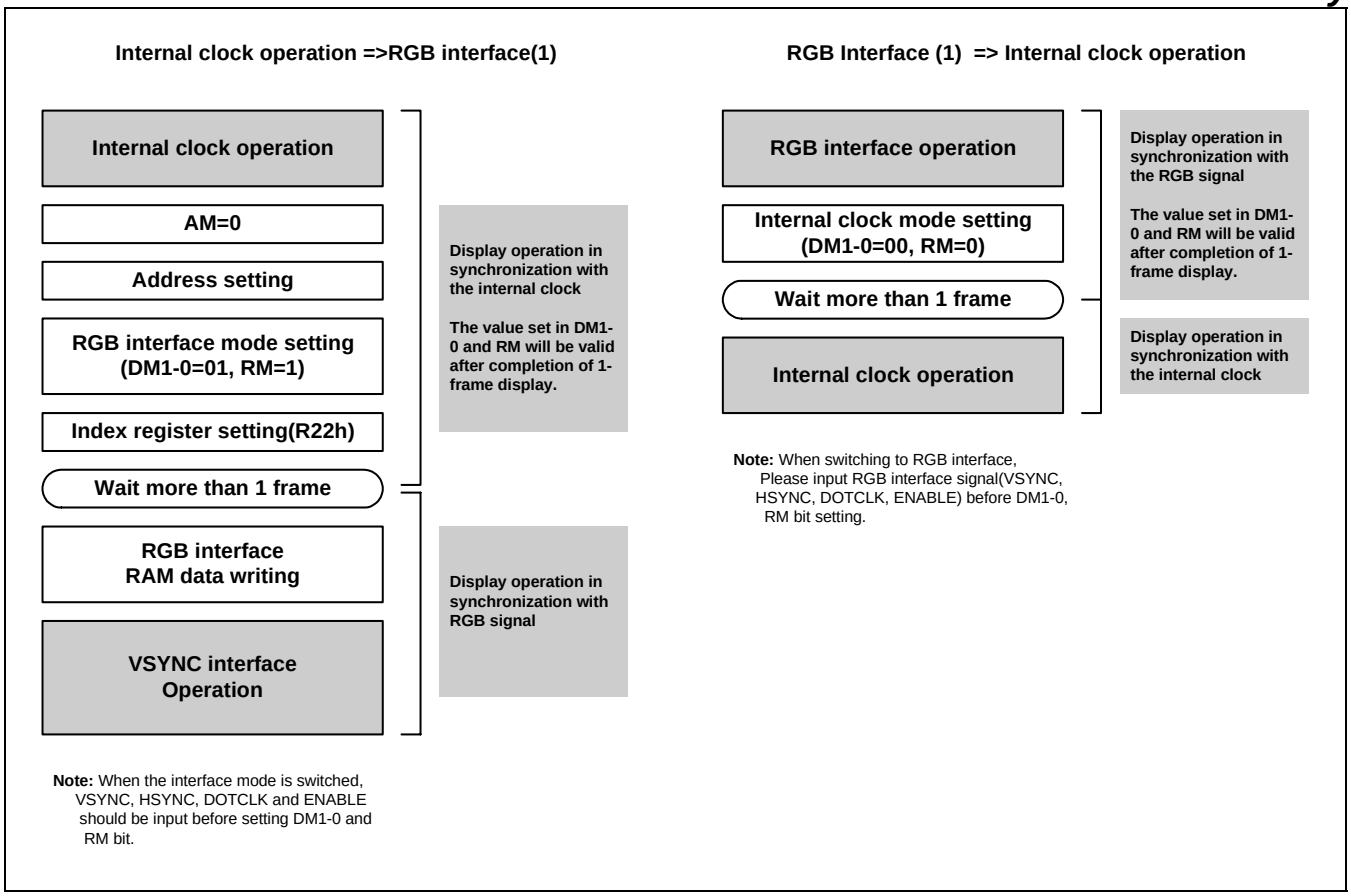


Figure 66. Transition between the Internal Operating Clock Mode and RGB Interface Mode

Preliminary

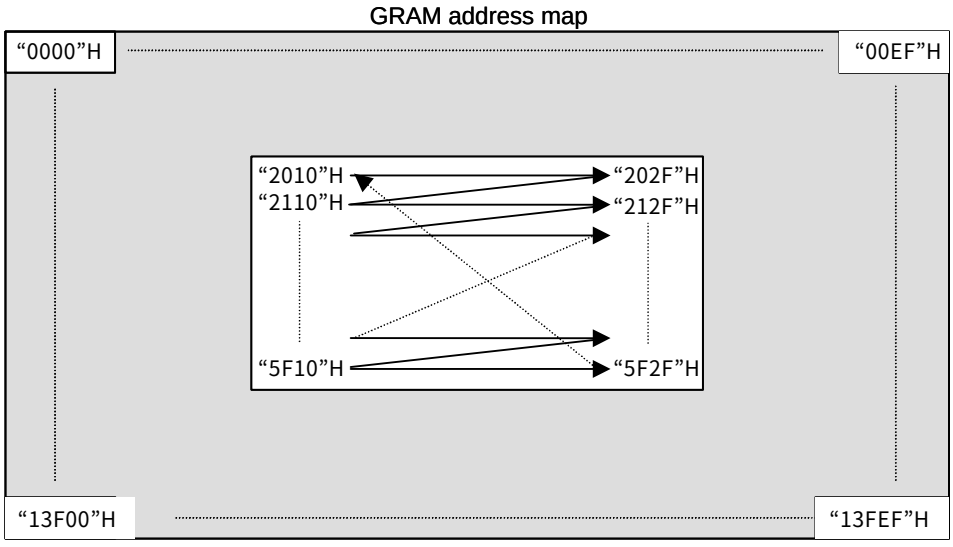
WINDOW ADDRESS FUNCTION

When data is written to the on-chip GRAM, a window address-range that is specified by the horizontal address register (start: HSA7-0, end: HEA 7-0) and vertical address register (start: VSA8-0, end: VEA8-0) can be updated consecutively.
Data is written to addresses in the direction specified by the AM and I/D1-0bit. When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.
The window must be specified to be within the GRAM address area described as following example. Addresses must be set within the window address.

[Restriction on window address range settings]

(horizontal direction) 00H ≤ HSA7-0 ≤ HEA7-0 ≤ EFH
(vertical direction) 00H ≤ VSA8-0 ≤ VEA8-0 ≤ 13F H

[Restriction on address settings during the window address]
(RAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0
VSA8-0 ≤ AD16-8 ≤ VEA8-0



Window address range specification area
HSA7-0 ="10"H HSE7-0 ="2F"H
VSA8-0 ="20"H VEA8-0 ="5F"H

I/D = 1 (increment)
AM = 0 (horizontal writing)

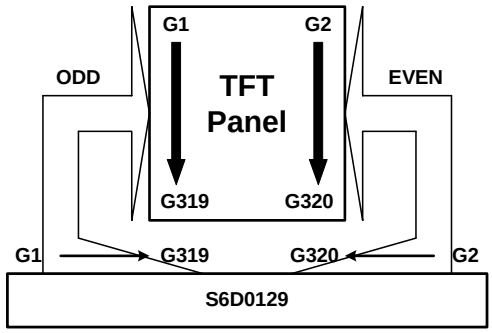
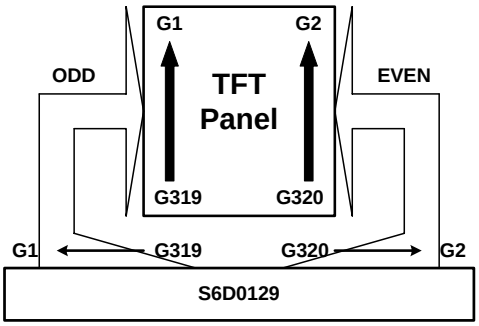
Figure 67. Example of address operation in the window address specification

Preliminary

GATE DRIVER SCAN MODE SETTING

GS bit set the gate scan mode of S6D0129. GS bit determines the scan direction whether the gate driver scans forward or reverse direction.

Figure 68. Scan mode setting

GS	Scan Mode	
0		G1➔G2➔G3➔ G4➔····➔G317➔ G318➔G319➔G320
1		G320➔G319➔G318 G317➔····➔G4➔ G3➔G2➔G1

Preliminary

GAMMA ADJUSTMENT FUNCTION

The S6D0129 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels. Furthermore, since the gradient adjustment register and the micro-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

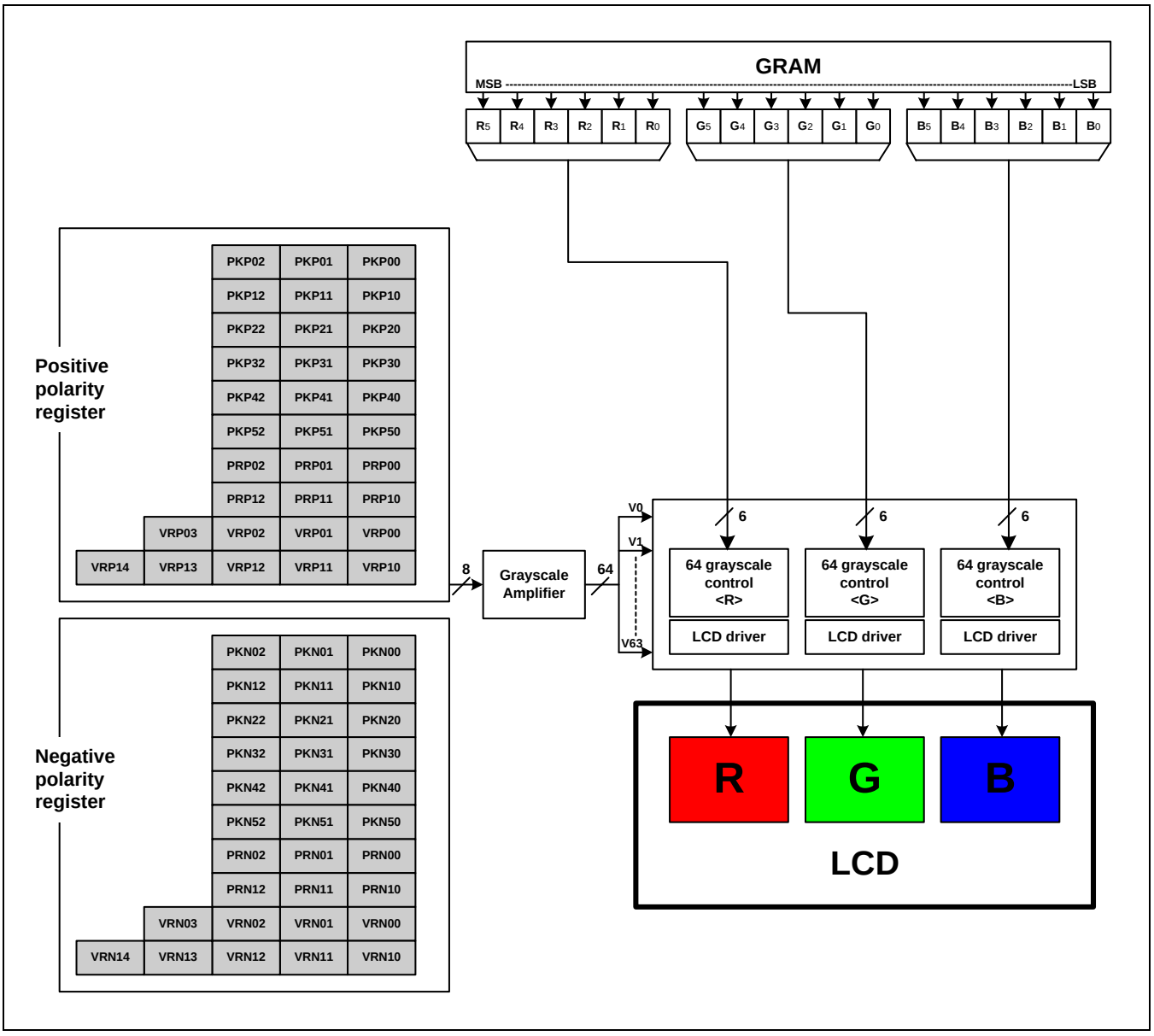


Figure 69. Grayscale control

Preliminary

STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of the grayscale amplifier is shown as below. Determine 8-level (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. The internal ladder resistance splits each level and level between V0 to V63 is generated.

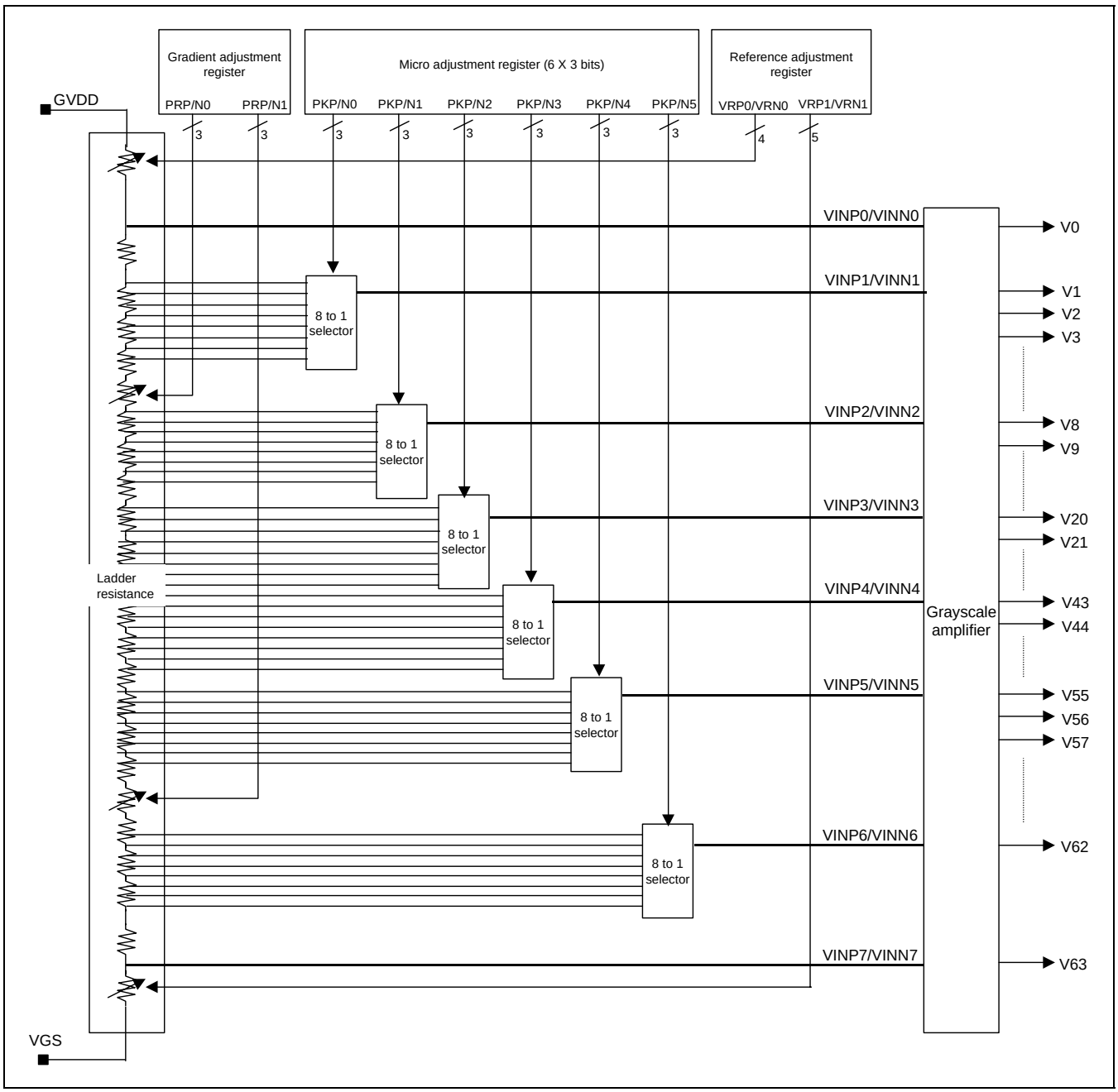


Figure 70. Structure of grayscale amplifier

Preliminary

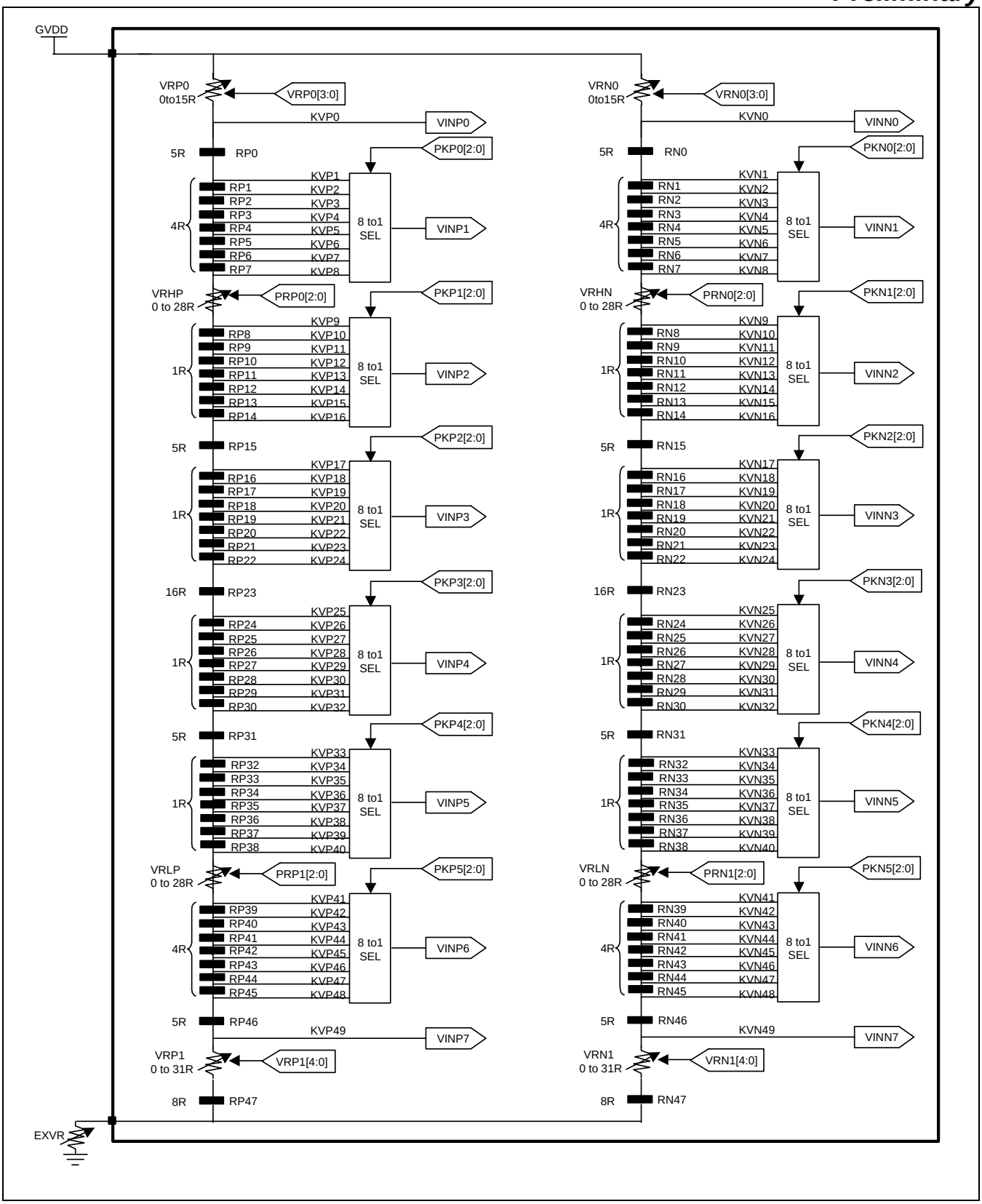


Figure 71. Structure of Ladder / 8 to 1 selector

SAMSUNG ELECTRONICS

Preliminary

GAMMA ADJUSTMENT REGISTER

This block has the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. These registers can independently set up to positive/negative polarities and there are 4 types of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. (average <R><G><B> are common.) The following figure indicates the operation of each adjusting register.

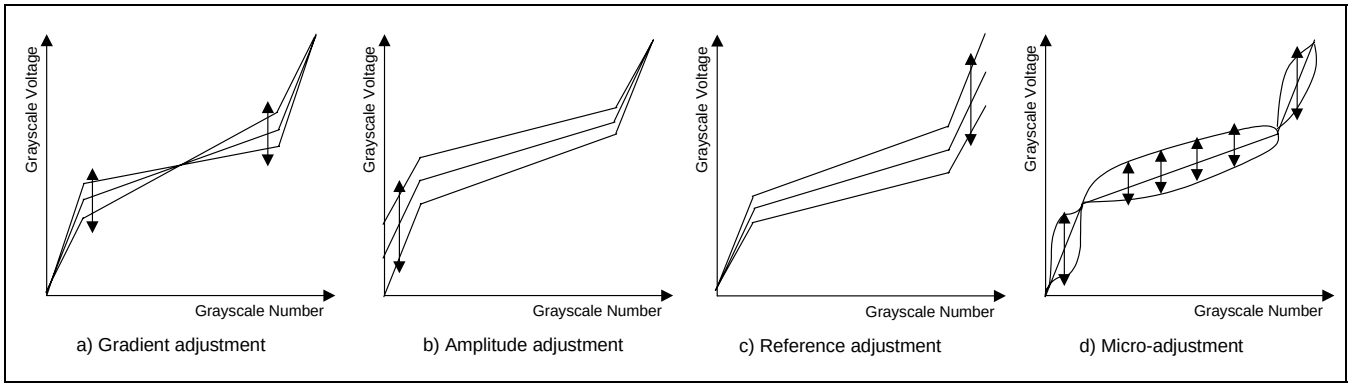


Figure 72. The operation of adjusting register

a) Gradient adjustment resistor

The gradient adjustment resistors are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP (N) / VRLP (N)) of the ladder resistor for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

b) Amplitude adjustment resistor

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP (N)) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor. (Adjust upper side by input GVDD level.) Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

c) Reference adjustment resistor

The Reference-adjusting resistor is to adjust reference of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)0) of the ladder resistor for the grayscale voltage generator located at upper side of the ladder resistor.

d) Micro adjustment resistor

The micro adjustment resistor is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Preliminary

Table 37. Gamma correction registers

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Amplitude adjustment	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Reference adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
Micro-adjustment	PKP0[2:0]	PKN0[2:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[2:0]	PKN1[2:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP2[2:0]	PKN2[2:0]	The voltage of grayscale number 20 is selected by the 8 to 1 selector
	PKP3[2:0]	PKN3[2:0]	The voltage of grayscale number 43 is selected by the 8 to 1 selector
	PKP4[2:0]	PKN4[2:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP5[2:0]	PKN5[2:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector

Preliminary

LADDER RESISTOR/8 TO 1 SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. The variable and 8 to 1 resistors are controlled by the gamma resistor. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel to another.

VARIABLE RESISTOR

There are 2 types of the variable resistors that is for the gradient adjustment (VRHP (N) / VRLP (N)) and for the amplitude adjustment (VRP (N)). The resistance value is set by the gradient adjusting resistor and the amplitude adjustment resistor as below.

Table 38. Gradient Adjustment (1)

Register value PRP(N)0 [2:0]	Resistance value VRHP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 39. Gradient Adjustment (2)

Register value PRP(N)1 [2:0]	Resistance value VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 40. Amplitude Adjustment (1)

Register value VRP(N)0 [3:0]	Resistance value VRP(N)0
0000	0R
0001	2R
0010	4R
. . .	. . .
1101	26R
1110	28R
1111	30R

Table 41. Amplitude Adjustment (2)

Register value VRP(N)1[4:0]	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
. . .	. . .
11101	29R
11110	30R
11111	31R

Preliminary

THE 8 TO 1 SELECTOR

In the 8 to 1 selector, the voltage level must be selected given by the ladder resistance and the micro-adjusting register. And output the voltage the six types of the reference voltage, the VIN1- to VIN6.
Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Table 42. Relationship between Micro-adjustment Register and Selected Voltage

Register value PKP(N) [2:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

Preliminary

Table 43. Gamma Adjusting Voltage Formula (Positive polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	GVDD	-	VINP0
KVP1	GVDD-ΔV*5R/SUMRP	PKP02-00 = “000”	VINP1
KVP2	GVDD-ΔV*9R/SUMRP	PKP02-00 = “001”	
KVP3	GVDD-ΔV*13R/SUMRP	PKP02-00 = “010”	
KVP4	GVDD-ΔV*17R/SUMRP	PKP02-00 = “011”	
KVP5	GVDD-ΔV*21R/SUMRP	PKP02-00 = “100”	
KVP6	GVDD-ΔV*25R/SUMRP	PKP02-00 = “101”	
KVP7	GVDD-ΔV*29R/SUMRP	PKP02-00 = “110”	
KVP8	GVDD-ΔV*33R/SUMRP	PKP02-00 = “111”	
KVP9	GVDD-ΔV*(33R+VRHP)/SUMRP	PKP12-10 = “000”	VINP2
KVP10	GVDD-ΔV*(34R+VRHP)/SUMRP	PKP12-10 = “001”	
KVP11	GVDD-ΔV*(35R+VRHP)/SUMRP	PKP12-10 = “010”	
KVP12	GVDD-ΔV*(36R+VRHP)/SUMRP	PKP12-10 = “011”	
KVP13	GVDD-ΔV*(37R+VRHP)/SUMRP	PKP12-10 = “100”	
KVP14	GVDD-ΔV*(38R+VRHP)/SUMRP	PKP12-10 = “101”	
KVP15	GVDD-ΔV*(39R+VRHP)/SUMRP	PKP12-10 = “110”	
KVP16	GVDD-ΔV*(40R+VRHP)/SUMRP	PKP12-10 = “111”	
KVP17	GVDD-ΔV*(45R+VRHP)/SUMRP	PKP22-20 = “000”	VINP3
KVP18	GVDD-ΔV*(46R+VRHP)/SUMRP	PKP22-20 = “001”	
KVP19	GVDD-ΔV*(47R+VRHP)/SUMRP	PKP22-20 = “010”	
KVP20	GVDD-ΔV*(48R+VRHP)/SUMRP	PKP22-20 = “011”	
KVP21	GVDD-ΔV*(49R+VRHP)/SUMRP	PKP22-20 = “100”	
KVP22	GVDD-ΔV*(50R+VRHP)/SUMRP	PKP22-20 = “101”	
KVP23	GVDD-ΔV*(51R+VRHP)/SUMRP	PKP22-20 = “110”	
KVP24	GVDD-ΔV*(52R+VRHP)/SUMRP	PKP22-20 = “111”	
KVP25	GVDD-ΔV*(68R+VRHP)/SUMRP	PKP32-30 = “000”	VINP4
KVP26	GVDD-ΔV*(69R+VRHP)/SUMRP	PKP32-30 = “001”	
KVP27	GVDD-ΔV*(70R+VRHP)/SUMRP	PKP32-30 = “010”	
KVP28	GVDD-ΔV*(71R+VRHP)/SUMRP	PKP32-30 = “011”	
KVP29	GVDD-ΔV*(72R+VRHP)/SUMRP	PKP32-30 = “100”	
KVP30	GVDD-ΔV*(73R+VRHP)/SUMRP	PKP32-30 = “101”	
KVP31	GVDD-ΔV*(74R+VRHP)/SUMRP	PKP32-30 = “110”	
KVP32	GVDD-ΔV*(75R+VRHP)/SUMRP	PKP32-30 = “111”	
KVP33	GVDD-ΔV*(80R+VRHP)/SUMRP	PKP42-40 = “000”	VINP5
KVP34	GVDD-ΔV*(81R+VRHP)/SUMRP	PKP42-40 = “001”	
KVP35	GVDD-ΔV*(82R+VRHP)/SUMRP	PKP42-40 = “010”	
KVP36	GVDD-ΔV*(83R+VRHP)/SUMRP	PKP42-40 = “011”	
KVP37	GVDD-ΔV*(84R+VRHP)/SUMRP	PKP42-40 = “100”	
KVP38	GVDD-ΔV*(85R+VRHP)/SUMRP	PKP42-40 = “101”	
KVP39	GVDD-ΔV*(86R+VRHP)/SUMRP	PKP42-40 = “110”	
KVP40	GVDD-ΔV*(87R+VRHP)/SUMRP	PKP42-40 = “111”	
KVP41	GVDD-ΔV*(87R+VRHP+VRLP)/SUMRP	PKP52-50 = “000”	VINP6
KVP42	GVDD-ΔV*(91R+VRHP+VRLP)/SUMRP	PKP52-50 = “001”	
KVP43	GVDD-ΔV*(95R+VRHP+VRLP)/SUMRP	PKP52-50 = “010”	
KVP44	GVDD-ΔV*(99R+VRHP+VRLP)/SUMRP	PKP52-50 = “011”	
KVP45	GVDD-ΔV*(103R+VRHP+VRLP)/SUMRP	PKP52-50 = “100”	
KVP46	GVDD-ΔV*(107R+VRHP+VRLP)/SUMRP	PKP52-50 = “101”	
KVP47	GVDD-ΔV*(111R+VRHP+VRLP)/SUMRP	PKP52-50 = “110”	
KVP48	GVDD-ΔV*(115R+VRHP+VRLP)/SUMRP	PKP52-50 = “111”	
KVP49	GVDD-ΔV*(120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP
SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN
ΔV: Potential difference between KV0 and KV49 = GVDD*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Table 44. Gamma Voltage Formula (Positive Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V43+(V20-V43)*(11/23)
V1	VINP1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINP2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINP4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINP3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINP5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINP6
V31	V43+(V20-V43)*(12/23)	V63	VINP7

Preliminary

Table 45. Gamma Adjusting Voltage Formula (Negative polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	GVDD	-	VINN0
KVN1	GVDD-ΔV*5R/SUMRN	PKN02-00 = “000”	VINN1
KVN2	GVDD-ΔV*9R/SUMRN	PKN02-00 = “001”	
KVN3	GVDD-ΔV*13R/SUMRN	PKN02-00 = “010”	
KVN4	GVDD-ΔV*17R/SUMRN	PKN02-00 = “011”	
KVN5	GVDD-ΔV*21R/SUMRN	PKN02-00 = “100”	
KVN6	GVDD-ΔV*25R/SUMRN	PKN02-00 = “101”	
KVN7	GVDD-ΔV*29R/SUMRN	PKN02-00 = “110”	
KVN8	GVDD-ΔV*33R/SUMRN	PKN02-00 = “111”	
KVN9	GVDD-ΔV*(33R+VRHN)/SUMRN	PKN12-10 = “000”	VINN2
KVN10	GVDD-ΔV*(34R+VRHN)/SUMRN	PKN12-10 = “001”	
KVN11	GVDD-ΔV*(35R+VRHN)/SUMRN	PKN12-10 = “010”	
KVN12	GVDD-ΔV*(36R+VRHN)/SUMRN	PKN12-10 = “011”	
KVN13	GVDD-ΔV*(37R+VRHN)/SUMRN	PKN12-10 = “100”	
KVN14	GVDD-ΔV*(38R+VRHN)/SUMRN	PKN12-10 = “101”	
KVN15	GVDD-ΔV*(39R+VRHN)/SUMRN	PKN12-10 = “110”	
KVN16	GVDD-ΔV*(40R+VRHN)/SUMRN	PKN12-10 = “111”	
KVN17	GVDD-ΔV*(45R+VRHN)/SUMRN	PKN22-20 = “000”	VINN3
KVN18	GVDD-ΔV*(46R+VRHN)/SUMRN	PKN22-20 = “001”	
KVN19	GVDD-ΔV*(47R+VRHN)/SUMRN	PKN22-20 = “010”	
KVN20	GVDD-ΔV*(48R+VRHN)/SUMRN	PKN22-20 = “011”	
KVN21	GVDD-ΔV*(49R+VRHN)/SUMRN	PKN22-20 = “100”	
KVN22	GVDD-ΔV*(50R+VRHN)/SUMRN	PKN22-20 = “101”	
KVN23	GVDD-ΔV*(51R+VRHN)/SUMRN	PKN22-20 = “110”	
KVN24	GVDD-ΔV*(52R+VRHN)/SUMRN	PKN22-20 = “111”	
KVN25	GVDD-ΔV*(68R+VRHN)/SUMRN	PKN32-30 = “000”	VINN4
KVN26	GVDD-ΔV*(69R+VRHN)/SUMRN	PKN32-30 = “001”	
KVN27	GVDD-ΔV*(70R+VRHN)/SUMRN	PKN32-30 = “010”	
KVN28	GVDD-ΔV*(71R+VRHN)/SUMRN	PKN32-30 = “011”	
KVN29	GVDD-ΔV*(72R+VRHN)/SUMRN	PKN32-30 = “100”	
KVN30	GVDD-ΔV*(73R+VRHN)/SUMRN	PKN32-30 = “101”	
KVN31	GVDD-ΔV*(74R+VRHN)/SUMRN	PKN32-30 = “110”	
KVN32	GVDD-ΔV*(75R+VRHN)/SUMRN	PKN32-30 = “111”	
KVN33	GVDD-ΔV*(80R+VRHN)/SUMRN	PKN42-40 = “000”	VINN5
KVN34	GVDD-ΔV*(81R+VRHN)/SUMRN	PKN42-40 = “001”	
KVN35	GVDD-ΔV*(82R+VRHN)/SUMRN	PKN42-40 = “010”	
KVN36	GVDD-ΔV*(83R+VRHN)/SUMRN	PKN42-40 = “011”	
KVN37	GVDD-ΔV*(84R+VRHN)/SUMRN	PKN42-40 = “100”	
KVN38	GVDD-ΔV*(85R+VRHN)/SUMRN	PKN42-40 = “101”	
KVN39	GVDD-ΔV*(86R+VRHN)/SUMRN	PKN42-40 = “110”	
KVN40	GVDD-ΔV*(87R+VRHN)/SUMRN	PKN42-40 = “111”	
KVN41	GVDD-ΔV*(87R+VRHN+VRLN)/SUMRN	PKN52-50 = “000”	VINN6
KVN42	GVDD-ΔV*(91R+VRHN+VRLN)/SUMRN	PKN52-50 = “001”	
KVN43	GVDD-ΔV*(95R+VRHN+VRLN)/SUMRN	PKN52-50 = “010”	
KVN44	GVDD-ΔV*(99R+VRHN+VRLN)/SUMRN	PKN52-50 = “011”	
KVN45	GVDD-ΔV*(103R+VRHN+VRLN)/SUMRN	PKN52-50 = “100”	
KVN46	GVDD-ΔV*(107R+VRHN+VRLN)/SUMRN	PKN52-50 = “101”	
KVN47	GVDD-ΔV*(111R+VRHN+VRLN)/SUMRN	PKN52-50 = “110”	
KVN48	GVDD-ΔV*(115R+VRHN+VRLN)/SUMRN	PKN52-50 = “111”	
KVN49	GVDD-ΔV*(120R+VRHN+VRLN)/SUMRN	-	VINN7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP
SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN
ΔV: Potential difference between KV0 and KV49 = GVDD*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Table 46. Gamma Voltage Formula (Negative Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V43+(V20-V43)*(11/23)
V1	VINN1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINN2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINN4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINN3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINN5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINN6
V31	V43+(V20-V43)*(12/23)	V63	VINN7

Preliminary

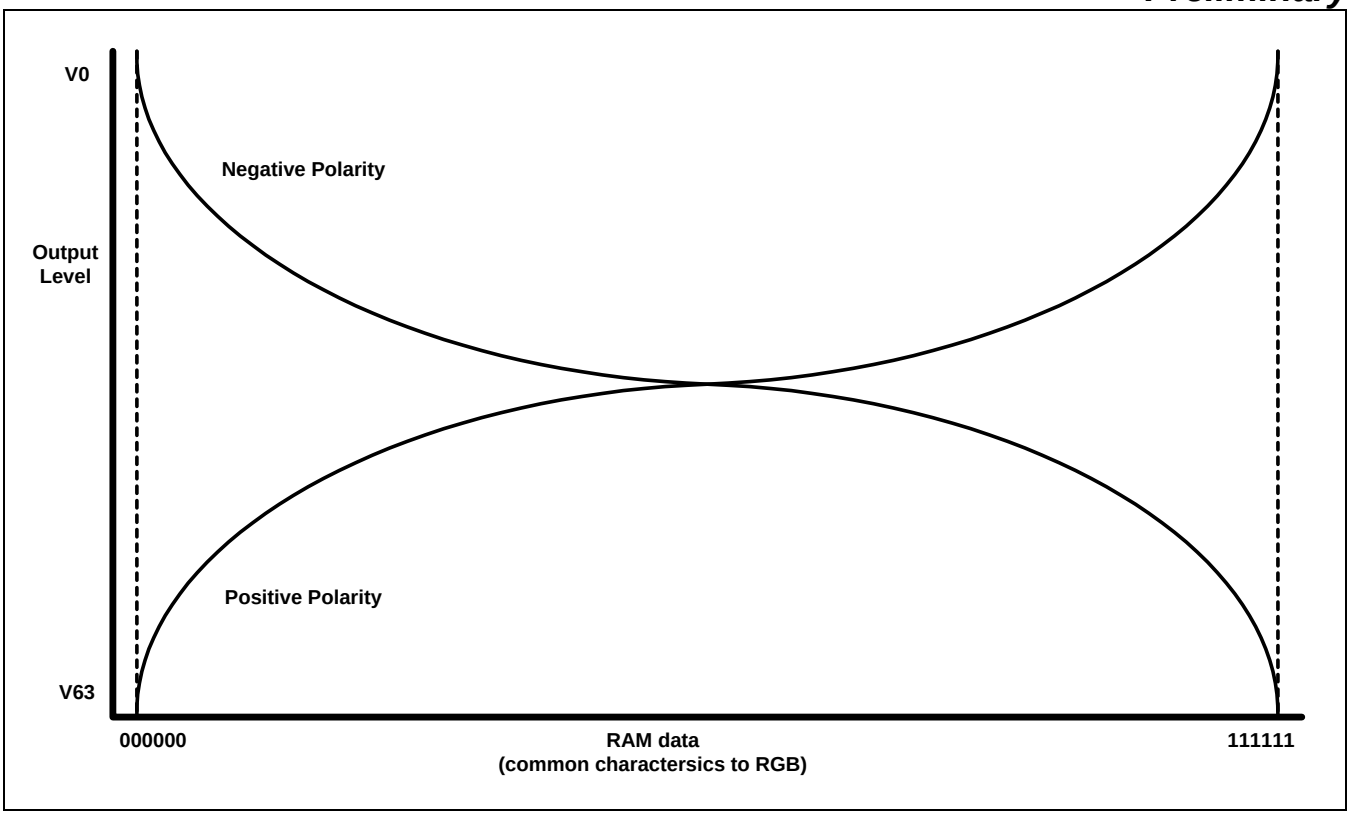


Figure 73. Relationship between RAM data and output voltage

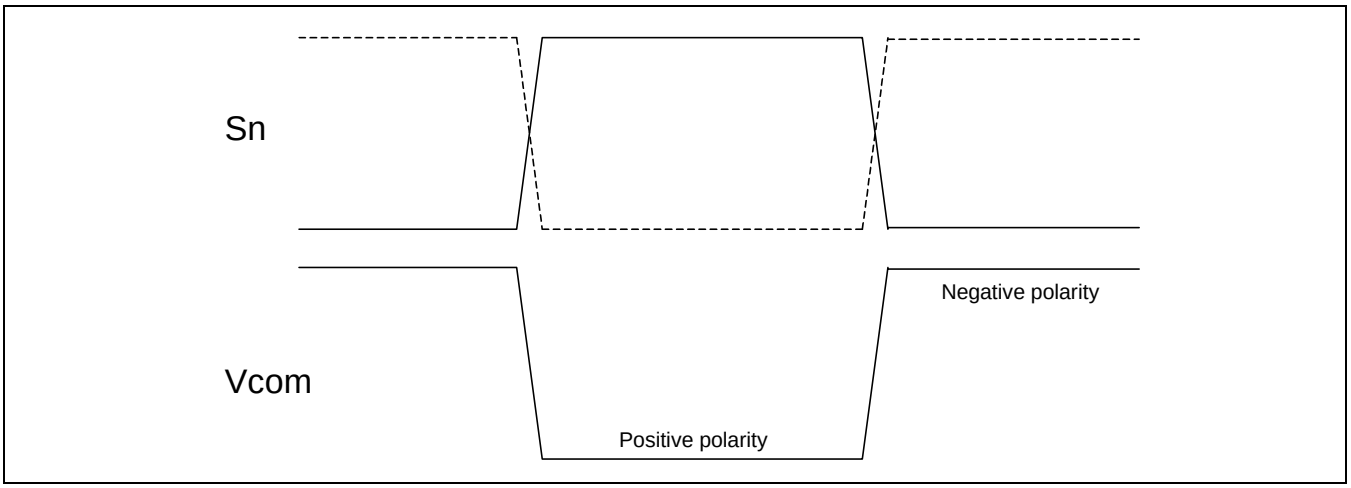


Figure 74. Relationship between source output and Vcom

Preliminary

THE 8-COLOR DISPLAY MODE

The S6D0129 incorporates 8-color display mode. The grayscale levels to be used are V0 and V63 and all the other levels (V1~V62) are halt. So that it attempts to lower power consumption.
During the 8-color mode, the Gamma micro adjustment register, PKP00-PKP52 and PKN00-PKN52 are invalid. The level power supply (V1-V62) is in OFF condition during the 8-color mode in order to select V0/V63.

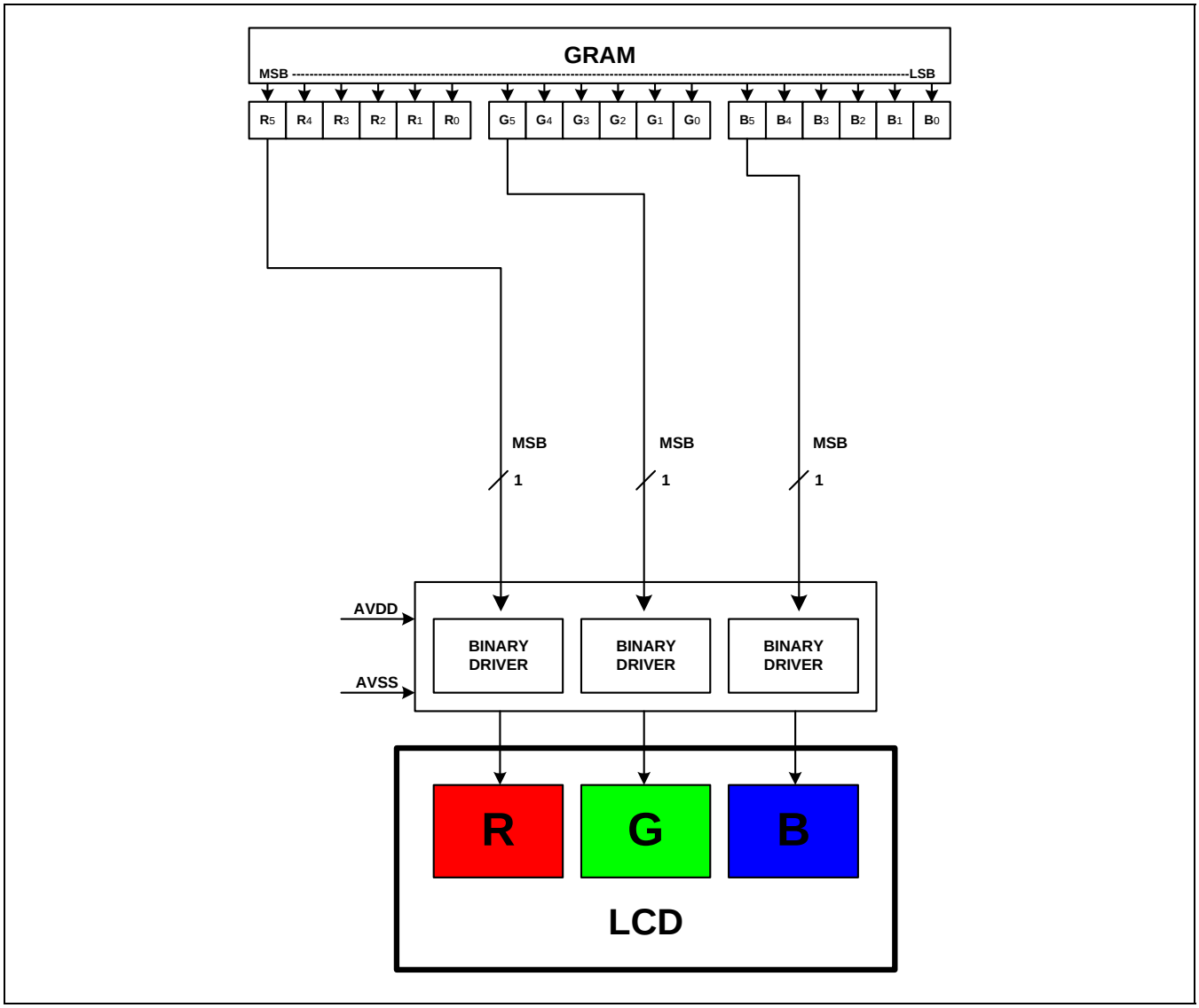


Figure 75. 8-color display control

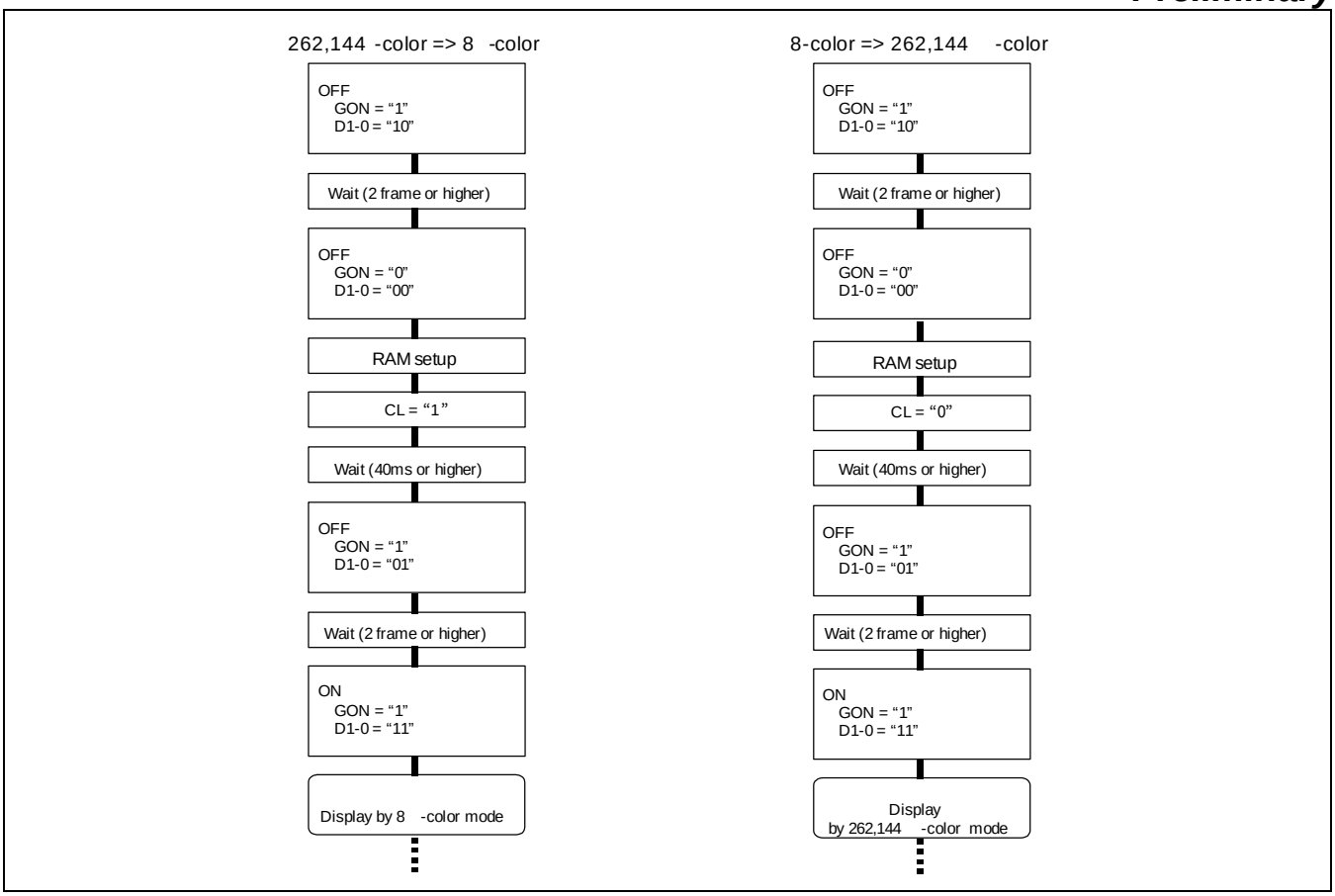


Figure 76. Set up procedure for the 8-color mode

Preliminary

SYSTEM STRUCTURE EXAMPLE

The following figure indicates the system structure, which composes the 240 (width) x 320 (length) dots TFT-LCD panel.

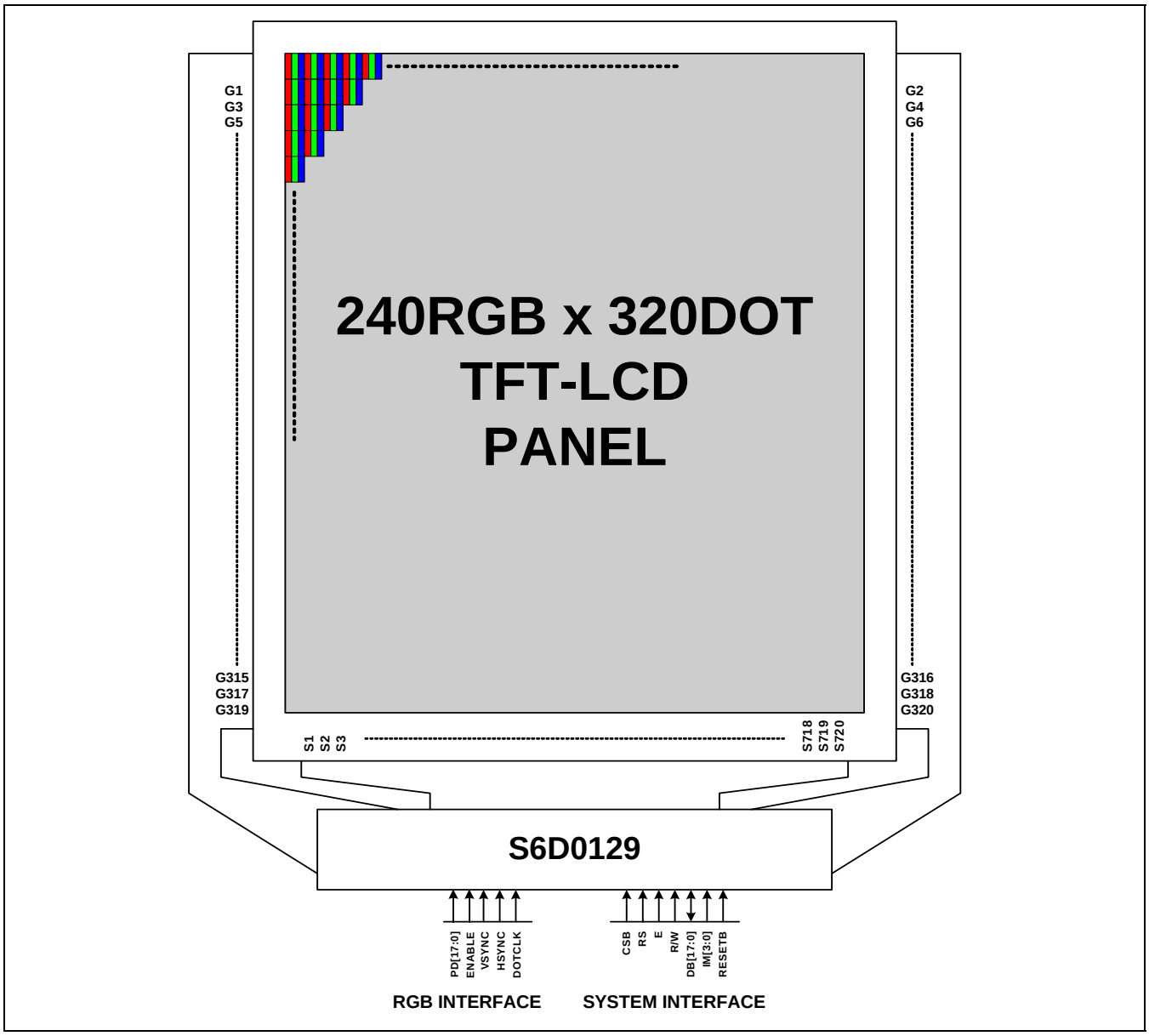


Figure 77. System structure

Preliminary

INSTRUCTION SET UP FLOW

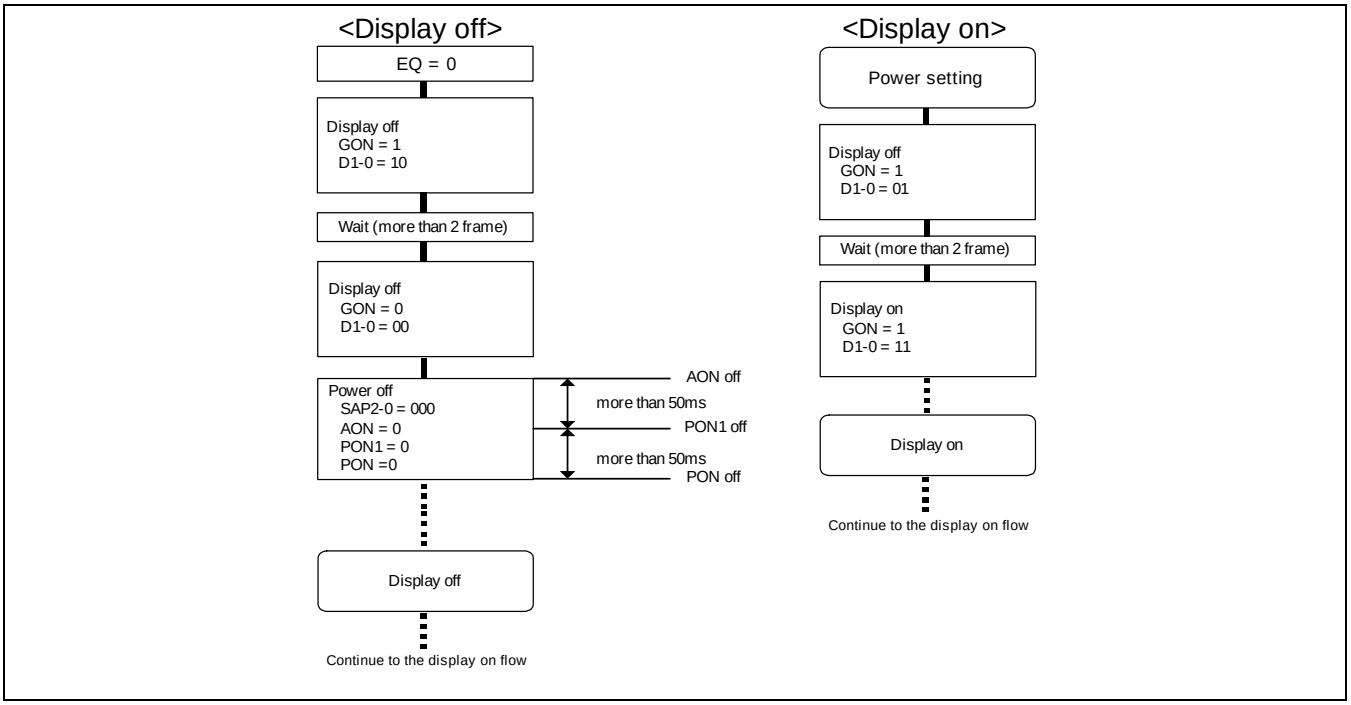


Figure 78. Instruction set up flow

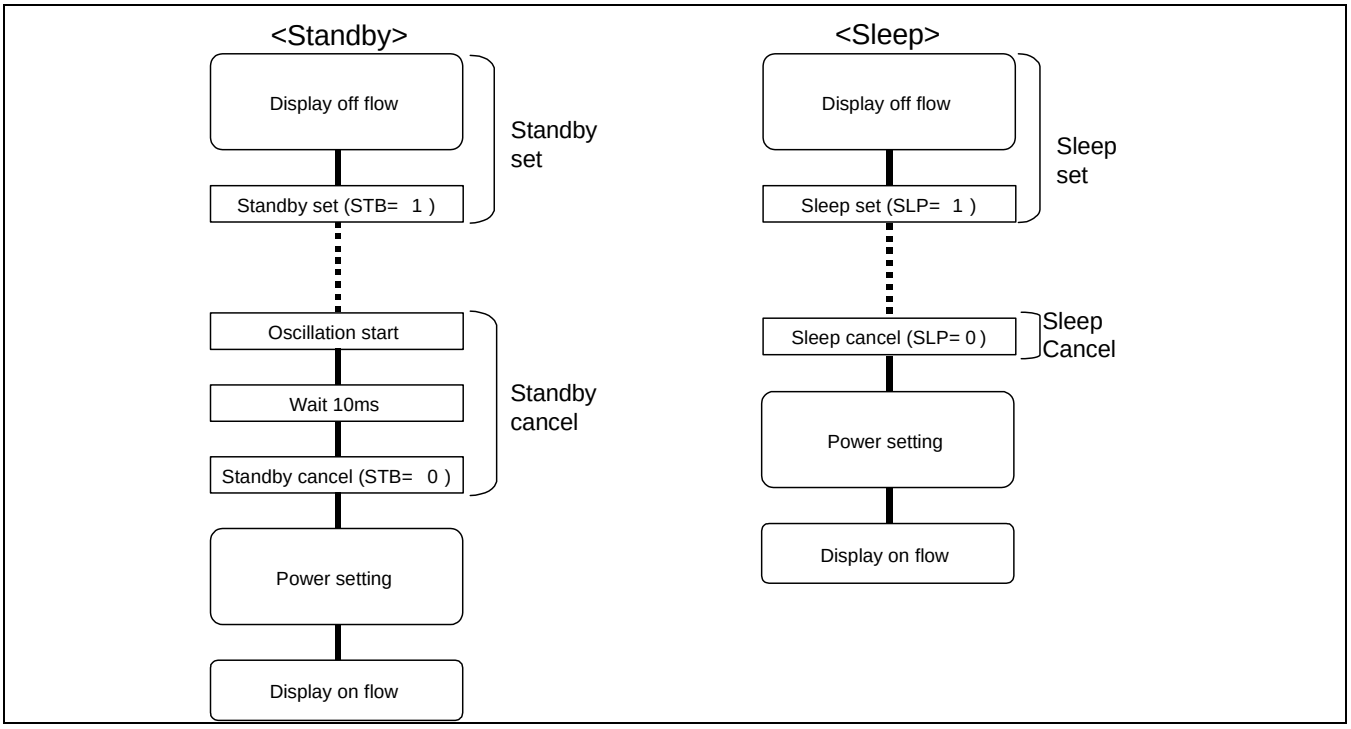


Figure 79. Instruction setup flow (continued)

SAMSUNG ELECTRONICS

Preliminary

OSCILLATION CIRCUIT

The S6D0129 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

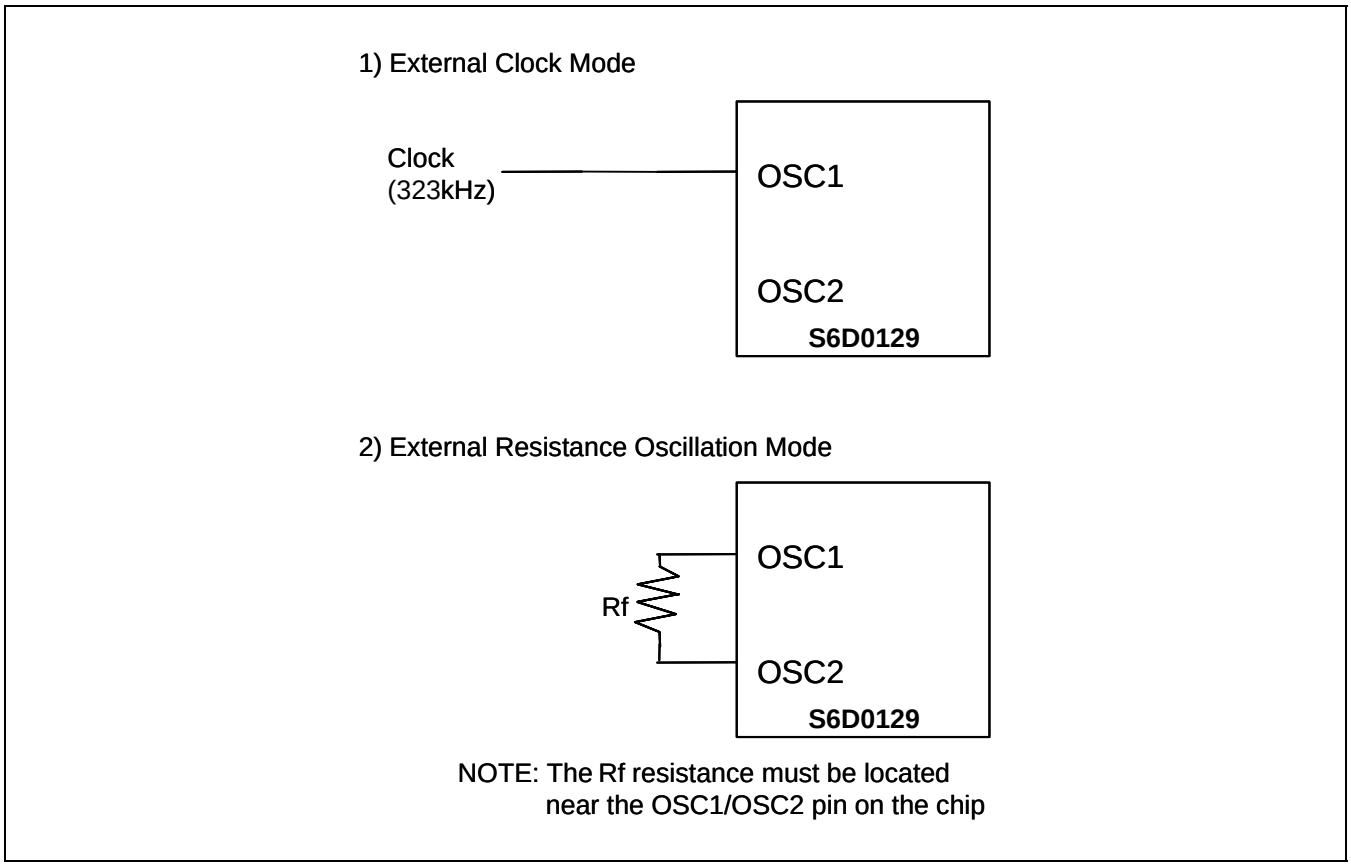


Figure 80. Oscillation Circuit

Preliminary

N-RASTER-ROW REVERSED AC DRIVE

The S6D0129 supports not only the LCD reversed AC drive in a one-frame unit but also the one-raster-row reversed AC drive which alternates in a one-raster-row unit. When a problem affecting display quality occurs, the one-raster-row reversed AC drive can improve the quality.

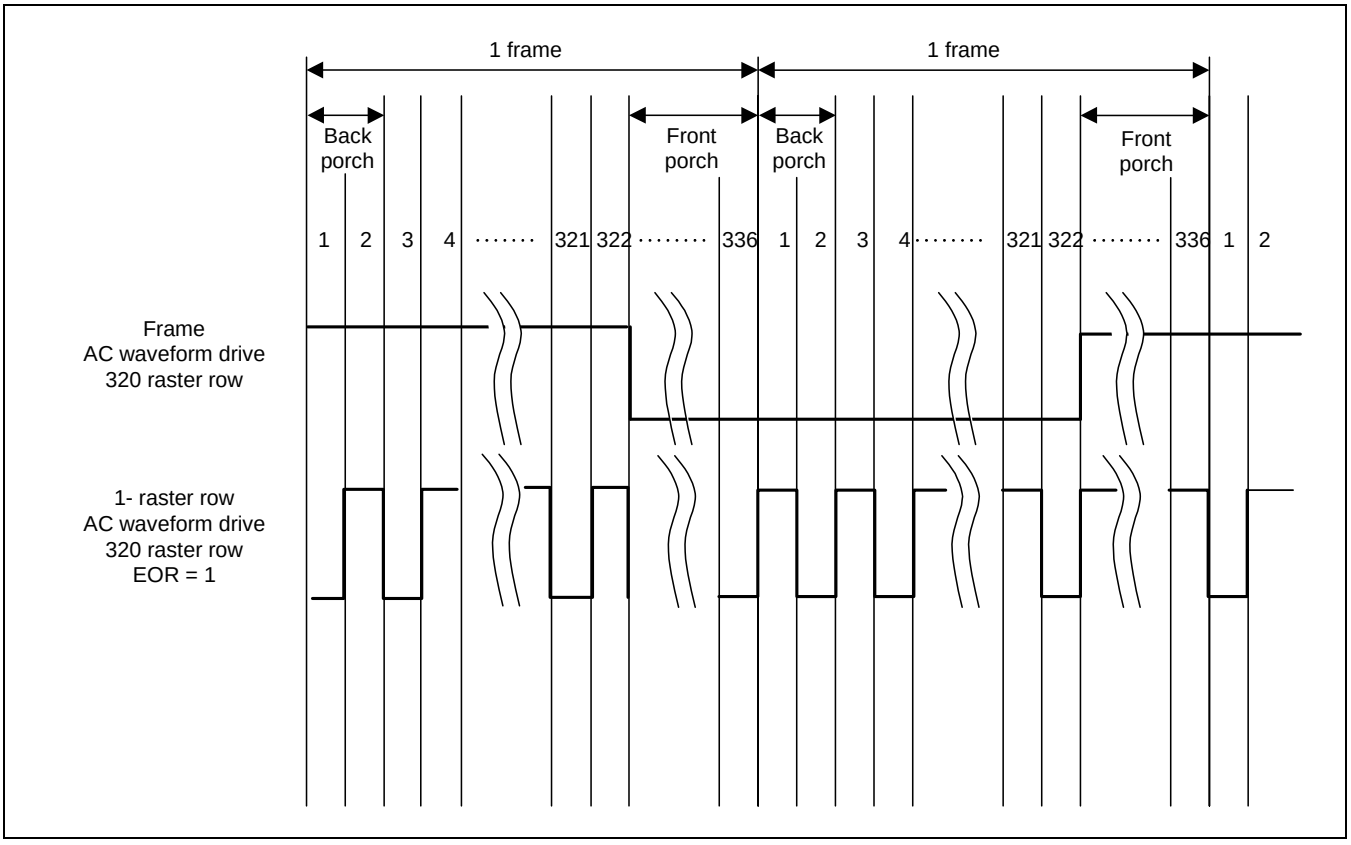


Figure 81. Example of an AC signal under one-raster-row reversed AC drive (BP=2, FP=14)

SAMSUNG ELECTRONICS

Preliminary

INTERLACE DRIVE

S6D0129 supports the interlace drive to protect from the flicker. It splits one frame into n fields and drives. Determine the n fields (FLD bit stetting value) after confirming on the actual LCD display.
Following table indicates n fields: the gate selecting position when it is 1 or 3. and the diagram below indicates the output waveform when the field interlace drive is active.

GS = "0"

FLD1-0 :setting value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G1	O	O		
G2	O		O	
G3	O			O
G4	O	O		
G5	O		O	
G6	O			O
G7	O	O		
G8	O		O	
G9	O			O
G317	O		O	
G318	O			O
G319	O	O		
G320	O		O	

GS = "1"

FLD1-0 :setting value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G320	O	O		
G319	O		O	
G318	O			O
G317	O	O		
G316	O		O	
G315	O			O
G314	O	O		
G313	O		O	
G312	O			O
G4	O		O	
G3	O			O
G2	O	O		
G1	O		O	

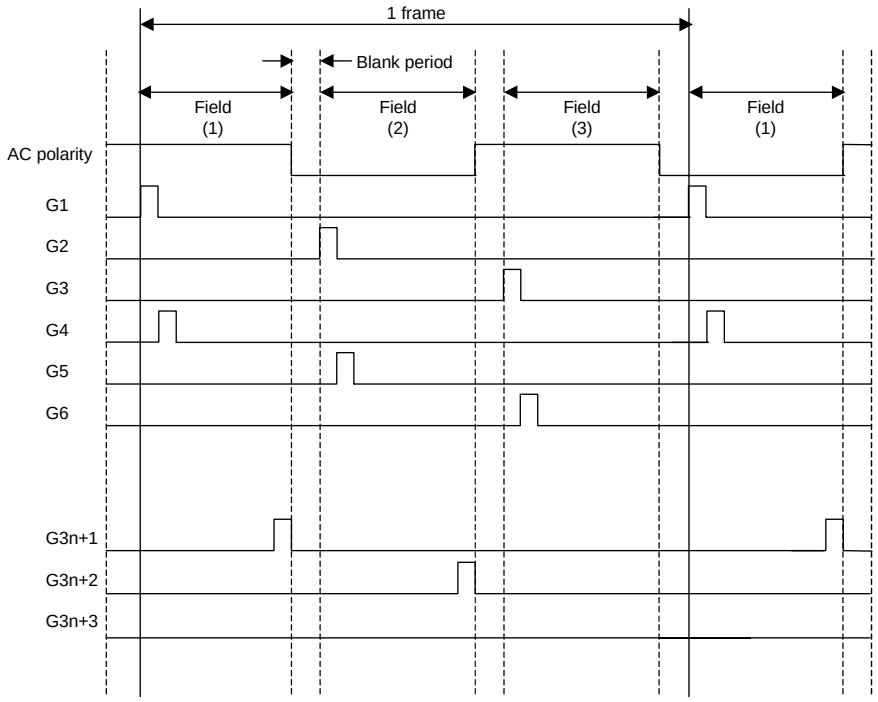


Figure 82. Interlace drive and output waveform

Preliminary

A/C TIMING

Following diagram indicates the A/C timing on the each A/C drive method. After every 1 drawing, the A/C timing is occurred on the reversed frame AC drive. After the A/C timing, the blank (all gate output: VGL level) period described below is inserted. When it is on the interlace drive, blank period is inserted every A/C timing. When the reversed n-raster-row is driving, a blank period is inserted after all screens are drawn. Front and Back porch can be adjusted using FP3-0 and BP3-0 bits (R08h).

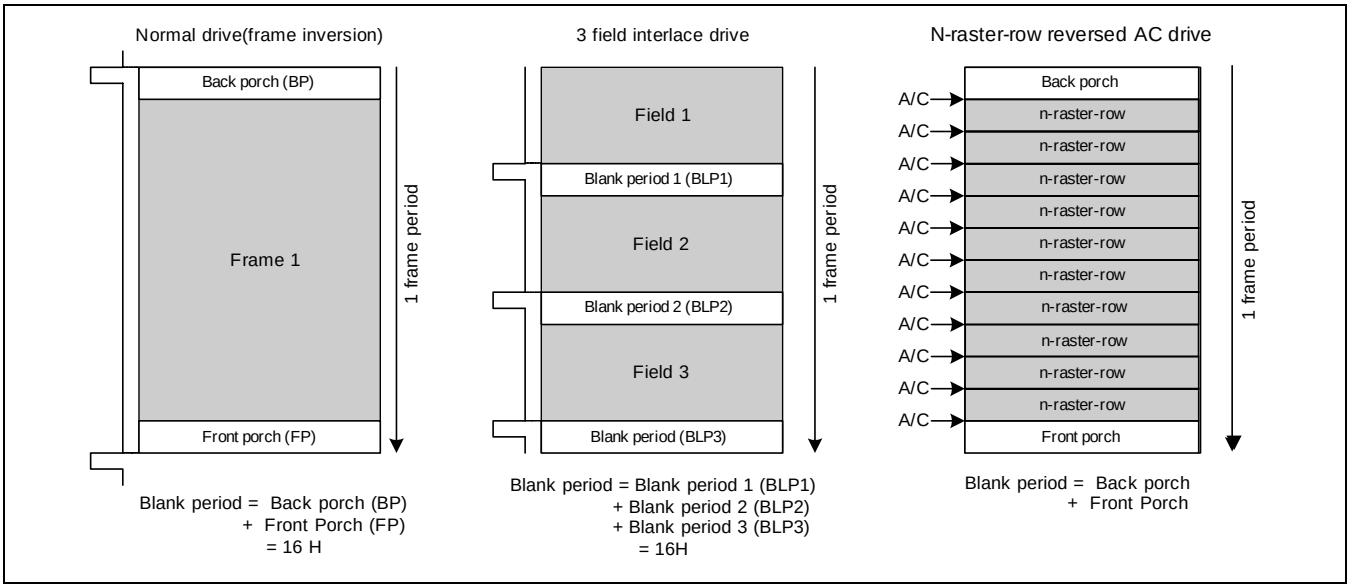


Figure 83. A/C timing

SAMSUNG ELECTRONICS

Preliminary

FRAME FREQUENCY ADJUSTING FUNCTION

The S6D0129 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD driver as the oscillation frequency is always same.
If the oscillation frequency is set to high, animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display, etc. is required, the frame frequency can be set high.

RELATIONSHIP BETWEEN LCD DRIVE DUTY AND FRAME FREQUENCY

The relationships between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1H period adjusting bit (RTN) and in the operation clock division bit (DIV) by the instruction.

$$\text{Frame Frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row x division ratio x (Line+B)}} \text{ [Hz]}$$

f_{osc}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
B: Blank period(Back porch + Front Porch)

Figure 84. Formula for the frame frequency

Example calculation

Driver raster-row: 320
1H period: 16 clock (RTN3 to 0 = 0000)
Operation clock division ratio: 1division
B: Blank period (BP + FP): 16

fosc = 60Hz x (0+16) clock x 1 division x (320+16) lines = 323 [kHz]

In this case, the RC oscillation frequency becomes 323 kHz. The external resistance value of the RC oscillator must be adjusted to be 323 kHz.

Preliminary

SCREEN-DIVISION DRIVING FUNCTION

The S6D0129 can select and drive two screens at any position with the screen-driving position registers (R42h/R43h and R44h/R45h). Any two screens required for display are selectively driven and reducing LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS18 to 10) and end line (SE18 to 10) are specified by the 1st screen-driving position register (R42h/R43h). For the 2nd division screen, start line (SS28 to 20) and end line (SE28 to 20) are specified by the 2nd screen-driving position register (R44h/R45h). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

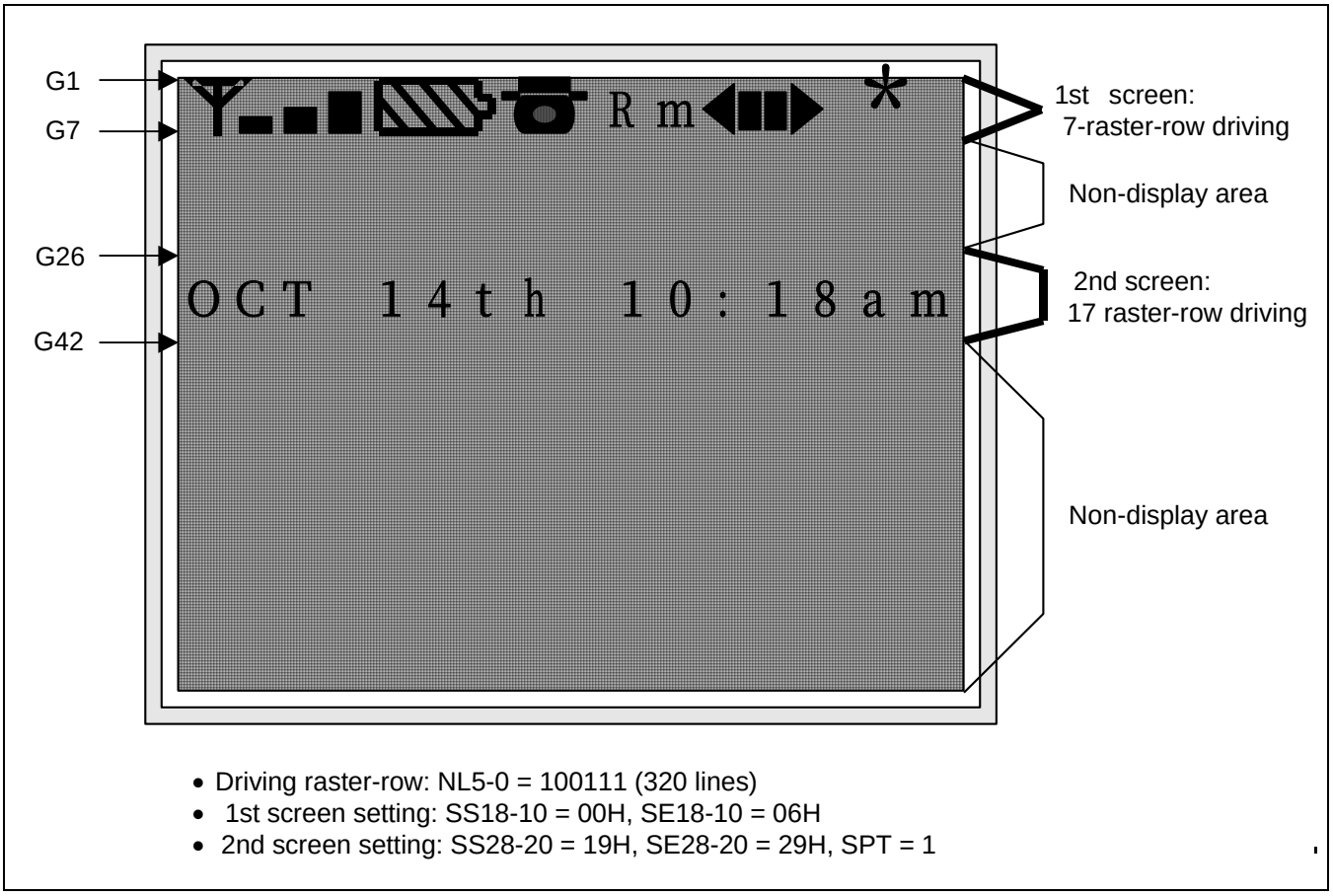


Figure 85. Driving on 2 screen

Preliminary

RESTRICTION ON THE 1ST/2ND SCREEN DRIVING POSITION REGISTER SETTINGS

The following restrictions must be satisfied when setting the start line (SS18 to 10) and end line (SE18 to 10) of the 1st screen driving position register (R42h/R43h) and the start line (SS28 to 20) and end line (SE28 to 20) of the 2nd screen driving position register (R44h/R45h) for the S6D0129. Note that incorrect display may occur if the restrictions are not satisfied.

Table 47. Restrictions on the 1st/2nd Screen Driving Position Register Setting

1st Screen Driving (SPT=0)

Register setting	Display operation
(SE18 to 10) – (SS18 to 10) = NL	Full screen display Normally displays (SE18 to 10) to (SS18 to 10)
(SE18 to 10) – (SS18 to 10) < NL	Partial display Normally displays (SE18 to 10) to (SS18 to 10) White display for all other times (RAM data is not related at all)
(SE18 to 10) – (SS18 to 10) > NL	Setting disabled

NOTE 1: SS18 to 10 ≤ SE18 to 10 ≤ 13Fh
NOTE 2: Setting SE28 to 20 and SS28 to 20 are invalid

2nd Screen Driving (SPT=1)

Register setting	Display operation
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) = NL	Full screen display Normally displays (SE28 to 10) to (SS18 to 10)
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) < NL	Partial display Normally displays (SE28 to 10) to (SS18 to 10) White display for all other times (RAM data is not related at all)
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) > NL	Setting disabled

NOTE 1: SS18 to 10 ≤ SE18 to 10 < SS28 to 20 ≤ SE28 to 20 ≤ 13Fh
NOTE 2: (SE28 to 20) – (SS18 to 10) ≤ NL

The driver output can't be set for non-display area during the partial display. Determine based on specification of the panels.

PT1	PT0	Source output in non-display area		Gate output in Non-display area
		Positive polarity	Negative polarity	
0	0	AVSS	AVSS	PTG setting
0	1	AVSS	GVDD	PTG setting
1	0	GVDD	AVSS	PTG setting
1	1	Hi-Z	Hi-Z	PTG setting

Refer to the following flow to set up the partial display.

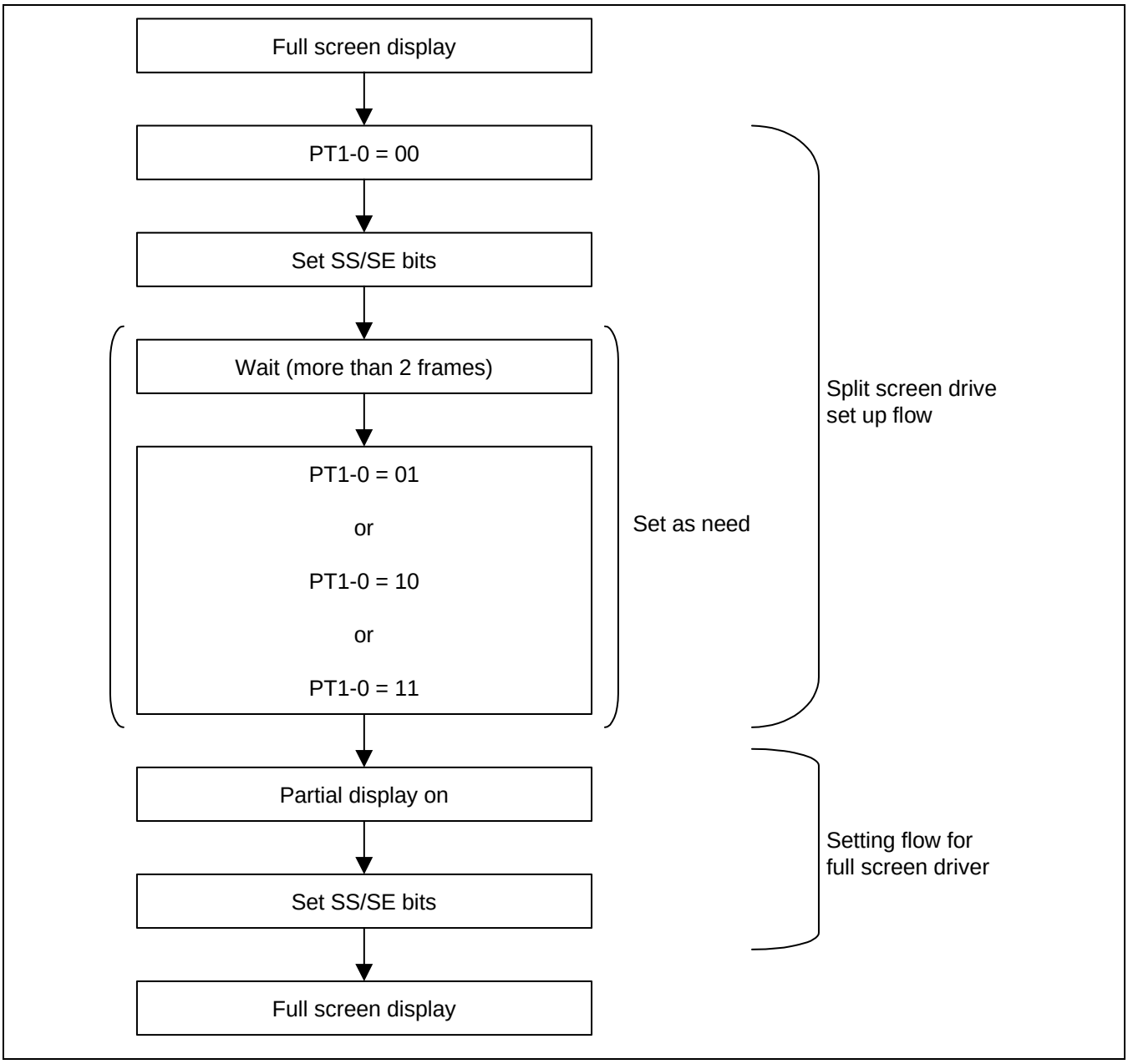


Figure 86. Partial display set up flow

Preliminary

APPLICATION CIRCUIT

The following figure indicates a schematic diagram of application circuit for S6D0129.

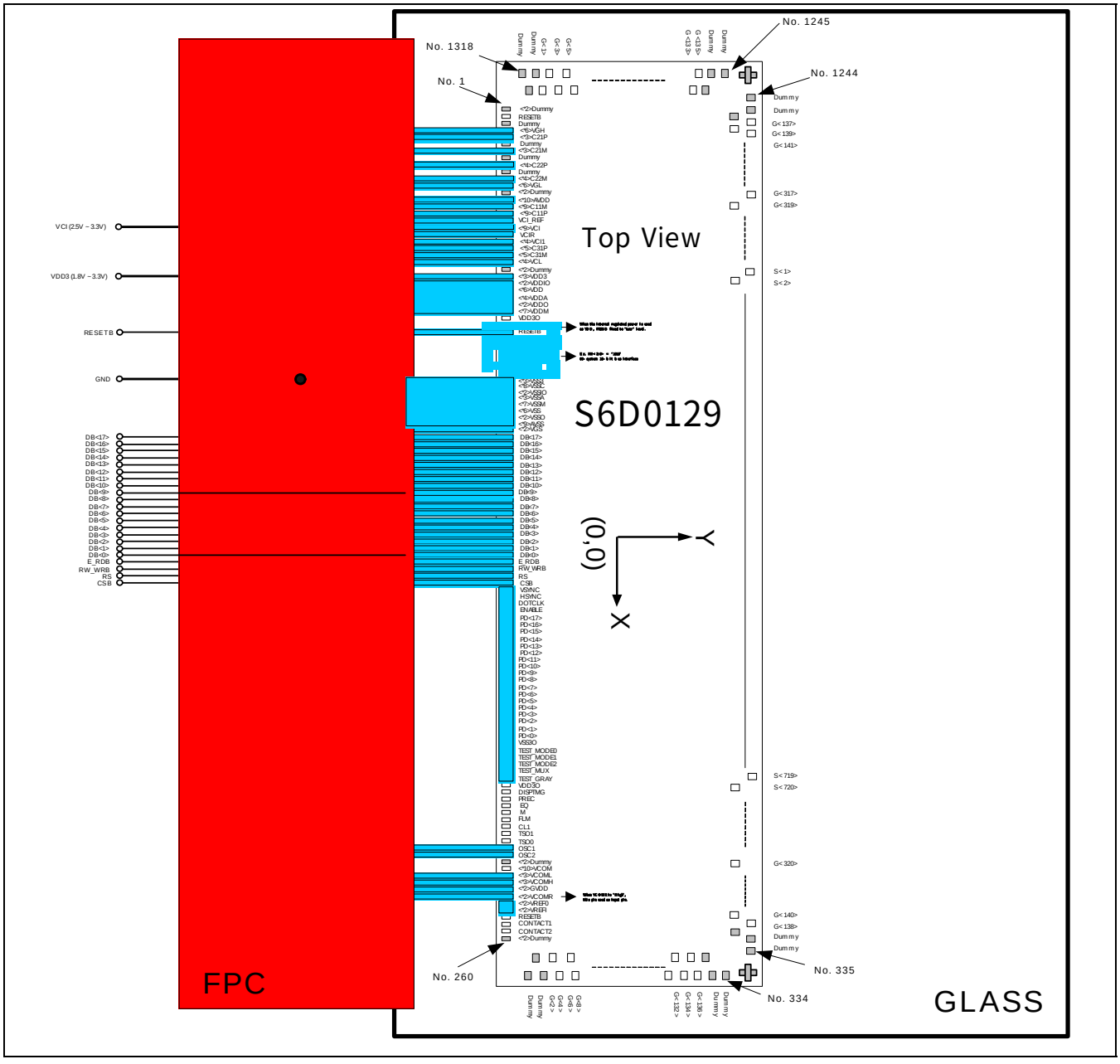


Figure 87. Application Circuit (18 bits - 80 CPU Interface Mode)

Preliminary

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 48. Absolute Maximum Rating

(VSS = 0V)

Item	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 ~ 5.0	V
Supply voltage 3	VDD3	-0.3 ~ 5.0	V
Supply voltage for step-up circuit	Vci	-0.3 ~ 5.0	V
LCD Supply Voltage range	|VGH – VGL|	TBD	V
Input Voltage range	Vin	-0.3 to VDD +0.5	V
Operating temperature	T_{opr}	-45 ~ 85	°C
Storage temperature	T_{stg}	-55 ~ 110	°C

Notes:

1. Absolute maximum rating is the limit value beyond which the IC may be broken. They do not assure operations.
2. Operating temperature is the range of device-operating temperature. They do not guarantee chip performance.
3. Absolute maximum rating is guaranteed when our company's package used.

Preliminary

DC CHARACTERISTICS

Table 49. DC Characteristics

(VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Operating voltage	VDD		-	1.8	-	V	*1
	VDD3		1.8	-	3.3	V	*1
LCD driving voltage	VGH		10	-	16.5	V	
	VGL		-13.5	-	-8	V	
	VCL		-2.75	-	-1.7	V	
	AVDD		3.5	-	5.5	V	
	GVDD		3.0	-	5.0	V	
Input high voltage	V_{IH}						*2
Input low voltage	V_{IL}						*2
Output high voltage	V_{OH}	I_{OH} = -0.5mA					*3
Output low voltage	V_{OL}	I_{OL} = 0.5mA					*3
Input leakage current	I_{IL}	VIN = VSS or VDD3					*2
Output leakage current	I_{OL}	VIN = VSS or VDD3					*3
Operating frequency	fosc	Frame freq. = 60 Hz Display line = 320				kHz	*4
Internal reference power supply voltage	VCI		2.5		3.3	V	
1st step-up input voltage	VCI1		1.75		2.75	V	
1st step-up output efficiency	AVDD	I_{LOAD} = 1 mA	90	95	100	%	
2nd step-up output efficiency	VGH	I_{LOAD} = 0.1 mA	90	95	100	%	
3rd step-up output efficiency	VGL	I_{LOAD} = 0.1 mA	90	95	100	%	
4th step-up output efficiency	VCL	I_{LOAD} = 0.3 mA	90	95	100	%	

Notes :

1. VSS = 0V.
2. Applied pins; IM3-0, CSB, E_RDB, RW_WRB, RS, DB0 to DB17, PD0 to PD17, PREGB, RESETB.
3. Applied pins; DB0 to DB17
4. Target frame frequency = 60 Hz, Display line = 320, Back porch = 8, Front porch = 8
   Internal RTN[3:0] register = “0000”, Internal DIV[1:0] register = “00”
   (You Can measure OSC2(fosc) or CL1(fosc/16))

Table 50. DC Characteristics for LCD driver outputs(TBD)

(VDD = 1.8V, VDD3 = 3.0V, VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
LCD gate driver output On resistance	Ron	VGH–VGL=30.0V, VGH=16.5V, VGL=-13.5V					
LCD source driver delay	t_{SD}	AVDD = 5.5V GVDD = 5.0V SAP = “001”					
Current consumption during standby mode	Istby	Standby mode, Ta = 25 °C					
Current consumption during normal operation	I_{VDD}	No load, Ta = 25 °C					
	I_{VCI}						

Preliminary

AC CHARACTERISTICS

Table 51. Parallel Write Interface Characteristics (68 Mode)

(VDD = 1.8(±0.15)V, VDD3 = 1.8 to 3.3V, T_A = -40 to +85 °C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	t_{CYCW68}	100	-	ns
	Read	t_{CYCR68}	500	-	
Pulse rise / fall time		t_R, t_F	-	2	
E pulse width high	Write	t_{WHW68}	40	-	
	Read	t_{WHR68}	250	-	
E pulse width low	Write	t_{WLW68}	40	-	
	Read	t_{WLR68}	200	-	
RW, RS and CSB setup time		t_{AS68}	10	-	
RW, RS and CSB hold time		t_{AH68}	2	-	
Write data setup time		t_{WDS68}	60	-	
Write data hold time		t_{WDH68}	15	-	
Read data delay time		t_{RDD68}	-	200	
Read data hold time		t_{RDH68}	5	-	

Preliminary

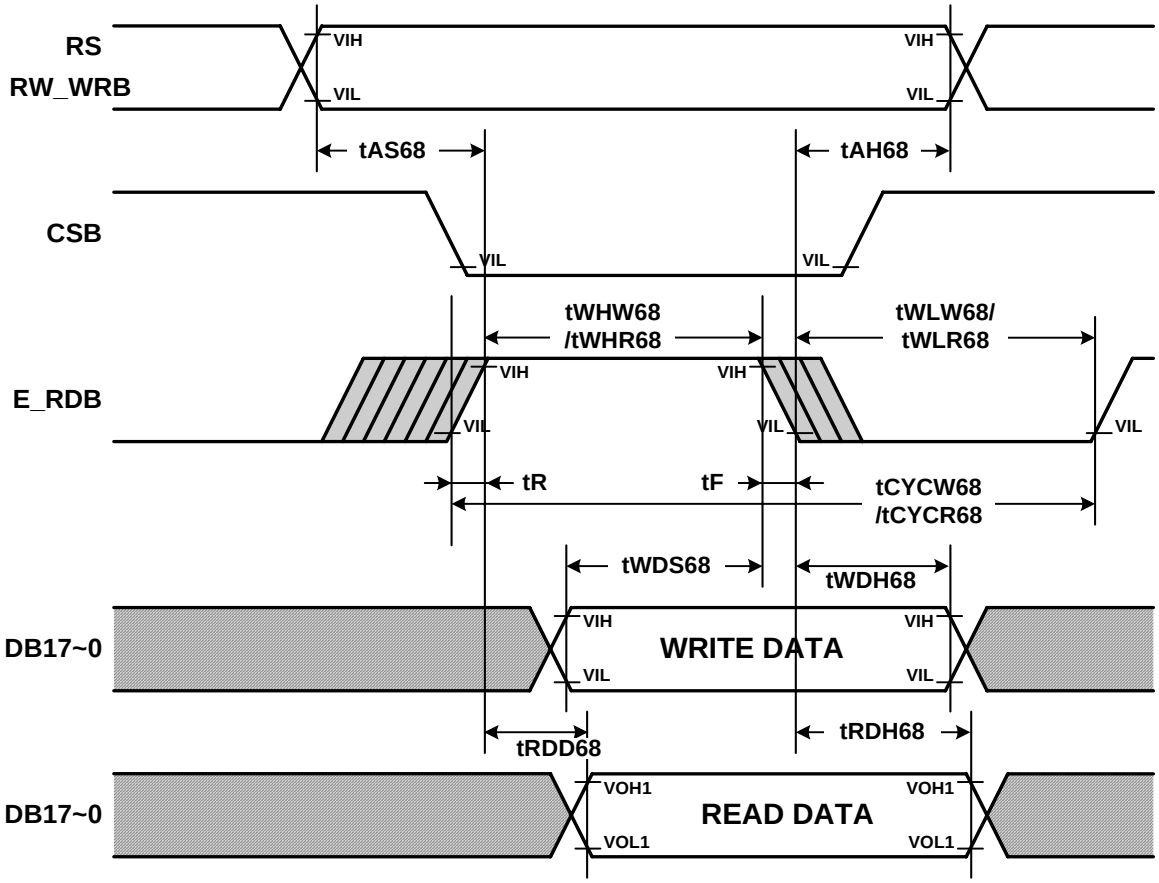


Figure 88. AC characteristics (68 Mode)

SAMSUNG ELECTRONICS

Preliminary

Table 52. Parallel Write Interface Characteristics (80 Mode)

(VDD = 1.8(±0.15) V, VDD3 = 1.8 to 3.3V, T_A = -40 to +85 °C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	t_{CYCW80}	100	-	ns
	Read	t_{CYCR80}	500	-	
Pulse rise / fall time		t_R, t_F	-	2	
Pulse width low	Write	t_{WLW80}	40	-	
	Read	t_{WLR80}	250	-	
Pulse width high	Write	t_{WHW80}	40	-	
	Read	t_{WHR80}	200	-	
RW, RS and CSB setup time		t_{AS80}	10	-	
RW, RS and CSB hold time		t_{AH80}	10	-	
Write data setup time		t_{WDS80}	20	-	
Write data hold time		t_{WDH80}	10	-	
Read data delay time		t_{RDD80}	-	200	
Read data hold time		t_{RDH80}	10	-	

Preliminary

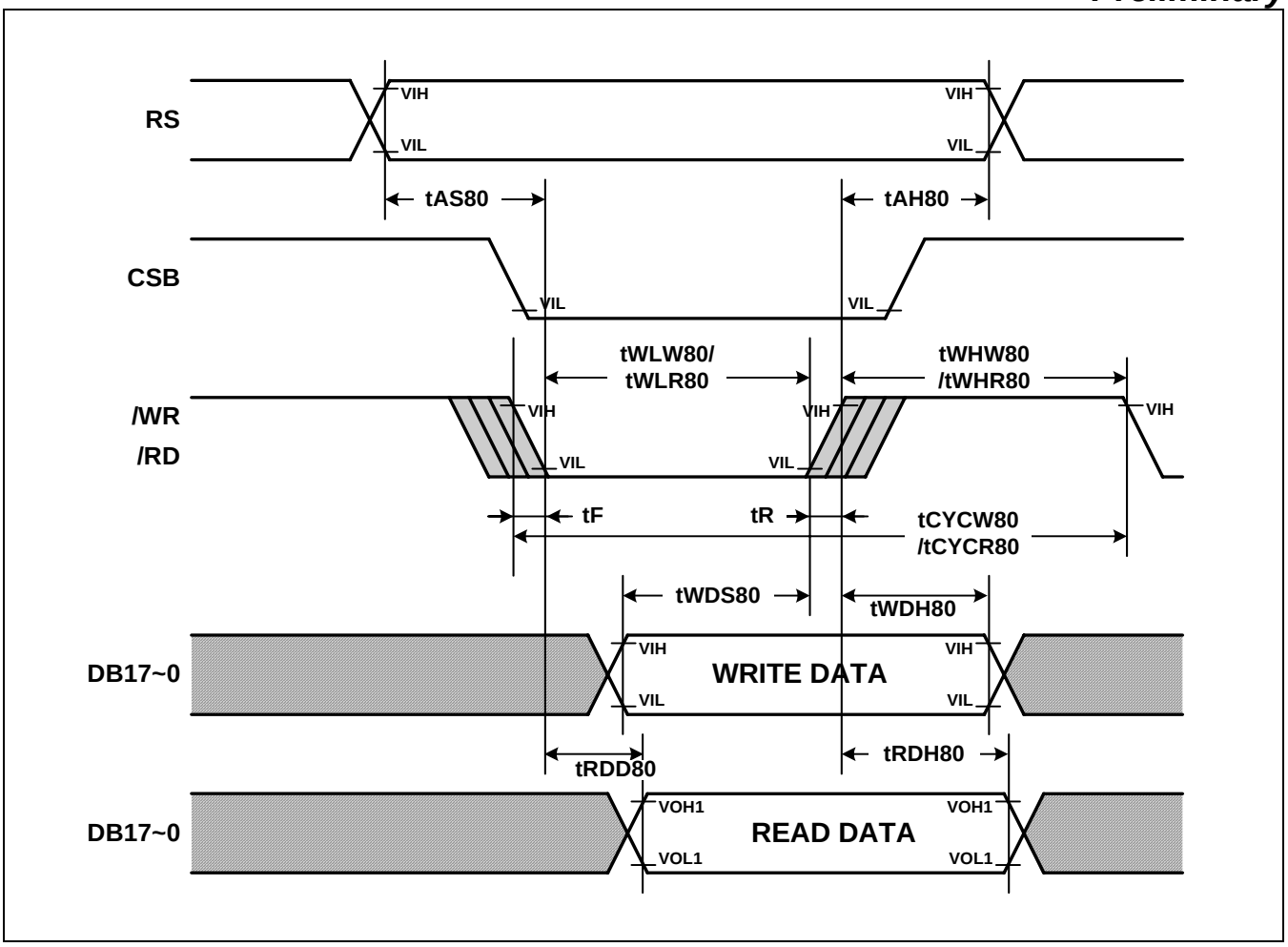


Figure 89. AC characteristics (80 Mode)

Preliminary

Table 53. Clock Synchronized Serial Write Mode Characteristics

(VDD = 1.8(±0.15)V, VDD3 = 1.8 to 3.3V, T_A = -40 to +85 °C)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock cycle time	tscyc	250	-	ns
Serial clock rise / fall time	tR, tF	-	2	ns
Pulse width high for write	tSCHW	40	-	ns
Pulse width high for read	tSCHR	230	-	ns
Pulse width low for write	tSCLW	60	-	ns
Pulse width low for read	tSCLR	230	-	ns
Chip Select setup time	tCSS	20	-	ns
Chip Select hold time	tCSH	60	-	ns
Serial input data setup time	tSIDS	30	-	ns
Serial input data hold time	tSIDH	30	-	ns
Serial output data delay time	tSODD	-	130	ns
Serial output data hold time	tSODH	5	-	ns

Table 54. Reset Timing Characteristics

(VDD = 1.8(±0.15)V, VDD3 = 1.8 to 3.3V ,T_A = -40 to +85 °C)

Characteristic	Symbol	Min.	Max.	Unit
Reset low pulse width	tRES	1	-	us

Preliminary

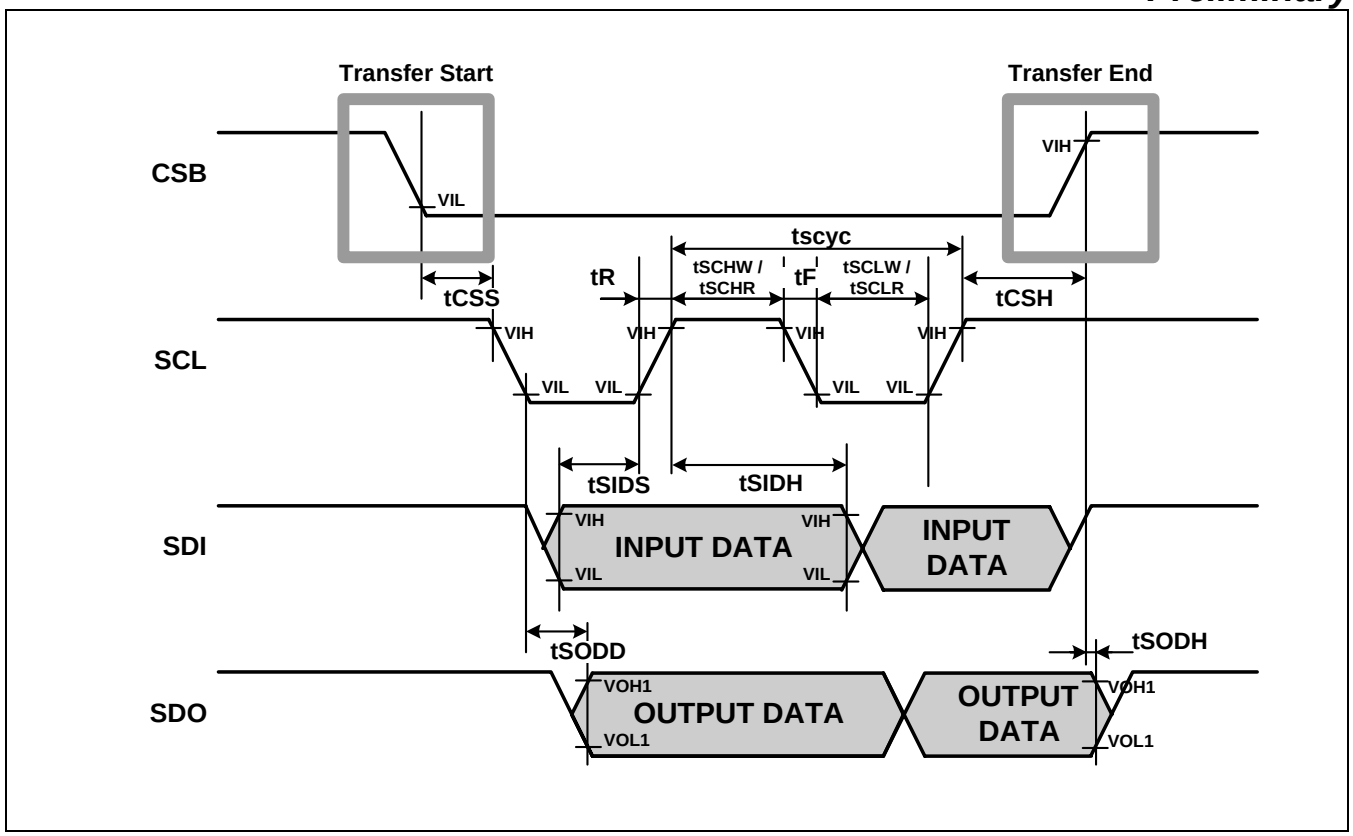


Figure 90. AC characteristics (SPI Mode)

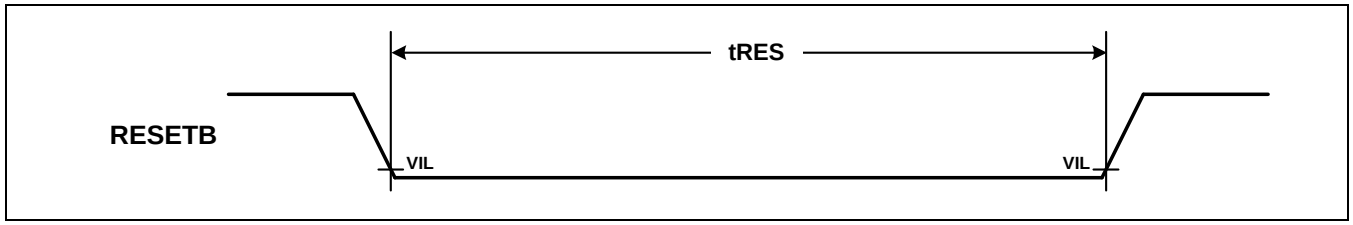


Figure 91. AC characteristics (RESET timing)

Preliminary

Table 55. RGB Data Interface Characteristics

(VDD = 1.8(±0.15)V, VDD3 = 1.8 to 3.3V, T_A = -40 to +85 °C)

Characteristic	Symbol	18/16bit RGB interface		6bit RGB interface		Unit
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	tDCYC	100	-	55	-	ns
DOTCLK rise / fall time	tR, tF	-	2		2	
DOTCLK Pulse width high	tDCHW	40	-	27	-	
DOTCLK Pulse width low	tDCLW	40	-	27	-	
ENABLE setup time	tENS	30	-	15	-	
ENABLE hold time	tENH	20	-	7	-	
PD data setup time	tPDS	30	-	15	-	
PD data hold time	tPDH	20	-	7	-	

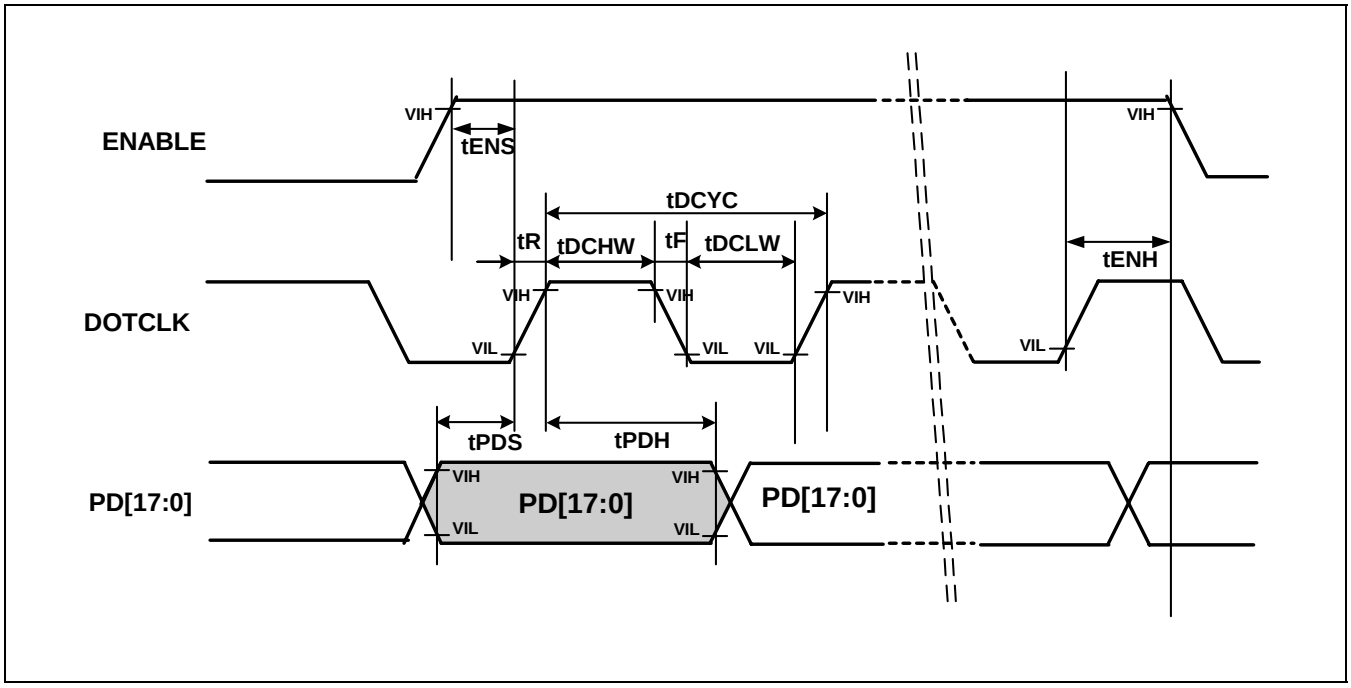


Figure 92. AC characteristics (RGB Mode)

Preliminary

REVISION HISTORY

S6D0129 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Feb. 26, 2004
0.1	Recycling Function, 260K color data transfer on 16-bits data bus	June 30, 2004
0.2	P.6 Figure1 revised P.58 VC2-0 Table : Vci => VCI_REF P.79 Figure28 revised P.80 Figure29 revised P.82 Figure31 revised P.138 Table50 revised	July 1, 2004
0.3	P.145 Table55 revised	July 27, 2004
0.4	P.7 Figure 7 revised P.8 Table 1 revised P.9 Figure 3 revised P.10 Figure 4 revised P.11 Table 2 ~ P.16 Table 7 revised	Aug 16. 2004

NOTICE

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.