TPG110

400CH LTPS TFT LCD Single Chip Digital Driver

Preliminary Data sheet

Product Design department

Toppoly Optoelectronics Corp.

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TPG110

400CH LTPS TFT LCD Single Chip Digital Driver

<1. Description>

TPG110 is a single chip solution to drive LTPS TFT LCD panel. This driver supports display resolutions including WQVGA, VGA, and WVGA, with functions of 400-channel 8-bit dot inversion source driver (SD), timing controller (TCON), serial peripheral interface (SPI), and power supply circuits.

<2. Features>

Source Driver

- Support 400 channels output
- 8-bit(256 level) grayscales
- Dot-inversion driving method
- Right and left shift capability

Timing controller

- Support 24-bit parallel RGB interface
- Support contrast (gain) control on RGB data separately
- Support brightness (offset) control on RGB separately
- Support digital gamma control
- Provide control signals for gate driver on panel
- Provide control signals for source driver and switches on panel
- Support 3-wire SPI commands setting

Power

- 3.3V power supply (2.7~3.6V) for digital circuit
- 5V/-5V power supply for analog circuit
- Embedded PWM buckboost control circuit
- Embedded regulated intermediate voltages +1.8V and –1.8V
- Internal DC/DC circuit for VGL voltage

Other

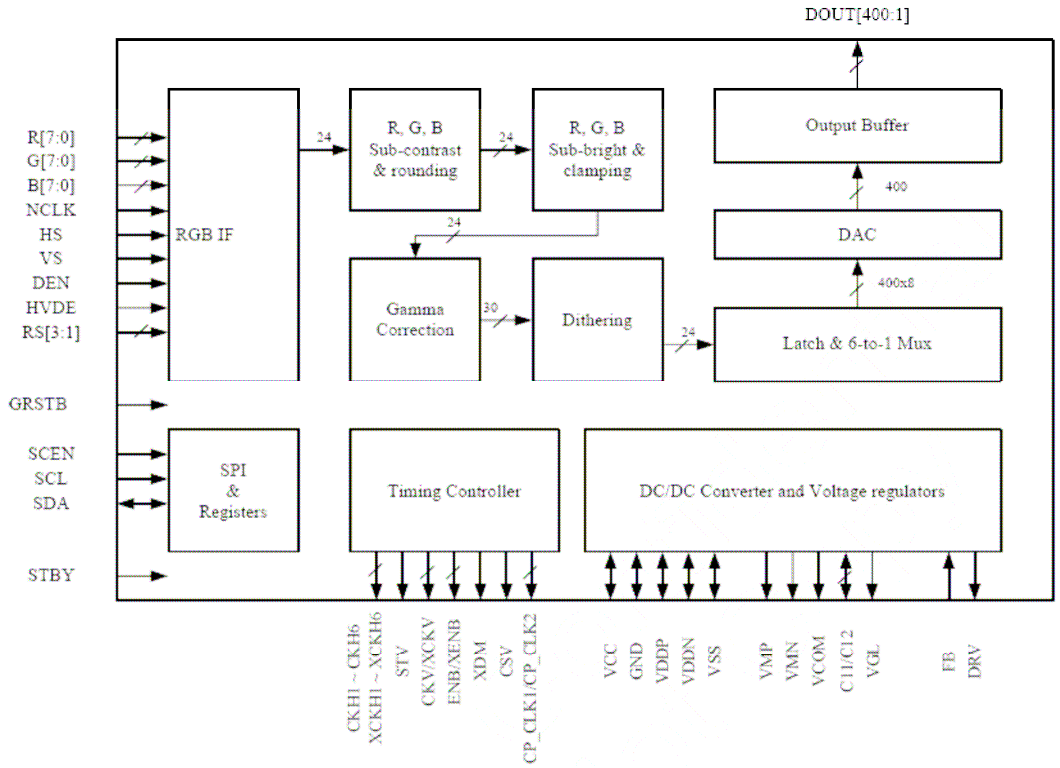
- Source Driver Output Pad Pitch: 35um stagger
- COG package

<3. Absolute Maximum Ratings>

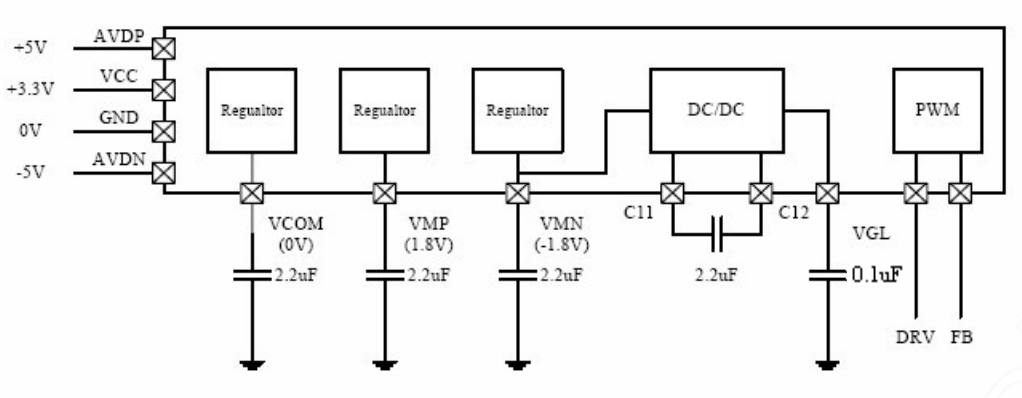
Parameter	Symbol	Rating			Unit
Logic power supply	VCC	-0.5	to	5.0	V
Driver power supply	VDDP	-0.5	to	6.0	V
Driver power supply	VDDN	-6.0	to	0.5	V
Logic input voltage	V_{I1}	-0.3	to	VCC +0.3	V
Operation ambient temperature	T_A	-30	to	85	V
Storage temperature	T_{STG}	-50	to	100	ºC

<4. Block Diagram>

IC Block Diagram



<5. Charge Pump Circuit>



The reference voltage generating circuit generates intermediate reference voltage VMP (1.8V). When PWM buck-boost converter is activated for the generation of VDDN (-5V), VMP will be used as the reference voltage for the voltage divider. The feedback threshold voltage for the buck-boost converter is 1.2V normally.

Another reference voltage VMN (-1.8V) will also be generated from VSS (0V) and VDDN (-5V) for the charge pump to generate VGL= VDDN+VMN. VMN is also used internally.

A DC VCOM level is also generated with 16 levels from –1V to +0.5V, selectable by the registers programmed through Serial Port Interface. And the default value of VCOM is connected to VSS (0V).

<6. FPC Pad Description>

Recommend 60-pin connector: **FH28 Blank-60S-0.5SH (51)**

Pin	Symbol	I/O	Description	Remark
1	T1	D	Only for Toppoly test pin	
2	CGH	C	Capacitor for VGH(+9.0 V)(2.2 uF)	
3	CPL1	C	Capacitor for charge pump clock (0.2 uF)	
4	CPL2	C	Capacitor for charge pump clock (0.2 uF)	

5	VCOM	C	Capacitor for VCOM (2.2 uF)	
6	VD	I	Vertical sync input	
7	HD	I	Horizontal sync input	
8	DEN	I	Data Enable	
9	NCLK	I	Clock signal, latch data onto line latches	
10	B0	I	Blue data (LSB)	
11	B1	I	Blue data	
12	B2	I	Blue data	
13	B3	I	Blue data	
14	B4	I	Blue data	
15	B5	I	Blue data	
16	B6	I	Blue data	
17	B7	I	Blue data (MSB)	
18	GND	P	Ground	
19	G0	I	Green data (LSB)	
20	G1	I	Green data	
21	G2	I	Green data	
22	G3	I	Green data	
23	G4	I	Green data	
24	G5	I	Green data	
25	G6	I	Green data	
26	G7	I	Green data (MSB)	
27	VCC	P	Power supply (3.3 V) for digital circuit and charge pump circuit	
28	R0	I	Red data (LSB)	
29	R1	I	Red data	
30	R2	I	Red data	
31	R3	I	Red data	
32	R4	I	Red data	
33	R5	I	Red data	
34	R6	I	Red data	
35	R7	I	Red data (MSB)	
36	VDDP	P	+5 V power supply	
37	VSS	P	Ground	

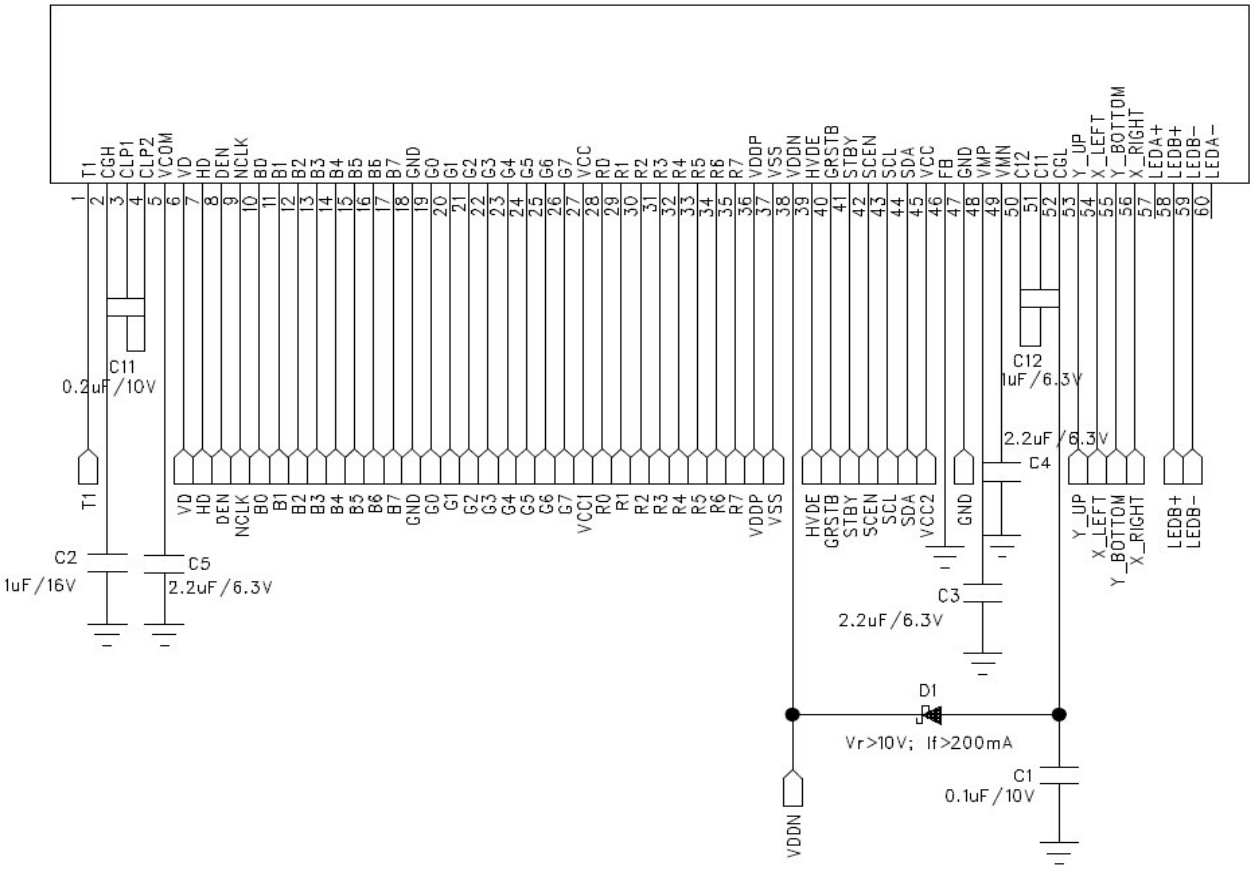
38	VDDN	P	-5 V power supply	
39	HVDE	I	Mode selection pin. HVDE="H" for SYNC(use HD +VD) mode, HVDE="L" for DE(use DEN) mode.	
40	GREST	I	Global reset pin	
41	STBY	I	Standby mode setting pin	
42	SCEN	I	Serial interface chip enable line	
43	SCL	I	Serial interface clock line	
44	SDA	I/O	Serial interface data line	
45	VCC	P	Power supply (3.3 V) for digital circuit and charge pump circuit	
46	FB	I	Main boost regulator feedback input(default:disable)	
47	GND	P	Ground	
48	VMP	C	Capacitor for +1.8 V power supply(2.2 uF)	
49	VMN	C	Capacitor for –1.8 V power supply(2.2 uF)	
50	C11	C	Capacitor for charge pump (DC/DC) circuit	
51	C12	C	Capacitor for charge pump (DC/DC) circuit	
52	CGL	C	Capacitor for VGL(-6.5V) (2.2 uF)	
53	Y_UP	I	For Touch panel Y_UP	Note 2
54	X_LEFT	I	For Touch panel X_LEFT	
55	Y_BOTTOM	I	For Touch panel Y_BOTTOM	
56	X_RIGHT	I	For Touch panel X_RIGHT	
57	LED A+	P	LEDA power: anode	Note 1
58	LED B+	P	LEDB power: anode	
59	LED B-	P	LEDB power: cathode	
60	LED A-	P	LEDA power: cathode	

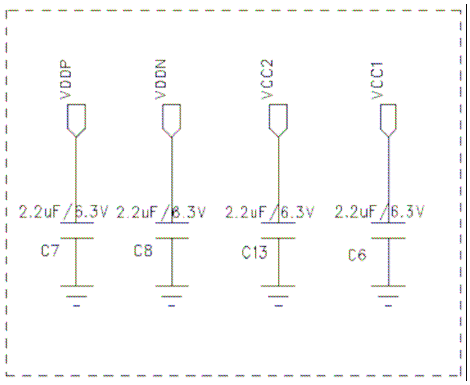
I : Input O: Output P: Power C: Capacitor D: Dummy I/O : Input/Output

Note 1: The figure below shows the connection of backlight LED

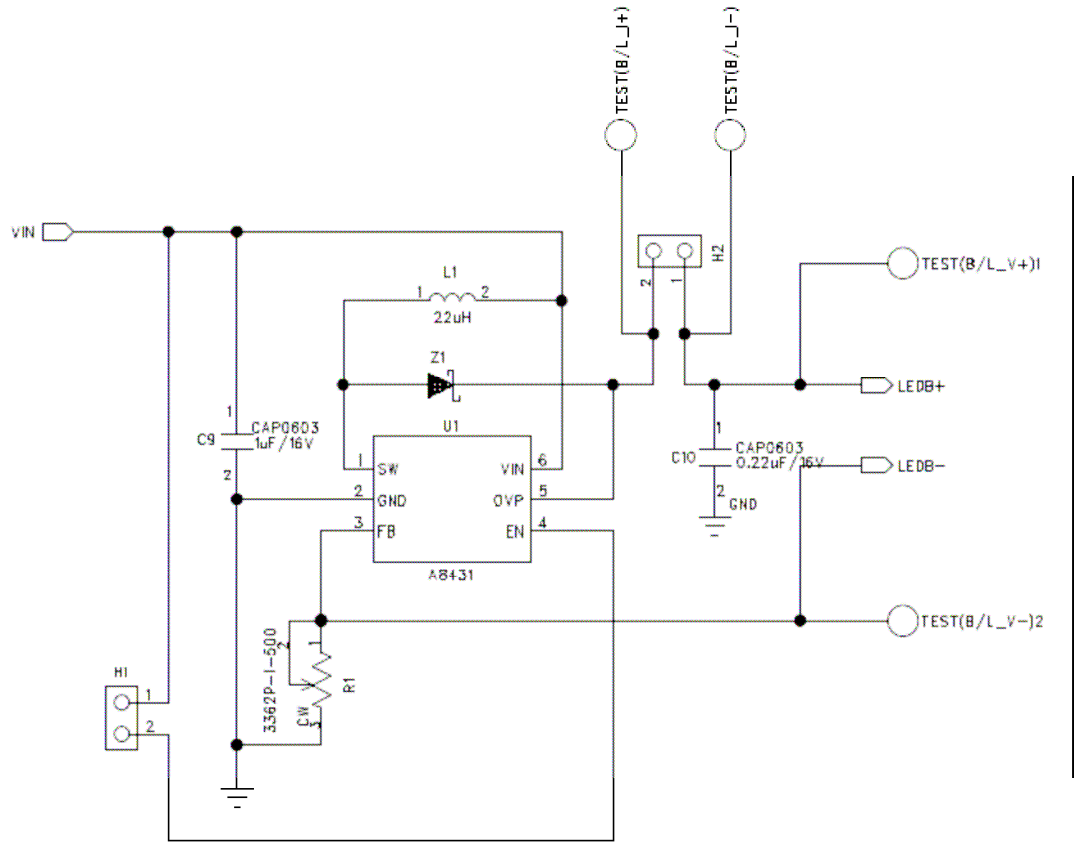
Note 2: The figure below shows the connection of Touch panel.

<7. Application circuit>

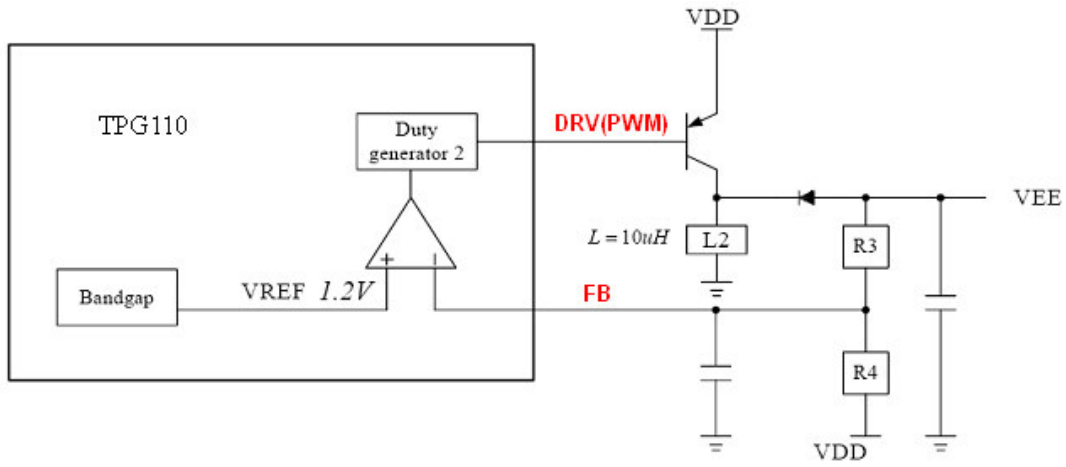




Backlight application circuit:



VDDN (-5V) generation by using PWM circuit in ASIC: (optional)

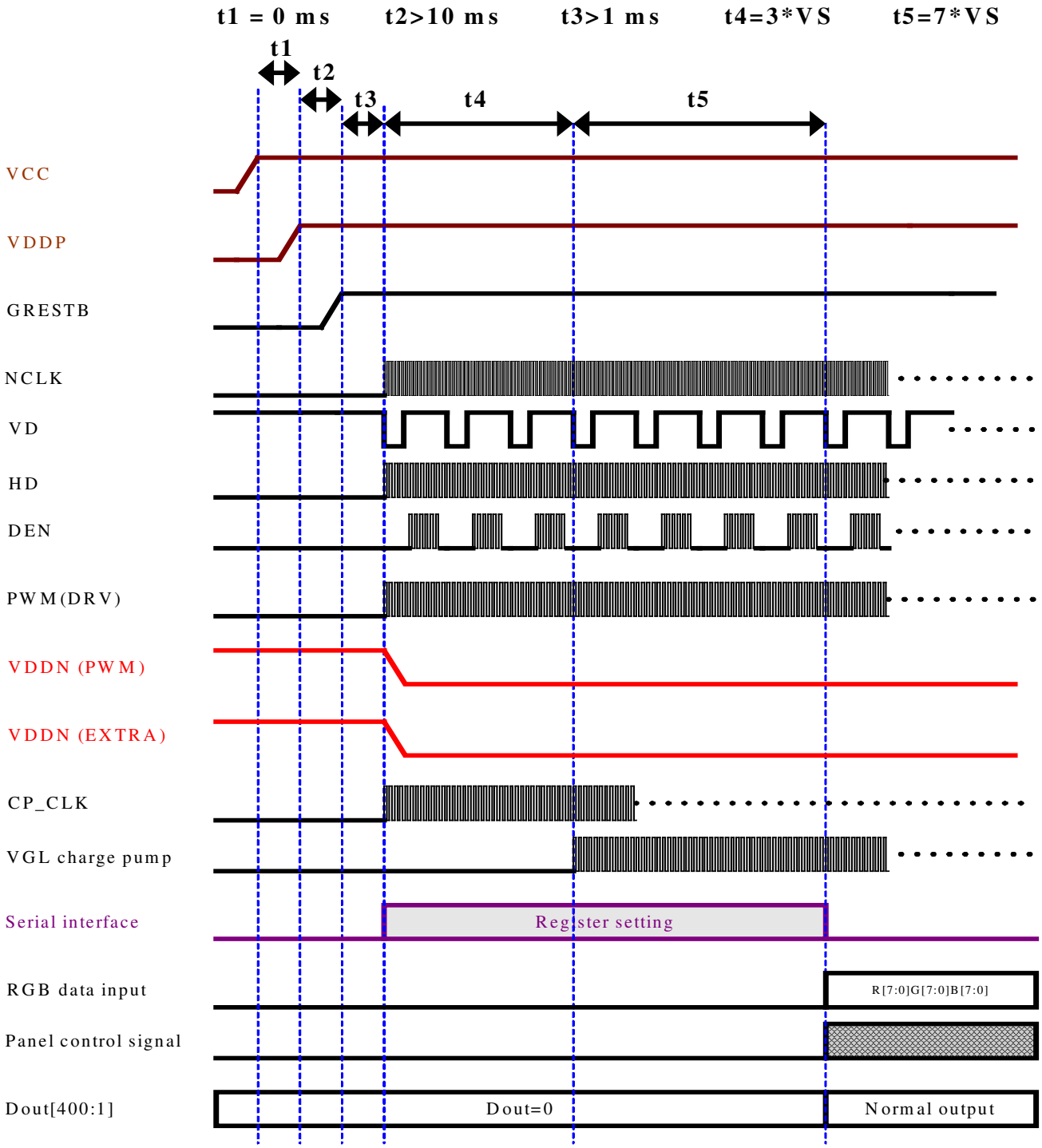


$$VEE = VFB(1.2V) \times (1 + \frac{R3}{R4}) - VDD\frac{R3}{R4}$$

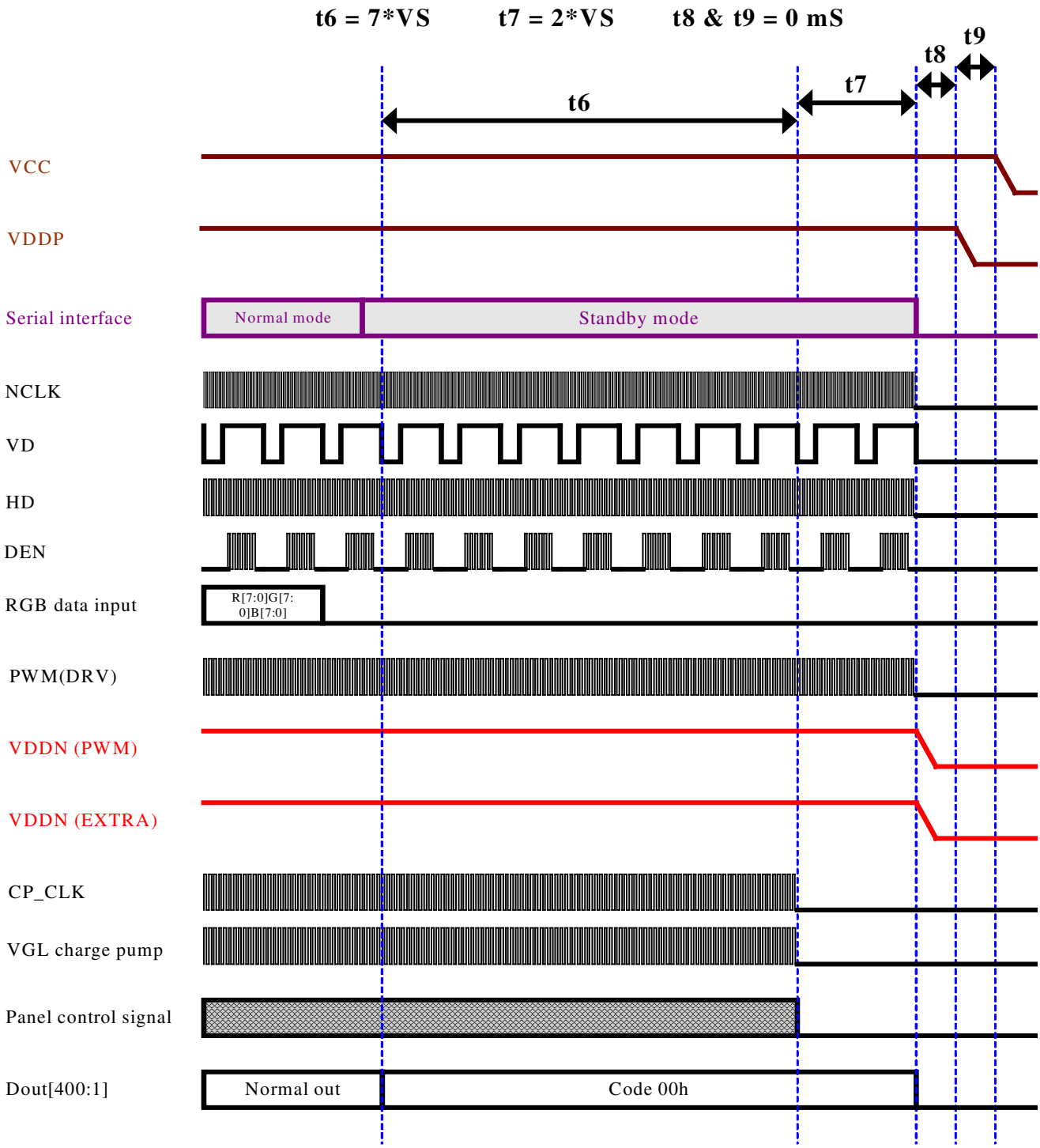
$VDD=3V,\ R3=124K,\ R4=36K$ ➔ $VEE = -5V$

<8. Power on/off sequence>

Power ON sequence:



Power OFF sequence:



<9. DC Electrical Characteristics>

Digital circuit (T_A = -30 ~ +85°C, VCC=2.7V to 3.6V, VSS= 0V)

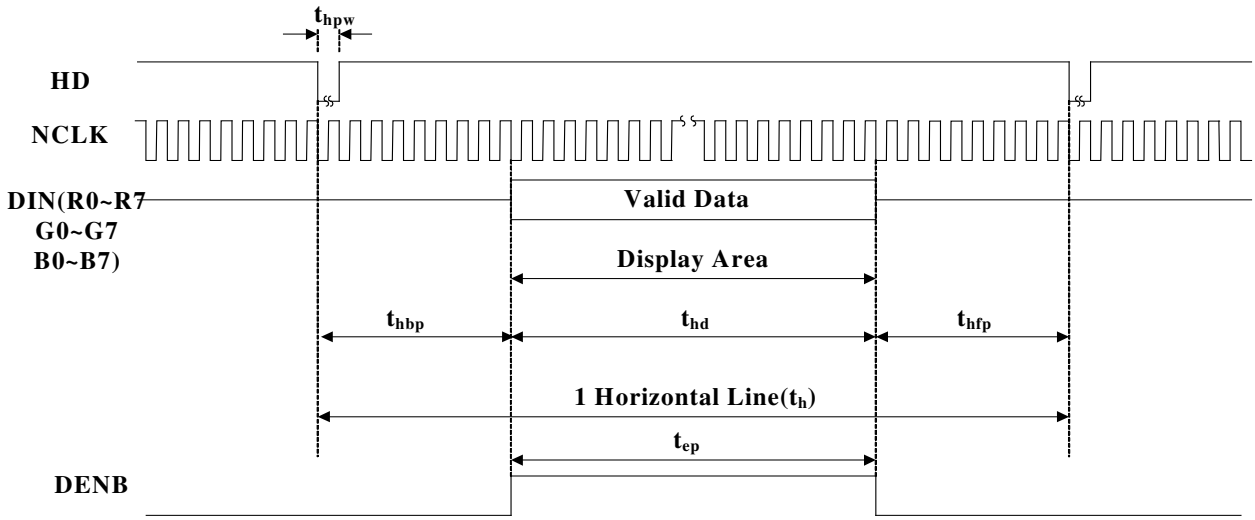
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Low Level Input Voltage	V_{il}	GND	-	0.3xV_{CC}	V
High Level Input Voltage	V_{ih}	0.7xV_{CC}	-	V_{CC}	V
Input Leakage Current	I_i	-	-	±1	µA
Pull-high Impedance	R_{inh}	0.5x typ	550	1.5x typ	kΩ
Pull-low Impedance	R_{inl}	0.5x typ	350	1.5x typ	kΩ
Output low voltage (IOL=1mA)	V_{OL}	VSS	-	VSS+0.4	V
Output high voltage (IOH=-1mA)	V_{OH}	VCC-0.4	-	VCC	V
Digital operation current	I_{STBY}			TBD	mA
Digital standby current	I_{CC}			(10)	mA

Analog circuit (T_A = -30 ~ +85°C, VCC=2.7V to 3.6V, VSS= 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDDP		4.5	5.0	5.5	V
	VDDN		-5.5	-5.0	-4.5	V
Voltage Deviation of Output	V_{CD}	0.5V ~ VDDP-0.5V, or -0.5V ~ VDDN+0.5V	-	±15	±20	mV
Dynamic Range of Output	V_{DR}		0.1	-	VDDP-0.1	V
			VDDN+0.1		-0.1	V
Low-Level Output Current	I_{OL}	0.1V vs 1.0V	-	-0.25	-	mA
High-Level Output Current	I_{OH}	4.9V vs 4.0V	-	0.25	-	mA
Analog Standby Current	I_{st}		-	-	TBD	µA
Analog Operating Current	I_{DDP}	VDDP=5V	-	-	(10)	mA
PWM Feed back voltage	V_{FB}		1.1	1.2	1.3	V

<10. Input timing >

--Horizontal--



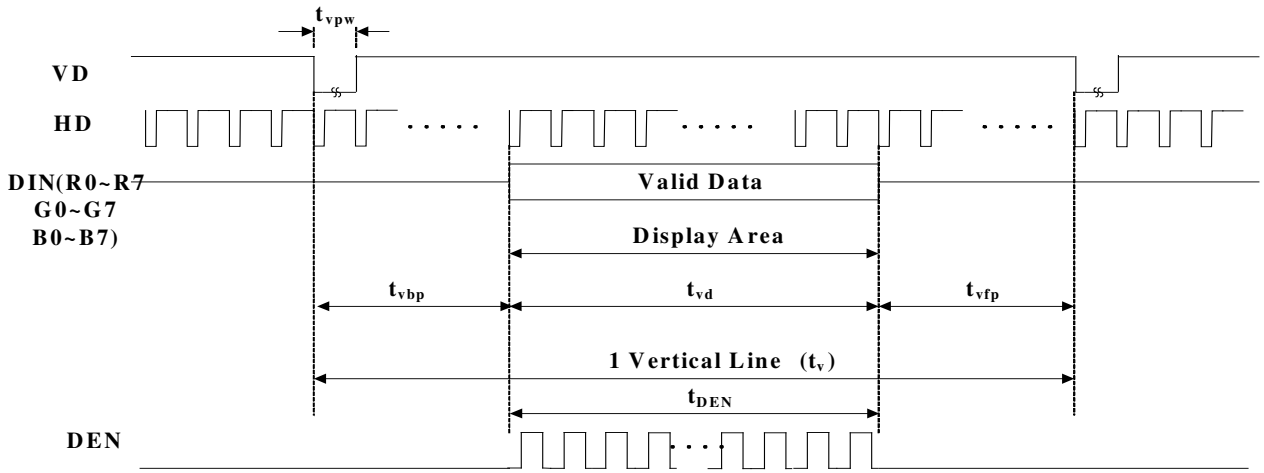
Parameter		Symbol	800RGBx480	640RGBx480	480RGBx272	480RGBx640	400RGBx240	Unit
NCLK Frequency		F_{NCLK}	33.2	25.2	9	20.5	8.3	MHz
Horizontal valid data		t_{hd}	800	640	480	480	400	NCLK
1 Horizontal Line		t_h	1056	800	525	525	528	NCLK
HSYNC	Min.	t_{hpw}	1	1	1	1	1	NCLK
Pulse	Typ.							
Width	Max.							
Hsync blanking		t_{hbp}	216	136	43	43	108	NCLK
Hsync front porch		t_{hfp}	40	24	2	2	20	NCLK
DENB Enable Time		t_{ep}	800	640	480	480	400	NCLK
Operation mode			Normal	Normal	Normal/Dual	Normal	Dual	

Notice:

Normal mode: (Input)800x480→(Output)800x480; (Input)640x480→(Output)640x480; (Input)480x272→(Output)480x272; (Input)480x640→(Output)480x640

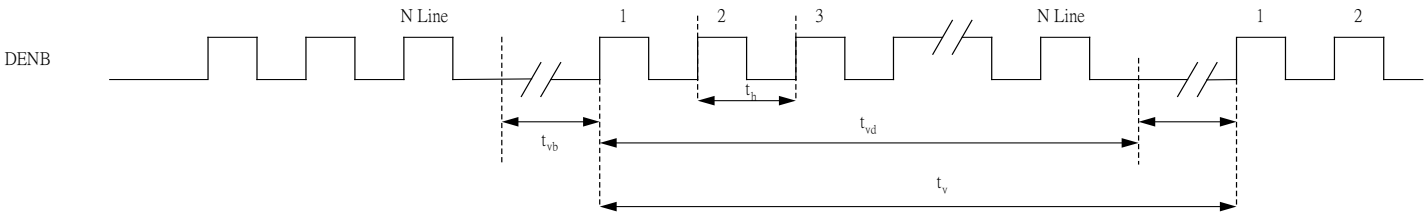
Dual scan mode: (Input)480x272→(Output)800x480 ; (Input)400x240→(Output)800x480

--Vertical--



Parameter		Symbol	800RGBx480	640RGBx480	480RGBx272	480RGBx640	400RGBx240	Unit
Vertical valid data		t_{vd}	480	480	272	640	240	H
Vertical period		t_v	525	525	286	652	262	H
VSYNC	Min.	t_{vpw}	1	1	1	1	1	H
Pulse	Typ.							
Width	Max.							
Vertical back porch		t_{vbp}	35	27	12	8	20	H
Vertical front porch		t_{vfp}	10	18	2	4	2	H
Vertical blanking of DEN mode		t_{vb}	45	45	14	12	22	H
DENB Enable		t_{DEN}	480	480	272	640	240	H
Operation mode			Normal	Normal	Normal/Dual	Normal	Dual	

DENB mode (The DENB signal can instead of HD and VD signals for ASIC to identify the input data)



<11. Timing Requirement>

Timing Requirement (T_A =25ºC, VCC=3.0V to 3.6V, VSS= 0V)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
NCLK period	PW_{CLK} *1	25	-	-	ns
NCLK pulse high period	PWH *1	10	-	-	ns
NCLK pulse low period	PWL *1	10	-	-	ns
HS, VS, DE, data setup time	t_{ds}	5	-	-	ns
HS, VS, DE, data hold time	t_{dh}	5	-	-	ns
XVD to XHD setup time	t_{vhs}	0	-	-	CLK

Note:

1 **Maximum clock frequency is 40MHz.**

2 **tr, tf is defined 10% to 90% of signal amplitude.**

<12. 3-Wires Serial Port Interface>

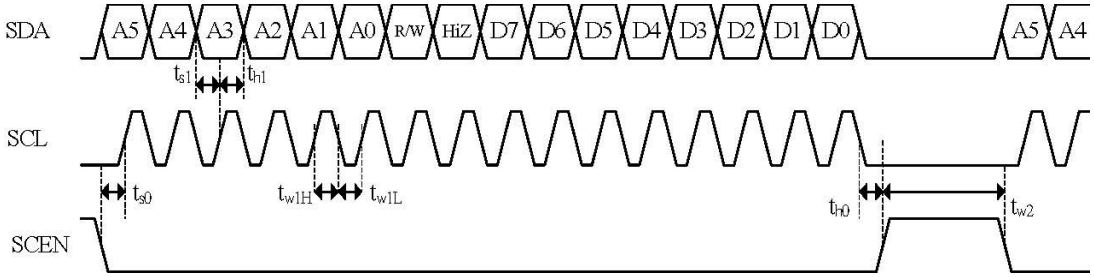
The TPG110 supports a clock synchronous serial interface as the interface to the microcomputer to enable instruction setting. Please notice that in addition to the 3 wire signals, DCLK input should also be provided while setting the registers.

The TPG110 recognizes the start of data transfer on the falling edge of SCEN input and starts data transfer. When setting instruction, the TPG110 input the setting values via SDA on the rising edge of input SCL.

The first 6 bits (A5 ~ A0) specify the address of the register. And next bit mean Read/Write command. “0” is write. “1” is read. And next cycle is turn-round cycle. And the last 8 bits are for Data setting (D7 ~ D0). The address and data are transferred from the MSB to LSB sequentially.

The data is written to the register of assigned address when “End of transfer” is detected after the 16th SCL rising cycles. Data is not accepted if there are less or more than 16 cycles for one transaction.

3 wires Serial data transfer format :



Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDA Setup Time	ts0	SCEN to SCL	150			ns
	ts1	SDA to SCL	150			ns
SDA Hold Time	th0	SCEN to SCL	150			ns
	th1	SDA to SCL	150			ns
Pulse Width	tw1L	SCL pulse width	160			ns
	tw1H	SCL pulse width	160			ns
	tw2	SCEN pulse width	1.0			us
Clock duty			40		60	%

<13. Register description>

Address	Default	Read/Write	Meaning
0x00	0x00	R/W	[7:0]: Testing register
0x01	0xC1	R	[7:4]: Chip ID [3:0]: Chip version
0x02	0x07	R/W	[7:6]: Dot inversion method selection [5]: VD polarity [4]: HD polarity [3]: Input clock latch data edge [2:0]: Resolution selection
0x03	0x5F	R/W	[7]: Hardware or software selection for resolution and standby. [6]: Pre-charge on/off [5:4]: Output driving capability [3]: PWM output on/off [2]: VGL pump output on/off [1]: CP_CLK output on/off [0]: Power management
0x04	0x17	R/W	[5:4] VGL pump frequency [3:2]: CP_CLK frequency [1]: Vertical reverse mode [0]: Horizontal reverse mode
0x05	0x20	R/W	[5:0]: Horizontal start position for Sync mode
0x06	0x08	R/W	[3:0]: Vertical start position for Sync mode
0x07	0x20	R/W	[5:0]: CKH high pulse width
0x08	0x20	R/W	[5:0]: CKH non-overlap
0x09	0x20	R/W	[5:0]: ENB rising to CKH non-overlap
0x0A	0x20	R/W	[5:0]: ENB low pulse width
0x0B	0x20	R/W	[5:0]: R gain of contrast
0x0C	0x20	R/W	[5:0]: G gain of contrast
0x0D	0x20	R/W	[5:0]: B gain of contrast
0x0E	0x10	R/W	[5:0]: Offset of brightness R
0x0F	0x10	R/W	[5:0]: Offset of brightness G
0x10	0x10	R/W	[5:0]: Offset of brightness B
0x11	0x00	R/W	[7:6]: GAMMA 0[9:8] of gamma Correction [5:4]: GAMMA 8[9:8] of gamma Correction [3:2]: GAMMA 16[9:8] of gamma Correction [1:0]: GAMMA 32[9:8] of gamma Correction
0x12	0x5B	R/W	[7:6]: GAMMA 64[9:8] of gamma Correction [5:4]: GAMMA 96[9:8] of gamma Correction [3:2]: GAMMA 128[9:8] of gamma Correction [1:0]: GAMMA 192[9:8] of gamma Correction

0x13	0xFF	R/W	[7:6]: GAMMA 224[9:8] of gamma Correction [5:4]: GAMMA 240[9:8] of gamma Correction [3:2]: GAMMA 248[9:8] of gamma Correction [1:0]: GAMMA 256[9:8] of gamma Correction
0x14	0X00	R/W	[7:0]: GAMMA 0[7:0] of gamma Correction
0x15	0X20	R/W	[7:0]: GAMMA 8[7:0] of gamma Correction
0X16	0X40	R/W	[7:0]: GAMMA 16[7:0] of gamma Correction
0X17	0X80	R/W	[7:0]: GAMMA 32[7:0] of gamma Correction
0X18	0x00	R/W	[7:0]: GAMMA 64[7:0] of gamma Correction
0X19	0X80	R/W	[7:0]: GAMMA 96[7:0] of gamma Correction
0x1A	0x00	R/W	[7:0]: GAMMA 128[7:0] of gamma Correction
0x1B	0x00	R/W	[7:0]: GAMMA 192[7:0] of gamma Correction
0x1C	0X80	R/W	[7:0]: GAMMA 224[7:0] of gamma Correction
0x1D	0XC0	R/W	[7:0]: GAMMA 240[7:0] of gamma Correction
0x1E	0XE0	R/W	[7:0]: GAMMA 248[7:0] of gamma Correction
0x1F	0XFF	R/W	[7:0]: GAMMA 256[7:0] of gamma Correction
0x20	0xD2	R/W	[7:4]: Positive gamma output voltage level for source driver input FFH [3:0]: Positive gamma output voltage level for source driver input 00H
0X21	0xD2	R/W	[7:4]: Negative gamma output voltage level for source driver input FFH [3:0]: Negative gamma output voltage level for source driver input 00H
0X22	0x05	R/W	[3:0]: DC VCOM level

R02h:

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	-	0	0	0	0	0	1	1	1

R02[7:6]: Dot inversion method selection

R02[7:6]		Function	Note
0	0	Type 1	Default (initial setting value)
0	1	Type 2	
1	0	Type 3	
1	1	Setting prohibited (Type 1)	

R02[5]: VD polarity

R02[5]	Function	Note
0	Low pulse	Default (initial setting value)
1	High pulse	

R02[4]: HD polarity

R02[4]	Function	Note
0	Low pulse	Default (initial setting value)
1	High pulse	

R02[3]: Input clock latch data edge

R02[3]	Function	Note
0	Latch data at NCLK falling edge	Default (initial setting value)
1	Latch data at NCLK rising edge	

R02[2:0]: Resolution selection

R02[2:0]			Input Sequence	Output Resolution	Note
0	0	0	400RGBx240	800RGBx480	(Dual Scan)
0	0	1	480RGBx272	800RGBx480	(Dual Scan)
0	1	0	Setting Prohibited		
0	1	1	Setting Prohibited		
1	0	0	480RGBx640	480RGBx640	
1	0	1	480RGBx272	480RGBx272	
1	1	0	640RGBx480	640RGBx480	
1	1	1	800RGBx480	800RGBx480	Default

R03h:

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	-	0	1	0	1	1	1	1	1

R03[7]: Hardware or Software selection for resolution and standby

R03[7]	Function	Note
0	Hardware pin (RS[3:1], STBY)	Default (initial setting value)
1	Software register (R02[2:0], R03[0])	

R03[6]: Pre-charge ON/OFF

R03[6]	Function	Note
0	Pre-charge disable	
1	Pre-charge enable	Default (initial setting value)

R03[5:4]: Driving capability

R03[5:4]		Function	Note
0	0	75%	
0	1	100%	Default (initial setting value)
1	0	150%	
1	1	200%	

R03[3]: PWM output ON/OFF

R03[3]	Function	Note
0	PWM disable	
1	PWM enable	Default (initial setting value)

R03[2]: VGL pump output ON/OFF

R03[2]	Function	Note
0	VGL pump disable	
1	VGL pump enable	Default (initial setting value)

R03[1]: CP_CLK output ON/OFF

R03[1]	Function	Note
0	CP_CLK disable	
1	CP_CLK enable	Default (initial setting value)

R03[0]: Power management

R03[0]	Function	Note
0	Standby mode	
1	Normal operation	Default (initial setting value)

In standby mode, DOUT[400:1], VCOM are connected to GND. PWM disabled. Control signals STV, CKV, CKH1~CKH6, and XENB are low, while XCKV, XCKH1~XCKH6, and ENB are high. CP_CLK1 is pulled high and CP_CLK is pulled low.

R04h:

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	-	-	-	0	1	0	1	1	1

R04[5:4]: VGL pump frequency

R04[5:4]		Period (frequency for WVGA)	Note
0	0	2 * H (~16KHz)	
0	1	1 * H (~32KHz)	Default (initial setting value)
1	0	1/2 * H (~64KHz)	
1	1	1/4 * H (~128KHz)	

R04[3:2]: CP_CLK frequency

R04[3:2]		Period (frequency for WVGA)	Note
0	0	2 * H (~16KHz)	
0	1	1 * H (~32KHz)	Default (initial setting value)
1	0	1/2 * H (~64KHz)	
1	1	1/4 * H (~128KHz)	

R04[1]: Vertical reverse function

R04[1]	Function	Note
0	Reverse (CSV = L)	
1	Normal (CSV = H)	Default (initial setting value)

R04[0]: Horizontal reverse function

R04[0]	Function	Note
0	Reverse	
1	Normal operation	Default (initial setting value)

R05h:

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	-	-	-	1	0	0	0	0	0

R05[5:0]: Horizontal display position shift for SYNC mode

R05[5:0]						Function	
0	0	0	0	0	0	-32 NCLK	
0	0	0	0	0	1	-31 NCLK	
:	:	:	:	:	:	:	(display shift right)
0	1	1	1	1	0	-2NCLK	
0	1	1	1	1	1	-1 NCLK	
1	0	0	0	0	0	Center	Default (initial setting value)
1	0	0	0	0	1	+1 NCLK	
1	0	0	0	1	0	+2 NCLK	
:	:	:	:	:	:	:	(display shift left)
1	1	1	1	1	0	+30 NCLK	
1	1	1	1	1	1	+31 NCLK	

R06h:

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	-	-	-	-	-	1	0	0	0

R06[3:0]: Vertical display position shift for SYNC mode

R06[3:0]				Function	Note
0	0	0	0	-8 NCLK	
0	0	0	1	-7 NCLK	
:	:	:	:	:	(display shift down)
0	1	1	0	-2NCLK	
0	1	1	1	-1 NCLK	
1	0	0	0	Center	Default (initial setting value)
1	0	0	1	+1 NCLK	
1	0	1	0	+2 NCLK	
:	:	:	:	:	(display shift up)
1	1	1	0	+6 NCLK	
1	1	1	1	+7 NCLK	

R07h~R0Ah:

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	-	-	-	1	0	0	0	0	0
0	0	1	0	0	0	0	-	-	-	1	0	0	0	0	0
0	0	1	0	0	1	0	-	-	-	1	0	0	0	0	0
0	0	1	0	1	0	0	-	-	-	1	0	0	0	0	0

R07[5:0]: CKH high pulse width adjustment. Set 0x20 for normal operation.
R08[5:0]: CKH non-overlap adjustment. Set 0x20 for normal operation (around 0.6us).
R09[5:0]: ENB to CKH1 non-overlap adjustment. Set 0x20 for normal operation (around 1.2us).
R0A[5:0]: ENB low pulse width adjustment. Set 0x20 for normal operation (around 2.8us).
Notice that CKV transition timing is in the middle of ENB low pulse.

R07~R0A[5:0]						Function	
0	0	0	0	0	0	-32 NCLK	
0	0	0	0	0	1	-31 NCLK	
:	:	:	:	:	:	:	
0	1	1	1	1	0	-2NCLK	
0	1	1	1	1	1	-1 NCLK	
1	0	0	0	0	0	Center	Default (initial setting value)
1	0	0	0	0	1	+1 NCLK	
1	0	0	0	1	0	+2 NCLK	
:	:	:	:	:	:	:	
1	1	1	1	1	0	+30 NCLK	
1	1	1	1	1	1	+31 NCLK	

R0Bh ~ R0Dh:

R0B [5:0]	0x00	0x20(Default)	0x3F
R Gain of Contrast	0.00000	1.00000	1.96875
R0C [5:0]	0x00	0x20(Default)	0x3F
G gain of contrast	0.00000	1.00000	1.96875

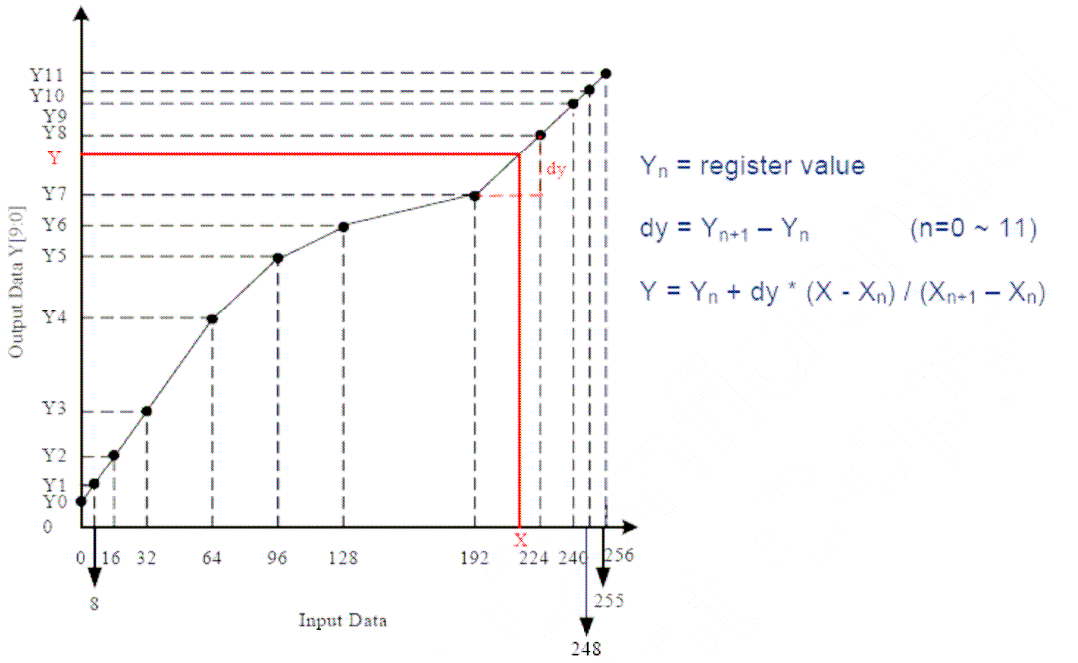
R0D [5:0]	0x00	0x20(Default)	0x3F
B gain of contrast	0.00000	1.00000	1.96875

R0Eh ~ R10h:

R0C [5:0]	0x00	0x10(Default)	0x3F
R Offset of Brightness	-16	0	47
R0D [5:0]	0x00	0x10(Default)	0x3F
G Offset of Brightness	-16	0	47
R0E [5:0]	0x00	0x10(Default)	0x3F
B Offset of Brightness	-16	0	47

R11h ~ R1Fh: Gamma Correction

The gamma correction is done by 11-segment piecewise linear interpolation. The 11 segments are defined with 12 register values for level 0, 8, 16, 32, 64, 96, 128, 192, 224, 240, 248, and 256 for positive polarity. Negative polarity data are generated symmetrically. The gamma correction output is then fed to 8-bit DAC and OP to drive the source lines on the panel.



R20h:

Voltage range for positive polarity (when VDDP=5V and VDDN=-5V)

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	-	1	1	0	1	0	0	1	0

R20[7:4] defines positive polarity DAC reference voltage for code FFH

R20[7:4]	0	1	2	3	4	5	6	7	8	9	0XA	0XB	0XC	0XD (Default)	0XE	0XF
Gamma Level	3.3	3.4	3.5	3.6	3.7	3.8	3.9	4.0	4.1	4.2	4.3	4.3	4.5	4.6	4.7	4.8

R20[3:0] defines positive polarity DAC reference voltage for code 00H

R20[3:0]	0	1	2 (Default)	3	4	5	6	7	8	9	0XA	0XB	0XC	0XD	0XE	0XF
Gamma Level	0.2	0.25	0.3	0.35	0.4	0.45	0.5	0.55	0.6	0.65	0.7	0.75	0.8	0.85	0.9	0.95

R21h:

Voltage range for negative polarity (when VDDP=5V and VDDN=-5V)

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	-	1	1	0	1	0	0	1	0

R21[7:4] defines negative polarity DAC reference voltage for code FFH

R21[7:4]	0	1	2	3	4	5	6	7	8	9	0XA	0XB	0XC	0XD (Default)	0XE	0XF
Gamma Level	-3.3	-3.4	-3.5	-3.6	-3.7	-3.8	-3.9	-4.0	-4.1	-4.2	-4.3	-4.3	-4.5	-4.6	-4.7	-4.8

R21[3:0] defines negative polarity DAC reference voltage for code 00H

R21[3:0]	0	1	2 (Default)	3	4	5	6	7	8	9	0XA	0XB	0XC	0XD	0XE	0XF
Gamma Level	-0.2	-0.25	-0.3	-0.35	-0.4	-0.45	-0.5	-0.55	-0.6	-0.65	-0.7	-0.75	-0.8	-0.85	-0.9	-0.95

R22h:

DC VCOM level

Address								Data setting default							
A5	A4	A3	A2	A1	A0	RW	-	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	-	-	-	-	-	0	1	0	1

R22[3:0] defines DC VCOM level

R22[3:0]	0	1	2	3	4	5 (Default)	6	7	8	9	0XA	0XB	0XC	0XD	0XE	0XF
VCOM Level	0.5	0.4	0.3	0.2	0.1	0	-01	-0.2	-0.3	-0.4	-0.5	-0.6	-0.7	-0.8	-0.9	-1.0

<14. Revision History>

Version	EFF.DATE	DESCRIPTION OF CHANGES
0.4	2006/8/10	Page 6: Modify pin assignment Page 8: Modify application circuit Page 12: Correct symbols of input timing

Version	EFF.DATE	DESCRIPTION OF CHANGES
0.5	2006/8/25	Page 8: Modify application circuit

Version	EFF.DATE	DESCRIPTION OF CHANGES
0.6	2006/11/20	Page 5: Add the statement of the charge pump circuit in ASIC. Page 10: Add the application circuit for VDDN (-5V) generation by using PWM circuit in ASIC Page 11,12: Update the power on/off sequence. Page 14,15: Update the data of Input timing