

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K Color

Datasheet

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1. Introduction

ILI9325C is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes RAM for graphic data of 240RGBx320 dots, and power supply circuit.

ILI9325C has five kinds of system interfaces which are i80-system MPU interface (8-/9-/16-/18-bit bus width), VSYNC interface (system interface + VSYNC, internal clock, DB[17:0]), serial data transfer interface (SPI), RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

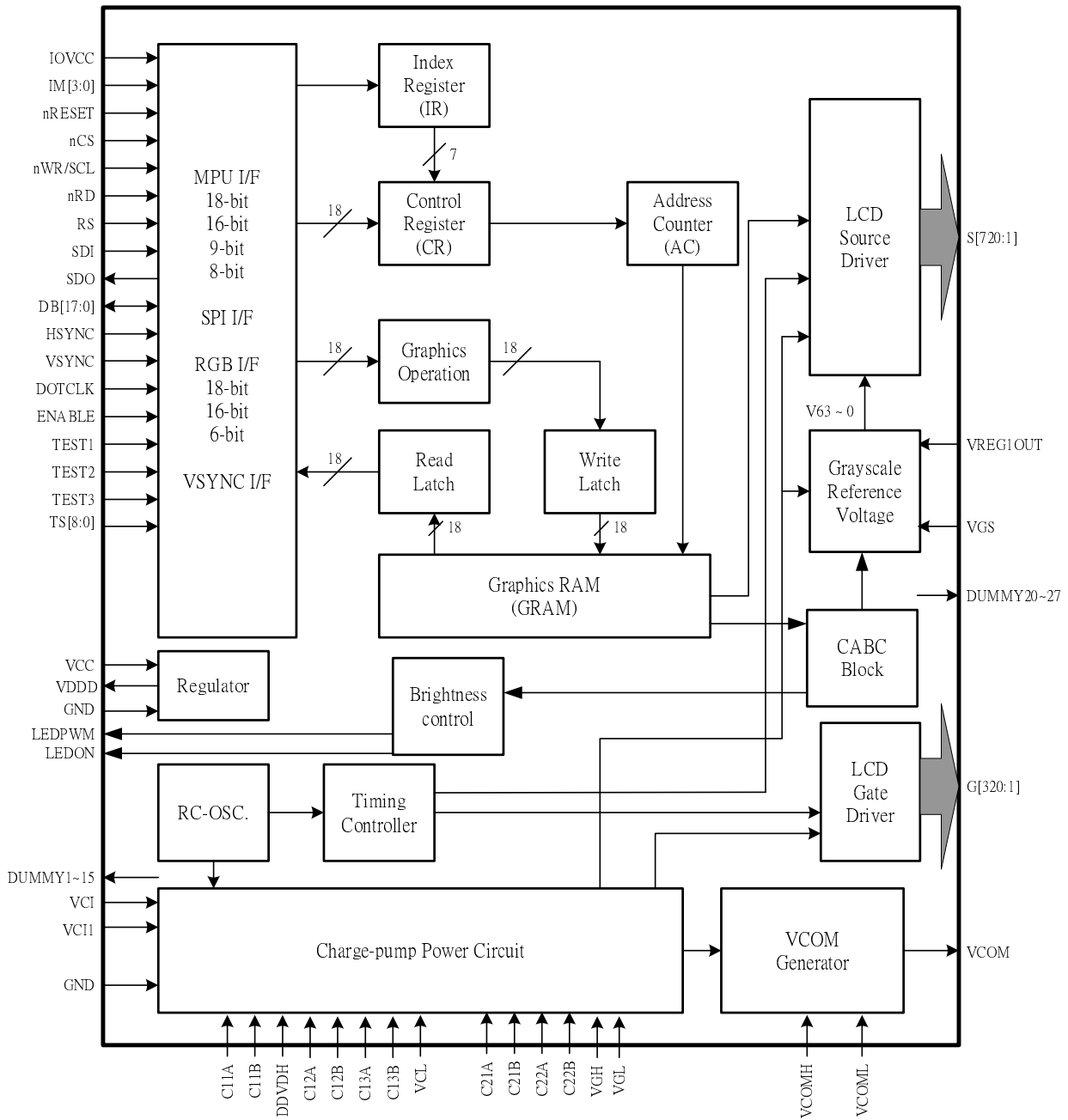
ILI9325C can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9325C also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9325C an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

2. Features

- ◆ Single chip solution for a liquid crystal QVGA TFT LCD display
- ◆ 240RGBx320-dot resolution capable with real 262,144 display color
- ◆ Support MVA (Multi-domain Vertical Alignment) wide view display
- ◆ Incorporate 720-channel source driver and 320-channel gate driver
- ◆ Internal 172,800 bytes graphic RAM
- ◆ CABC (Content Adaptive Brightness Control)
- ◆ System interfaces
 - i80 system interface with 8-/9-/16-/18-bit bus width
 - Serial Peripheral Interface (SPI)
 - RGB interface with 6-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
 - VSYNC interface (System interface + VSYNC)
- ◆ Internal oscillator and hardware reset
- ◆ Reversible source/gate driver shift direction
- ◆ Window address function to specify a rectangular area for internal GRAM access
- ◆ Bit operation function for facilitating graphics data processing
 - Bit-unit write data mask function
 - Pixel-unit logical/conditional write function
- ◆ Abundant functions for color display control
 - γ -correction function enabling display in 262,144 colors
 - Line-unit vertical scrolling function
- ◆ Partial drive function, enabling partially driving an LCD panel at positions specified by user
- ◆ Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- ◆ Power saving functions
 - 8-color mode
 - standby mode
 - sleep mode
- ◆ Low -power consumption architecture
 - Low operating power supplies:
 - IOVcc = 1.65V ~ 3.3 V (interface I/O)
 - VCI = 2.5V ~ 3.3 V (analog)
- ◆ LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH - GND = 4.5V ~ 6.0
 - VCL – GND = -2.0V ~ -3.0V
 - VCI – VCL \leq 6.0V
 - Gate driver output voltage
 - VGH - GND = 10V ~ 20V
 - VGL – GND = -5V ~ -15V

- $V_{GH} - V_{GL} \leq 30V$
- VCOM driver output voltage
 - $V_{COMH} = (V_{CI} + 0.2)V \sim (DDVDH - 0.2)V$
 - $V_{COML} = (V_{CL} + 0.2)V \sim 0V$
 - $V_{COMH} - V_{COML} \leq 6.0V$
- ◆ a-TFT LCD storage capacitor: Cst only

3. Block Diagram



4. Pin Descriptions

Pin Name	I/O	Type	Descriptions																																																																														
Input Interface																																																																																	
IM3, IM2, IM1, IM0/ID	I	IOVcc	Select the MPU system interface mode																																																																														
			<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>MPU-Interface Mode</th> <th>DB Pin in use</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>i80-system 16-bit interface</td> <td>DB[17:10], DB[8:1]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>i80-system 8-bit interface</td> <td>DB[17:10]</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>ID</td> <td>Serial Peripheral Interface (SPI)</td> <td>SDI, SDO</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>9-bit 3 wires Serial Peripheral Interface</td> <td>SDA, SCL, nCS</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>8-bit 4 wires Serial Peripheral Interface</td> <td>SDA, SCL, nCS, RS (D/CX)</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>i80-system 18-bit interface</td> <td>DB[17:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>i80-system 9-bit interface</td> <td>DB[17:9]</td> </tr> <tr> <td>1</td> <td>1</td> <td>*</td> <td>*</td> <td>Setting invalid</td> <td></td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	0	0	0	0	Setting invalid		0	0	0	1	Setting invalid		0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]	0	0	1	1	i80-system 8-bit interface	DB[17:10]	0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO	0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDA, SCL, nCS	0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDA, SCL, nCS, RS (D/CX)	1	0	0	0	Setting invalid		1	0	0	1	Setting invalid		1	0	1	0	i80-system 18-bit interface	DB[17:0]	1	0	1	1	i80-system 9-bit interface	DB[17:9]	1	1	*	*	Setting invalid	
			IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use																																																																									
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1	0	1	1	i80-system 9-bit interface	DB[17:9]																																																																												
1	1	*	*	Setting invalid																																																																													
When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.																																																																																	
nCS	I	MPU IOVcc	A chip select signal. Low: the ILI9325C is selected and accessible High: the ILI9325C is not selected and not accessible Fix to the GND level when not in use.																																																																														
RS	I	MPU IOVcc	A register select signal. Low: select an index or status register High: select a control register Fix to either IOVcc or GND level when not in use.																																																																														
nWR/SCL	I	MPU IOVcc	A write strobe signal and enables an operation to write data when the signal is low. Fix to either IOVcc or GND level when not in use. SPI Mode: Synchronizing clock signal in SPI mode.																																																																														
nRD	I	MPU IOVcc	A read strobe signal and enables an operation to read out data when the signal is low. Fix to either IOVcc or GND level when not in use.																																																																														
nRESET	I	MPU IOVcc	A reset pin. Initializes the ILI9325B with a low input. Be sure to execute a power-on reset after supplying power.																																																																														
SDI / SDA	I/O	MPU IOVcc	SPI interface input pin. The data is latched on the rising edge of the SCL signal. In the 8/9-bit serial peripheral interface, this pin is used as bi-directional data pin.																																																																														
SDO	O	MPU IOVcc	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. Let SDO as floating when not used.																																																																														
DB[17:0]	I/O	MPU IOVcc	An 18-bit parallel bi-directional data bus for MPU system interface mode																																																																														

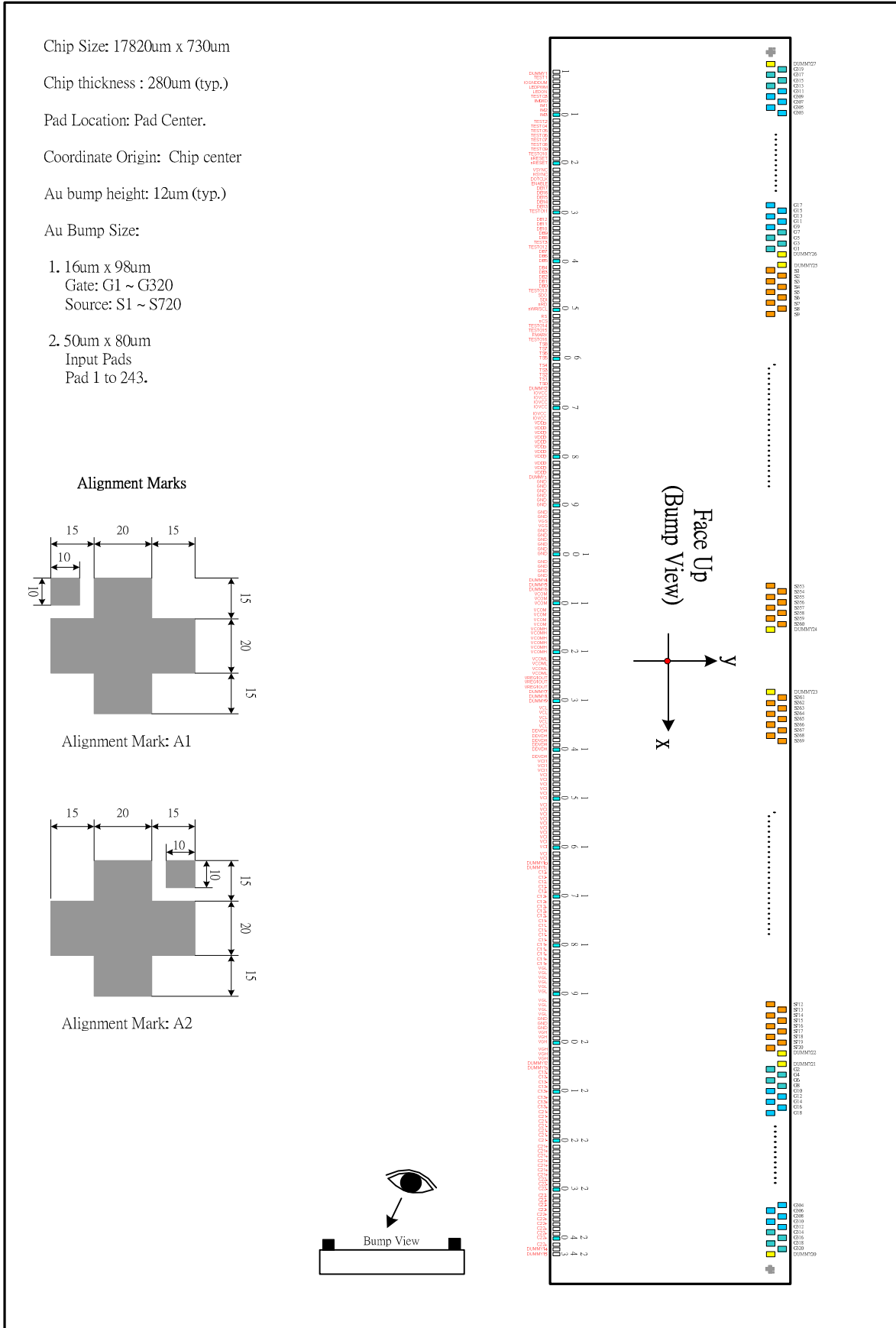
Pin Name	I/O	Type	Descriptions
			<p>8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used.</p> <p>18-bit parallel bi-directional data bus for RGB interface operation 6-bit RGB I/F: DB[17:12] are used. 16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used.</p> <p>Unused pins must be fixed to GND level.</p>
ENABLE	I	MPU IOVcc	<p>Data ENEABLE signal for RGB interface operation. Low: Select (access enabled) High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal.</p> <p>Fix to either IOVcc or GND level when not in use.</p>
DOTCLK	I	MPU IOVcc	<p>Dot clock signal for RGB interface operation. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK Fix to the GND level when not in use</p>
VSYNC	I	MPU IOVcc	<p>Frame synchronizing signal for RGB interface operation. VSPL = "0": Active low. VSPL = "1": Active high. Fix to the GND level when not in use.</p>
HSYNC	I	MPU IOVcc	<p>Line synchronizing signal for RGB interface operation. HSPL = "0": Active low. HSPL = "1": Active high. Fix to the GND level when not in use</p>
FMARK	O	MPU IOVcc	<p>Output a frame head pulse signal. The FMARK signal is used when writing RAM data in synchronization with frame. Leave the pin open when not in use.</p>
LEDPWM/ TESTO1	O	VCI	PWM signal output to control LED driver for LED brightness dimming.
LEDON/ TESTO2	O	VCI	This pin is connected to external LED driver. It's a LED driver control pin which is used for turning ON/OFF of LED backlight.
LCD Driving signals			
S720~S1	O	LCD	<p>Source output voltage signals applied to liquid crystal. To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "h00000" is output from S1. SS = "1", the data in the RAM address "h00000" is output from S720. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).</p>
G320~G1	O	LCD	<p>Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines</p>
VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.
VCOMH	O	Stabilizing capacitor	The high level of VCOM AC voltage.
VCOML	O	Stabilizing capacitor	The low level of VCOM AC voltage. Adjust the VCOML level with the VDV bits.
VGS	I	GND or	Reference level for the grayscale voltage generating circuit. The

Pin Name	I/O	Type	Descriptions
		external resistor	VGS level can be changed by connecting to an external resistor.
Charge-pump and Regulator Circuit			
Vci	I	Power supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V.
GND	I	Power supply	GND for the analog side: GND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
Vci1	O		An internal reference voltage for the step-up circuit1. The amplitude between Vci and GND is determined by the VC[2:0] bits. Make sure to set the Vci1 voltage so that the DDVDH, VGH and VGL voltages are set within the respective specification.
DDVDH	O	Stabilizing capacitor	Power supply for the source driver and Vcom drive.
VGH	O	Stabilizing capacitor	Power supply for the gate driver.
VGL	O	Stabilizing capacitor	Power supply for the gate driver.
VCL	O	Stabilizing capacitor	VcomL driver power supply. VCL = 0.5 ~ -VCI . Place a stabilizing capacitor between GND
C11+, C11-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.
C13+, C13- C21+, C21- C22+, C22-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.
VREG1OUT	I/O	Stabilizing capacitor	Output voltage generated from the reference voltage. The voltage level is set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage, (2) VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH - 0.2)V.
Power Pads			
IOVcc	I	Power supply	A supply voltage to the interface pins: IM[3:0], nRESET, nCS, nWR, nRD, RS, DB[17:0], VSYNC, HSYNC, DOTCLK, ENABLE, SCL, SDI, SDO. IOVcc = 1.65 ~ 3.3V and Vcc ≥ IOVcc. In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.
VDDD	O	Power	Digital circuit power pad. Connect these pins with the 1uF capacitor.
GND	I	Power supply	GND = 0V.
Test Pads			
DUMMY3~ 15 DUMMY20 ~ 27	-	-	Dummy pad. Leave these pins as open.
IOGNDDUM	O	GND	GND pin.
TESTO1~16	O	Open	Test pins. Leave them open.
TEST1, 2, 3	I	IOGND	Test pins (internal pull low). Connect to GND or leave these pins as open.
TS0~8	I	OPEN	Test pins (internal pull low). Leave them open.
TSO	O	OPEN	Test output pin. Let it open
TEST_EN	I	OPEN	Test pins Enable (internal pull low). Leave them open.

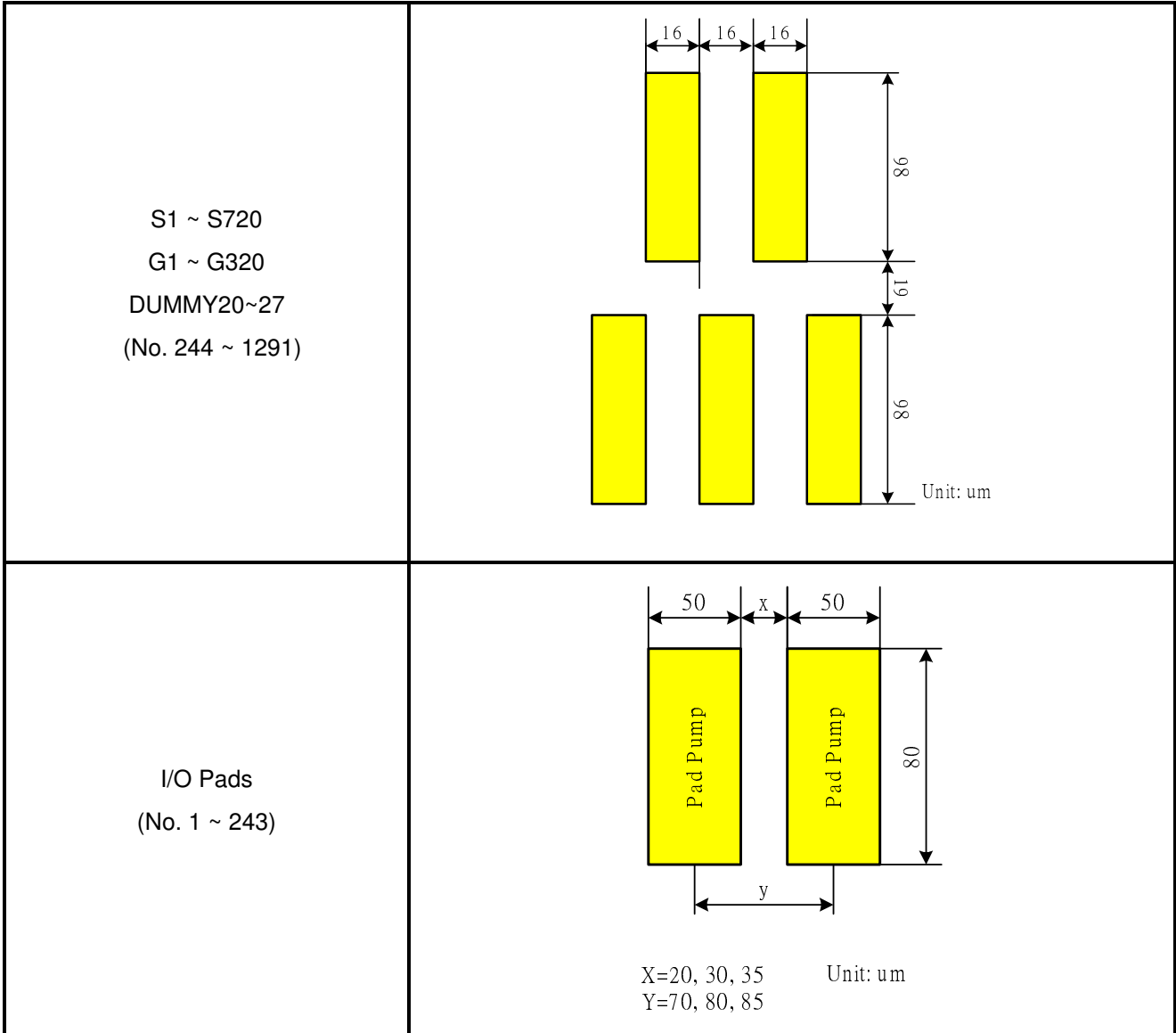
Liquid crystal power supply specifications Table 1

No.	Item	Description	
1	TFT Source Driver	720 pins (240 x RGB)	
2	TFT Gate Driver	320 pins	
3	TFT Display's Capacitor Structure	Cst structure only (Common VCOM)	
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVcc	1.65 ~ 3.30V
		VCI	2.50 ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 20V
		VGL	-5V ~ -15V
		VCL	-1.9V ~ -3.0V
		VGH - VGL	Max. 30V
		VCI - VCL	Max. 6.0V
7	Internal Step-up Circuits	DDVDH	VC11 x2
		VGH	VC11 x4, x5, x6
		VGL	VC11 x-3, x-4, x-5
		VCL	VC11 x-1

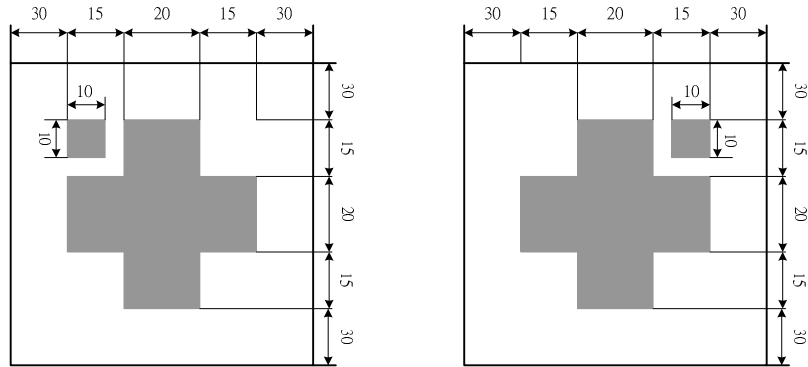
5. Pad Arrangement and Coordination



No.	Name	X	Y	No.	Name	X	Y
1201	G141	-7219	148	1261	G261	-8179	148
1202	G143	-7235	265	1262	G263	-8195	265
1203	G145	-7251	148	1263	G265	-8211	148
1204	G147	-7267	265	1264	G267	-8227	265
1205	G149	-7283	148	1265	G269	-8243	148
1206	G151	-7299	265	1266	G271	-8259	265
1207	G153	-7315	148	1267	G273	-8275	148
1208	G155	-7331	265	1268	G275	-8291	265
1209	G157	-7347	148	1269	G277	-8307	148
1210	G159	-7363	265	1270	G279	-8323	265
1211	G161	-7379	148	1271	G281	-8339	148
1212	G163	-7395	265	1272	G283	-8355	265
1213	G165	-7411	148	1273	G285	-8371	148
1214	G167	-7427	265	1274	G287	-8387	265
1215	G169	-7443	148	1275	G289	-8403	148
1216	G171	-7459	265	1276	G291	-8419	265
1217	G173	-7475	148	1277	G293	-8435	148
1218	G175	-7491	265	1278	G295	-8451	265
1219	G177	-7507	148	1279	G297	-8467	148
1220	G179	-7523	265	1280	G299	-8483	265
1221	G181	-7539	148	1281	G301	-8499	148
1222	G183	-7555	265	1282	G303	-8515	265
1223	G185	-7571	148	1283	G305	-8531	148
1224	G187	-7587	265	1284	G307	-8547	265
1225	G189	-7603	148	1285	G309	-8563	148
1226	G191	-7619	265	1286	G311	-8579	265
1227	G193	-7635	148	1287	G313	-8595	148
1228	G195	-7651	265	1288	G315	-8611	265
1229	G197	-7667	148	1289	G317	-8627	148
1230	G199	-7683	265	1290	G319	-8643	265
1231	G201	-7699	148	1291	DUMMY27	-8659	148
1232	G203	-7715	265				
1233	G205	-7731	148				
1234	G207	-7747	265				
1235	G209	-7763	148				
1236	G211	-7779	265				
1237	G213	-7795	148				
1238	G215	-7811	265				
1239	G217	-7827	148				
1240	G219	-7843	265				
1241	G221	-7859	148				
1242	G223	-7875	265				
1243	G225	-7891	148				
1244	G227	-7907	265				
1245	G229	-7923	148				
1246	G231	-7939	265				
1247	G233	-7955	148				
1248	G235	-7971	265				
1249	G237	-7987	148				
1250	G239	-8003	265				
1251	G241	-8019	148				
1252	G243	-8035	265				
1253	G245	-8051	148				
1254	G247	-8067	265				
1255	G249	-8083	148				
1256	G251	-8099	265				
1257	G253	-8115	148				
1258	G255	-8131	265				
1259	G257	-8147	148				
1260	G259	-8163	265				



Alignment mark



Alignment Mark: 1

Alignment Mark: 2

Alignment mark	X	Y
1	-8751	214.5
2	8751	214.5

6. Block Description

MPU System Interface

ILI9325C supports three system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9325C has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9325C read the first data from the internal GRAM. Valid data are read out after the ILI9325C performs the second read operation.

Registers are written consecutively as the register execution time.

Registers selection by system interface (8-/9-/16-/18-bit bus width)	I80		
	RS	nWR	nRD
Function			
Write an index to IR register	0	0	1
Write to control registers or the internal GRAM by WDR register.	1	0	1
Read from the internal GRAM by RDR register.	1	1	0

Registers selection by the SPI system interface		
Function	R/W	RS
Write an index to IR register	0	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

ILI9325C supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section. The ILI9325C allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Bit Operation

The ILI9325C supports a write data mask function for selectively writing data to the internal RAM in units of bits and a logical/compare operation to write data to the GRAM only when a condition is met as a result of comparing the data and the compare register bits. For details, see “Graphics Operation Functions”.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 172,800 (240 x 320x 18/8) bytes with 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ -correction register to display in 262,144 colors. For details, see the “ γ -Correction Register” section.

Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

ILI9325C generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

LCD Driver Circuit

The LCD driver circuit of ILI9325C consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). Display pattern data are latched when the 720th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720 source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for

driving an LCD

7. System Interface

7.1. Interface Specifications

ILI9325C has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9325C also has the RGB interface and VSYNC interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

ILI9325C operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM[1:0] = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 01)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available simultaneously.

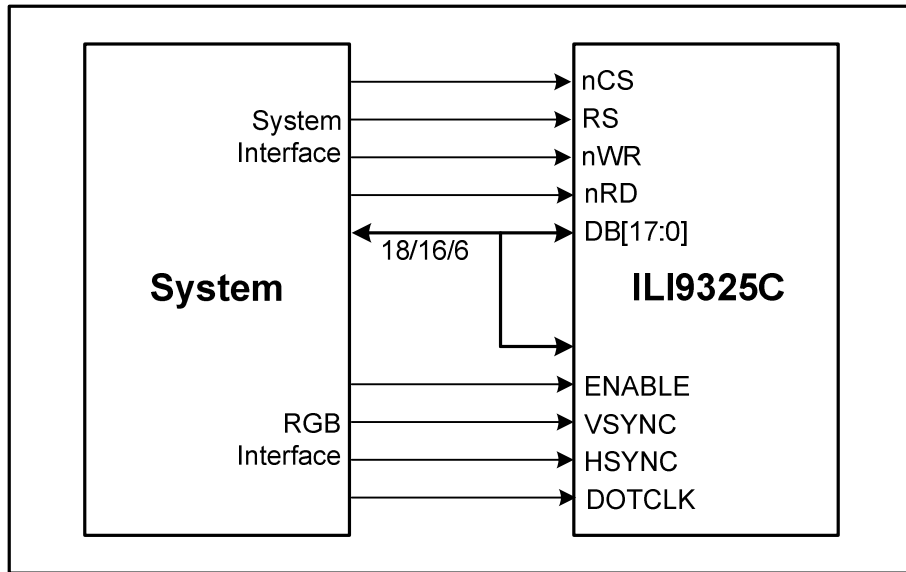


Figure1 System Interface and RGB Interface connection

7.2. Input Interfaces

The following are the system interfaces available with the ILI9325C. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting registers and GRAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO (DB[1:0])
0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDA, SCL, nCS
0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDA, SCL, nCS, RS (D/CX)
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	0	1	0	i80-system 18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

7.2.1. i80/18-bit System Interface

The i80/18-bit system interface is selected by setting the IM[3:0] as “1010” levels.

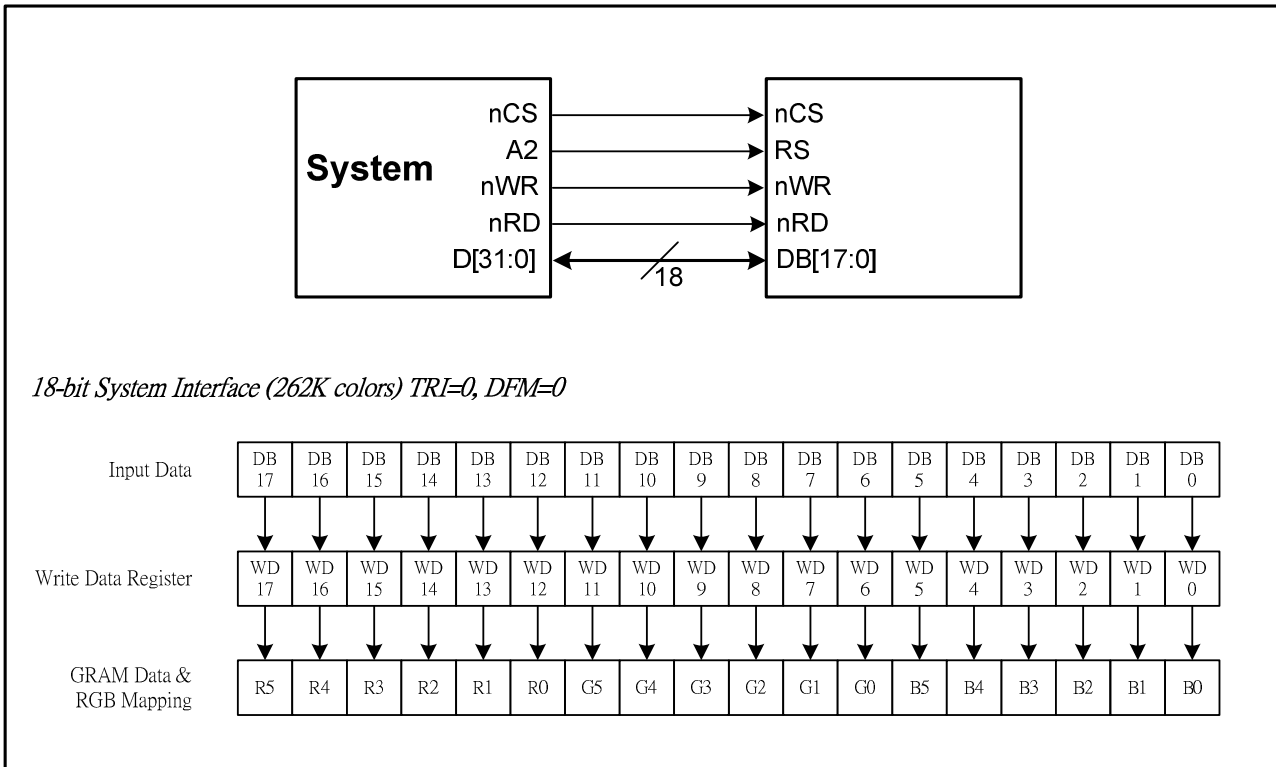


Figure2 18-bit System Interface Data Format

7.2.2. i80/16-bit System Interface

The i80/16-bit system interface is selected by setting the IM[3:0] as “0010” levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.

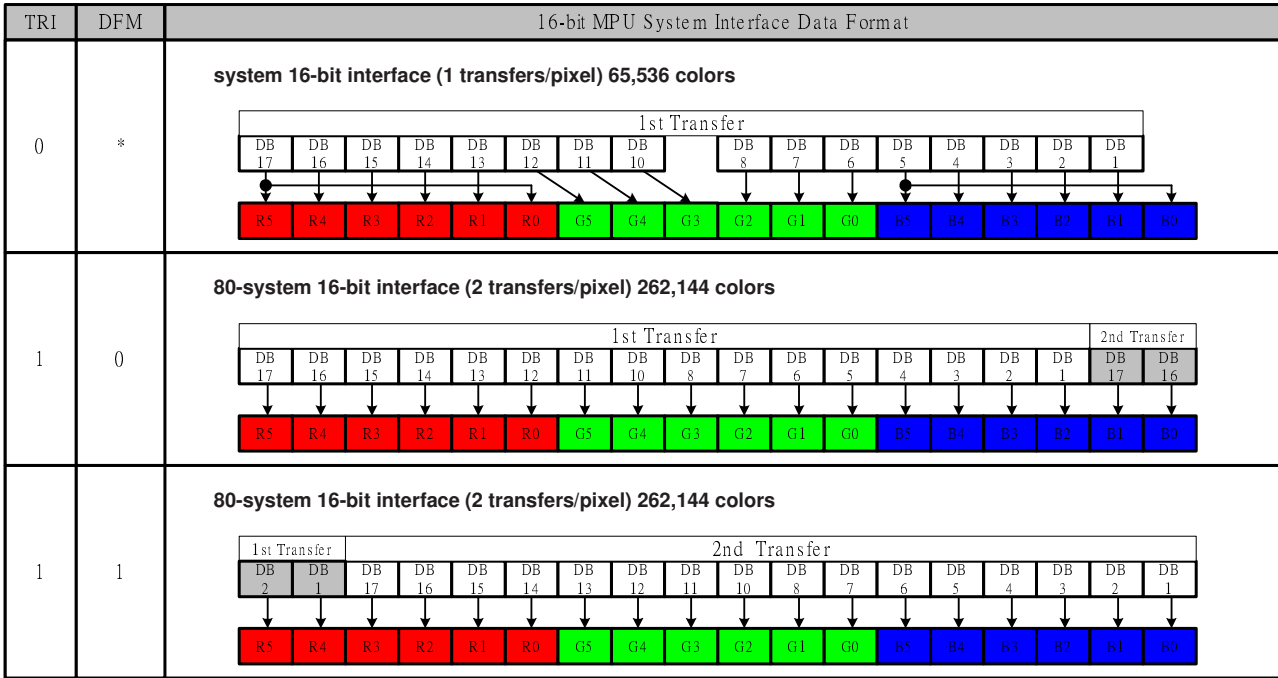


Figure3 16-bit System Interface Data Format

7.2.3. i80/9-bit System Interface

The i80/9-bit system interface is selected by setting the IM[3:0] as “1011” and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to GND.

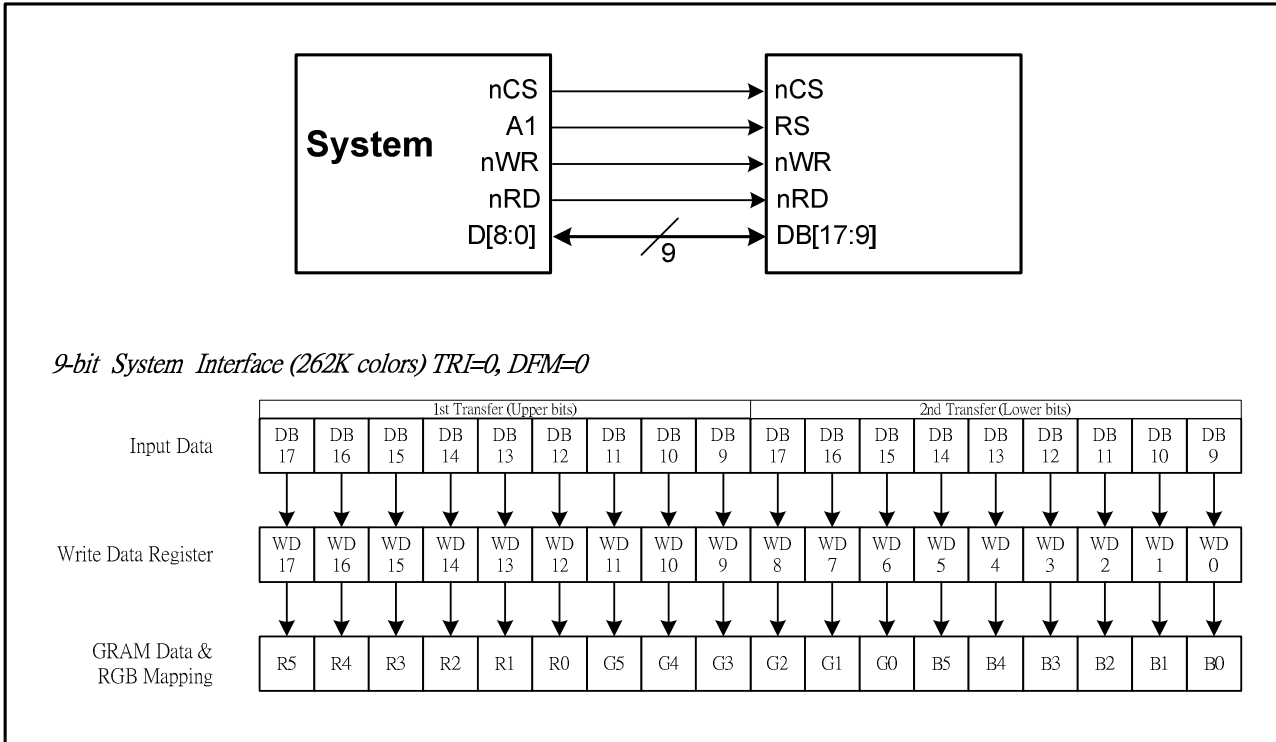


Figure4 9-bit System Interface Data Format

7.2.4. i80/8-bit System Interface

The i80/8-bit system interface is selected by setting the IM[3:0] as “0011” and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to GND.

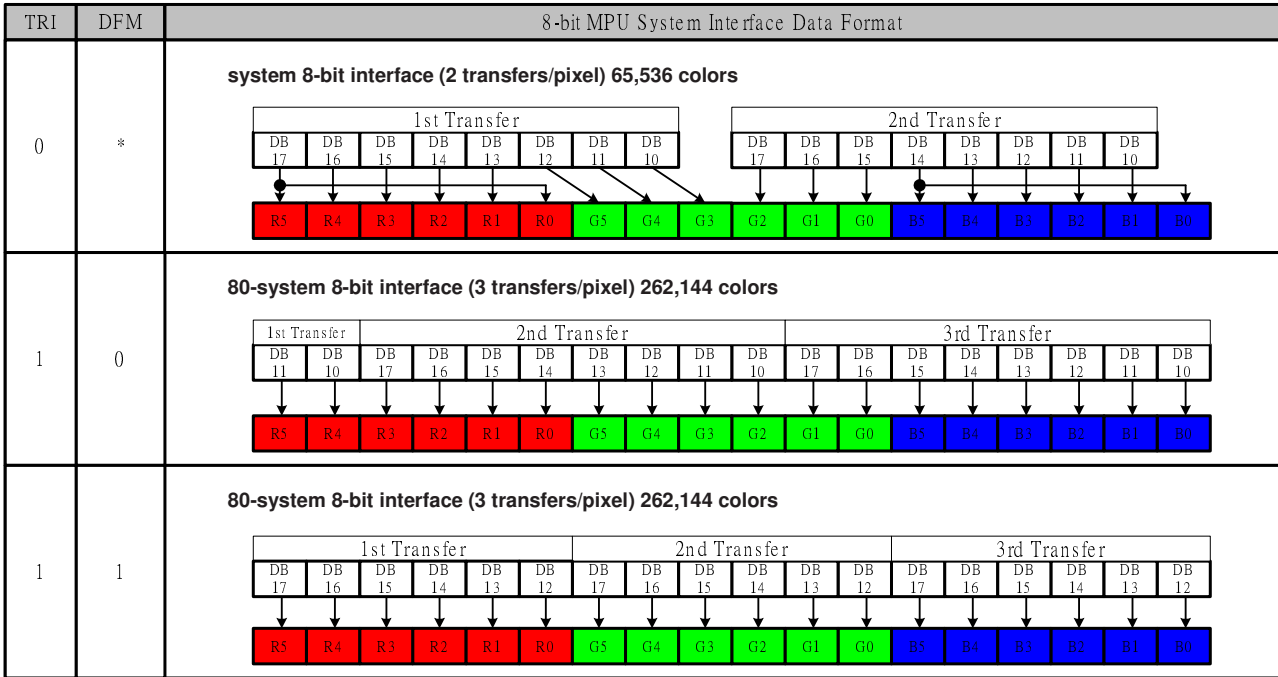


Figure5 8-bit System Interface Data Format

7.3. Serial Peripheral Interface (SPI)

7.3.1. 24-bit 4 wires Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “010x” level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9325C.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, ILI9325C starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9325C are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin.

RS and R/W Bit Function

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

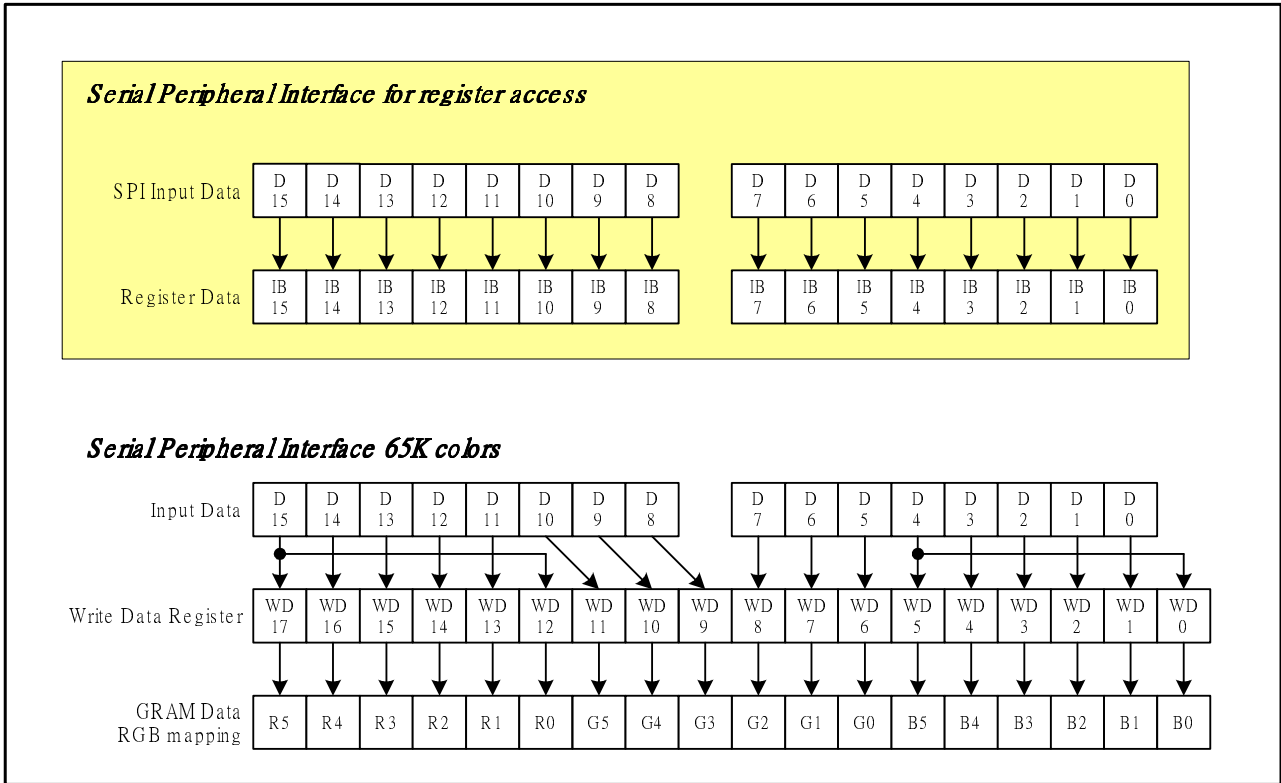


Figure 6 Data Format of SPI Interface

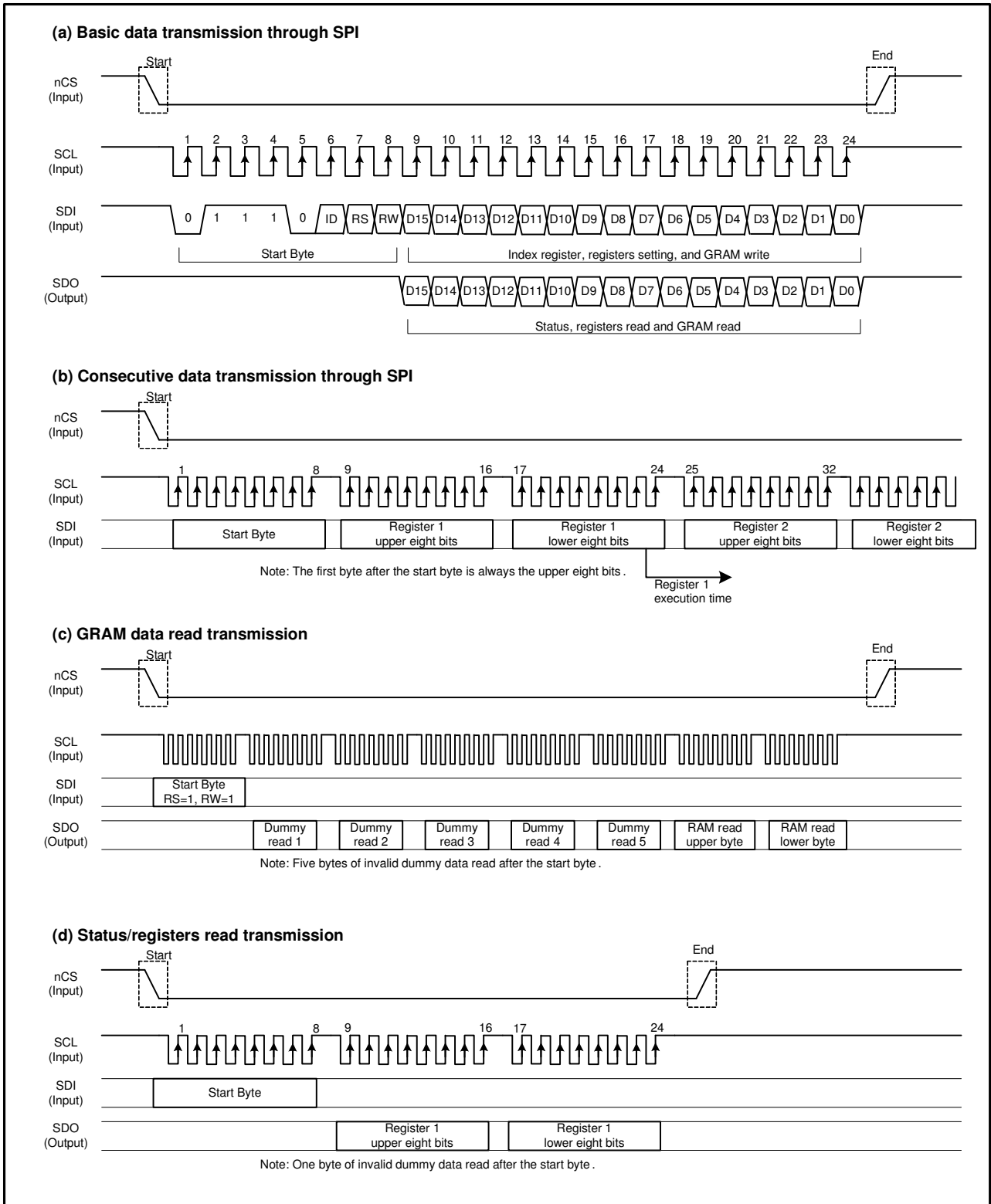


Figure7 Data transmission through serial peripheral interface (SPI)

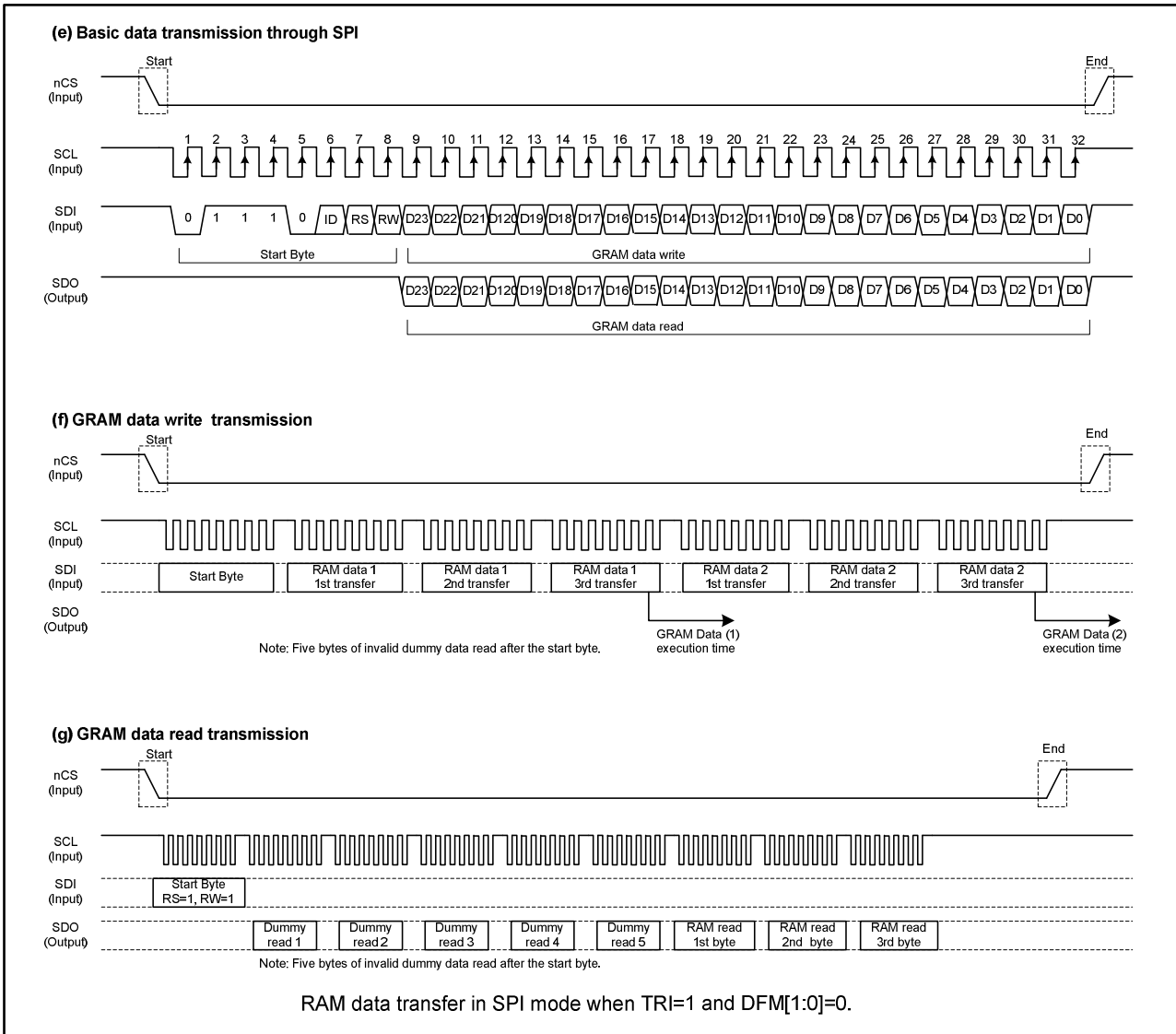


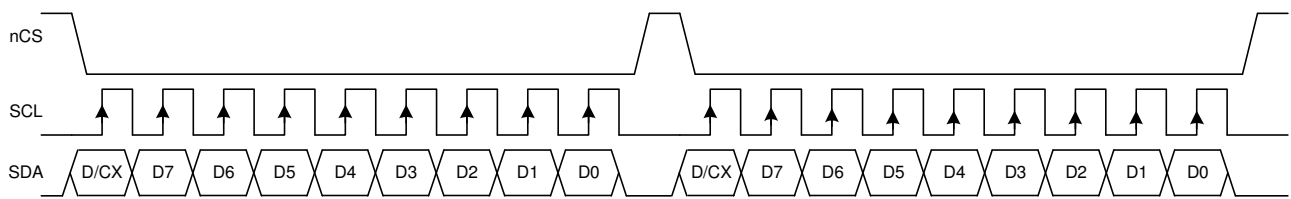
Figure8 Data transmission through serial peripheral interface (SPI), TRI="1" and DFM="0"

7.3.2. 3-wire 9-bit Serial Interface

This SPI mode uses a 3-wire 9-bit serial interface. The chip-select **nCS** (active low) enables and disables the serial interface. **SCL** is the serial data clock and **SDA** is serial data.

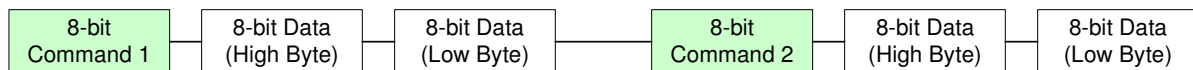
Serial data must be input to **SDA** in the sequence D/CX, D7 to D0. The ILI9325C reads the data at the rising edge of **SCL** signal. The first bit of serial data D/CX is data/command flag. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

Register Write Mode:



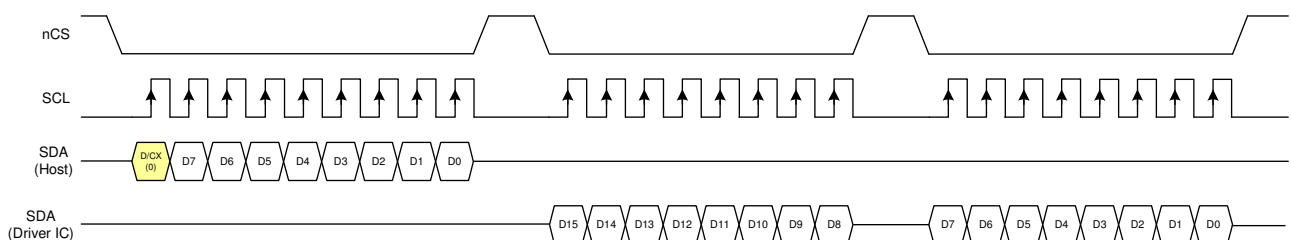
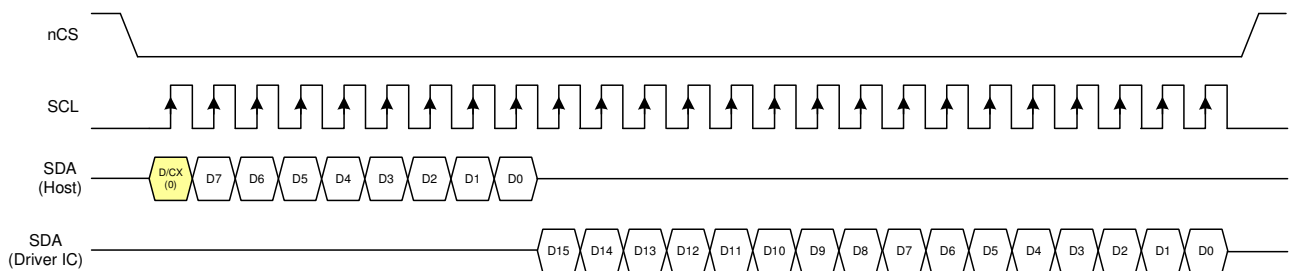
D/CX=0: Register Index (command).

D/CX: register data or GRAM data.

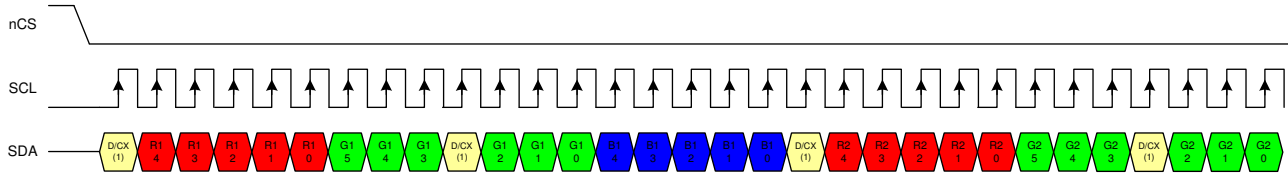


Register Read Mode:

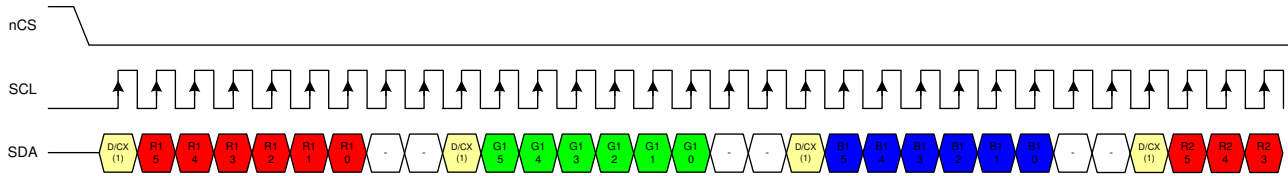
When users need to read back the register or GRAM data, **the register R66h must be set as "1" first**, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.



Serial Data Transfer Interface (65K colors)



Serial Data Transfer Interface (262K colors)

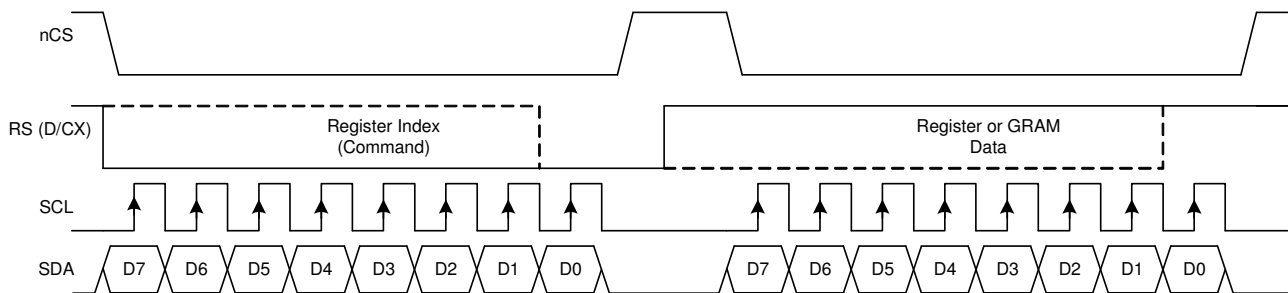


7.3.3. 4-wire 8-bit Serial Interface

This SPI mode uses a 4-wire 8-bit serial interface. The chip-select **nCS** (active low) enables and disables the serial interface. **D/CX** is the command or data select signal, **SCL** is the serial data clock and **SDA** is serial data.

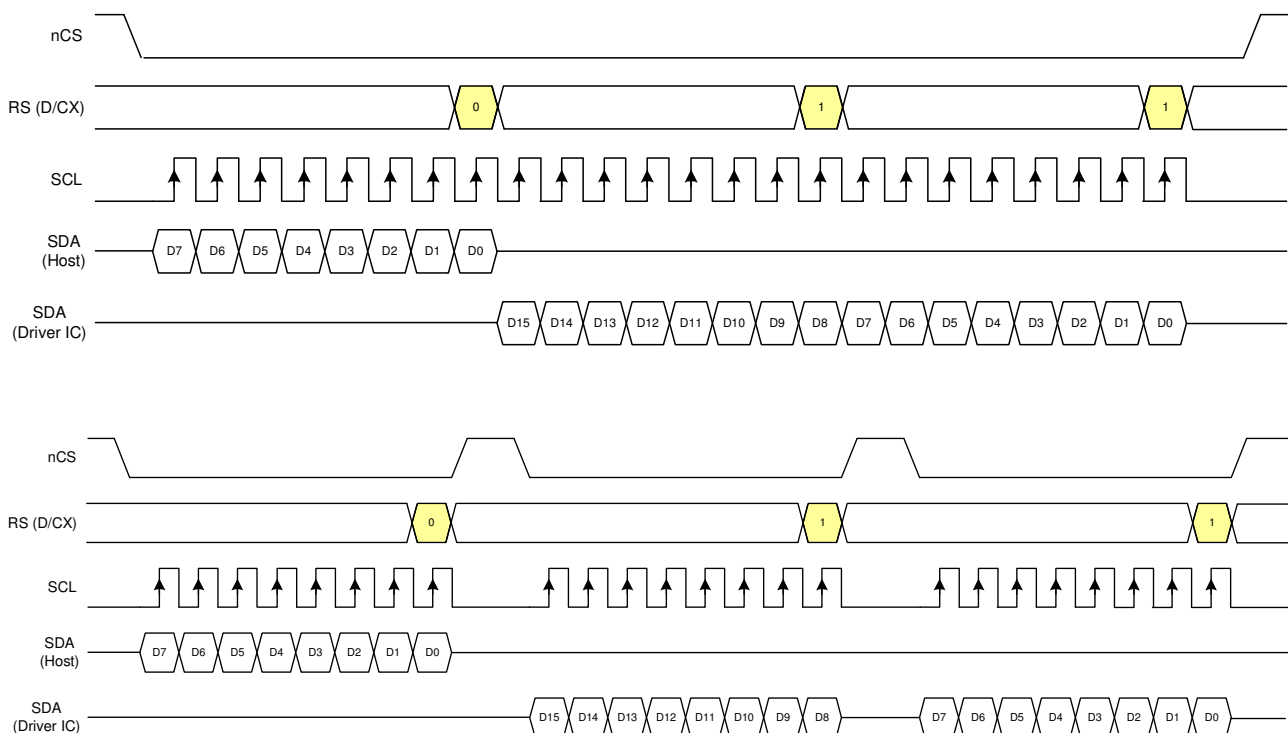
Serial data must be input to **SDA** in the sequence D7 to D0. The ILI9325C reads the data at the rising edge of **SCL** signal. The **D/CX** signal indicates data/command. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

Register Write Mode:

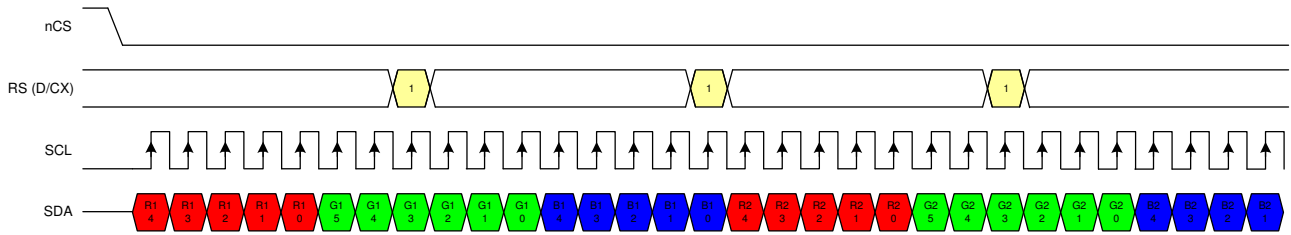


Register Read Mode:

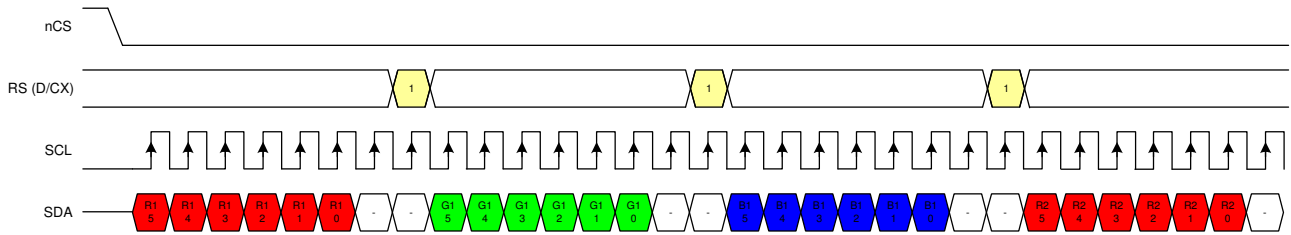
When users need to read back the register or GRAM data, the register R66h must be set as "1" first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.



Serial Data Transfer Interface (65K colors)



Serial Data Transfer Interface (262K colors)



7.4. VSYNC Interface

ILI9325C supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the i80 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

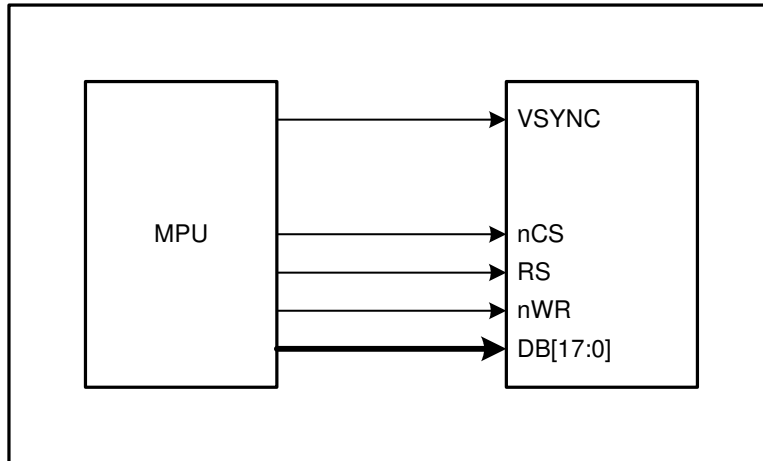


Figure9 Data transmission through VSYNC interface)

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

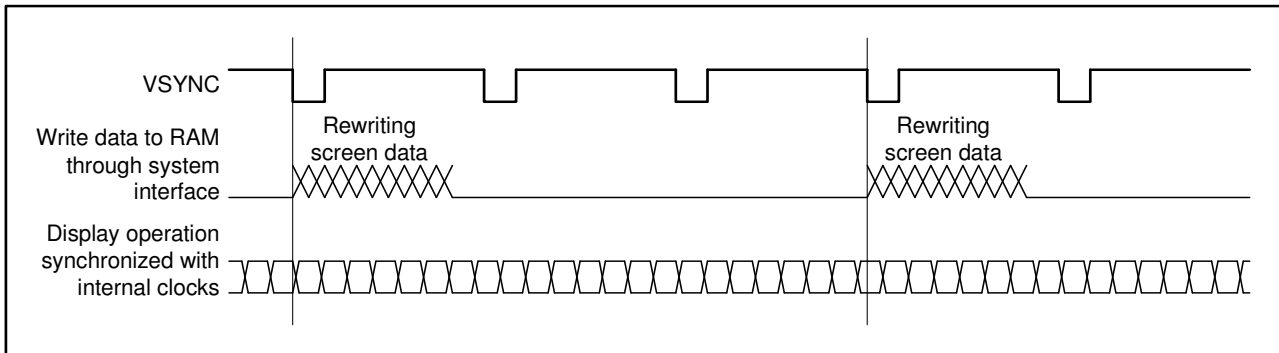


Figure10 Moving picture data transmission through VSYNC interface

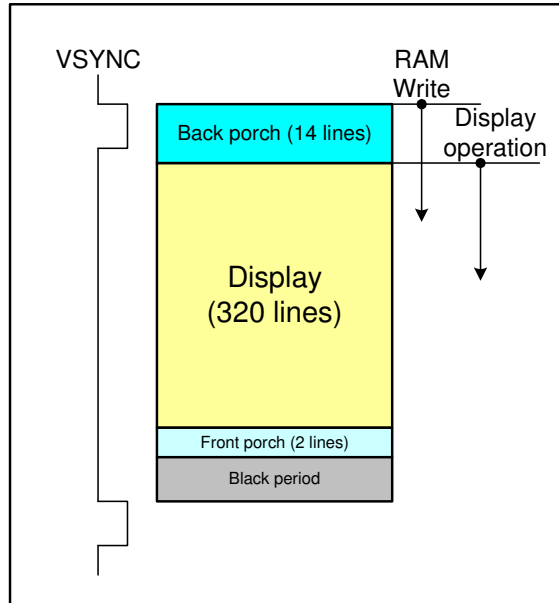


Figure11 Operation through VSYNC Interface

The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (FP) + BackPorch (BP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\text{Minimum RAM write speed (HZ)} > \frac{240 \times \text{DisplayLines (NL)}}{[(\text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times 16 \text{ (clocks)} \times 1/\text{fosc}]}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

- Display size: 240 RGB x 320 lines
- Lines: 320 lines (NL = 1000111)
- Back porch: 14 lines (BP = 1110)
- Front porch: 2 lines (FP = 0010)
- Frame frequency: 60 Hz
- Frequency fluctuation: 10%

$$\text{Internal oscillator clock (fosc.) [Hz]} = 60 \times [320 + 2 + 14] \times 16 \text{ clocks} \times (1.1/0.9) \doteq 394\text{KHz}$$

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When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with $\pm 10\%$ margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

$$\text{Minimum speed for RAM writing [Hz]} > 240 \times 320 \times 394K / [(14 + 320 - 2)\text{lines} \times 16\text{clocks}] \doteq 5.7 \text{ MHz}$$

The above theoretical value is calculated based on the premise that the ILI9325C starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the ILI9325C starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.

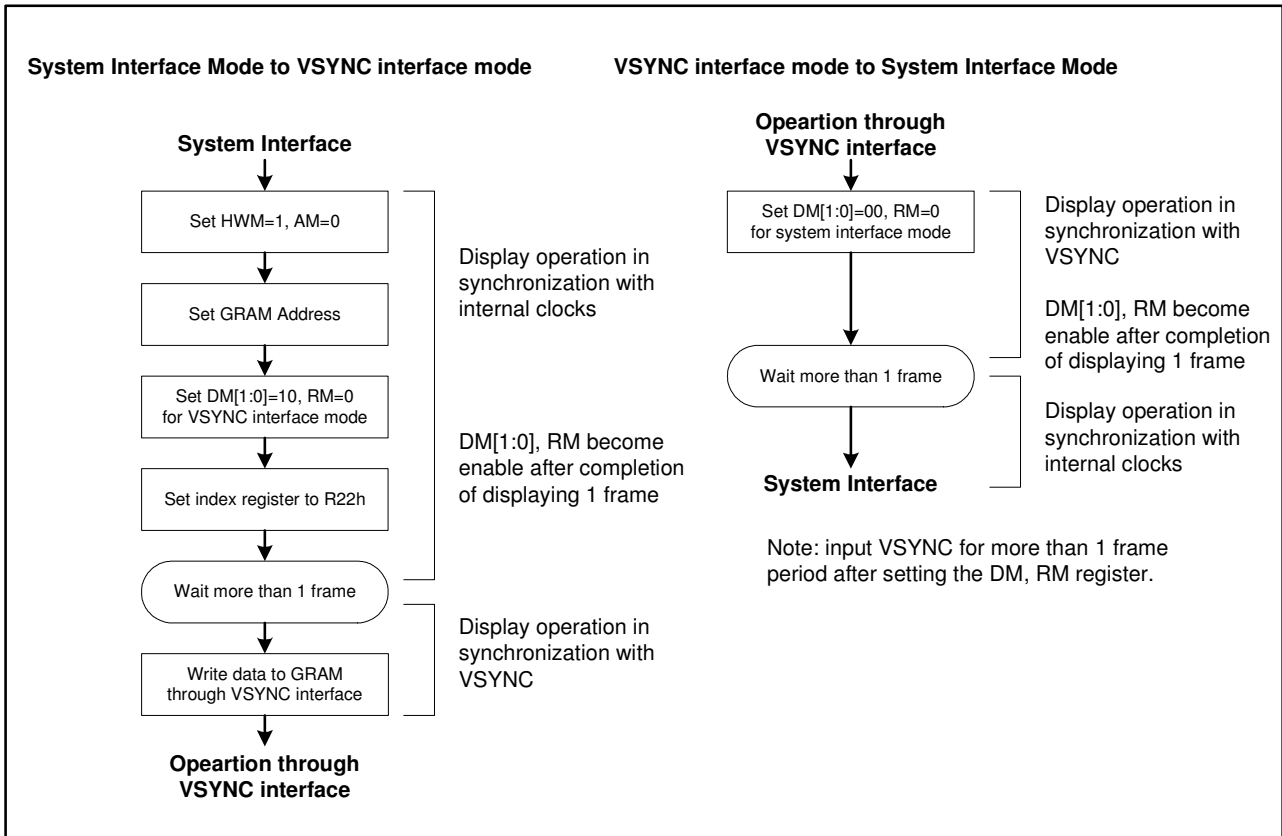


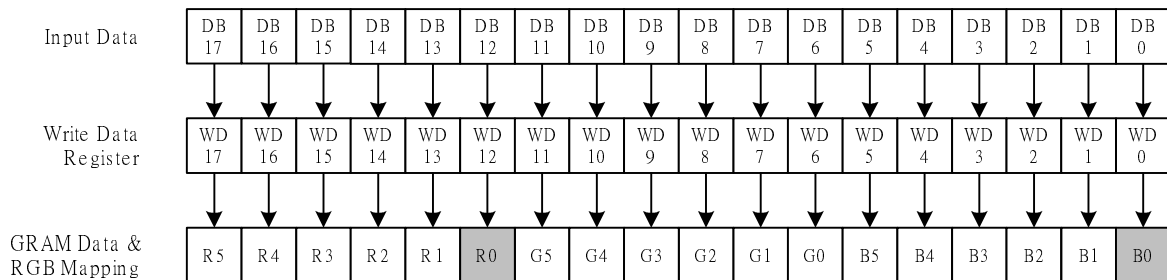
Figure12 Transition flow between VSYNC and internal clock operation modes

7.5. RGB Input Interface

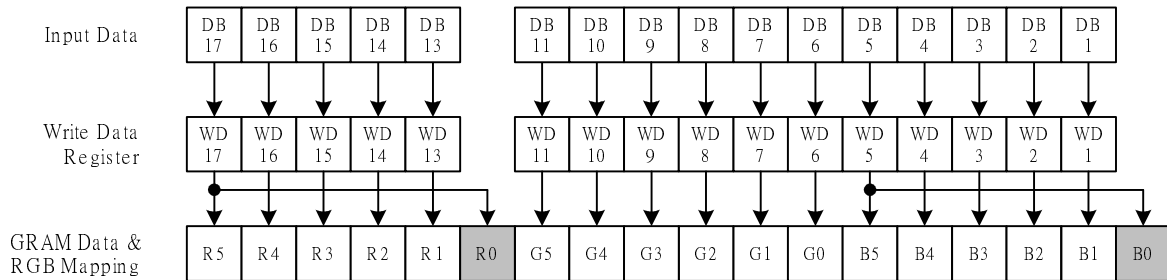
The RGB Interface mode is available for ILI9325C and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

18-bit RGB Interface (262K colors)



16-bit RGB Interface (65K colors)



6-bit RGB Interface (262K colors)

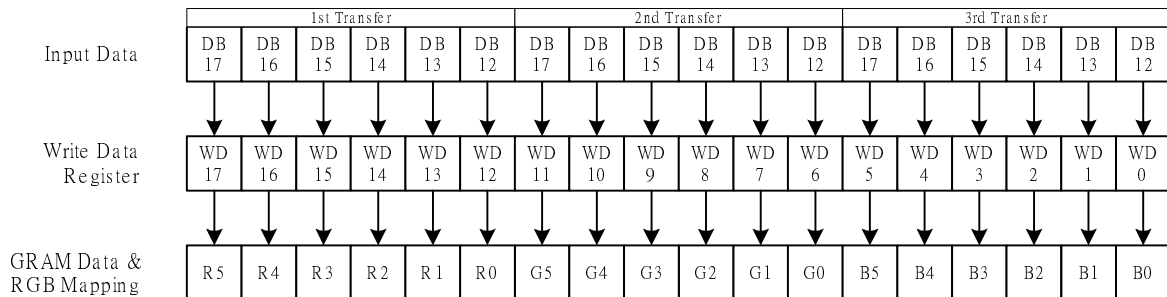


Figure13 RGB Interface Data Format

7.5.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

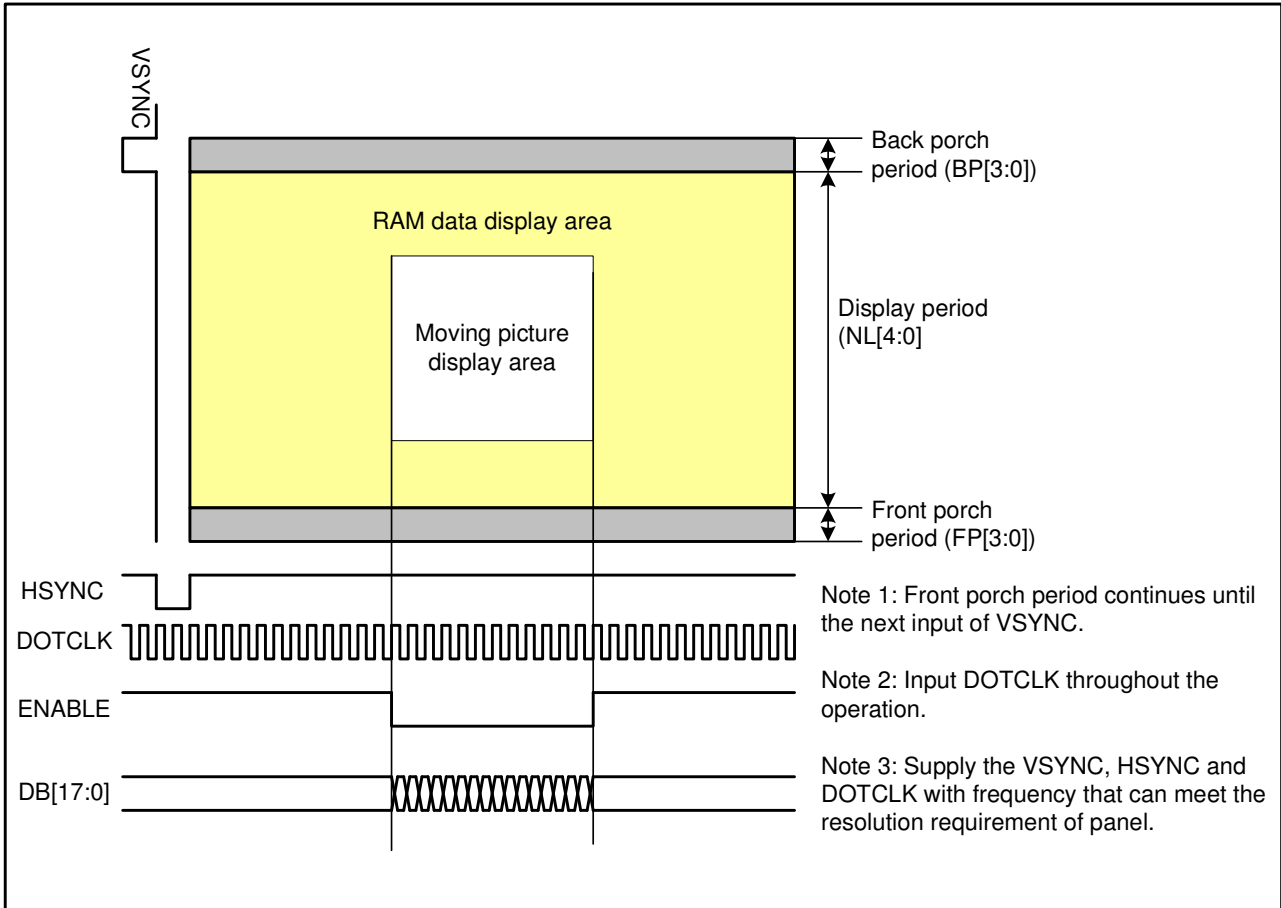


Figure14 GRAM Access Area by RGB Interface

7.5.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.

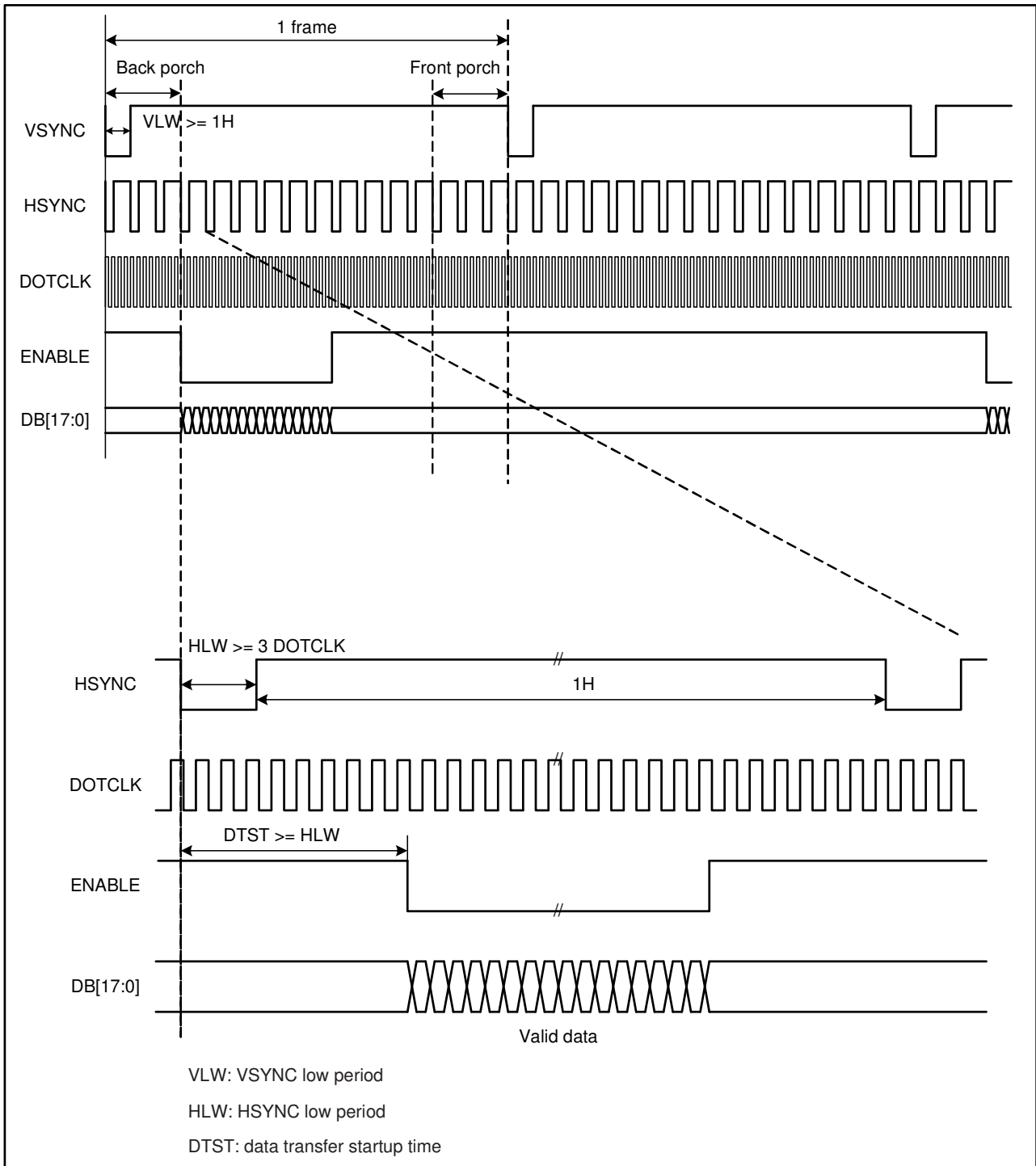


Figure15 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as follows.

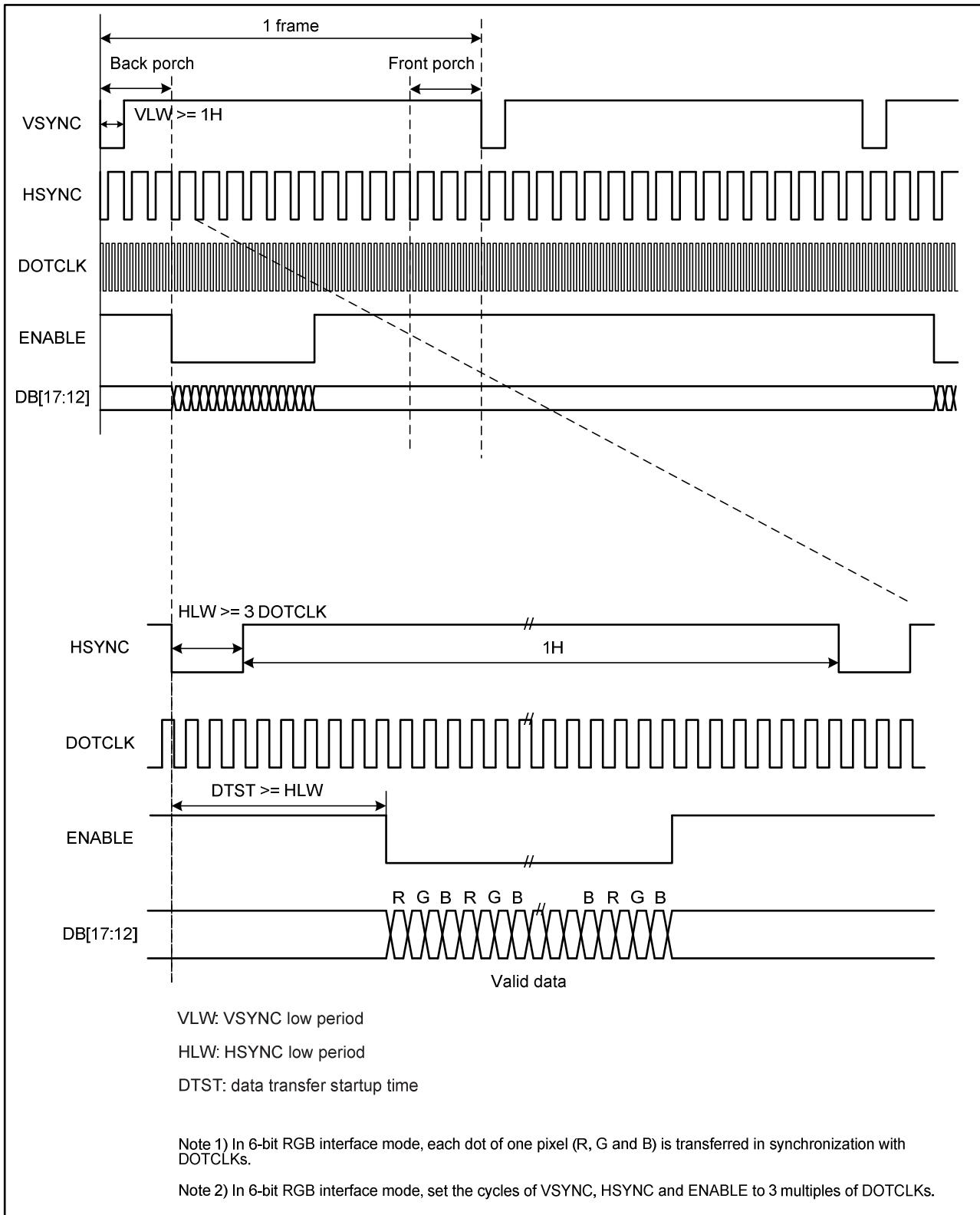


Figure16 Timing chart of signals in 6-bit RGB interface mode

7.5.3. Moving Picture Mode

ILI9325C has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

ILI9325C allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the ILI9325C when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

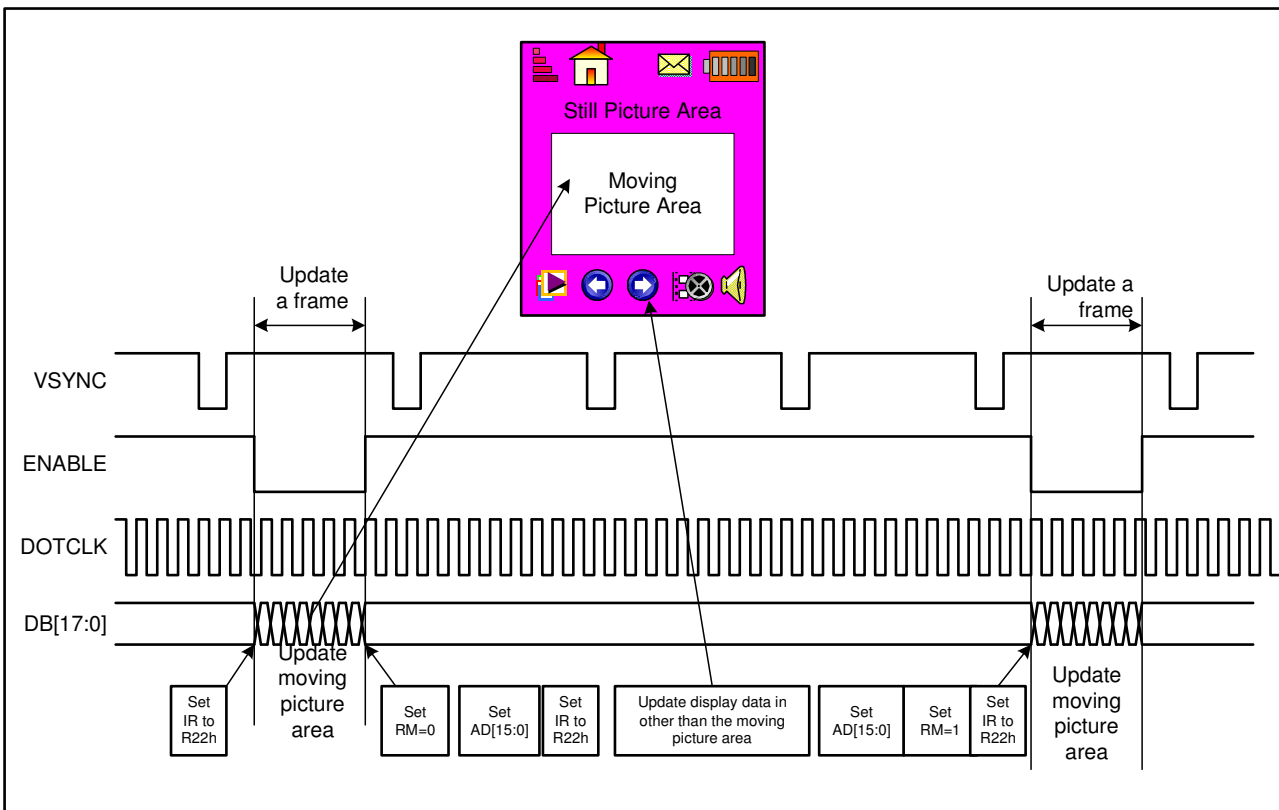
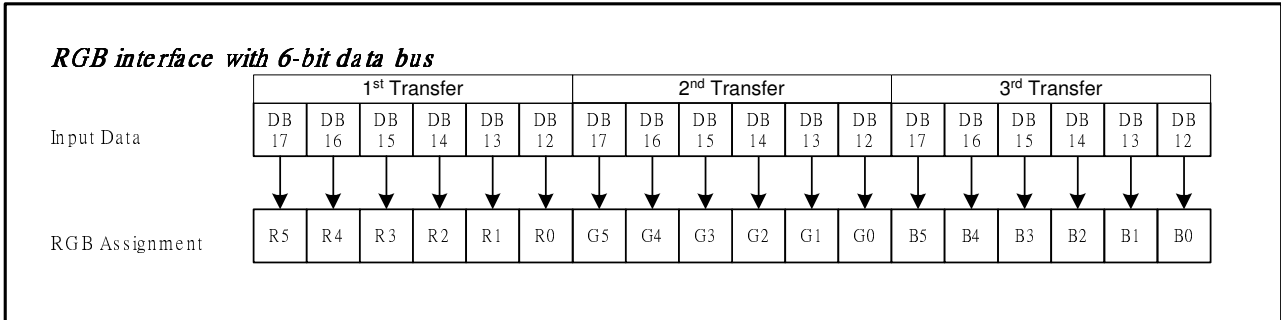


Figure17 Example of update the still and moving picture

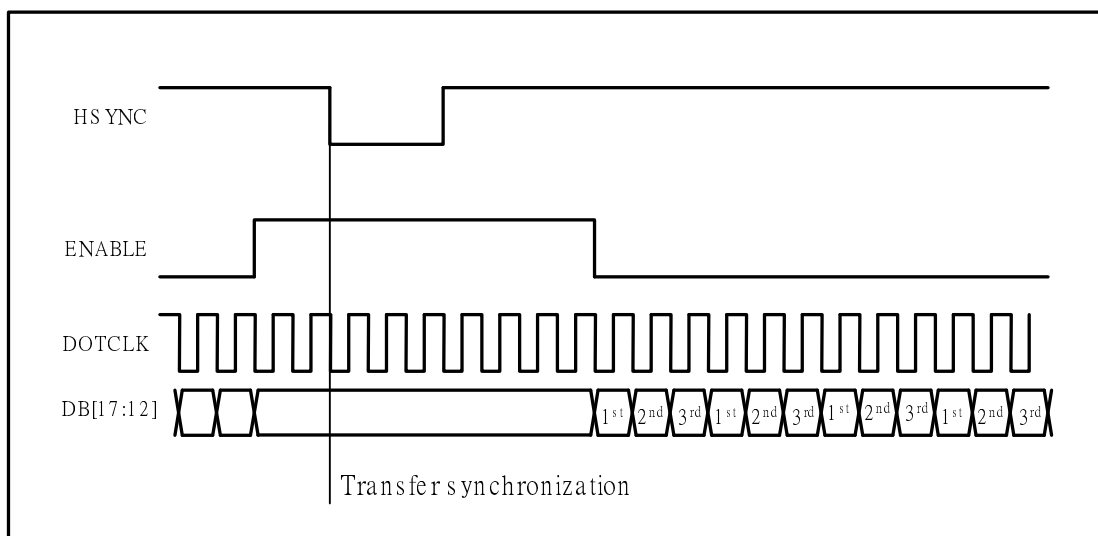
7.5.4. 6-bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at GND level. Registers can be set by the system interface (i80/SPI).



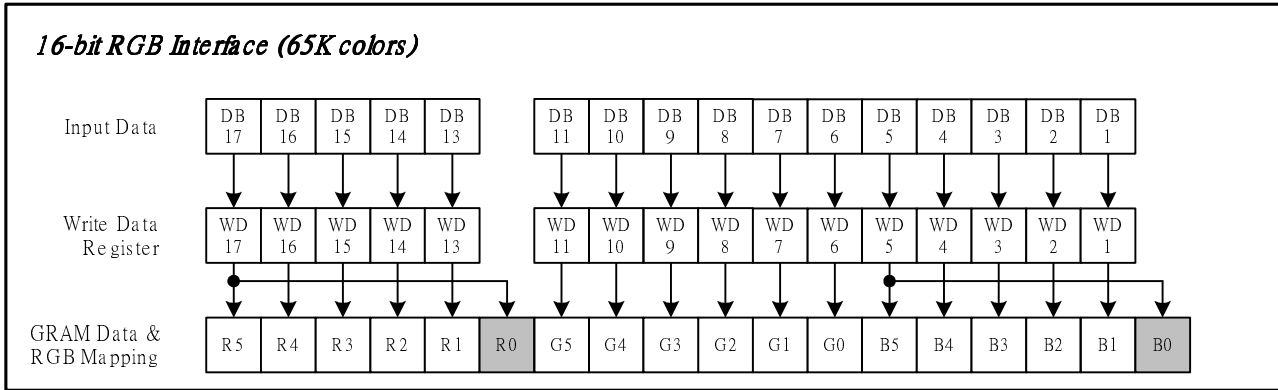
Data transfer synchronization in 6-bit RGB interface mode

ILI9325C has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state. Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



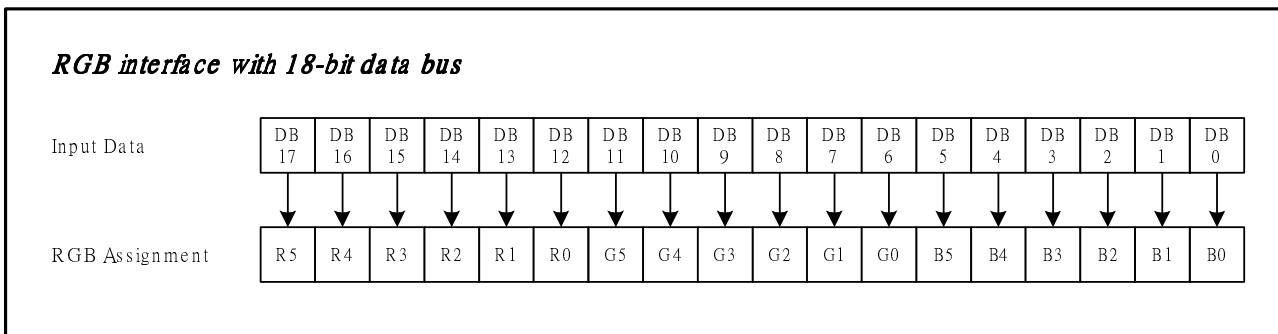
7.5.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



7.5.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB interface	I80 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in

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- RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
 5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
 6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
 7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
 8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

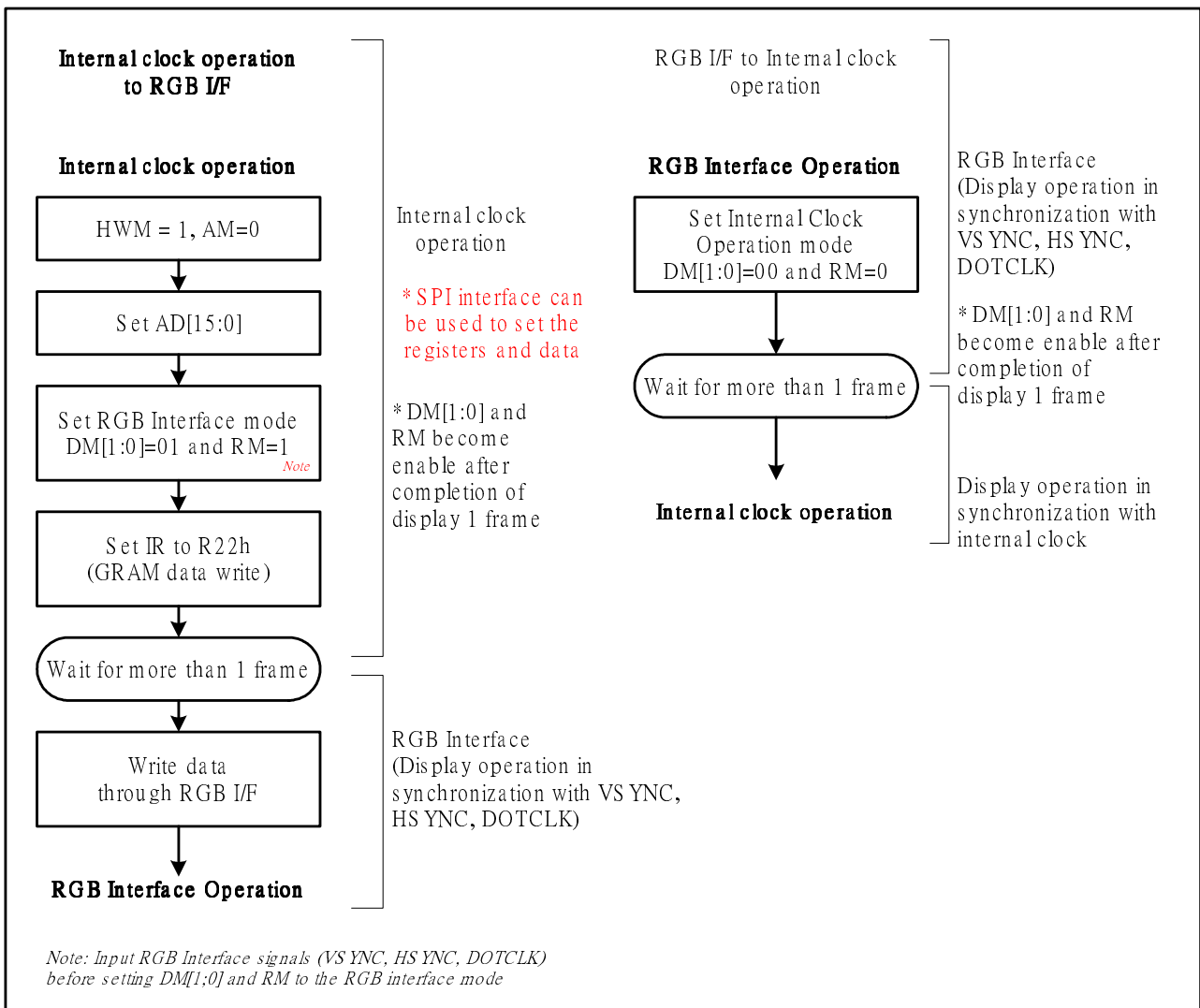


Figure18 Internal clock operation/RGB interface mode switching

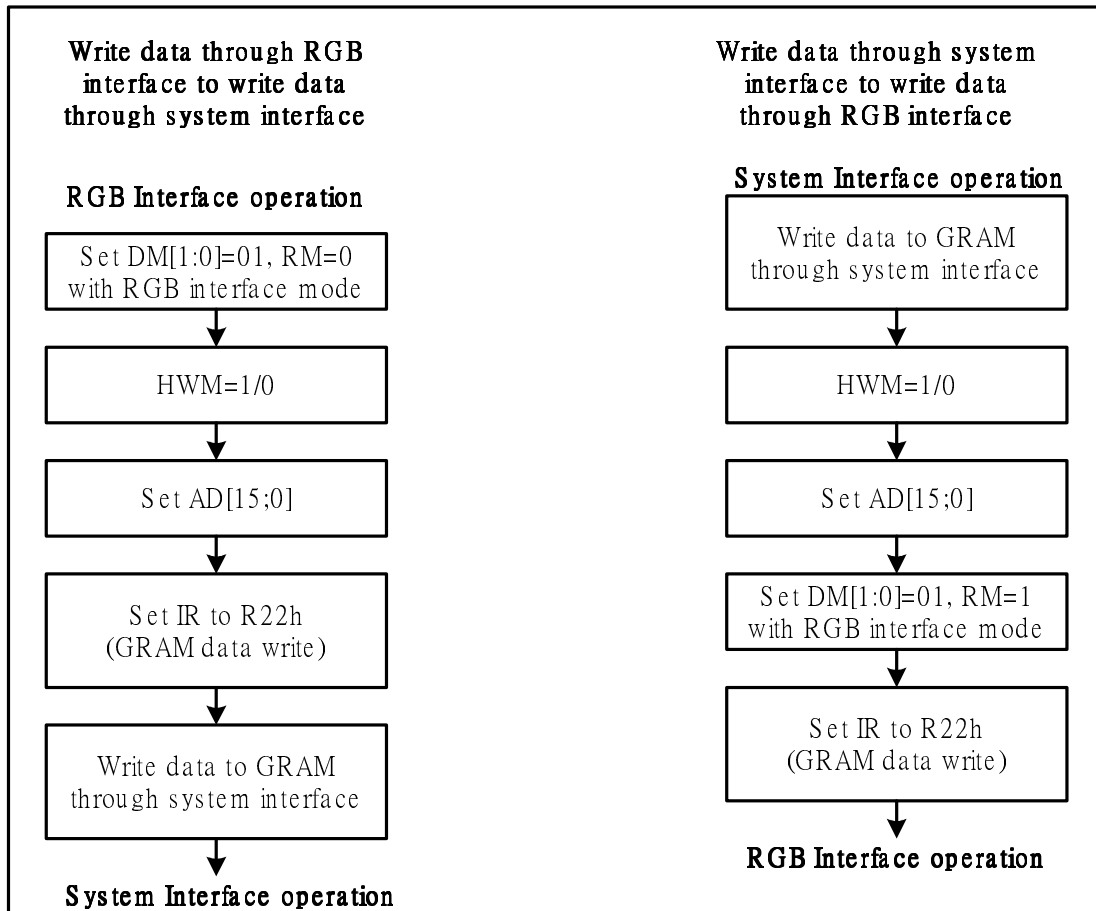


Figure19 GRAM access between system interface and RGB interface

Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

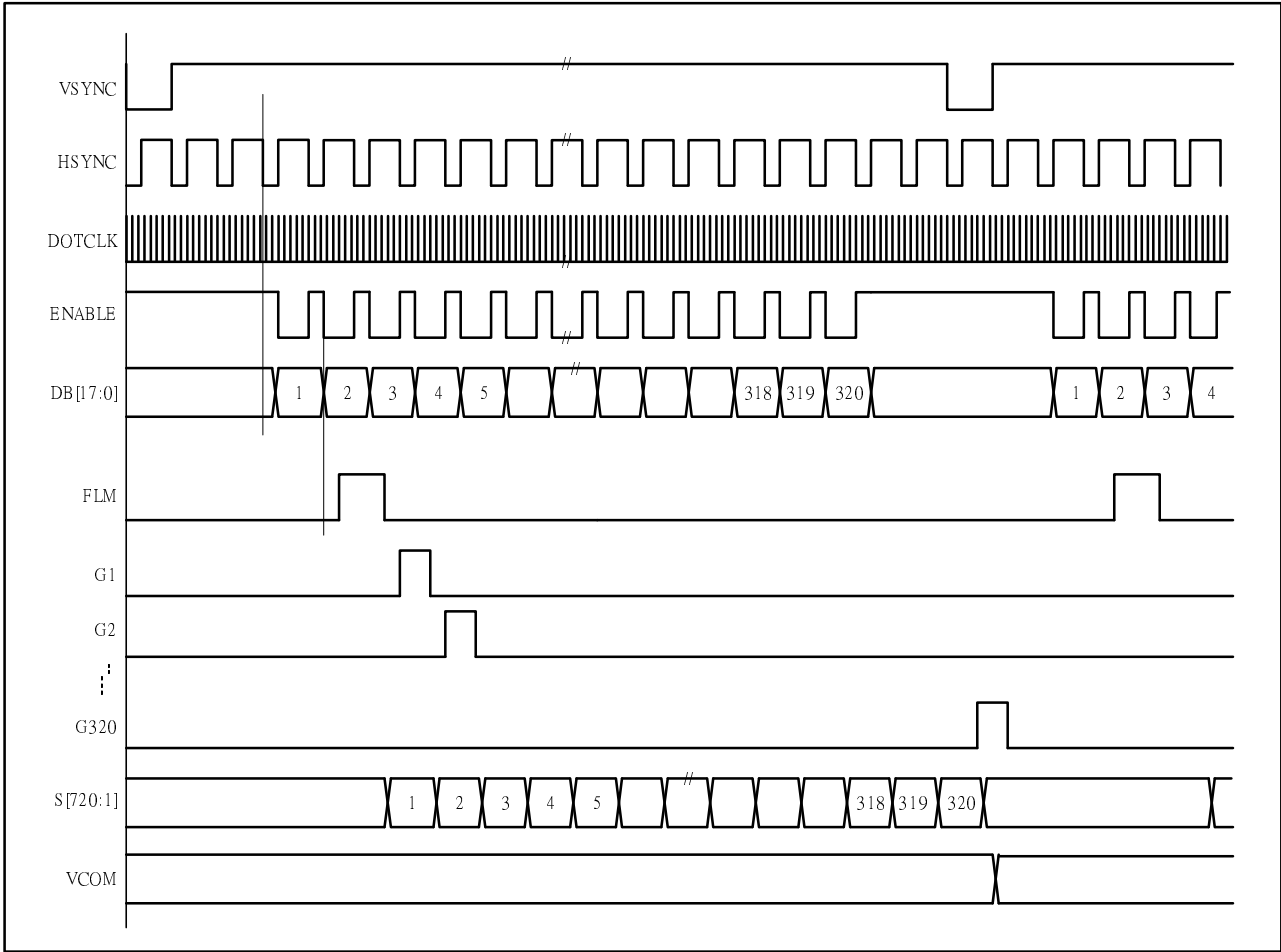


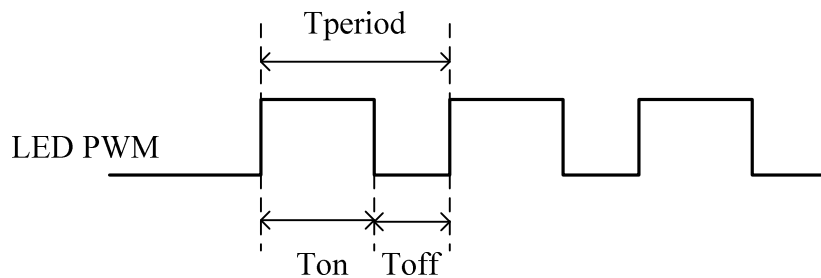
Figure20 Relationship between RGB I/F signals and LCD Driving Signals for Panel

7.6. CABC (Content Adaptive Brightness Control)

ILI9325C provide a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce

the power consumption of the luminance source. ILI9325C will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.

LIL9325C can calculate the backlight brightness level and send a PWM pulse to LED driver via LEDPWM pin for backlight brightness control purpose. The figure in the following is the basic timing diagram which is applied ILI9325C to control LED driver.



The period T_{period} of PWM pulse can be changed by the PWM_DIV[7:0] bits of the command “PWM_DIV (F2h)”. The LED-on time T_{on} and the LED-off time T_{off} are decided by the backlight brightness level which is calculated with CABC in ILI9325C. If CABC is off, then LEDPWM will forced to “H” level.

The PWM period value will be calculated via the equation as below.

$$f_{PWM_OUT} = \frac{5.8MHz}{(PWM_DIV[7:0]+1) \times 255}$$

8. Register Descriptions

8.1. Registers Access

ILI9325C adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9325C starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9325C. The registers of the ILI9325C are categorized into the following groups.

1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale γ -correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9325C can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

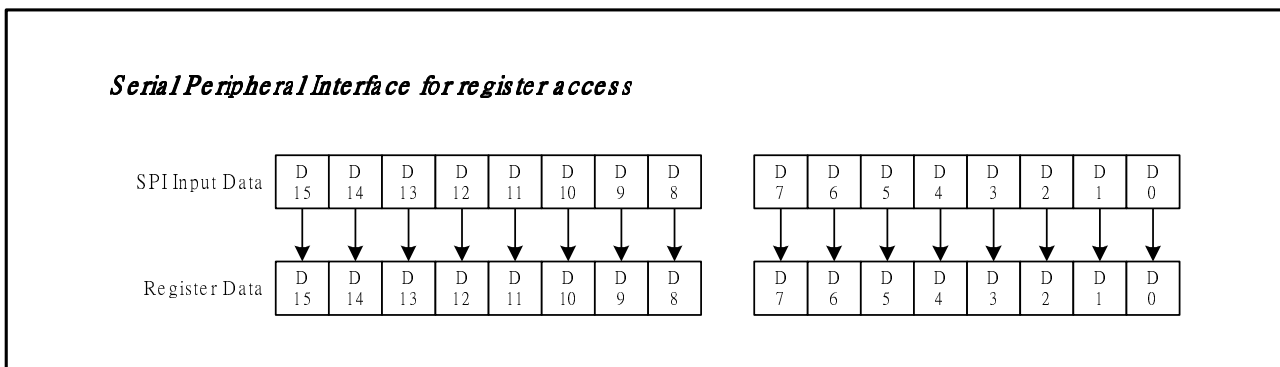
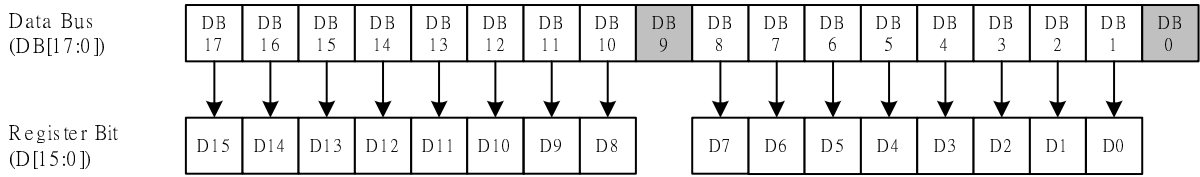
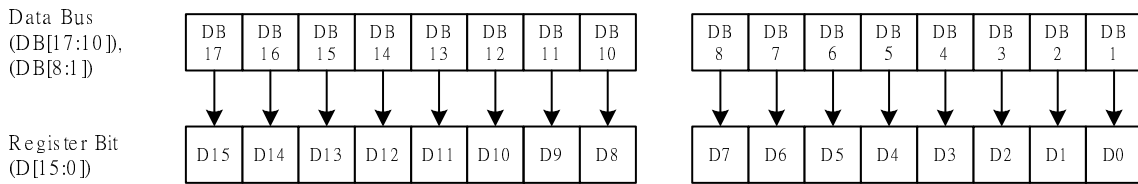


Figure21 Register Setting with Serial Peripheral Interface (SPI)

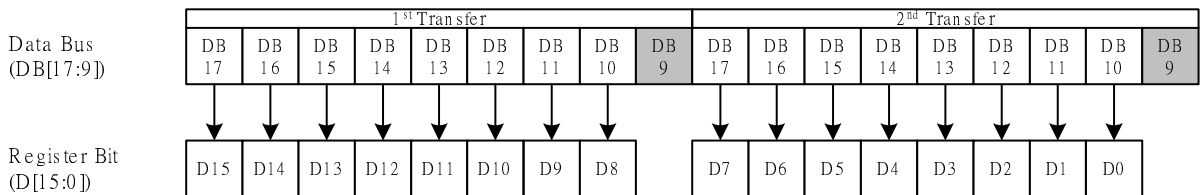
i80/M68 system 18-bit data bus interface



i80/M68 system 16-bit data bus interface



i80/M68 system 9-bit data bus interface



i80/M68 system 8-bit data bus interface/Serial peripheral interface (2/3 transmission)

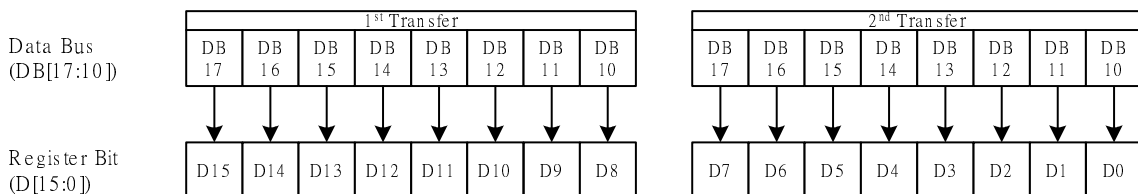


Figure22 Register setting with i80 System Interface

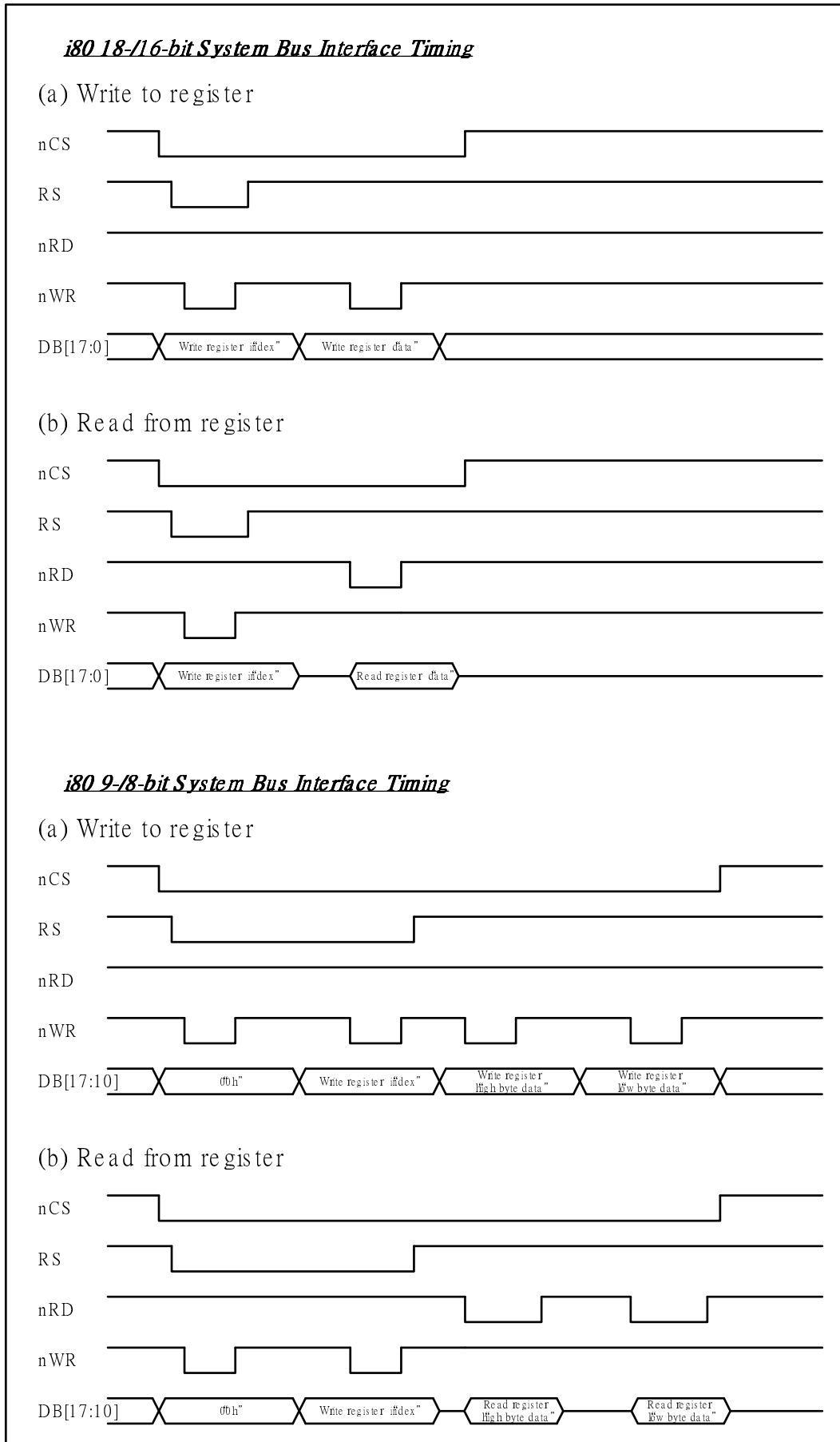


Figure 23 Register Read/Write Timing of i80 System Interface

8.2. Instruction Descriptions

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
05h	16 bits data format control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS[3]	FRS[2]	FRS[1]	FRS[0]
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV	
66h	SPI Read/Write Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX (0)	
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00	
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00	
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00	
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10	
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10	
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10	
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIV11	DIV10	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOW12	NOW11	NOW10	0	0	0	0	0	0	0	0	
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0	
97h	Panel Interface Control 5	W	1	0	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	
A1h	OTP VCM Programming Control	W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0	
A2h	OTP VCM Status and Enable	W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN	
A5h	OTP Programming ID Key	W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0	
B1h	Write Display Brightness	W	1	X	X	X	X	X	X	X	X	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
B2h	Read Display Brightness	R	1	X	X	X	X	X	X	X	X	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
B3h	Write CTRL Display value	W	1	X	X	X	X	X	X	X	X	X	X	BCTRL	X	DD	BL	X	X	
B4h	Read CTRL Display value	R	1	X	X	X	X	X	X	X	X	X	X	BCTRL	X	DD	BL	X	X	
B5h	Write Content Adaptive Brightness Control value	W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	C[1:0]		
B6h	Read Content Adaptive Brightness Control value	R	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	C[1:0]		
BEh	Write CABC Minimum Brightness	W	1	X	X	X	X	X	X	X	X	CMB[7:0]								

No.	Registers Name	R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BFh	Read CABC Minimum Brightness	R	1		X	X	X	X	X	X	X	X	CMB[7:0]							
C8h	CABC Control 1	W	1		X	X	X	X	X	X	X	X	PWM_DIV[7:0]							
C9h	CABC Control 2	W	1		X	X	X	X	X	X	X	X	THRES_MOV[3:0]				THRES_STILL[3:0]			
CAh	CABC Control 3	W	1		X	X	X	X	X	X	X	X	0	0	0	0	THRES_UI[3:0]			
CBh	CABC Control 4	W	1		X	X	X	X	X	X	X	X	DTH_MOV[3:0]				DTH_STILL[3:0]			
CCh	CABC Control 5	W	1		X	X	X	X	X	X	X	X	0	0	0	0	DTH_UI[3:0]			
CDh	CABC Control 6	W	1		X	X	X	X	X	X	X	X	DIM_OPT2[3:0]				0	DIM_OPT1[2:0]		
CEh	CABC Control 7	W	1		X	X	X	X	X	X	X	SCD_VLINE[8:0]								

8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ RFFh) or RAM which will be accessed.

8.2.2. ID code (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RO	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1

The device code "9325C" is read out when read this register.

8.2.3. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Select the shift direction of outputs from the source driver.

When SS = 0, the shift direction of outputs is from S1 to S720

When SS = 1, the shift direction of outputs is from S720 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

When changing SS or BGR bits, RAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		<p>G1, G2, G3, G4, ...,G316 G317, G318, G319, G320</p>
0	1		<p>G320, G319, G318, ..., G6, G5, G4, G3, G2, G1</p>
1	0		<p>G1, G3, G5, G7, ...,G311 G313, G315, G317, G319 G2, G4, G6, G8, ...,G312 G314, G316, G318, G320</p>
1	1		<p>G320, G318, G316, ..., G10, G8, G6, G4, G2 G319, G317, G315, ..., G9, G78, G5, G3, G1</p>

8.2.4. LCD Driving Wave Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

.B/C 0 : Frame/Field inversion
1 : Line inversion

8.2.5. Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM Control the GRAM update direction.

When AM = "0", the address is updated in horizontal writing direction.

When AM = "1", the address is updated in vertical writing direction.

When a window area is set by registers R50h ~R53h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.

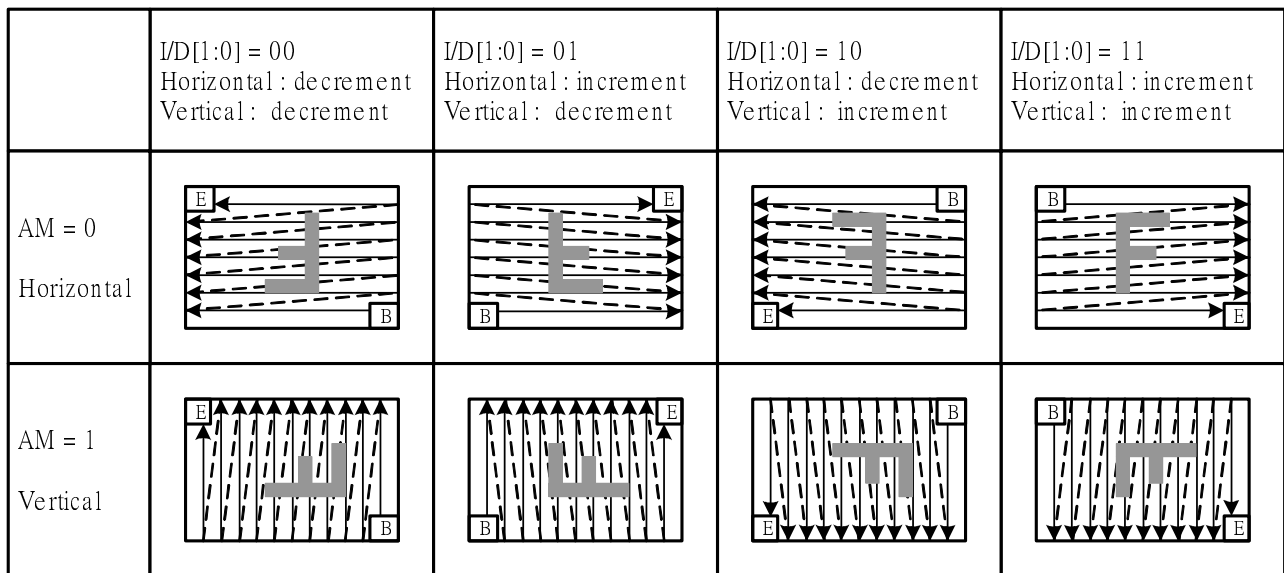


Figure24 GRAM Access Direction Setting

ORG Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = "0": The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.

ORG = "1": The original address "00000h" moves according to the I/D[1:0] setting.

Notes: 1. When ORG=1, only the origin address address"00000h" can be set in the RAM address set registers R20h, and R21h.

2. In RAM read operation, make sure to set ORG=0.

BGR Swap the R and B order of written data.

BGR="0": Follow the RGB order to write the pixel data.

BGR="1": Swap the RGB data to BGR in writing into GRAM.

TRI When TRI = "1", data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = "0".

DFM Set the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.

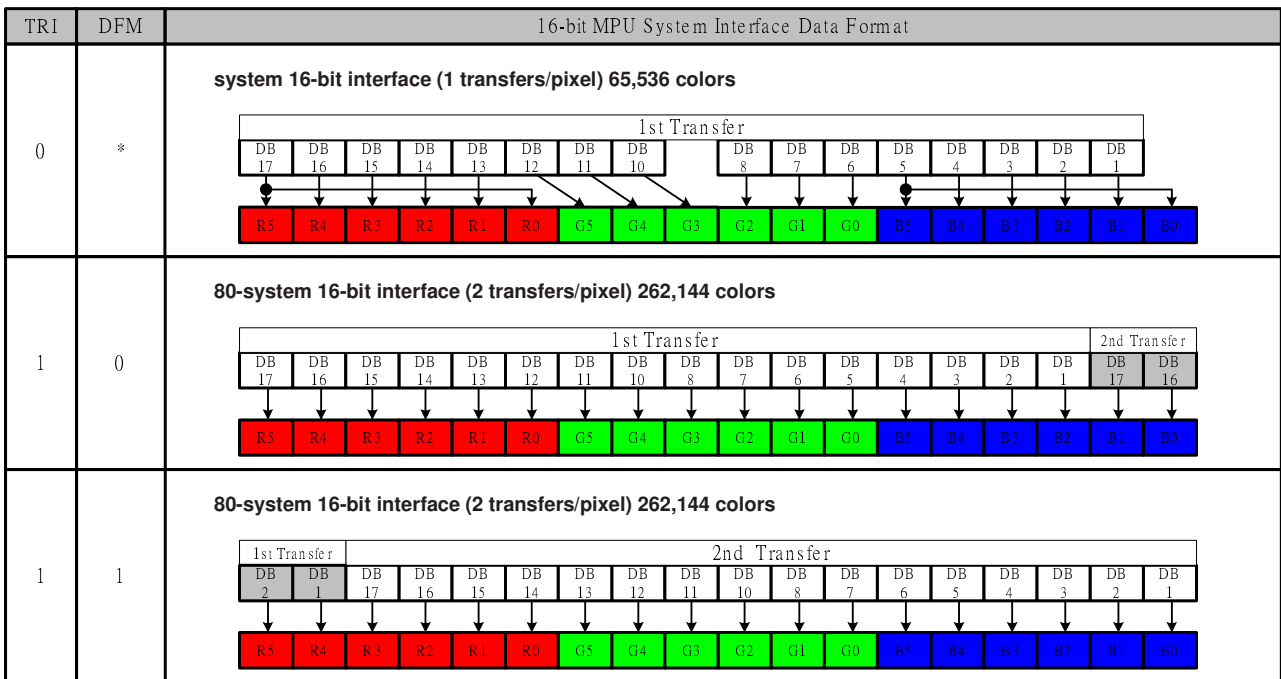


Figure25 16-bit MPU System Interface Data Format

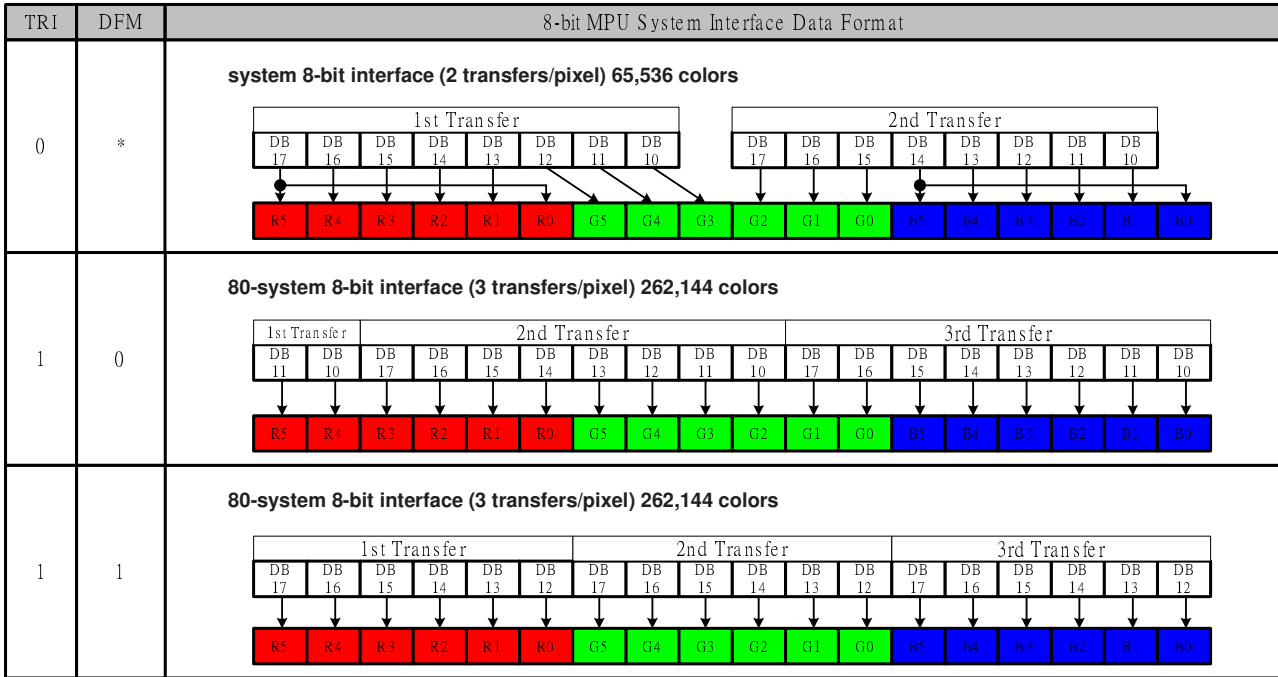
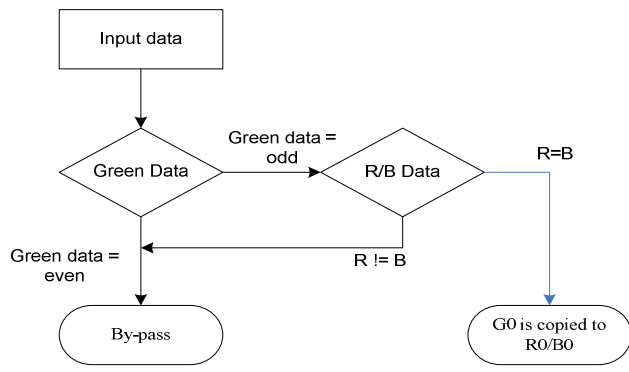
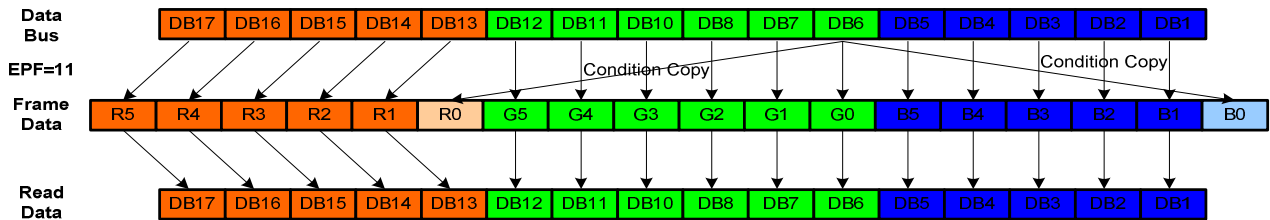
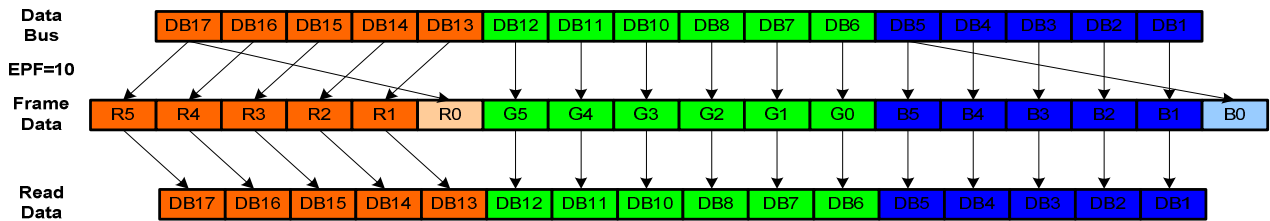
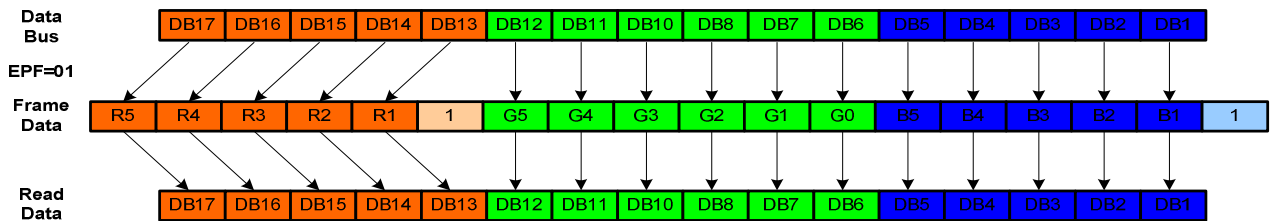
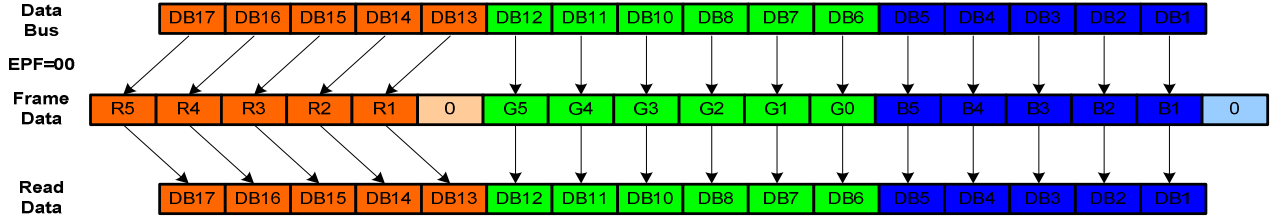


Figure26 8-bit MPU System Interface Data Format

8.2.6. 16bits Data Format Selection (R05h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FPF1	EPF0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



8.2.7. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0] Set D[1:0]="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0".

When writing D1 = "0", the graphics display data is retained in the internal GRAM and the ILI9325C displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1:0] = "01", the ILI9325C continues internal display operation. When the display is turned off by setting D[1:0] = "00", the ILI9325C internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D1	D0	BASEE	Source, VCOM Output	ILI9325C internal operation
0	0	0	GND	Halt
0	1	1	GND	Operate
1	0	0	Non-lit display	Operate
1	1	0	Non-lit display	Operate
1	1	1	Base image display	Operate

Note: 1. data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

2. The D[1:0] setting is valid on both 1st and 2nd displays.
3. The non-lit display level from the source output pins is determined by instruction (PTS).

CL When CL = "1", the 8-color display mode is selected.

CL	Colors
0	262,144
1	8

GON and DTE Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1 ~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal Display

BASEE

Base image display enable bit. When BASEE = "0", no base image is displayed. The ILI9325C drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed. The D[1:0] setting has higher priority over the BASEE setting.

PTDE[1:0]

Partial image 2 and Partial image 1 enable bits

PTDE1/0 = 0: turns off partial image. Only base image is displayed.

PTDE1/0 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

8.2.8. Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP[3:0]/BP[3:0]

The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively.

When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

$BP + FP \leq 16$ lines

$FP \geq 2$ lines

$BP \geq 2$ lines

Set the BP[3:0] and FP[3:0] bits as below for each operation modes

Operation Mode	BP	FP	BP+FP
I80 System Interface Operation Mode	$BP \geq 2$ lines	$FP \geq 2$ lines	$FP + BP \leq 16$ lines
RGB interface Operation	$BP \geq 2$ lines	$FP \geq 2$ lines	$FP + BP \leq 16$ lines
VSYNC interface Operation	$BP \geq 2$ lines	$FP \geq 2$ lines	$FP + BP = 16$ lines

FP[3:0]	Number of lines for Front Porch	<p>The diagram shows a rectangular display area. On the left side, a vertical line represents the VSYNC signal, which is high for a short duration and then low. The display area is divided into three horizontal sections: a yellow 'Back Porch' at the top, a white 'Display Area' in the middle, and a green 'Front Porch' at the bottom. The VSYNC signal is shown to be active during the back porch and front porch periods.</p>
BP[3:0]	Number of lines for Back Porch	
0000	Setting Prohibited	
0001	Setting Prohibited	
0010	2 lines	
0011	3 lines	
0100	4 lines	
0101	5 lines	
0110	6 lines	
0111	7 lines	
1000	8 lines	
1001	9 lines	
1010	10 lines	
1011	11 lines	
1100	12 lines	
1101	13 lines	
1110	14 lines	
1111	Setting Prohibited	

Note: The output timing to the LCD is delayed by 2 lines period from the input of synchronizing signal.

8.2.9. Display Control 3 (R09h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC[3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG[1:0]="10" to select interval scan. Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f _{FLM} =60 Hz
0	0	0	0	0 frame	-
0	0	0	1	0 frame	-
0	0	1	0	3 frame	50ms
0	0	1	1	5 frame	84ms
0	1	0	0	7 frame	117ms
0	1	0	1	9 frame	150ms
0	1	1	0	11 frame	184ms
0	1	1	1	13 frame	217ms
1	0	0	0	15 frame	251ms
1	0	0	1	17 frame	284ms
1	0	1	0	19 frame	317ms
1	0	1	1	21 frame	351ms
1	1	0	0	23 frame	384ms
1	1	0	1	25 frame	418ms
1	1	1	0	27 frame	451ms
1	1	1	1	29 frame	484ms

PTG[1:0] Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	0	Normal scan	Set with the PTS[1:0] bits	VcomH/VcomL
0	1	Setting Prohibited	-	-
1	0	Interval scan	Set with the PTS[1:0] bits	VcomH/VcomL
1	1	Setting Prohibited	-	-

PTS[1:0]

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

PTS[1:0]		SOURCE / VCOM output level in non-display area driver period
00	frame with gate scan	white
	frame without gate scan	V63 / VCOML
01	frame with gate scan	black
	frame without gate scan	V0 / VCOML
10	frame with gate scan	white
	frame without gate scan	GND / GND
11	frame with gate scan	white
	frame without gate scan	Hi-Z / Hi-Z

8.2.10. Display Control 4 (R0Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0] Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE When FMARKOE=1, ILI9325C starts to output FMARK signal in the output interval set by FMI[2:0] bits.

FMI[2:0]	Output Interval
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Setting disabled

8.2.11. RGB Display Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0] Select the RGB interface data width.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (1 transfer/pixel), DB[17:0]
0	1	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1]
1	0	6-bit RGB interface (3 transfers/pixel), DB[17:12]
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

DM[1:0] Select the display operation mode.

DM1	DM0	Display Interface
0	0	Internal system clock
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
----	--------------------------

0	System interface/VSYNC interface
1	RGB interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0])
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
Rewrite still picture area while RGB interface Displaying moving pictures.		System interface (RM = 0)	RGB interface (DM[1:0] = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1: Registers are set only via the system interface or SPI interface.

Note 2: Refer to the flowcharts of “RGB Input Interface” section for the mode switch.

ENC[2:0] Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

8.2.12. Frame Marker Position (R0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EMP[8:0] Sets the output position of frame cycle (frame marker).

When FMP[8:0]=0, a high-active pulse FMARK is output at the start of back porch period for one display line period (1H).

Make sure the $9'h000 \leq FMP \leq BP+NL+FP$

FMP[8:0]	FMARK Output Position
9'h000	0 th line
9'h001	1 st line
9'h002	2 nd line
9'h003	3 rd line
.	.
.	.
.	.
9'h175	373 rd line
9'h176	374 th line
9'h177	375 th line

8.2.13. RGB Display Interface Control 2 (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	----	-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

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W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the rising edge of DOTCLK

DPL = "1" The data is input on the falling edge of DOTCLK

EPL: Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".

EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of the HSYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

VSPL: Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

8.2.14. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP: When SLP = 1, ILI9325C enters the sleep mode and the display operation stops except the RC oscillator to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following instruction.

- a. Exit sleep mode (SLP = "0")

STB: When STB = 1, ILI9325C enters the standby mode and the display operation stops except the GRAM power supply to reduce the power consumption. In the STB mode, the GRAM data and instructions cannot be updated except the following instruction.

- a. Exit standby mode (STB = "0")

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = "000" to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Gamma driver amplifiers	Source driver amplifiers
000	Halt	Halt
001	1.00	1.00
010	1.00	0.75
011	1.00	0.50
100	0.75	1.00

101	0.75	0.75
110	0.75	0.50
111	0.50	0.50

SAP: Source Driver output control

SAP=0, Source driver is disabled.

SAP=1, Source driver is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

APE: Power supply enable bit.

Set APE = "1" to start the generation of power supply according to the power supply startup sequence.

BT[3:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	VCI1 x 2	- VCI1	VCI1 x 6	- VCI1 x 5
3'h1	VCI1 x 2	- VCI1		- VCI1 x 4
3'h2				- VCI1 x 3
3'h3	VCI1 x 2	- VCI1	VCI1 x 5	- VCI1 x 5
3'h4				- VCI1 x 4
3'h5				- VCI1 x 3
3'h6	VCI1 x 2	- VCI1	VCI1 x 4	- VCI1 x 4
3'h7				- VCI1 x 3

Notes: 1. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL and VCL levels.

2. Make sure DDVDH = 6.0V (max.),

8.2.15. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

VC[2:0] Sets the ratio factor of VCI to generate the reference voltages VCI1.

VC2	VC1	VC0	VCI1 voltage
0	0	0	0.95 x VCI
0	0	1	0.90 x VCI
0	1	0	0.85 x VCI
0	1	1	0.80 x VCI
1	0	0	0.75 x VCI
1	0	1	0.70 x VCI
1	1	0	Disabled
1	1	1	1.0 x VCI

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC02	DC01	DC00	Step-up circuit1 step-up frequency (f_{DCDC1})	DC12	DC11	DC10	Step-up circuit2 step-up frequency (f_{DCDC2})
0	0	0	Fosc	0	0	0	Fosc / 4
0	0	1	Fosc / 2	0	0	1	Fosc / 8
0	1	0	Fosc / 4	0	1	0	Fosc / 16
0	1	1	Fosc / 8	0	1	1	Fosc / 32
1	0	0	Fosc / 16	1	0	0	Fosc / 64
1	0	1	Fosc / 32	1	0	1	Fosc / 128
1	1	0	Fosc / 64	1	1	0	Fosc / 256
1	1	1	Halt step-up circuit 1	1	1	1	Halt step-up circuit 2

Note: Be sure $f_{DCDC1} \geq f_{DCDC2}$ when setting DC0[2:0] and DC1[2:0].

8.2.16. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VRH[3:0] Set the amplifying rate (1.6 ~ 1.9) of VCI applied to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VCIRE: Select the external reference voltage VCI or internal reference voltage VCIR.

VCIRE=0	External reference voltage VCI (default)
VCIRE =1	Internal reference voltage 2.5V

VCIRE =0					VCIRE =1				
VRH3	VRH2	VRH1	VRH0	VREG1OUT	VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt	0	0	0	0	Halt
0	0	0	1	VCI x 2.00	0	0	0	1	2.5V x 2.00 = 5.000V
0	0	1	0	VCI x 2.05	0	0	1	0	2.5V x 2.05 = 5.125V
0	0	1	1	VCI x 2.10	0	0	1	1	2.5V x 2.10 = 5.250V
0	1	0	0	VCI x 2.20	0	1	0	0	2.5V x 2.20 = 5.500V
0	1	0	1	VCI x 2.30	0	1	0	1	2.5V x 2.30 = 5.750V
0	1	1	0	VCI x 2.40	0	1	1	0	2.5V x 2.40 = 6.000V
0	1	1	1	VCI x 2.40	0	1	1	1	2.5V x 2.40 = 6.000V
1	0	0	0	VCI x 1.60	1	0	0	0	2.5V x 1.60 = 4.000V
1	0	0	1	VCI x 1.65	1	0	0	1	2.5V x 1.65 = 4.125V
1	0	1	0	VCI x 1.70	1	0	1	0	2.5V x 1.70 = 4.250V
1	0	1	1	VCI x 1.75	1	0	1	1	2.5V x 1.75 = 4.375V
1	1	0	0	VCI x 1.80	1	1	0	0	2.5V x 1.80 = 4.500V

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1	1	0	1	VCI x 1.85
1	1	1	0	VCI x 1.90
1	1	1	1	VCI x 1.95

1	1	0	1	2.5V x 1.85 = 4.625V
1	1	1	0	2.5V x 1.90 = 4.750V
1	1	1	1	2.5V x 1.95 = 4.875V

When VCI<2.5V, Internal reference voltage will be same as VCI.

Make sure that VC and VRH setting restriction: VREG1OUT ≤ (DDVDH - 0.2)V.

8.2.17. Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0] Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.24 x VREG1OUT .

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
1	0	0	0	0	VREG1OUT x 0.94
1	0	0	0	1	VREG1OUT x 0.96
1	0	0	1	0	VREG1OUT x 0.98
1	0	0	1	1	VREG1OUT x 1.00
1	0	1	0	0	VREG1OUT x 1.02
1	0	1	0	1	VREG1OUT x 1.04
1	0	1	1	0	VREG1OUT x 1.06
1	0	1	1	1	VREG1OUT x 1.08
1	1	0	0	0	VREG1OUT x 1.10
1	1	0	0	1	VREG1OUT x 1.12
1	1	0	1	0	VREG1OUT x 1.14
1	1	0	1	1	VREG1OUT x 1.16
1	1	1	0	0	VREG1OUT x 1.18
1	1	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 1.22
1	1	1	1	1	VREG1OUT x 1.24

Set VDV[4:0] to let Vcom amplitude less than 6V.

8.2.18. GRAM Horizontal/Vertical Address Set (R20h, R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0] Set the initial value of address counter (AC).

The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

AD[16:0]	GRAM Data Map
17'h00000 ~ 17'h000EF	1 st line GRAM Data
17'h00100 ~ 17'h001EF	2 nd line GRAM Data
17'h00200 ~ 17'h002EF	3 rd line GRAM Data

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17'h00300 ~ 17'h003EF	4 th line GRAM Data
17'h13D00 ~ 17' h13DEF	318 th line GRAM Data
17'h13E00 ~ 17' h13EEF	319 th line GRAM Data
17'h13F00 ~ 17'h13FEF	320 th line GRAM Data

Note1: When the RGB interface is selected (RM = "1"), the address AD[16:0] is set to the address counter every frame on the falling edge of VSYNC.

8.2.19. Write Data to GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																	

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

8.2.20. Read Data from GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																	

RD[17:0] Read 18-bit data from GRAM through the read data register (RDR).

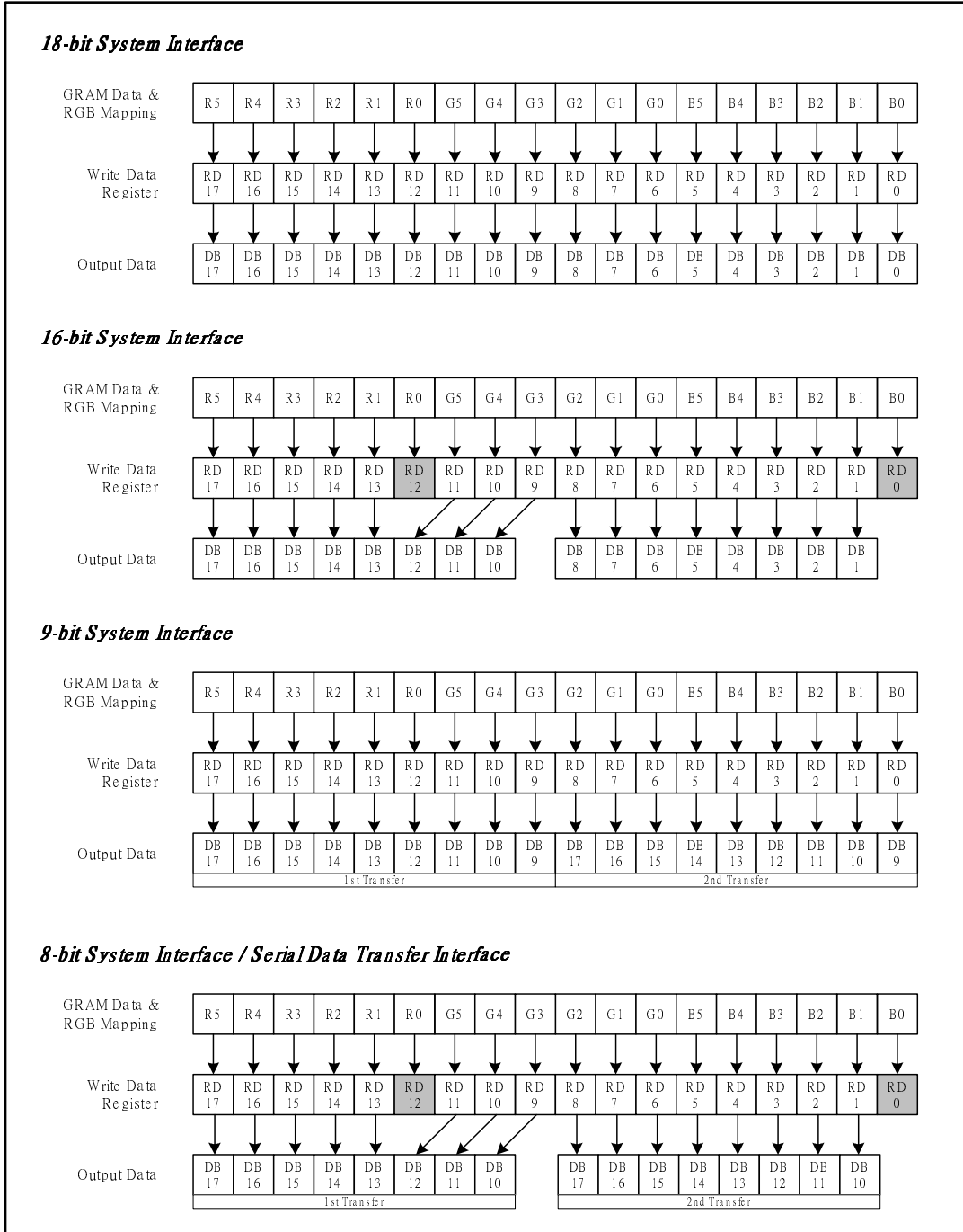


Figure 27 Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit Interface Mode

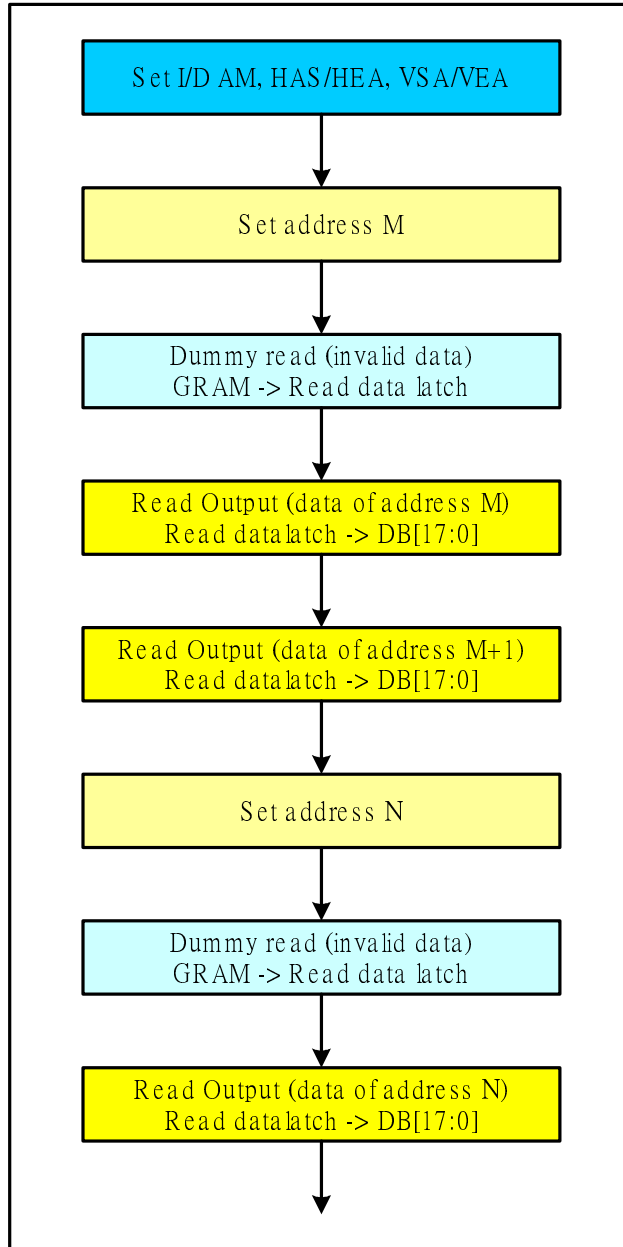


Figure 28 GRAM Data Read Back Flow Chart

8.2.21. Power Control 7 (R29h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM[5:0] Set the internal VcomH voltage.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	VREG1OUT x 0.685
0	0	0	0	0	1	VREG1OUT x 0.690
0	0	0	0	1	0	VREG1OUT x 0.695
0	0	0	0	1	1	VREG1OUT x 0.700
0	0	0	1	0	0	VREG1OUT x 0.705
0	0	0	1	0	1	VREG1OUT x 0.710
0	0	0	1	1	0	VREG1OUT x 0.715
0	0	0	1	1	1	VREG1OUT x 0.720
0	0	1	0	0	0	VREG1OUT x 0.725
0	0	1	0	0	1	VREG1OUT x 0.730
0	0	1	0	1	0	VREG1OUT x 0.735
0	0	1	0	1	1	VREG1OUT x 0.740
0	0	1	1	0	0	VREG1OUT x 0.745
0	0	1	1	0	1	VREG1OUT x 0.750
0	0	1	1	1	0	VREG1OUT x 0.755
0	0	1	1	1	1	VREG1OUT x 0.760
0	1	0	0	0	0	VREG1OUT x 0.765
0	1	0	0	0	1	VREG1OUT x 0.770
0	1	0	0	1	0	VREG1OUT x 0.775
0	1	0	0	1	1	VREG1OUT x 0.780
0	1	0	1	0	0	VREG1OUT x 0.785
0	1	0	1	0	1	VREG1OUT x 0.790
0	1	0	1	1	0	VREG1OUT x 0.795
0	1	0	1	1	1	VREG1OUT x 0.800
0	1	1	0	0	0	VREG1OUT x 0.805
0	1	1	0	0	1	VREG1OUT x 0.810
0	1	1	0	1	0	VREG1OUT x 0.815
0	1	1	1	0	1	VREG1OUT x 0.820
0	1	1	1	0	0	VREG1OUT x 0.825
0	1	1	1	0	1	VREG1OUT x 0.830
0	1	1	1	1	0	VREG1OUT x 0.835
0	1	1	1	1	1	VREG1OUT x 0.840

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
1	0	0	0	0	0	VREG1OUT x 0.845
1	0	0	0	0	1	VREG1OUT x 0.850
1	0	0	0	1	0	VREG1OUT x 0.855
1	0	0	0	1	1	VREG1OUT x 0.860
1	0	0	1	0	0	VREG1OUT x 0.865
1	0	0	1	0	1	VREG1OUT x 0.870
1	0	0	1	1	0	VREG1OUT x 0.875
1	0	0	1	1	1	VREG1OUT x 0.880
1	0	1	0	0	0	VREG1OUT x 0.885
1	0	1	0	0	1	VREG1OUT x 0.890
1	0	1	0	1	0	VREG1OUT x 0.895
1	0	1	0	1	1	VREG1OUT x 0.900
1	0	1	1	0	0	VREG1OUT x 0.905
1	0	1	1	0	1	VREG1OUT x 0.910
1	0	1	1	1	0	VREG1OUT x 0.915
1	0	1	1	1	1	VREG1OUT x 0.920
1	1	0	0	0	0	VREG1OUT x 0.925
1	1	0	0	0	1	VREG1OUT x 0.930
1	1	0	0	1	0	VREG1OUT x 0.935
1	1	0	0	1	1	VREG1OUT x 0.940
1	1	0	1	0	0	VREG1OUT x 0.945
1	1	0	1	0	1	VREG1OUT x 0.950
1	1	0	1	1	0	VREG1OUT x 0.955
1	1	0	1	1	1	VREG1OUT x 0.960
1	1	1	0	0	0	VREG1OUT x 0.965
1	1	1	0	0	1	VREG1OUT x 0.970
1	1	1	0	1	0	VREG1OUT x 0.975
1	1	1	1	0	1	VREG1OUT x 0.980
1	1	1	1	0	0	VREG1OUT x 0.985
1	1	1	1	0	1	VREG1OUT x 0.990
1	1	1	1	1	0	VREG1OUT x 0.995
1	1	1	1	1	1	VREG1OUT x 1.000

8.2.22. Frame Rate and Color Control (R2Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0
Default		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

FRS[4:0] Set the frame rate when the internal resistor is used for oscillator circuit.

FRS[3:0]	FRS[3:0]	Frame Rate
0000	4'h0	28
0001	4'h1	30
0010	4'h2	32
0011	4'h3	34
0100	4'h4	36
0101	4'h5	39
0110	4'h6	41
0111	4'h7	45
1000	4'h8	49
1001	4'h9	54
1010	4'hA	60
1011	4'hB	67
1100	4'hC	77
1101	4'hD	90
1110	4'hE	Setting Prohibited
1111	4'hF	Setting Prohibited

8.2.23. Gamma Control (R30h ~ R3Dh)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R30h	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31h	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32h	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35h	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R36h	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37h	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38h	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39h	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3Ch	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3Dh	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

KP5-0[2:0] : γ fine adjustment register for positive polarity

RP1-0[2:0] : γ gradient adjustment register for positive polarity

VRP1-0[4:0] : γ amplitude adjustment register for positive polarity

KN5-0[2:0] : γ fine adjustment register for negative polarity

RN1-0[2:0] : γ gradient adjustment register for negative polarity

VRN1-0[4:0] : γ amplitude adjustment register for negative polarity

For details “ γ -Correction Function” section.

8.2.24. Horizontal and Vertical RAM Address Position (R50h, R51h, R52h, R53h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R51h	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
R52h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R53h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
R50h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51h	Default		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R52h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53h	Default		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[7:0]/HEA[7:0] HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00”h \leq HSA[7:0] < HEA[7:0] \leq “EF”h. and “01”h \leq HEA-HAS.

VSA[8:0]/VEA[8:0] VSA[8:0] and VEA[8:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure “000”h \leq VSA[8:0] < VEA[8:0] \leq “13F”h.

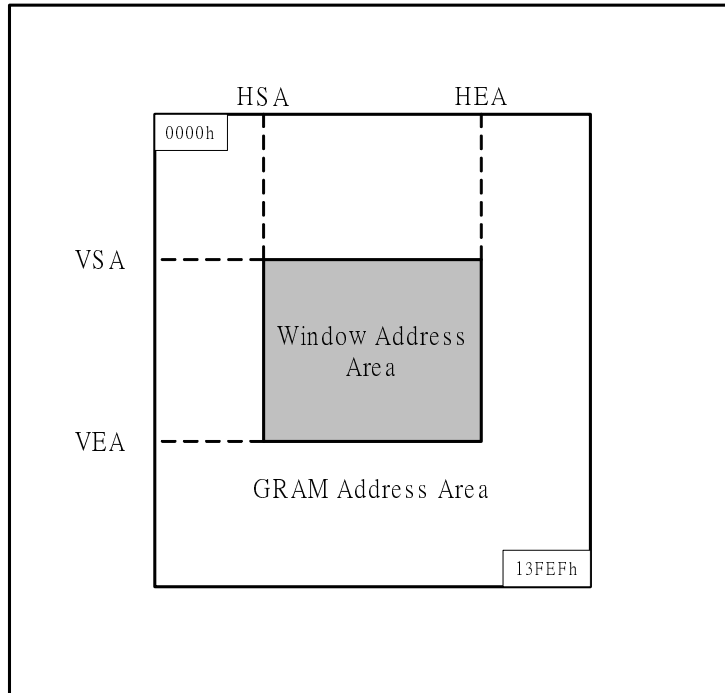


Figure 29 GRAM Access Range Configuration

$$"00"h \leq HSA[7:0] \leq HEA[7:0] \leq "EF"h$$

$$"00"h \leq VSA[8:0] \leq VEA[8:0] \leq "13F"h$$

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

8.2.25. Gate Scan Control (R60h, R61h, R6Ah)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R60h	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R61h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
R6Ah	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R60h	Default		0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
R61h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6Ah	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[5:0] The ILI9325C allows to specify the gate line from which the gate driver starts to scan by setting the SCN[5:0] bits.

SCN[5:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G320	G1	G320
01h	G9	G312	G17	G304
02h	G17	G304	G33	G288
03h	G25	G296	G49	G272
04h	G33	G288	G65	G256
05h	G41	G280	G81	G240
06h	G49	G272	G97	G224
07h	G57	G264	G113	G208
08h	G65	G256	G129	G192
09h	G73	G248	G145	G176
0Ah	G81	G240	G161	G160
0Bh	G89	G232	G177	G144
0Ch	G97	G224	G193	G128
0Dh	G105	G216	G209	G112
0Eh	G113	G208	G2	G96
0Fh	G121	G200	G18	G80
10h	G129	G192	G34	G64
11h	G137	G184	G50	G48
12h	G145	G176	G66	G32
13h	G153	G168	G82	G16
14h	G161	G160	G98	G319
15h	G169	G152	G114	G303
16h	G177	G144	G130	G287
17h	G185	G136	G146	G271
18h	G193	G128	G162	G255
19h	G201	G120	G178	G239
1Ah	G209	G112	G194	G223
1Bh	G217	G104	G114	G207
1Ch	G225	G96	G130	G191
1Dh	G233	G88	G146	G175
1Eh	G241	G80	G162	G159
1Fh	G249	G72	G178	G143
20h	G257	G64	G194	G127
21h	G265	G56	G210	G111
22h	G273	G48	G226	G95
23h	G281	G40	G242	G79
24h	G289	G32	G258	G63
25h	G297	G24	G274	G47
26h	G305	G16	G290	G31
27h	G313	G8	G306	G15
28h ~ 3Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Note: When SM=1, it is a interlacing scanning. Please reference page 72!

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00	8 lines
6'h01	16 lines
6'h02	24lines
...	...
6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 line
6'h27	320 line
Others	Setting inhibited

NDL: Sets the source driver output level in the non-display area.

NDL	Non-Display Area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

GS: Sets the direction of scan by the gate driver in the range determined by SCN[4:0] and NL[4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G320.

When GS = 1, the scan direction is from G320 to G1

REV: Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	.	.	.
	.	.	.
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the ILI9325C starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the

number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image Display
0	Fixed
1	Enable Scrolling

VL[8:0]: Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0] ≤ 320.

8.2.26. SPI Read/Write Control (R66h, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX

This register is used to control the read/write function of registers when the 8/9-bit serial interface is used.

If users need to read back the register data by the 8/9-bit serial interface, the R/WX bit must be set as '1'.

R/WX	Description
0	Register write mode (default)
1	Register read mode

8.2.27. Partial Image 1 Display Position (R80h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTD P0[8]	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDPO[8:0]: Sets the display start position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.

8.2.28. Partial Image 1 RAM Start/End Address (R81h, R82h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A0[8]	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
W	1	0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTSA0[8:0] PTEA0[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0].

8.2.29. Partial Image 2 Display Position (R83h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTD P1[8]	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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PTDP1[8:0]: Sets the display start position of partial image 2 The display areas of the partial images 1 and 2 must not overlap each another.

8.2.30. Partial Image 2 RAM Start/End Address (R84h, R85h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A1[8]	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTSA1[8:0] PTEA1[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 2 Make sure PTSA1[8:0] ≤ PTEA1[8:0].

8.2.31. Panel Interface Control 1 (R90h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVI1	DIVIO	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNIO
Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

RTNI[4:0]: Sets 1H (line) clock number of internal clock operating mode. In this mode, ILI9325C display operation is synchronized with internal clock signal.

RTNI[4:0]	Clocks/Line	RTNI[4:0]	Clocks/Line
00000~01111	Setting Disabled	11000	24 clocks
10000	16 clocks	11001	25 clocks
10001	17 clocks	11010	26 clocks
10010	18 clocks	11011	27 clocks
10011	19 clocks	11100	28 clocks
10100	20 clocks	11101	29 clocks
10101	21 clocks	11110	30 clocks
10110	22 clocks	11111	31 clocks
10111	23 clocks		

DIVI[1:0]: Sets the division ratio of internal clock frequency.

DIVI1	DIVIO	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

8.2.32. Panel Interface Control 2 (R92h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the gate output non-overlap period when ILI9325C display operation is synchronized with internal clock signal.

NOWI[2:0]	Gate Non-overlap Period
000	Setting inhibited
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks

111	Setting inhibited
-----	-------------------

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

8.2.33. Panel Interface Control 4 (R95h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DIVE[1:0]: Sets the division ratio of DOTCLK when ILI9325C display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	18/16-bit RGB Interface	DOTCLK=5MHz	6-bit x 3 Transfers RGB Interface	DOTCLK=5MHz
00	Setting Prohibited	Setting Prohibited	-	Setting Prohibited	-
01	1/4	4 DOTCLKS	0.8 μ s	12 DOTCLKS	0.8 μ s
10	1/8	8 DOTCLKS	1.6 μ s	24 DOTCLKS	1.6 μ s
11	1/16	16 DOTCLKS	3.2 μ s	48 DOTCLKS	3.2 μ s

8.2.34. Panel Interface Control 5 (R97h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

NOWE[3:0]: Sets the gate output non-overlap period when the ILI9325C display operation is synchronized with RGB interface signals.

NOWE[3:0]	Gate Non-overlap Period
0000	Setting inhibited
0001	1 clocks
0010	2 clocks
0011	3 clocks
0100	4 clocks
0101	5 clocks
0110	6 clocks
0111	7 clocks

NOWE[3:0]	Gate Non-overlap Period
1000	8 clocks
1001	9 clocks
1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	Setting inhibited
1110	Setting inhibited
1111	Setting inhibited

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

8.2.35. OTP VCM Programming Control (RA1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTP_PGM_EN: OTP programming enable. When program OTP, must set this bit. OTP data can be programmed 3 times.

VCM_OTP[5:0]: OTP programming data for VCOMH voltage, the voltage refer to VCM[5:0] value.

8.2.36. OTP VCM Status and Enable (RA2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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PGM_CNT[1:0]: OTP programmed record. These bits are read only.

OTP_PGM_CNT[1:0]	Description
00	OTP clean
01	OTP programmed 1 time
10	OTP programmed 2 times
11	OTP programmed 3 times

VCM_D[5:0]: OTP VCM data read value. These bits are read only.

VCM_EN: OTP VCM data enable.

'1': Set this bit to enable OTP VCM data to replace R29h VCM value.

'0': Default value, use R29h VCM value.

8.2.37. OTP Programming ID Key (RA5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KEY[15:0]: OTP Programming ID key protection. Before writing OTP programming data RA1h, it must write RA5h with 0xAA55 value first to make OTP programming successfully. If RA5h is not written with 0xAA55, OTP programming will be fail. See OTP Programming flow.

8.2.38. Write Display Brightness Value (RB1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

Description

This command is used to adjust the brightness value of the display.

DBV[7:0]: 8 bit, for display brightness of manual brightness setting and CABC in ILI9325C. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.

8.2.39. Read Display Brightness Value (RB2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	X	X	X	X	X	X	X	X	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

Description

This command is used to return the brightness value of the display.

DBV[7:0] is reset when display is in sleep-in mode.

DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (B3h)" command is '0'.

DBV[7:0] is manual set brightness specified with "Write CTRL Display (B3h)" command when BCTRL bit is '1'.

When bit BCTRL of "Write CTRL Display (B3h)" command is '1' and C1/C0 bit of "Write Content Adaptive Brightness Control (B5h)" command are '0', DBV[7:0] output is the brightness value specified with "Write Display Brightness (B1h)" command.

8.2.40. Write CTRL Display Value (RB3h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
w	1	X	X	X	X	X	X	X	X	X	X	BCTRL	X	DD	BL	X	X

Description

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected

X: don't care

8.2.41. Read CTRL Display Value (RB4h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	X	X	X	X	X	X	X	X	X	X	BCTRL	X	DD	BL	X	X

Description

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

X = Don't care

8.2.42. Write Content Adaptive Brightness Control Value (RB5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
w	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	C[1:0]

Description

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]		Description
0	0	CABC OFF
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

X = Don't care

8.2.43. Read Content Adaptive Brightness Control Value (RB6h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	C[1:0]

Description

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]		Description
0	0	CABC OFF
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

X = Don't care

8.2.44. Write CABC Minimum Brightness (RBEh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	CMB[7:0]							

Description

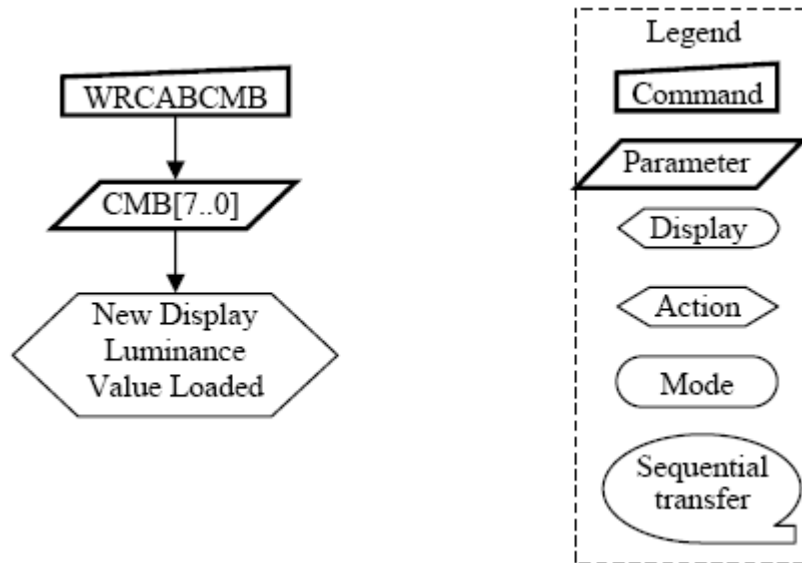
This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (B3h)"), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.



8.2.45. Read CABC Minimum Brightness (RBFh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	X	X	X	X	X	X	X	X								CMB[7:0]

Description

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (B3h)"), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

8.2.46. CABC Control 1 (RC7h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	LEDONR	LEDONPOL	LEDPWMPOL

LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.

BL	LEDPWMPOL	LEDPWM pin
0	0	0
0	1	1
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

LEDONPOL: This bit is used to control LEDON pin.

BL	LEDONPOL	LEDON pin
0	0	0
0	1	1
1	0	LEDONR
1	1	Inversed LEDONR

LEDONR: This bit is used to control LEDON pin.

LEDONR	Description
0	Low
1	High

8.2.47. CABC Control 1 (RC8h)

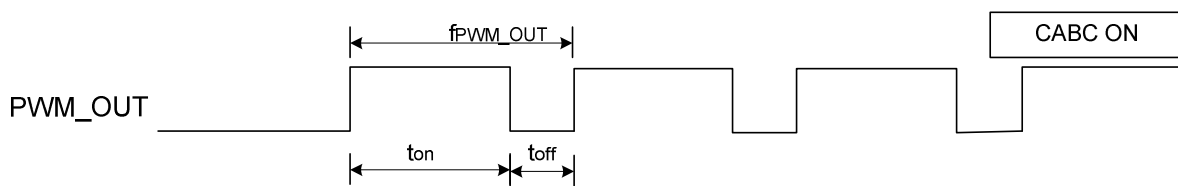
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	PWM_DIV[7:0]							

Description

PWM_DIV[7:0]: PWM_OUT output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period can be calculated using the equation in the following.

$$f_{PWM_OUT} = \frac{5.8MHz}{(PWM_DIV[7:0]+1) \times 255}$$

PWM_DIV[7:0]									f _{PWM_OUT}
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	0	22.74 KHz
0	0	0	0	0	0	0	0	1	11.37 KHz
0	0	0	0	0	0	0	1	0	7.58KHz
0	0	0	0	0	0	0	1	1	5.68 KHz
0	0	0	0	0	1	0	0	0	4.54 KHz
⋮									⋮
⋮									⋮
1	1	1	1	1	0	1	1		90.26 Hz
1	1	1	1	1	1	0	0		89.9Hz
1	1	1	1	1	1	0	1		89.53Hz
1	1	1	1	1	1	1	0		89.17 Hz
1	1	1	1	1	1	1	1		88.81 Hz



Note : The output frequency tolerance of internal frequency divider in CABC is ±10%

8.2.48. CABControl 2 (RC9h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	THRES_MOV[3:0]			THRES_STILL[3:0]				

Description

THRES_MOV[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in MOVING image mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

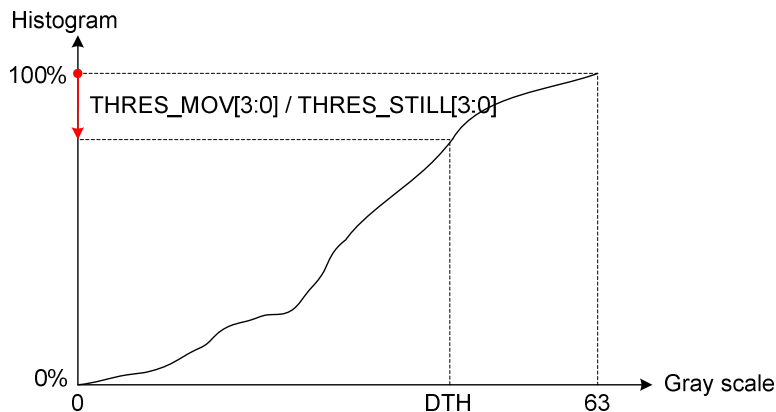
THRES_MOV[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_MOV[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %

THRES_STILL[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in STILL mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_STILL[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_STILL[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



8.2.49. CABControl 3 (RCAh)

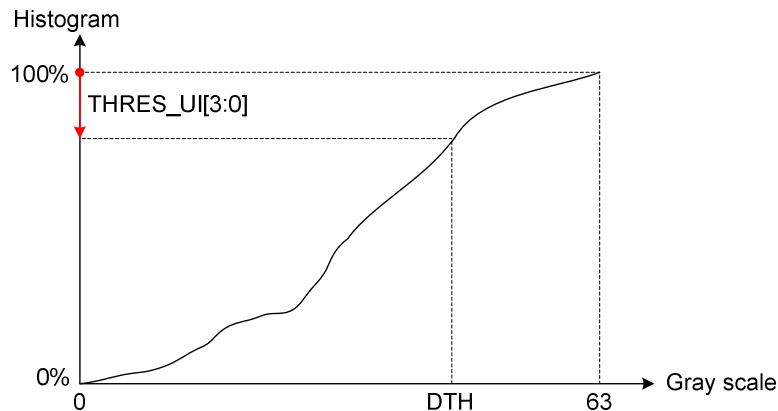
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	0	0	0	0	THRES_UI[3:0]			

Description

THRES_UI[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in USER INTERFACE mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



8.2.50. CABControl 4 (RCBh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	DTH_MOV[3:0]			DTH_STILL[3:0]				

Description

DTH_MOV[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in MOVING image mode.

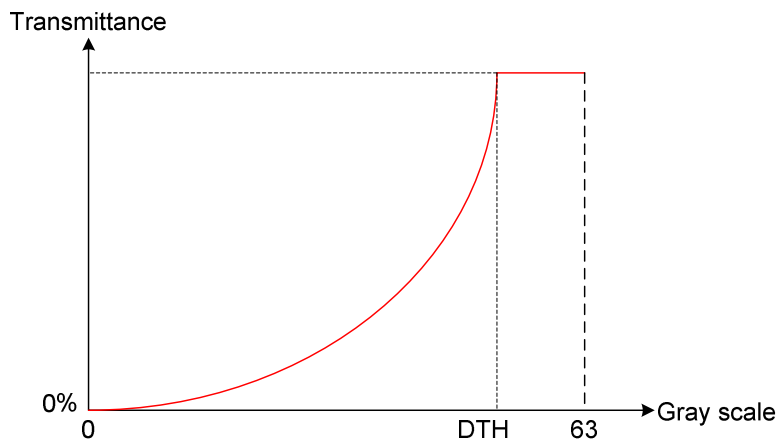
DTH_MOV[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	224
0	0	0	1	220
0	0	1	0	216
0	0	1	1	212
0	1	0	0	208
0	1	0	1	204
0	1	1	0	200
0	1	1	1	196

DTH_MOV[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	192
1	0	0	1	188
1	0	1	0	184
1	0	1	1	180
1	1	0	0	176
1	1	0	1	172
1	1	1	0	168
1	1	1	1	164

DTH_STILL[3:0]: This parameter is used to set the minimum limitation of grayscale threshold value in STILL image mode.

DTH_STILLI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	224
0	0	0	1	220
0	0	1	0	216
0	0	1	1	212
0	1	0	0	208
0	1	0	1	204
0	1	1	0	200
0	1	1	1	196

DTH_STILL[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	192
1	0	0	1	188
1	0	1	0	184
1	0	1	1	180
1	1	0	0	176
1	1	0	1	172
1	1	1	0	168
1	1	1	1	164



8.2.51. CABC Control 5 (RCCh)

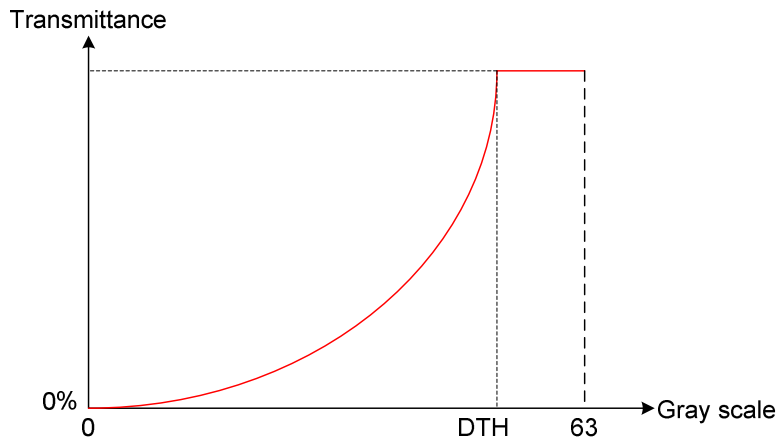
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	0	0	0	0	DTH_UI[3:0]			

Description

DTH_UI[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in USER INTERFACE mode.

DTH_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	252
0	0	0	1	248
0	0	1	0	244
0	0	1	1	240
0	1	0	0	236
0	1	0	1	232
0	1	1	0	228
0	1	1	1	224

DTH_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	220
1	0	0	1	216
1	0	1	0	212
1	0	1	1	208
1	1	0	0	2-4
1	1	0	1	200
1	1	1	0	196
1	1	1	1	192



8.2.52. CABC Control 6 (RCDh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	DIM_OPT2[3:0]			0	DIM_OPT1[2:0]			

Description

DIM_OPT1[2:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision.

DIM_OPT1[2:0]			Description
D2	D1	D0	
0	0	0	1 frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	4 frames
1	0	0	8 frames
1	0	1	16 frames
1	1	0	32 frames
1	1	1	64 frames

DIM_OPT2[3:0]: This parameter is used to set the imitation of minimum brightness change. If this parameter is large than the difference between target brightness and current brightness, then the brightness will not change.

nd

8.2.53. CABC Control 7 (RCEh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	X	X	X	X	X	X	X	X	SCD_VLINE[7:0]							
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SCD_VLINE[8]

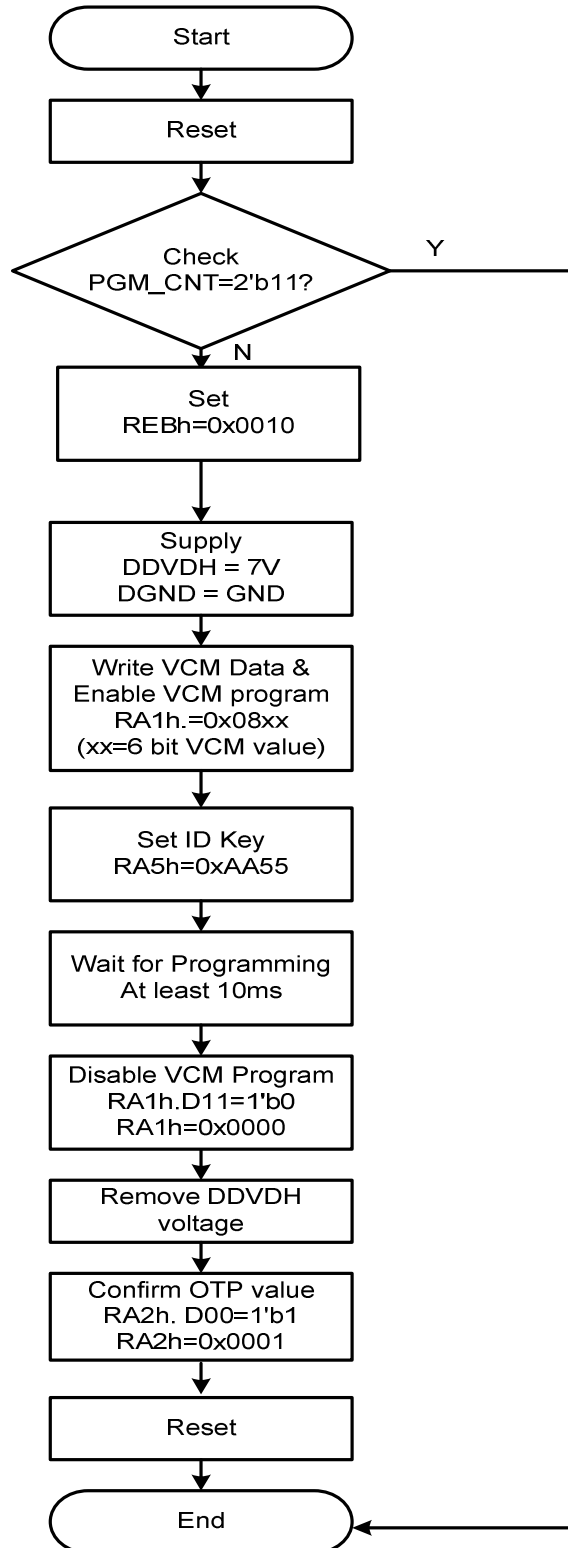
Description

SCD_VLINE[8:0]: This parameter is used set the display line per frame while partial mode ON.

SCD_VLINE[8:0]									Display line
D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	0	1	1	3 lines
0	0	0	0	0	0	1	0	0	4 lines
:									:
:									:
1	0	0	1	1	1	1	0	1	317 lines
1	0	0	1	1	1	1	1	0	318 lines
1	0	0	1	1	1	1	1	1	319lines
1	0	1	0	0	0	0	0	0	320 lines
Others									Setting prohibited

9. OTP Programming Flow

VCOMH OTP programming Flow



10. GRAM Address Map & Read/Write

ILI9325C has an internal graphics RAM (GRAM) of 172,800 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.

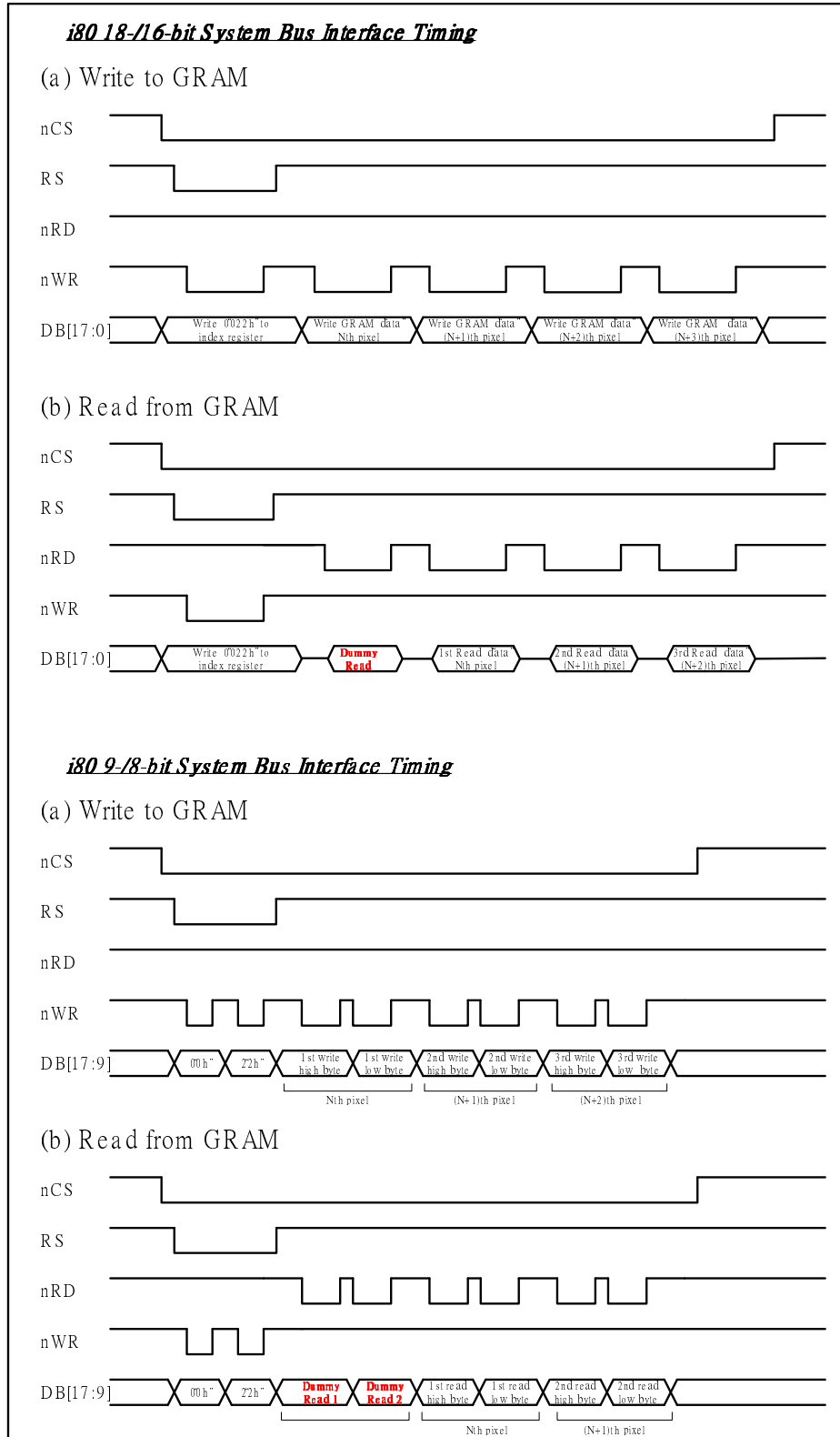


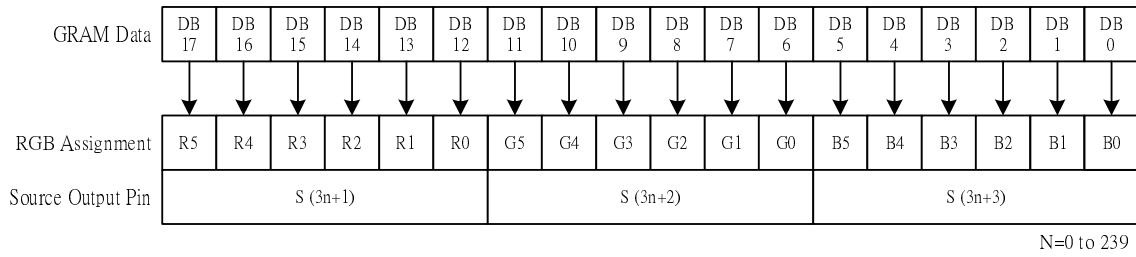
Figure30 GRAM Read/Write Timing of i80-System Interface

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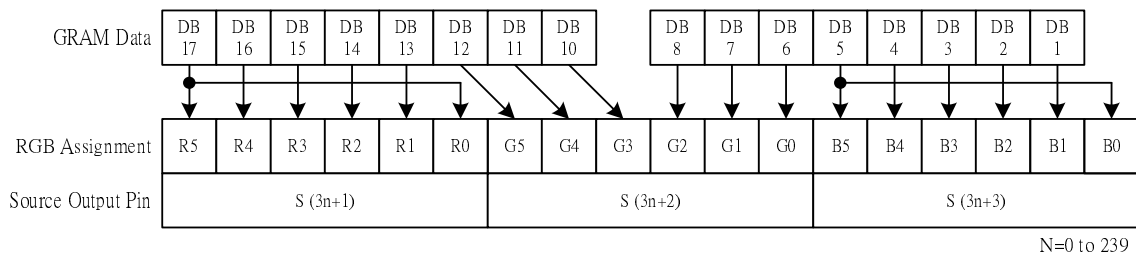
GRAM address map table of SS=0, BGR=0

SS=0, BGR=0		S1...S3	S4...S6	S7...S9	S10...S12	...	S517...S519	S520...S522	S523...S525	S526...S720
GS=0	GS=1	DB17...0	DB17...0	DB17...0	DB17...0	...	DB17...0	DB17...0	DB17...0	DB17...0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	...	"000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	...	"001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	...	"002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	...	"003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	...	"004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	...	"005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	...	"006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	...	"007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	...	"008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	...	"009ECh"	"009EDh"	"009EEh"	"009EFh"
.
.
.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	...	"136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	...	"137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	...	"138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	...	"139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	...	"13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	...	"13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	...	"13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	...	"13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	...	"13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	...	"13FECh"	"13FEDh"	"13FEEh"	"13FEFh"

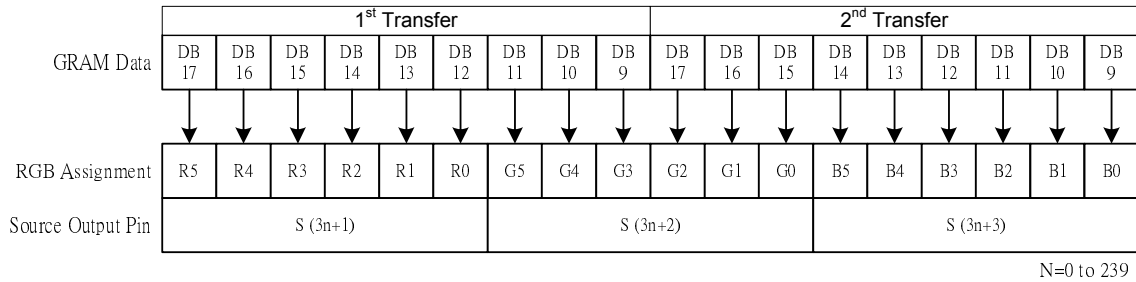
i80/M68 system 18-bit data bus interface



i80/M68 system 16-bit data bus interface



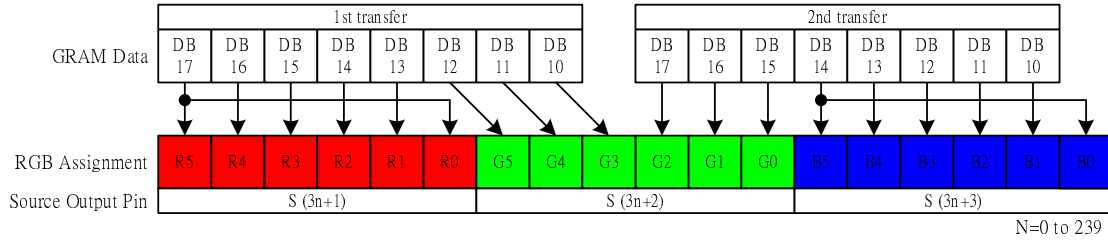
i80/M68 system 9-bit data bus interface



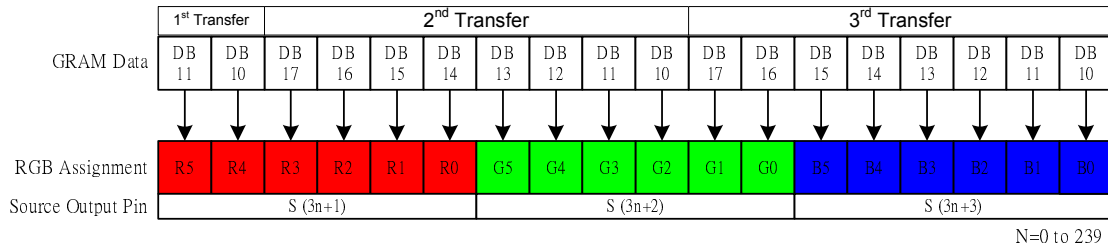
GRAM Data and display data of 18-/16-/9-bit system interface (SS=" 0", BGR=" 0")

Figure31 i80-System Interface with 18-/16-/9-bit Data Bus (SS="0", BGR="0")

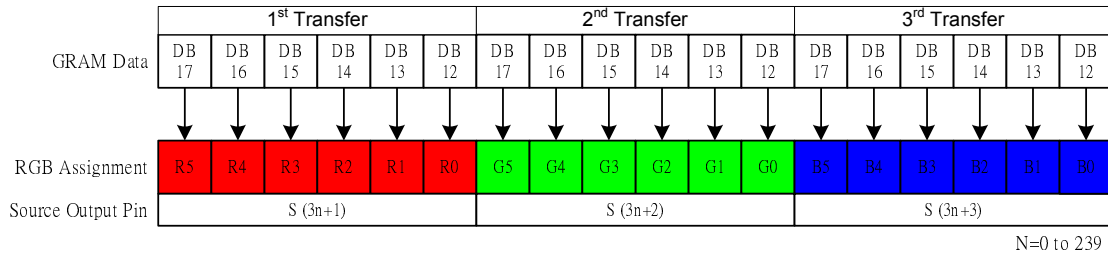
i80M68 system 8-bit interface / SPI Interface (2 transfers/pixel)



i80M68 system 8-bit interface (3 transfers/pixel, TRI=" 1", DFM[1:0]=" 00")



i80M68 system 8-bit interface (3 transfers/pixel, TRI=" 1", DFM[1:0]=" 10)



i80M68 system 8-bit interface (SS=" 0", BGR=" 0")

Figure32 i80-System Interface with 8-bit Data Bus (SS="0", BGR="0")

GRAM address map table of SS=1, BGR=1

SS=1, BGR=1		S720...S718	S717...S715	S714...S712	S711...S709	...	S12...S10	S9...S7	S6...S4	S3...S1
GS=0	GS=1	DB17...0	DB17...0	DB17...0	DB17...0	...	DB17...0	DB17...0	DB17...0	DB17...0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	...	"000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	...	"001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	...	"002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	...	"003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	...	"004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	...	"005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	...	"006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	...	"007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	...	"008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	...	"009ECh"	"009EDh"	"009EEh"	"009EFh"
.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	...	"136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	...	"137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	...	"138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	...	"139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	...	"13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	...	"13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	...	"13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	...	"13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	...	"13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	...	"13FECh"	"13FEDh"	"13FEEh"	"13FEFh"

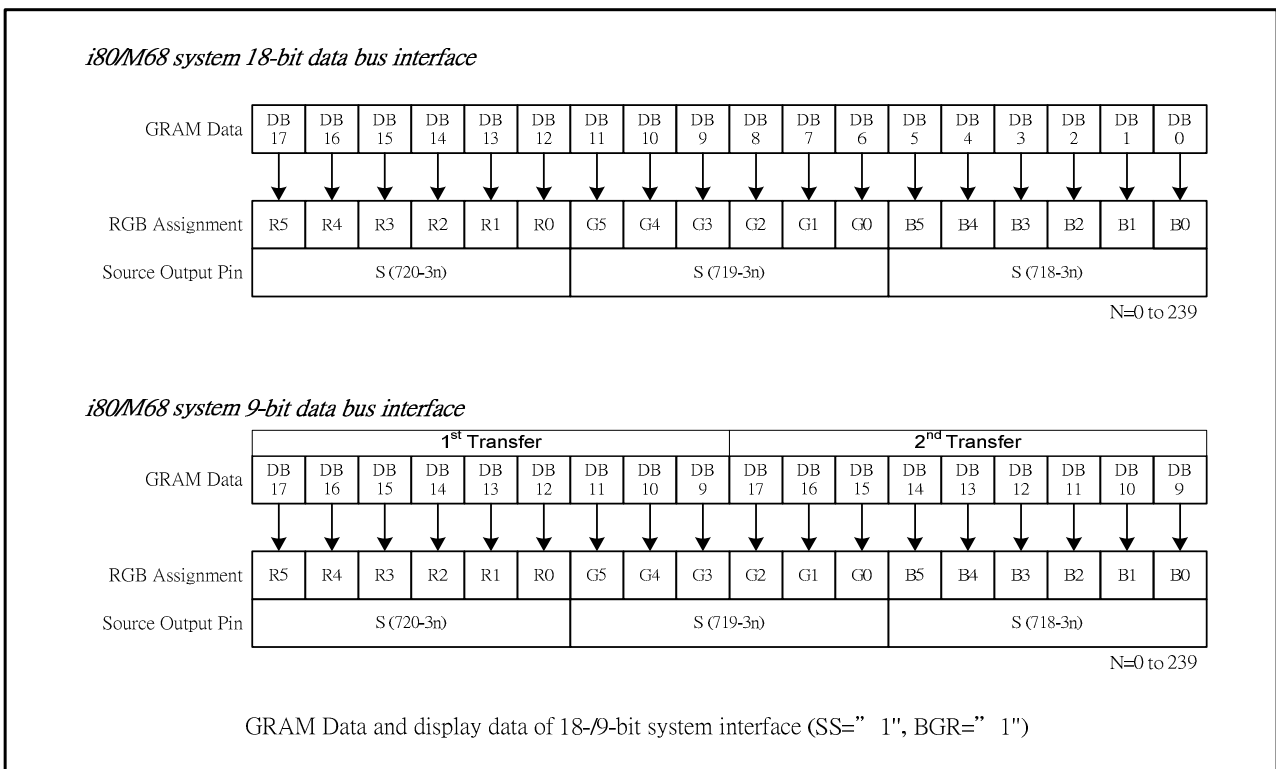


Figure 33 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")

11. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[8:0], end: VEA[8:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9325C to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the GRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

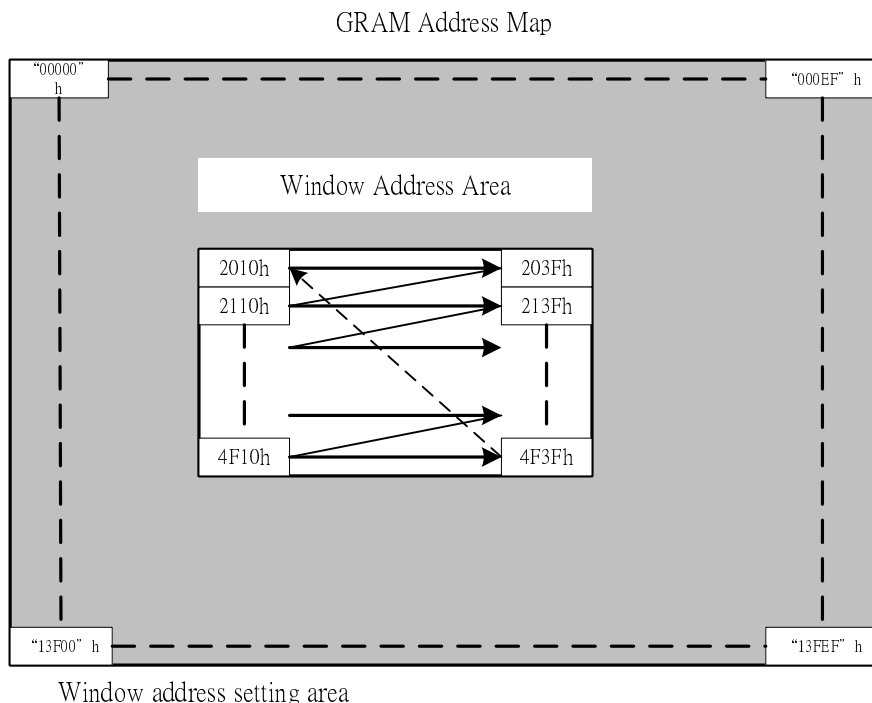
(Horizontal direction) $00H \leq HSA[7:0] \leq HEA[7:0] \leq "EF"H$

(Vertical direction) $00H \leq VSA[8:0] \leq VEA[8:0] \leq "13F"H$

[RAM address, AD (an address within a window address area)]

(RAM address) $HSA[7:0] \leq AD[7:0] \leq HEA[7:0]$

$VSA[8:0] \leq AD[15:8] \leq VEA[8:0]$



HSA[7:0] = 10h, HEA[7:0] = 3Fh, I/D = 1 (increment)
VSA[8:0] = 20h, VEA[8:0] = 4Fh, AM = 0 (horizontal writing)

Figure 34 GRAM Access Window Map

12. Gamma Correction

ILI9325C incorporates the γ -correction function to display 262,144 colors for the LCD panel. The γ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9325C available with liquid crystal panels of various characteristics.

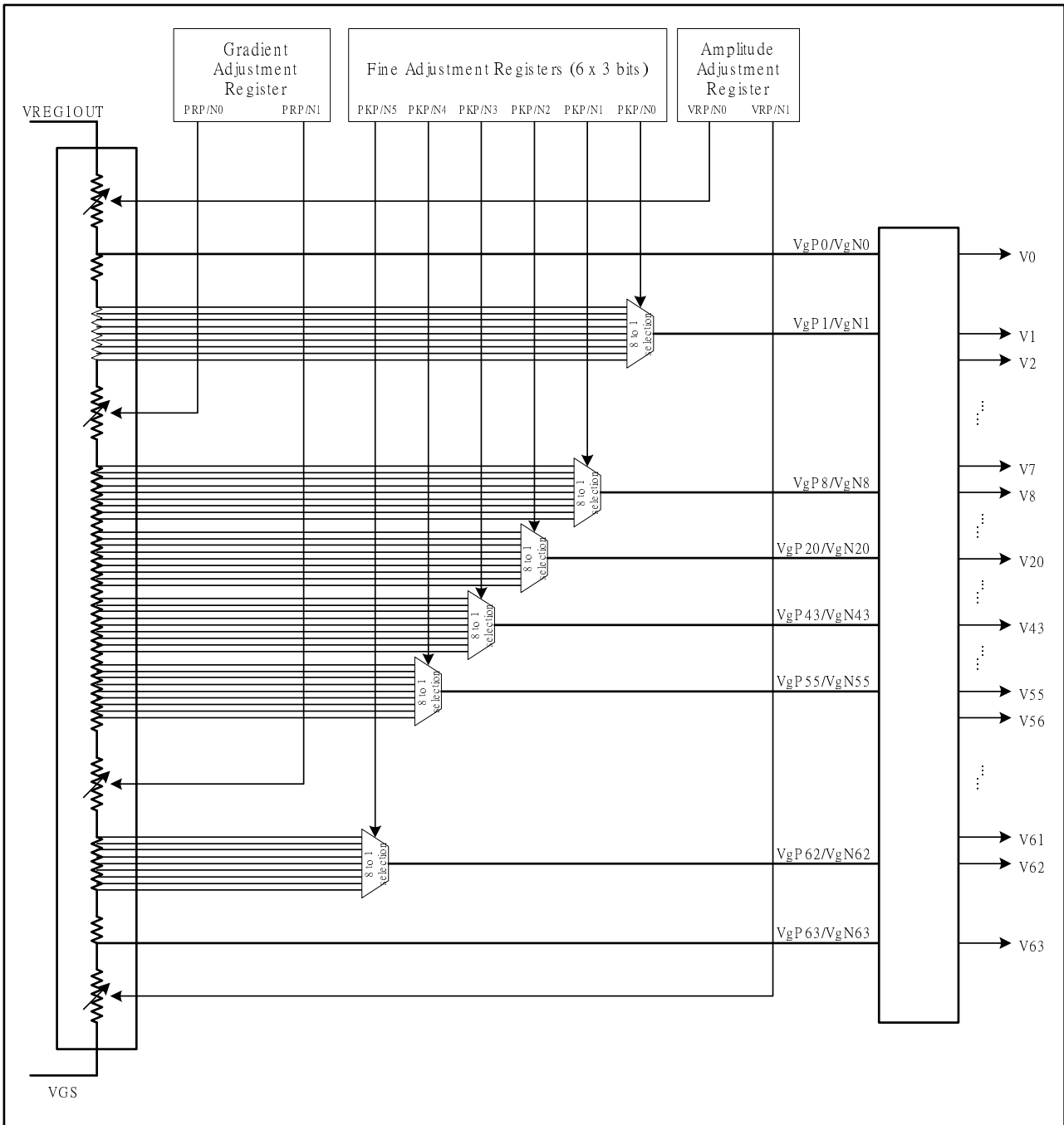


Figure 35 Grayscale Voltage Generation

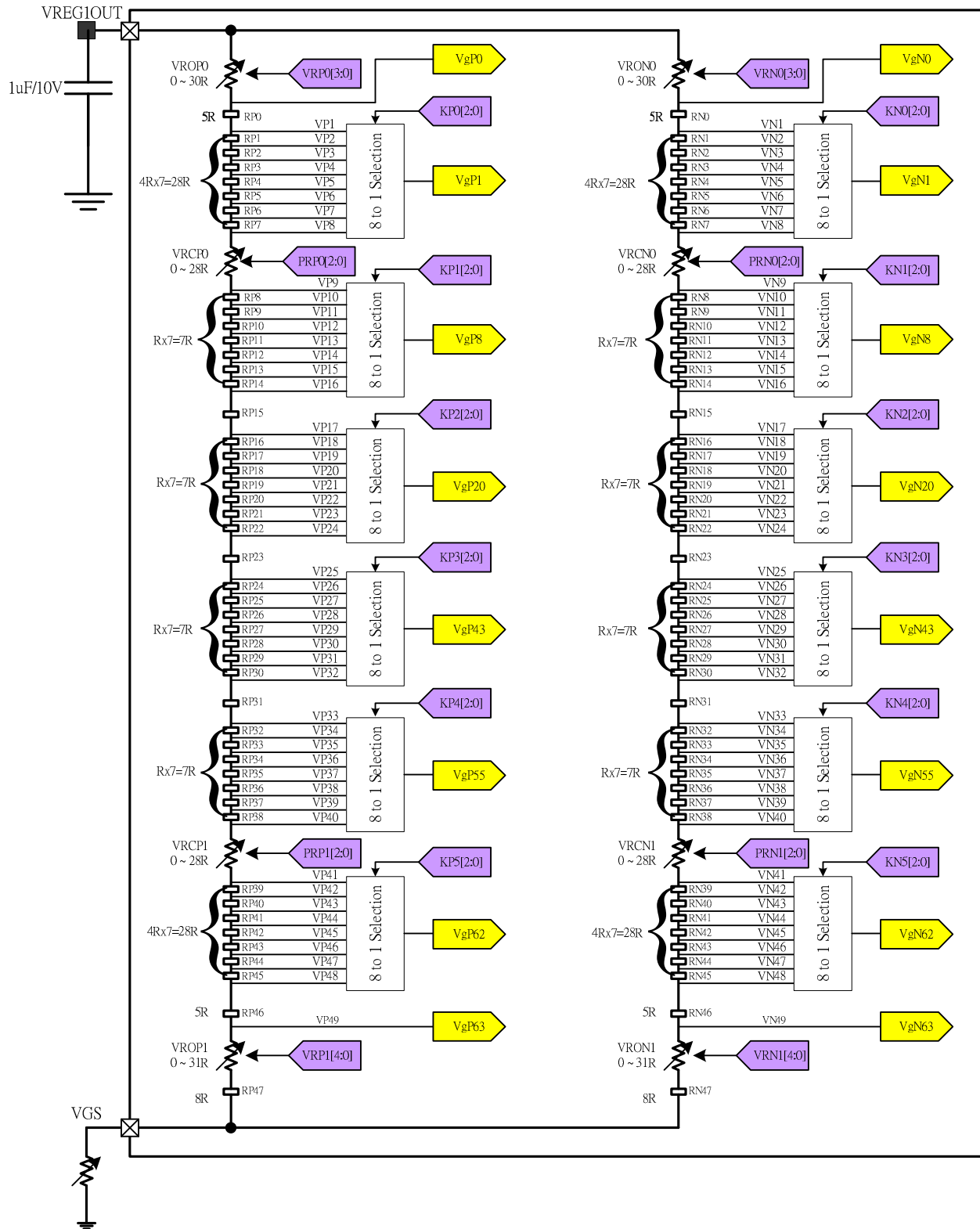


Figure 36 Grayscale Voltage Adjustment

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

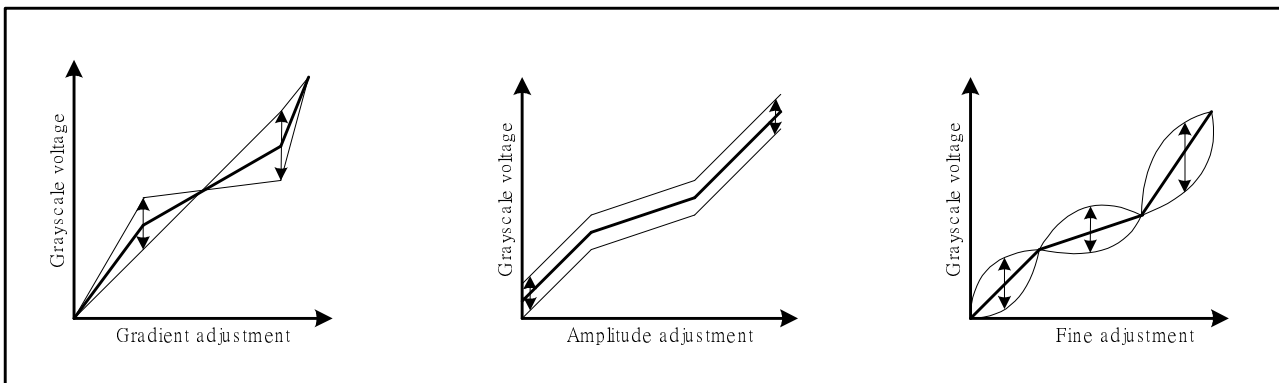


Figure 37 Gamma Curve Adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRCP0, VRCN0
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VROPO, VRON0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ -correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable resistors

ILI9325C uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment	
PRP(N)0/1[2:0] Register	VRCP(N)0/1 Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Amplitude adjustment (1)	
VRP(N)0[3:0] Register	VROP(N)0 Resistance
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1111	28R
1111	30R

Amplitude adjustment (2)	
VRP(N)1[4:0] Register	VROP(N)1 Resistance
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	Selected Voltage					
KP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Fine adjustment registers and selected resistor						
Register	Selected Resistor					
KP(N)[2:0]	RMP(N)0	RMP(N)1	RMP(N)2	RMP(N)3	RMP(N)4	RMP(N)5
000	0R	0R	0R	0R	0R	0R
001	4R	1R	1R	1R	1R	4R
010	8R	2R	2R	2R	2R	8R
011	12R	3R	3R	3R	3R	12R
100	16R	4R	4R	4R	4R	16R
101	20R	5R	5R	5R	5R	20R
110	24R	6R	6R	6R	6R	24R
111	28R	7R	7R	7R	7R	28R

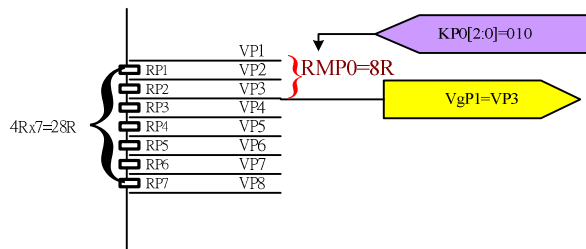


Figure 38 Example of RMP(N)0~5 definition

Gamma correction resistor ratio

Data	Positive polarity output voltage		Negative polarity output voltage	
00h	VP0	(VgP0)	VN0	(VgN0)
01h	VP1	(VgP1)	VN1	(VgN1)
02h	VP2	$(VP8+(VP1-VP8)*(30/48))$	VN2	$(VN8+(VN1-VN8)*(30/48))$
03h	VP3	$(VP8+(VP1-VP8)*(23/48))$	VN3	$(VN8+(VN1-VN8)*(23/48))$
04h	VP4	$(VP8+(VP1-VP8)*(16/48))$	VN4	$(VN8+(VN1-VN8)*(16/48))$
05h	VP5	$(VP8+(VP1-VP8)*(12/48))$	VN5	$(VN8+(VN1-VN8)*(12/48))$
06h	VP6	$(VP8+(VP1-VP8)*(8/48))$	VN6	$(VN8+(VN1-VN8)*(8/48))$
07h	VP7	$(VP8+(VP1-VP8)*(4/48))$	VN7	$(VN8+(VN1-VN8)*(4/48))$
08h	VP8	(VgP8)	VN8	(VgN8)
09h	VP9	$VP20+(VP8-VP20)*(22/24)$	VN9	$VN20+(VN8-VN20)*(22/24)$
0Ah	VP10	$VP20+(VP8-VP20)*(20/24)$	VN10	$VN20+(VN8-VN20)*(20/24)$
0Bh	VP11	$VP20+(VP8-VP20)*(18/24)$	VN11	$VN20+(VN8-VN20)*(18/24)$
0Ch	VP12	$VP20+(VP8-VP20)*(16/24)$	VN12	$VN20+(VN8-VN20)*(16/24)$
0Dh	VP13	$VP20+(VP8-VP20)*(14/24)$	VN13	$VN20+(VN8-VN20)*(14/24)$
0Eh	VP14	$VP20+(VP8-VP20)*(12/24)$	VN14	$VN20+(VN8-VN20)*(12/24)$
0Fh	VP15	$VP20+(VP8-VP20)*(10/24)$	VN15	$VN20+(VN8-VN20)*(10/24)$
10h	VP16	$VP20+(VP8-VP20)*(8/24)$	VN16	$VN20+(VN8-VN20)*(8/24)$
11h	VP17	$VP20+(VP8-VP20)*(6/24)$	VN17	$VN20+(VN8-VN20)*(6/24)$
12h	VP18	$VP20+(VP8-VP20)*(4/24)$	VN18	$VN20+(VN8-VN20)*(4/24)$
13h	VP19	$VP20+(VP8-VP20)*(2/24)$	VN19	$VN20+(VN8-VN20)*(2/24)$
14h	VP20	(VgP20)	VN20	(VgN20)
15h	VP21	$(VP43+(VP20-VP43)*(22/23))$	VN21	$(VN43+(VN20-VN43)*(22/23))$
16h	VP22	$(VP43+(VP20-VP43)*(21/23))$	VN22	$(VN43+(VN20-VN43)*(21/23))$
17h	VP23	$(VP43+(VP20-VP43)*(20/23))$	VN23	$(VN43+(VN20-VN43)*(20/23))$
18h	VP24	$(VP43+(VP20-VP43)*(19/23))$	VN24	$(VN43+(VN20-VN43)*(19/23))$
19h	VP25	$(VP43+(VP20-VP43)*(18/23))$	VN25	$(VN43+(VN20-VN43)*(18/23))$
1Ah	VP26	$(VP43+(VP20-VP43)*(17/23))$	VN26	$(VN43+(VN20-VN43)*(17/23))$
1Bh	VP27	$(VP43+(VP20-VP43)*(16/23))$	VN27	$(VN43+(VN20-VN43)*(16/23))$
1Ch	VP28	$(VP43+(VP20-VP43)*(15/23))$	VN28	$(VN43+(VN20-VN43)*(15/23))$
1Dh	VP29	$(VP43+(VP20-VP43)*(14/23))$	VN29	$(VN43+(VN20-VN43)*(14/23))$
1Eh	VP30	$(VP43+(VP20-VP43)*(13/23))$	VN30	$(VN43+(VN20-VN43)*(13/23))$
1Fh	VP31	$(VP43+(VP20-VP43)*(12/23))$	VN31	$(VN43+(VN20-VN43)*(12/23))$

Data	Positive polarity output voltage		Negative polarity output voltage	
20h	VP32	$(VP43+(VP20-VP43)*(11/23))$	VN32	$(VN43+(VN20-VN43)*(11/23))$
21h	VP33	$(VP43+(VP20-VP43)*(10/23))$	VN33	$(VN43+(VN20-VN43)*(10/23))$
22h	VP34	$(VP43+(VP20-VP43)*(9/23))$	VN34	$(VN43+(VN20-VN43)*(9/23))$
23h	VP35	$(VP43+(VP20-VP43)*(8/23))$	VN35	$(VN43+(VN20-VN43)*(8/23))$
24h	VP36	$(VP43+(VP20-VP43)*(7/23))$	VN36	$(VN43+(VN20-VN43)*(7/23))$
25h	VP37	$(VP43+(VP20-VP43)*(6/23))$	VN37	$(VN43+(VN20-VN43)*(6/23))$
26h	VP38	$(VP43+(VP20-VP43)*(5/23))$	VN38	$(VN43+(VN20-VN43)*(5/23))$
27h	VP39	$(VP43+(VP20-VP43)*(4/23))$	VN39	$(VN43+(VN20-VN43)*(4/23))$
28h	VP40	$(VP43+(VP20-VP43)*(3/23))$	VN40	$(VN43+(VN20-VN43)*(3/23))$
29h	VP41	$(VP43+(VP20-VP43)*(2/23))$	VN41	$(VN43+(VN20-VN43)*(2/23))$
2Ah	VP42	$(VP43+(VP20-VP43)*(1/23))$	VN42	$(VN43+(VN20-VN43)*(1/23))$
2Bh	VP43	(VgP43)	VN43	(VgN43)
2Ch	VP44	$(VP55+(VP43-VP55)*(22/24))$	VN44	$(VN55+(VN43-VN55)*(22/24))$
2Dh	VP45	$(VP55+(VP43-VP55)*(20/24))$	VN45	$(VN55+(VN43-VN55)*(20/24))$
2Eh	VP46	$(VP55+(VP43-VP55)*(18/24))$	VN46	$(VN55+(VN43-VN55)*(18/24))$
2Fh	VP47	$(VP55+(VP43-VP55)*(16/24))$	VN47	$(VN55+(VN43-VN55)*(16/24))$
30h	VP48	$(VP55+(VP43-VP55)*(14/24))$	VN48	$(VN55+(VN43-VN55)*(14/24))$
31h	VP49	$(VP55+(VP43-VP55)*(12/24))$	VN49	$(VN55+(VN43-VN55)*(12/24))$
32h	VP50	$(VP55+(VP43-VP55)*(10/24))$	VN50	$(VN55+(VN43-VN55)*(10/24))$
33h	VP51	$(VP55+(VP43-VP55)*(8/24))$	VN51	$(VN55+(VN43-VN55)*(8/24))$
34h	VP52	$(VP55+(VP43-VP55)*(6/24))$	VN52	$(VN55+(VN43-VN55)*(6/24))$
35h	VP53	$(VP55+(VP43-VP55)*(4/24))$	VN53	$(VN55+(VN43-VN55)*(4/24))$
36h	VP54	$(VP55+(VP43-VP55)*(2/24))$	VN54	$(VN55+(VN43-VN55)*(2/24))$
37h	VP55	(VgP55)	VN55	(VgN55)
38h	VP56	$(VP62+(VP55-VP62)*(44/48))$	VN56	$(VN62+(VN55-VN62)*(44/48))$
39h	VP57	$(VP62+(VP55-VP62)*(40/48))$	VN57	$(VN62+(VN55-VN62)*(40/48))$
3Ah	VP58	$(VP62+(VP55-VP62)*(36/48))$	VN58	$(VN62+(VN55-VN62)*(36/48))$
3Bh	VP59	$(VP62+(VP55-VP62)*(32/48))$	VN59	$(VN62+(VN55-VN62)*(32/48))$
3Ch	VP60	$(VP62+(VP55-VP62)*(25/48))$	VN60	$(VN62+(VN55-VN62)*(25/48))$
3Dh	VP61	$(VP62+(VP55-VP62)*(18/48))$	VN61	$(VN62+(VN55-VN62)*(18/48))$
3Eh	VP62	(VgP62)	VN62	(VgN62)
3Fh	VP63	(VgP63)	VN63	(VgN63)

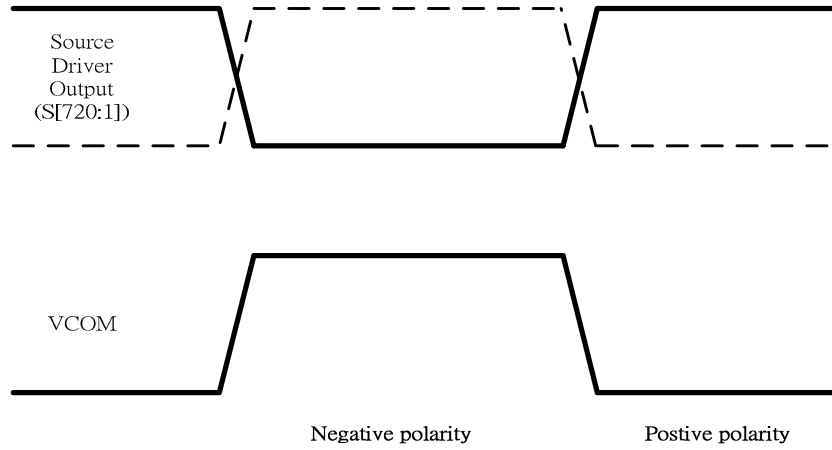


Figure 39 Relationship between Source Output and VCOM

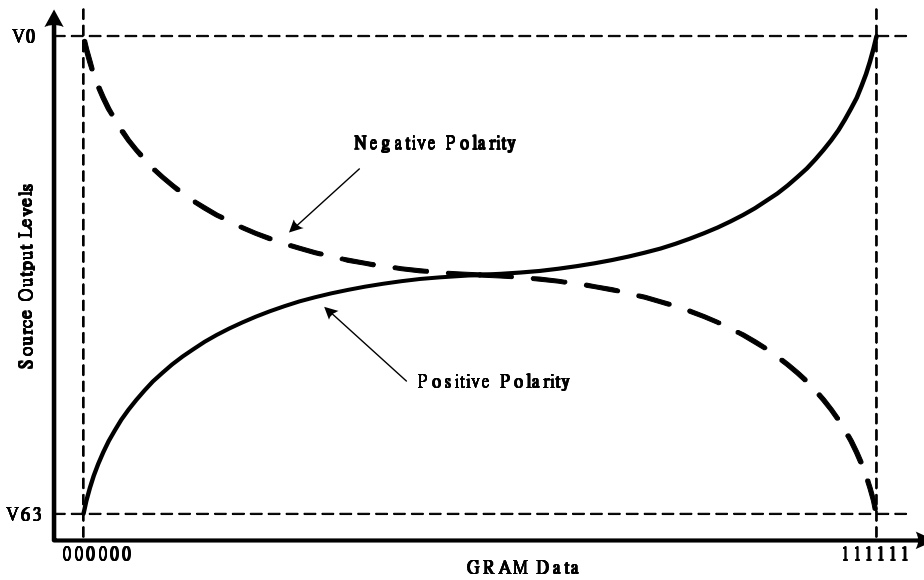


Figure 40 Relationship between GRAM Data and Output Level

13. Application

13.1. Configuration of Power Supply Circuit

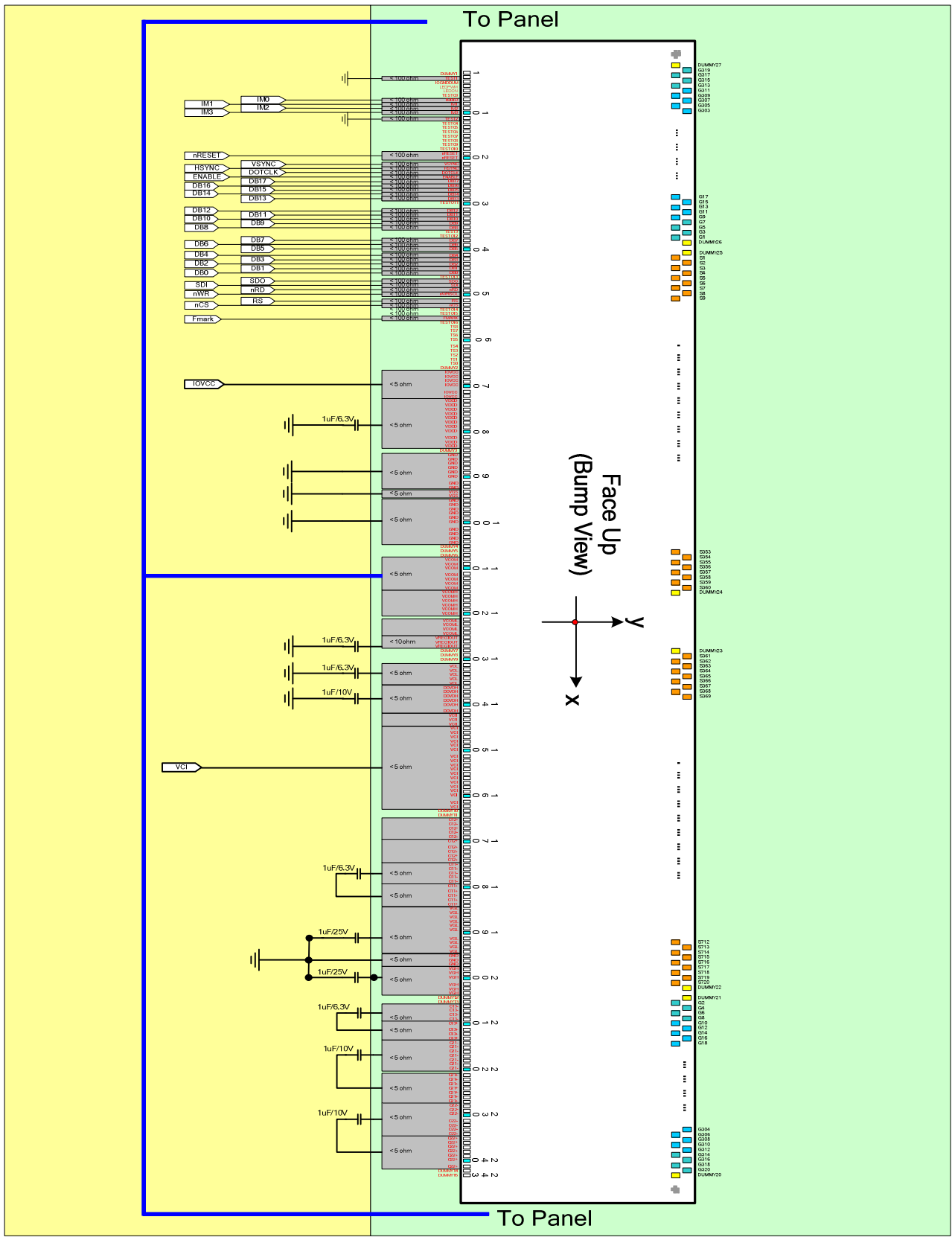


Figure 41 Power Supply Circuit Block

The following table shows specifications of external elements connected to the ILI9325C's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 μ F (B characteristics)	6.3V	VDD, VCL, C11A/B, C13 A/B, VREG1OUT
	10V	DDVDH, C21 A/B, C22 A/B
	25V	VGH, VGL

13.2. Display ON/OFF Sequence

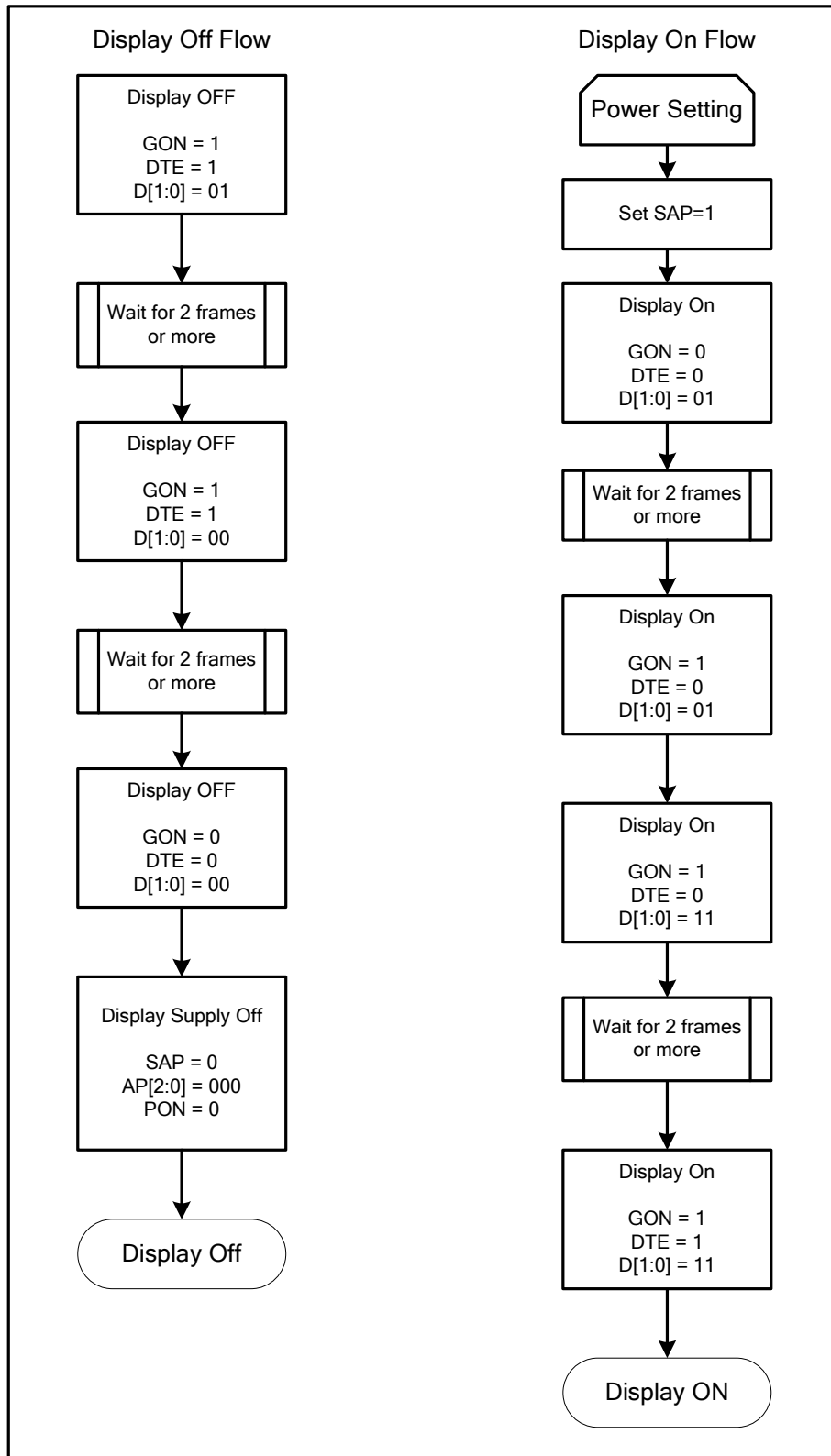


Figure 42 Display On/Off Register Setting Sequence

13.3. Standby and Sleep Mode

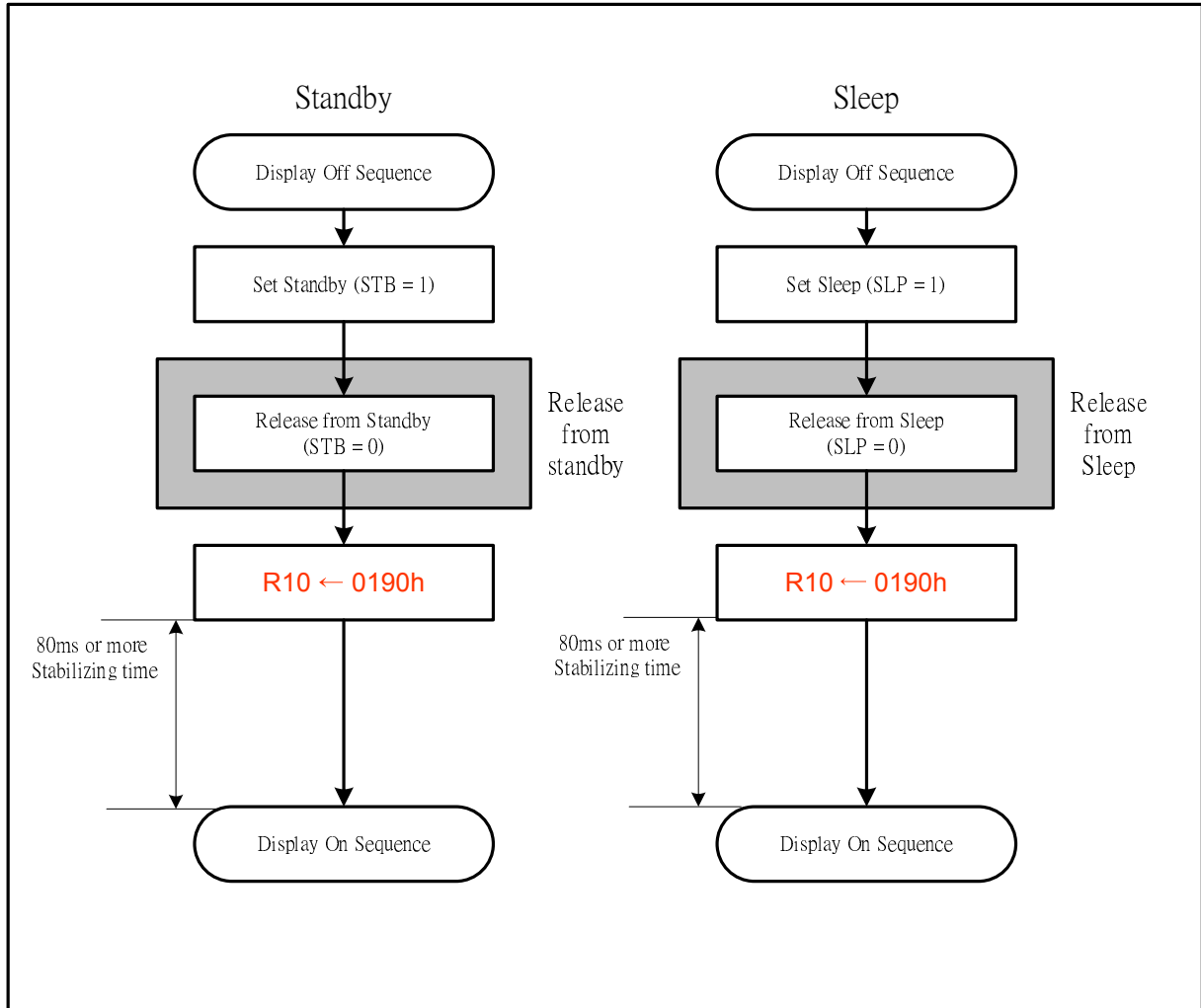


Figure 43 Standby/Sleep Mode Register Setting Sequence

13.4. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.

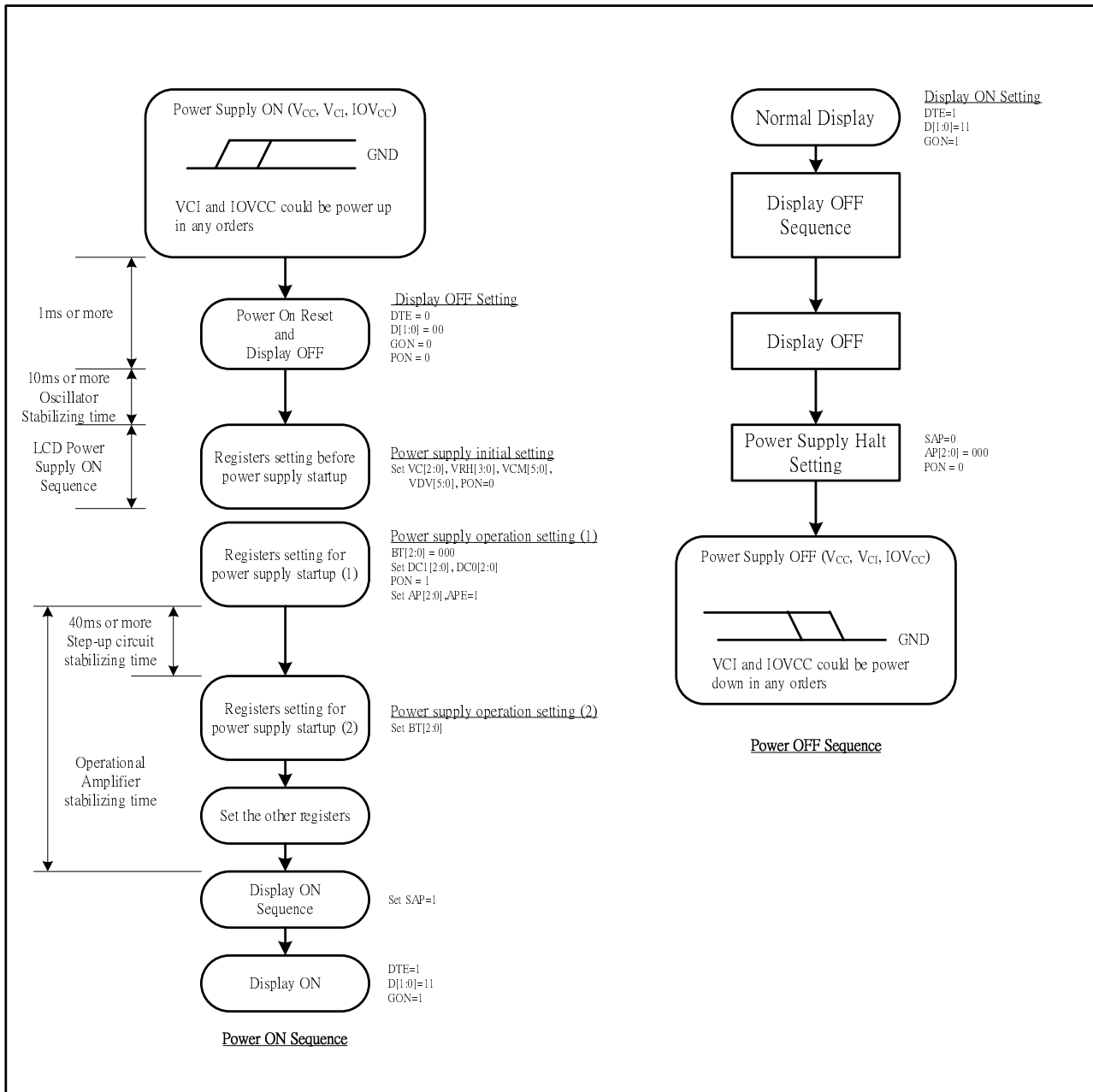


Figure 44 Power Supply ON/OFF Sequence

13.5. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9325C are as follows.

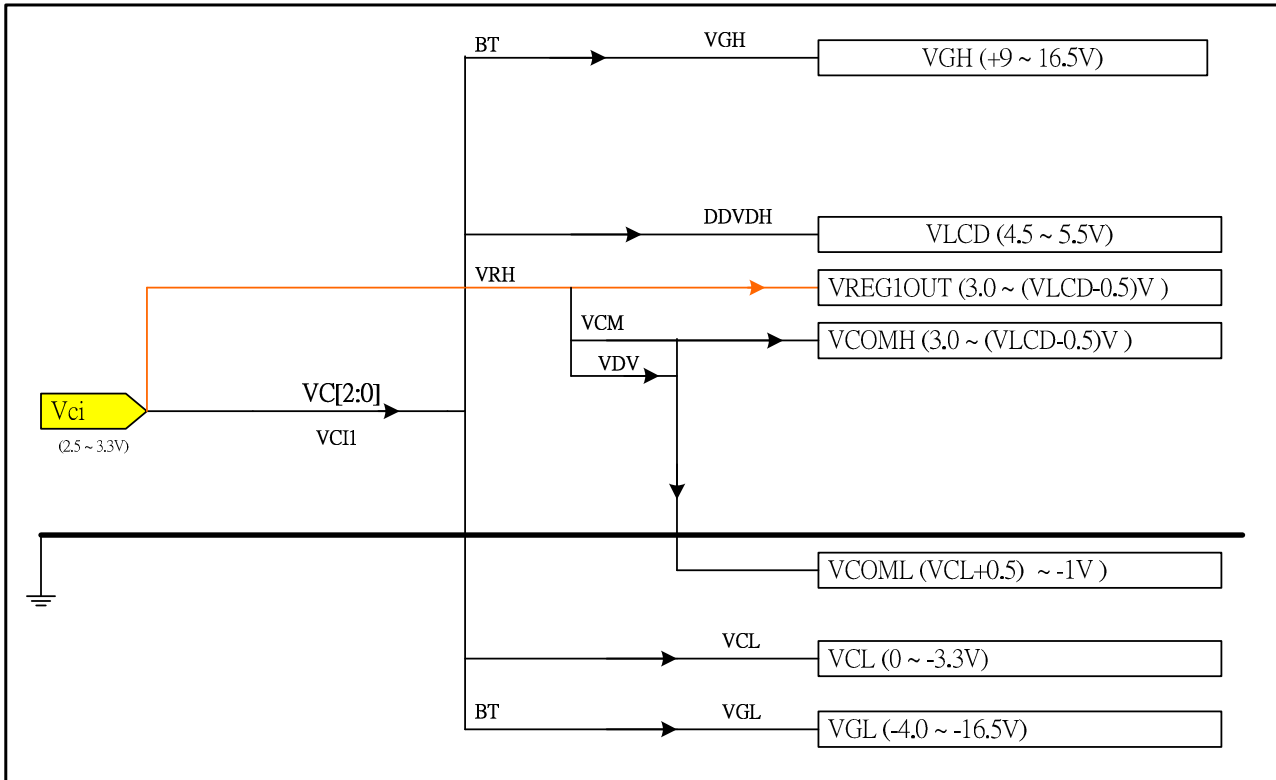


Figure 45 Voltage Configuration Diagram

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships $(DDVDH - VREG1OUT) > 0.2V$ and $(VCOML - VCL) > 0.5V$ are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

13.6. Applied Voltage to the TFT panel

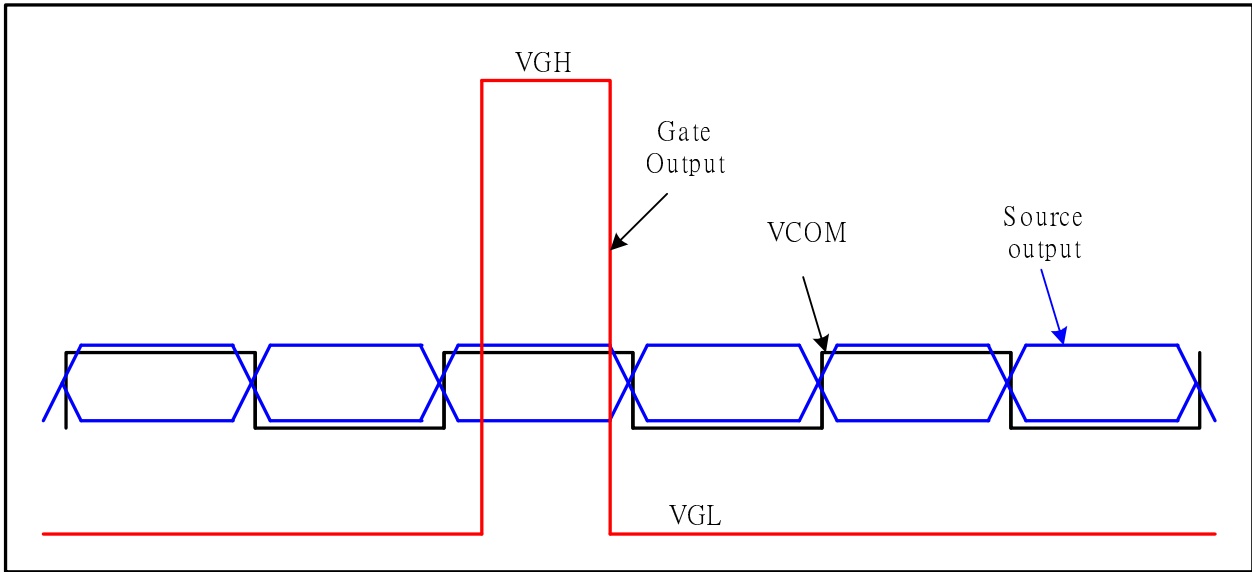


Figure 46 Voltage Output to TFT LCD Panel

13.7. Partial Display Function

The ILI9325C allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Base Image Display Setting	
BASEE	0
NL[5:0]	6'h27
Partial Image 1 Display Setting	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080
Partial Image 2 Display Setting	
PTDE1	1
PTSA1[8:0]	9'h020
PTEA1[8:0]	9'h02F
PTDP1[8:0]	9'h0C0

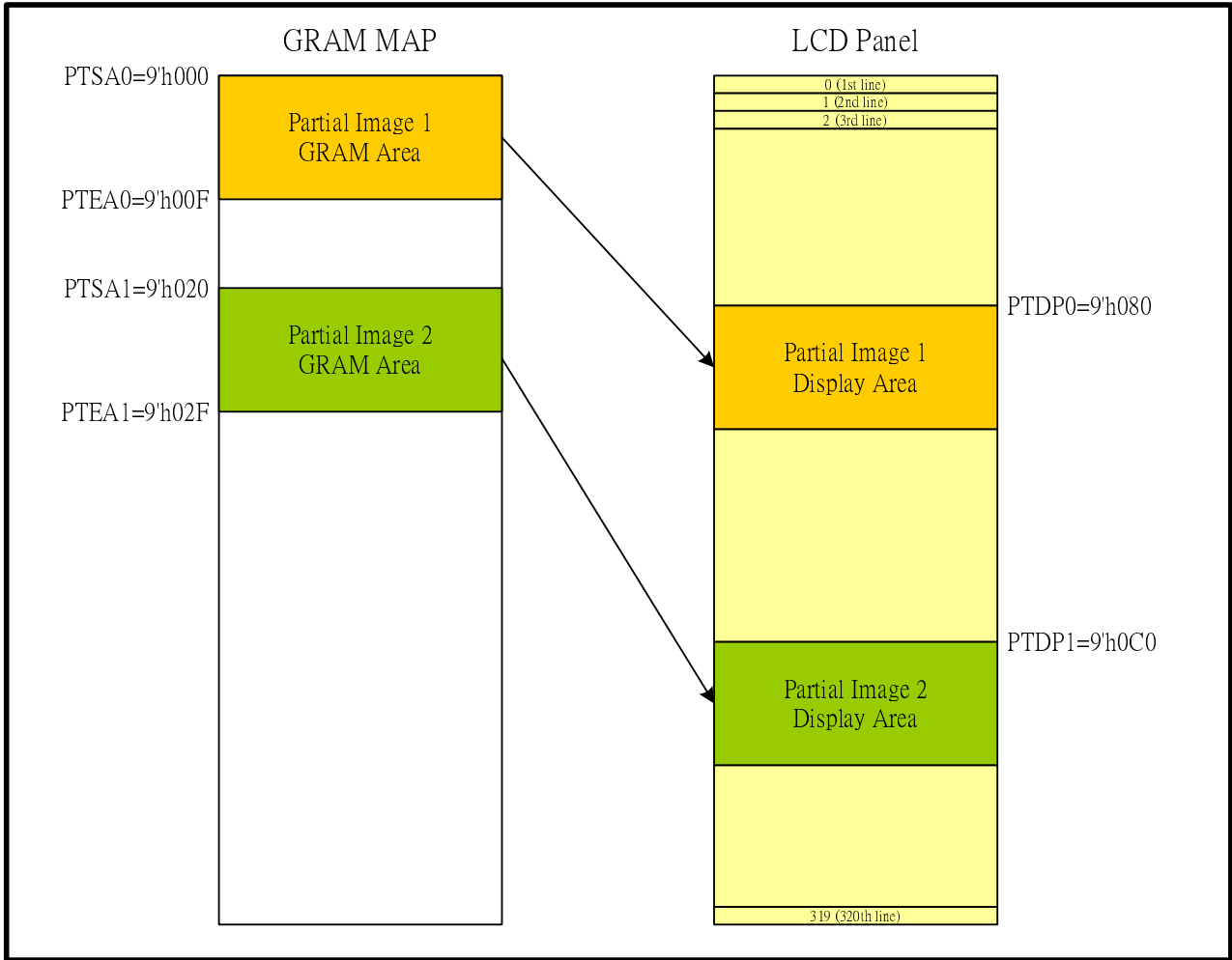


Figure 47 Partial Display Example

14. Electrical Characteristics

14.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9325C is used out of the absolute maximum ratings, the ILI9325C may be permanently damaged. To use the ILI9325C within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9325C will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	IOVCC	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI – GND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	DDVDH – GND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	GND –VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	DDVDH – VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH – VGL	V	0.3 ~ + 30	1, 5
Input voltage	Vt	V	-0.3 ~ VCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:

- GND must be maintained
- (High) (VCC = VCC) ≥ GND (Low), (High) IOVCC ≥ GND (Low).
- Make sure (High) VCI ≥ GND (Low).
- Make sure (High) DDVDH ≥ GND (Low).
- Make sure (High) DDVDH ≥ VCL (Low).
- Make sure (High) VGH ≥ GND (Low).
- Make sure (High) GND ≥ VGL (Low).
- For die and wafer products, specified up to 85°C.
- This temperature specifications apply to the TCP package

14.2. DC Characteristics

(VCC = VCI=2.50 ~ 3.3V, IOVCC = 1.65 ~ 3.30V, Ta= -40 ~ 85 °C)

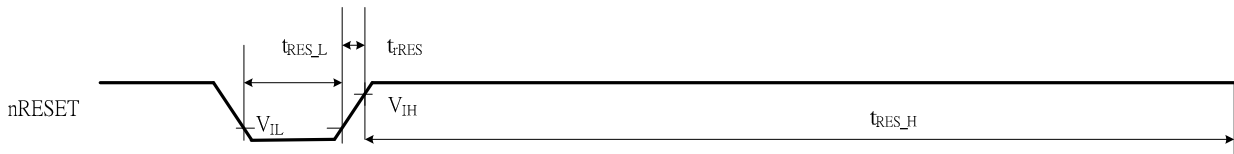
Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V _{IH}	V	IOVCC= 1.65 ~ 3.3V	0.8*IOVCC	-	IOVCC	-
Input low voltage	V _{IL}	V	IOVCC= 1.65 ~ 3.3V	-0.3	-	0.2*IOVCC	-
Output high voltage(1) (DB0-17 Pins)	V _{OH1}	V	IOH = -0.1 mA	0.8*IOVCC	-	-	-
Output low voltage (DB0-17 Pins)	V _{OL1}	V	IOVCC=1.65~3.3V	-	-	0.2*IOVCC	-
I/O leakage current	I _{LI}	μA	Vin = 0 ~ VCC	-0.1	-	0.1	-
Standby Current consumption (VCC - GND)+ (VCI - GND)	I _{ST}	μA	VCC=IOVCC=2.8V , Ta=25 °C	-	40	120	-
Sleep Current consumption (VCC - GND)+ (VCI - GND)	I _{SLP}	μA	VCC=IOVCC=2.8V , Ta=25 °C	-	70	200	-
Current consumption during normal operation (VCC - GND)+ (VCI - GND)	ILCD	mA	VCI=2.8V , VREG1OUT =4.8V DDVDH=5.2V , Frame Rate: 70Hz, line-inversion, Ta=25 °C, GRAM data = 0000h,	-	5.5	-	-
LCD Driving Voltage (DDVDH-GND)	DDVDH	V	-	4.5	-	6	-
Output deviation voltage	V _{DEV}	mV	-	-	-	50	-
Output offset voltage	V _{OFFSET}	mV	Note1	-	-	50	-

Note1: The Max. value is between with measure point and Gamma setting value.

14.3. Reset Timing Characteristics

Reset Timing Characteristics (IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t _{RES_L}	ms	1	-	-
Reset rise time	t _{RES}	μs	-	-	10
Reset high-level width	t _{RES_H}	ms	50	-	-



14.4. AC Characteristics

14.4.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	80	-	-
	Read	t_{CYCR}	ns	300	-	-
Write low-level pulse width	PW_{LW}	ns	50	-	500	-
Write high-level pulse width	PW_{HW}	ns	15	-	-	-
Read low-level pulse width	PW_{LR}	ns	150	-	-	-
Read high-level pulse width	PW_{HR}	ns	150	-	-	-
Write / Read rise / fall time	t_{WRr}/t_{WRf}	ns	-	-	25	-
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-
	Read (RS to nCS, RW/nRD)			5	-	-
Address hold time	t_{AH}	ns	5	-	-	-
Write data set up time	t_{DSW}	ns	10	-	-	-
Write data hold time	t_H	ns	15	-	-	-
Read data delay time	t_{DDR}	ns	-	-	100	-
Read data hold time	t_{DHR}	ns	5	-	-	-

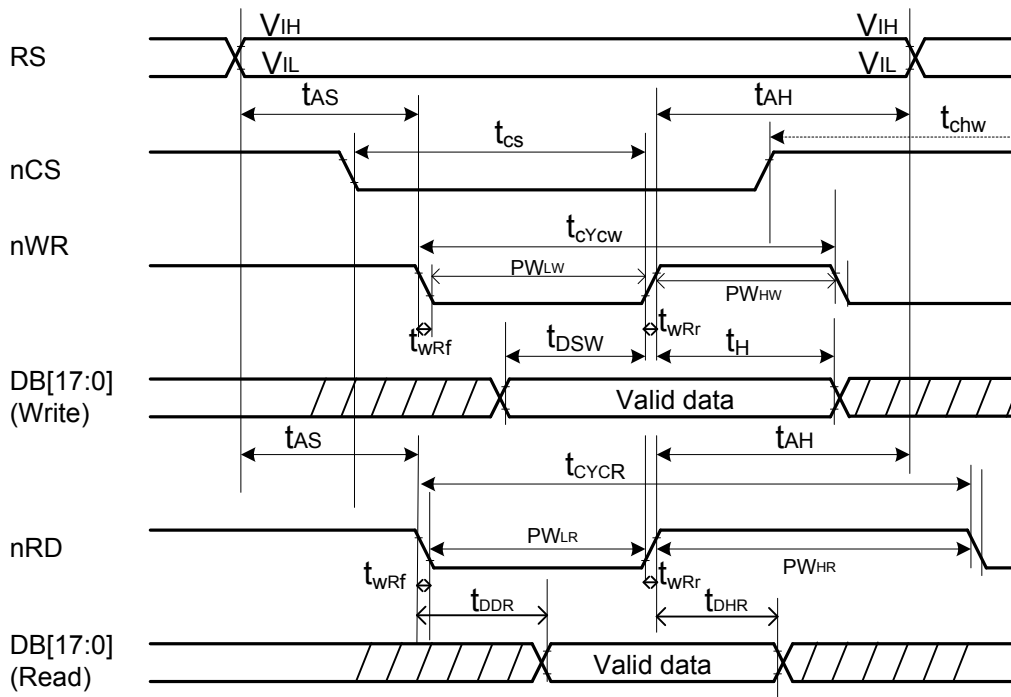


Figure 48 i80-System Bus Timing

14.4.2. Serial Data Transfer Interface Timing Characteristics
(IOVCC= 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	Ns	100	-	-
	Read (transmitted)	t_{SCYC}	ns	200	-	-
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-
	Read (transmitted)	t_{SCH}	ns	100	-	-
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-
	Read (transmitted)	t_{SCL}	ns	100	-	-
Serial clock rise / fall time	t_{SCR}, t_{SCF}	ns	-	-	5	
Chip select set up time	t_{CSU}	ns	10	-	-	
Chip select hold time	t_{CH}	ns	50	-	-	
Serial input data set up time	t_{SISU}	ns	20	-	-	
Serial input data hold time	t_{SIH}	ns	20	-	-	
Serial output data set up time	t_{SOD}	ns	-	-	100	
Serial output data hold time	t_{SOH}	ns	5	-	-	

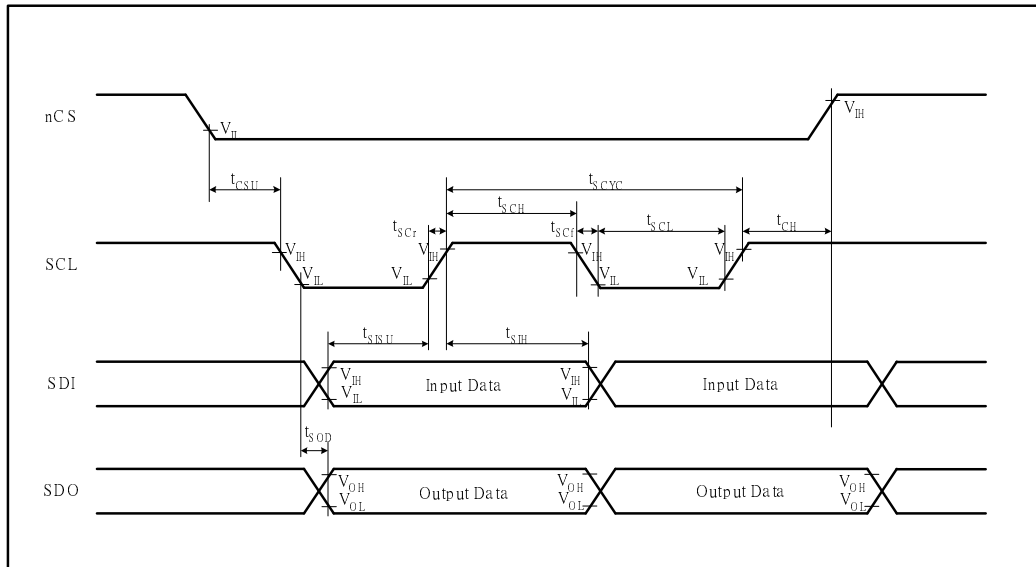


Figure 49 SPI System Bus Timing

14.4.3. RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

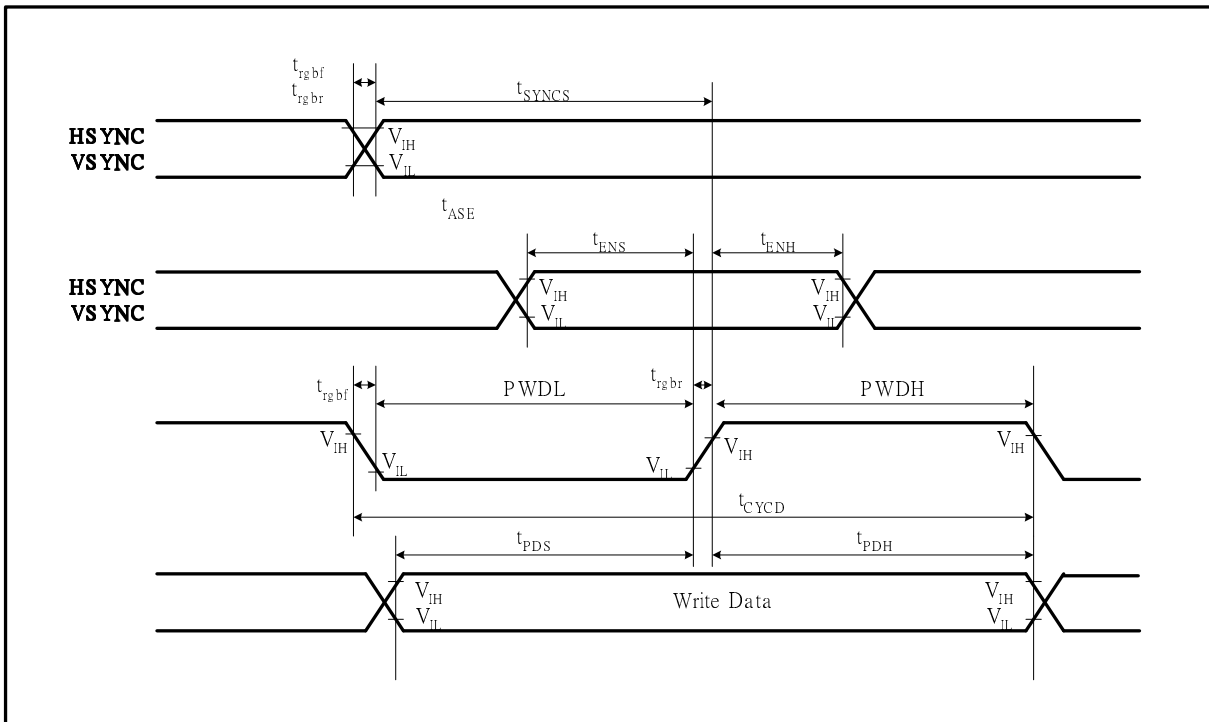


Figure50 RGB Interface Timing

