3 Device Pin Out and Signal Description

3.1 20-LD QFN Package

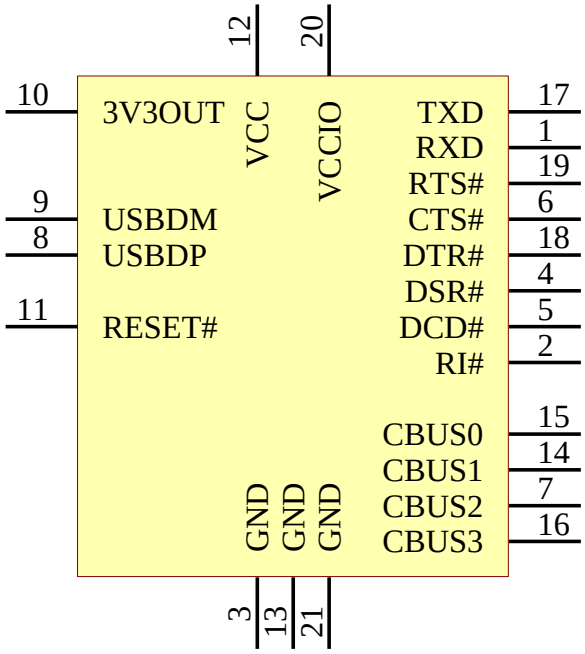


Figure 3.1 QFN Schematic Symbol

3.1.1 QFN Package PinOut Description

Note: # denotes an active low signal.

Pin No.	Name	Type	Description
12	** VCC	POWER Input	5 V or 3V3 supply to IC
20	VCCIO	POWER Input	1V8 – 3V3 supply for the IO cells
10	** 3V3OUT	POWER Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3; pin 10 is an input pin and should be connected to pin 12.
3, 13	GND	POWER Input	0V Ground input.

Table 3.1 Power and Ground

*Pin 21 on the symbol is the pad under the centre of the chip package and should be connected to GND

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

参考資料

Pin No.	Name	Type	Description
9	USBDM	INPUT	USB Data Signal Minus.
8	USBDP	INPUT	USB Data Signal Plus.
11	RESET#	INPUT	Reset input (active low).

Table 3.2 Common Function pins

Pin No.	Name	Type	Description
17	TXD	Output	Transmit Asynchronous Data Output.
1	RXD	Input	Receiving Asynchronous Data Input.
19	RTS#	Output	Request to Send Control Output / Handshake Signal.
6	CTS#	Input	Clear To Send Control Input / Handshake Signal.
18	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
4	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
5	DCD#	Input	Data Carrier Detect Control Input.
2	RI#	Input	Ring Indicator input for remote wake up.
15	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. The default configuration is TXDEN. See CBUS Signal Options, Table 3.7.
14	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. The default configuration is RXLED#. See CBUS Signal Options, Table 3.7.
7	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. The default configuration is TXLED#. See CBUS Signal Options, Table 3.7.
16	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. The default configuration is SLEEP#. See CBUS Signal Options, Table 3.7.

Table 3.3 UART Interface and CBUS Group (see note 1)

Notes:

1 When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the MTP memory.

3.2 20-LD SSOP Package

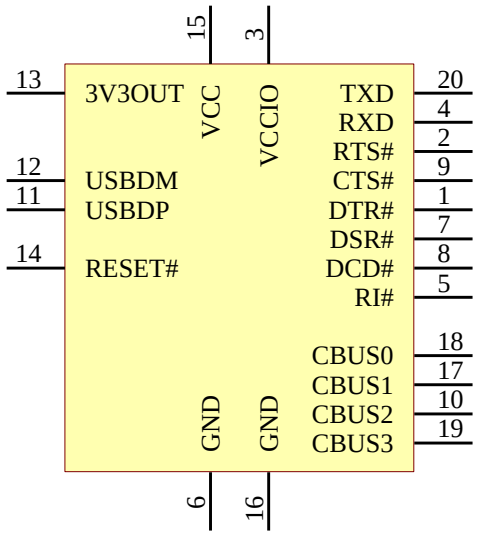


Figure 3.2 SSOP Schematic Symbol

3.2.1 SSOP Package PinOut Description

Note: # denotes an active low signal.

Pin No.	Name	Type	Description
15	** VCC	POWER Input	5 V or 3V3 supply to IC
3	VCCIO	POWER Input	1V8 – 3V3 supply for the IO cells
13	** 3V3OUT	POWER Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3, pin 13 is an input pin.
6, 16	GND	POWER Input	0V Ground input.

Table 3.4 Power and Ground

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

Pin No.	Name	Type	Description
12	USBDM	INPUT	USB Data Signal Minus.
11	USBDP	INPUT	USB Data Signal Plus.
14	RESET#	INPUT	Reset input (active low).

Table 3.5 Common Function pins

参考資料

Pin No.	Name	Type	Description
20	TXD	Output	Transmit Asynchronous Data Output.
4	RXD	Input	Receiving Asynchronous Data Input.
2	RTS#	Output	Request to Send Control Output / Handshake Signal.
9	CTS#	Input	Clear To Send Control Input / Handshake Signal.
1	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
7	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
8	DCD#	Input	Data Carrier Detect Control Input.
5	RI#	Input	Ring Indicator input for remote wake up.
18	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. The default configuration is TXDEN. See CBUS Signal Options, Table 3.7.
17	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. The default configuration is RXLED#. See CBUS Signal Options, Table 3.7.
10	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. The default configuration is TXLED#. See CBUS Signal Options, Table 3.7.
19	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. The default configuration is SLEEP#. See CBUS Signal Options, Table 3.7.

Table 3.6 UART Interface and CBUS Group (see note 1)

Notes:

1 When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the MTP memory.

3.3 CBUS Signal Options

参考資料

CBUS Signal Option	Available On CBUS Pin	Description
Time Stamp	CBUS0, CBUS1, CBUS2, CBUS3	Toggle signal which changes state each time a USB SOF is received
Keep_Awake#	CBUS0, CBUS1, CBUS2, CBUS3	Prevents the device from entering suspend state when unplugged.

Table 3.7 CBUS Configuration Control

*When in USB suspend mode the outputs clocks are also suspended.

5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT231X devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-65°C to 150°C	Degrees C	
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours	
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C	
MTTF FT231XS	TBD	Hours	
MTTF FT231XQ	TBD	Hours	
VCC Supply Voltage	-0.3 to +5.5	V	
VCCIO IO Voltage	-0.3 to +4.0	V	
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V	
DC Input Voltage – High Impedance Bi-directionals (powered from VCCIO)	-0.3 to +5.8	V	
DC Output Current – Outputs	22	mA	
ESD Charge Device Mode(CDM)	500	V	Class III
ESD Human Body Mode (HDM)	2000	V	Class 2

Table 5.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 ESD and Latch-up Specifications

Description	Specification
Human Body Mode (HBM)	**> ± 2kV**
Machine mode (MM)	**> ± 200V**
Charged Device Mode (CDM)	**> ± 500V**
Latch-up	**> ± 200mA**

Table 5.2 ESD and Latch-Up Specifications

参考資料

5.3 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC	VCC Operating Supply Voltage	2.97	5	5.5	V	Normal Operation
VCC2	VCCIO Operating Supply Voltage	1.62	---	3.63	V	
Icc1	Operating Supply Current	8	8	8.4	mA	Normal Operation
Icc2	Operating Supply Current		125		µA	USB Suspend
3V3	3.3v regulator output	2.97	3.3	3.63	V	VCC must be greater than 3V3 otherwise 3V3OUT is an input which must be driven with 3.3V

Table 5.3 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.97	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	2.0			V	LVTTL
Vt	Switching Threshold		1.49		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		1.15		V	
Vt+	Schmitt trigger positive going threshold voltage		1.64		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 5.4 I/O Pin Characteristics VCCIO = +3.3V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

参考資料

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.25	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	0.8			V	LVTTL
Vt	Switching Threshold		1.1		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.8		V	
Vt+	Schmitt trigger positive going threshold voltage		1.2		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 5.5 I/O Pin Characteristics VCCIO = +2.5V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

参考資料

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.62	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.77	V	LVTTL
Vih	Input High Switching Threshold	1.6			V	LVTTL
Vt	Switching Threshold		0.77		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.557		V	
Vt+	Schmitt trigger positive going threshold voltage		0.893		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 5.6 I/O Pin Characteristics VCCIO = +1.8V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCC-0.2			V	
Vol	Output Voltage Low			0.2	V	
Vil	Input low Switching Threshold		-	0.8	V	
Vih	Input High Switching Threshold	2.0	-		V	

Table 5.7 USB I/O Pin (USBDP, USBDM) Characteristics

5.4 MTP Memory Reliability Characteristics

The internal 2048 Byte MTP memory has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	10	Years
Write Cycle	2,000	Cycles
Read Cycle	Unlimited	Cycles

Table 5.8 MTP Memory Characteristics

5.5 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Table 5.9 Internal Clock Characteristics

Note 1: Equivalent to +/-1667ppm

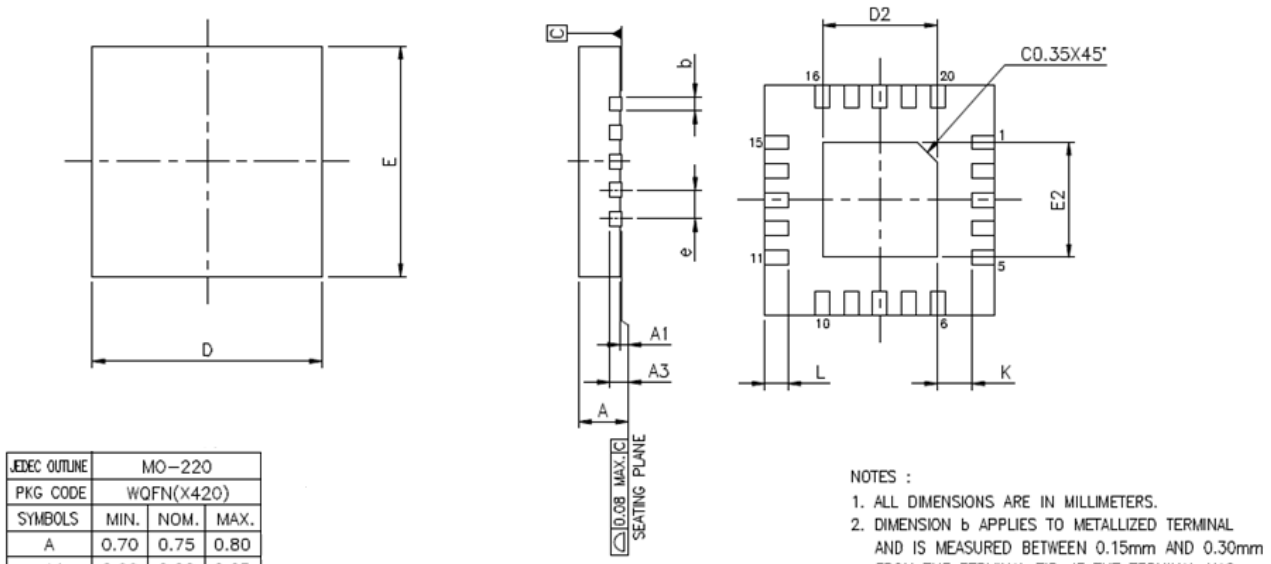
参考資料

Parameter	Value	Notes
CBUS Drive Current Strength	4mA	Options are 4mA, 8mA, 12mA, 16mA
CBUS slew rate	Slow	Options are slow or fast
CBUS Schmitt Trigger Enable	Normal	Options are normal or Schmitt
Load VCP Driver	Enabled**	Makes the device load the VCP driver interface for the device.
CBUS0	TXDEN	Default configuration of CBUS0 – Transmit data enable for RS485
CBUS1	RXLED#	Default configuration of CBUS1 – Receive LED drive.
CBUS2	TXLED#	Default configuration of CBUS2 – Transmit LED drive.
CBUS3	SLEEP#	Default configuration of CBUS3 – SLEEP#. Logic 0 when the device is in suspend.
Invert TXD	Disabled	Signal on this pin becomes TXD# if enable.
Invert RXD	Disabled	Signal on this pin becomes RXD# if enable.
Invert RTS#	Disabled	Signal on this pin becomes RTS if enable.
Invert CTS#	Disabled	Signal on this pin becomes CTS if enable.
Invert DTR#	Disabled	Signal on this pin becomes DTR if enable.
Invert DSR#	Disabled	Signal on this pin becomes DSR if enable.
Invert DCD#	Disabled	Signal on this pin becomes DCD if enable.
Invert RI#	Disabled	Signal on this pin becomes RI if enable.

Table 8.1 Default Internal MTP Memory Configuration

**VCP disabled in Rev B silicon in error.

9.3 QFN-20 Package Mechanical Dimensions



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X420)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.20	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
K	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	E2			D2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
114X114 MIL	1.90	2.00	2.05	1.90	2.00	2.05	0.30	0.40	0.50	V	V	W(V)GGD-1

Figure 9.3 QFN-20 Package Dimensions

The FT231XQ is supplied in a RoHS compliant leadless QFN-20 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 4.00mm x 4.00mm. The solder pads are on a 0.50mm pitch. The above mechanical drawing shows the QFN-20 package. All dimensions are in millimetres.

The centre pad on the base of the FT231XQ is internally connected to ground.

9.4 QFN-20 Package Markings

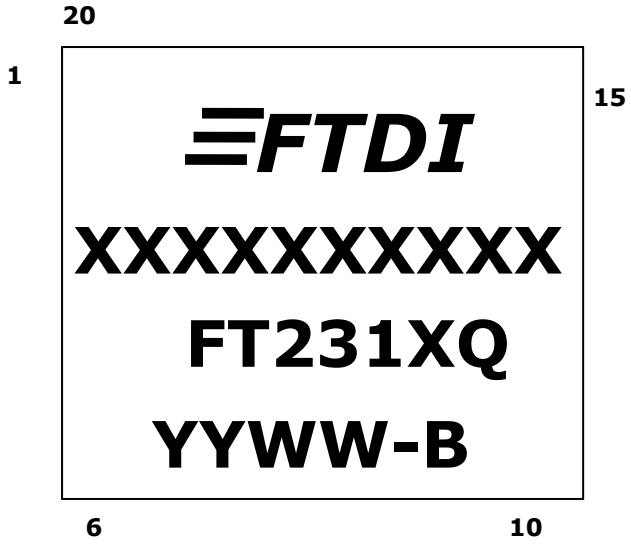


Figure 9.4 QFN-20 Package Markings

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number. This is followed by the revision number.

The code **XXXXXXX** is the manufacturing LOT code.

9.5 Solder Reflow Profile

The FT231X is supplied in Pb free 20 LD SSOP and QFN-20 packages. The recommended solder reflow profile for both package options is shown in Figure 9.5.

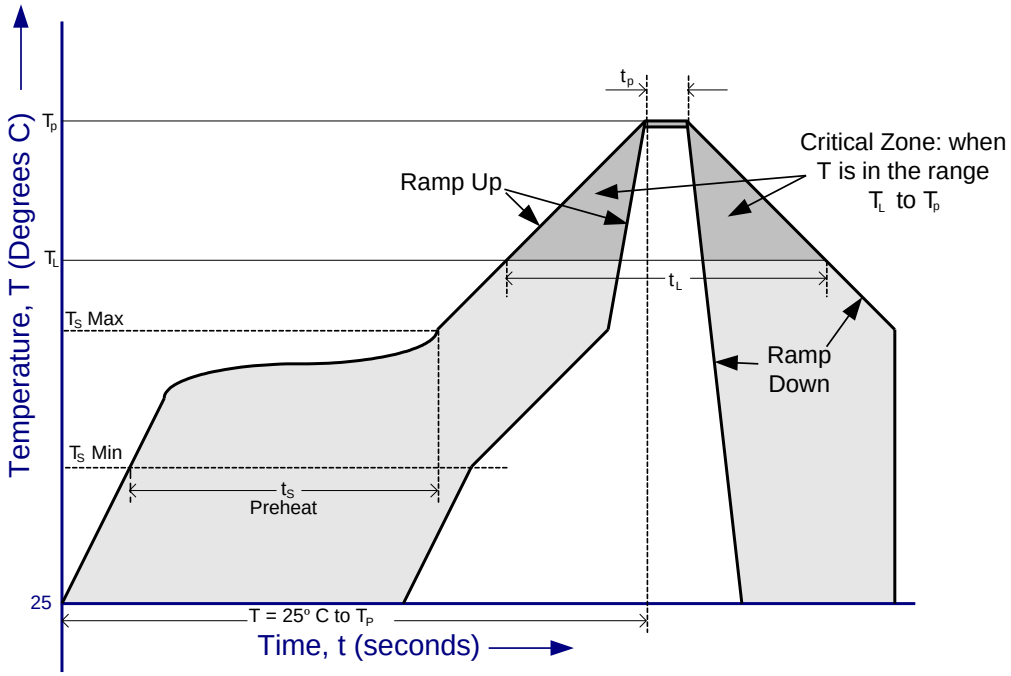


Figure 9.5 FT231X Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 9.1. Values are shown for both a completely Pb free solder process (i.e. the FT231X is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT231X is used with non-Pb free solder).

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 9.1 Reflow Profile Parameter Values

参考資料

List of Figures

List of Tables

参考資料

Appendix C – Revision History

Document Title:	USB to FULL HANDSHAKE UART IC FT231X
Document Reference No.:	FT_000565
Clearance No.:	FTDI# 261
Product Page:	http://www.ftdichip.com/FT-X.htm
Document Feedback:	Send Feedback

Version Draft	Initial draft available	2nd December 2011
Version 1.0	Initial release	8th February 2012
Version 1.1	Added USB compliance in section 1.3 Clarified MTP Reliability in table 5.8 Section 8.1, Added a Note "VCP disabled in Rev B Silicon in error	17th April 2012
Version 1.2	updated front page to clarify 5V tolerant Updated TID	15 February 2013