Honeywell Magnetic Sensor Products

Electronic Compass Design Guide Using The HMC5843 Digital Compass IC

Honeywell

Introduction

The HMC5843 Digital Compass IC is highly integrated 3-axis magnetic sensor with an Application Specific Integrated Circuit (ASIC) for measuring low magnetic field strengths, like the earth's magnetic field, and providing a digital numeric representation for interfacing with microprocessors. This design guide includes a designer's perspective on performance tradeoffs, reference circuit layouts, software code routines, and design tips to ensure a successful electronic compass assembly.

This design guide starts with basic assumptions of an electronic compass of moderate accuracy, with focus on keeping the costs minimal, and the component footprint small as possible. If these assumptions do not fit your desires, please feel free to consult with Honeywell's technical personnel to access more resources suitable to your design requirements. Also avail yourself to www.magneticsensors.com were the HMC5843 datasheet is located, along with many application notes and technical paper relating to compassing and navigation.

Process

Designing in the HMC5843 is meant to be a straightforward process when used in many applications. For handheld devices, the HMC5843 will work very well if strategically located in a magnetically quiet part of the product. The end objective is to be able to measure the ever present earth's magnetic field direction. However some normal design practices have to be scrutinized to not spoil the earth magnetic fields penetrating the product with the compass IC inside. While most electrical technicians and engineers can visualize the unseen currents in circuit conductors, grasping the idea of magnetic lines of flux flowing and emanating from circuit boards proves more difficult.

Once a candidate location or locations have been found for the HMC5843 Compass IC, it is recommended that prototype boards be constructed with the HMC5843 used to collect the localized magnetic field data at various orientations. Good locations will show little circuitry generated fields and mostly clean earth's field following sinusoidal patterns when rotated. Designers may also procure the HMC5843 demonstration board, and use the HMC5843 at the tip of the board to "sniff" the board components and locations for the quietest candidate locations for compass IC mounting. Things to avoid are ferrous metal RF shielding, steel chassis fasteners, vibrator/motors, dynamic microphones, and dynamic speakers without motor shielding. These items and more will either bend/distort the earth's magnetic lines of flux, or generate there own lines of flux creating a magnetic bias that must be calibrated out.

When the final location is determined, the HMC5843 orientation is the next step in the process. While some board layout auto-routing software will position the compass IC for shortest circuit trace routes, it is suggested that this part orientation be manually placed so that the X-axis direction on the HMC5843 be the same as the forward mechanical direction of the end product. This is so when an end-user points and clicks the product, the reference compass heading is directly read from the compassing algorithm without rotational corrections. If the HMC5843 can not be oriented for best direction, the output data can be re-polarized and rotational offsets employed to correct for forward direction.

Finally, the XYZ axis data from the HMC5843 can be collected by the application processor, and software routines written to interpret the data as required for heading output. The notes section will contain the math routines needed for heading computation from the raw magnetic data provided. Also the hard-iron calibration routine is described to arrive at data offsets to handle magnetic bias fields. While we offer no canned source code for free, the routines to be written are very basic in structure and follow the math equations. Source code under license is also available for heading computation and hard-iron calibration routines.

Notes

Spacing Between Compass IC and Other Components

Integration of a magnetic compass is not a simple task when placed within other circuitry for the end product. Many consumer electronic products have shielded Radio Frequency (RF) circuits, speakers with magnets, and motors with unknown amounts of magnetic leakage. In an ideal arrangement, the HMC5843 would be located in a magnetically quiet location, reasonably far away from magnets, motors, and ferrous metal RF shields that could distort the earth's magnetic field from flowing cleanly through the circuitry. Also most surface-mount electronic components contain the ferrous metal nickel as barrier plating between a copper under-metal and a tin/solder solderable contact. Because nickel can not be avoided in circuit board designs, it is important that the HMC5843 be given a couple millimeters space between the nickel

bearing components and the HMC5843. This also includes back-side components on a circuit board. See Figure 1 for a depiction of magnetic distortion of the earth's magnetic lines of flux.

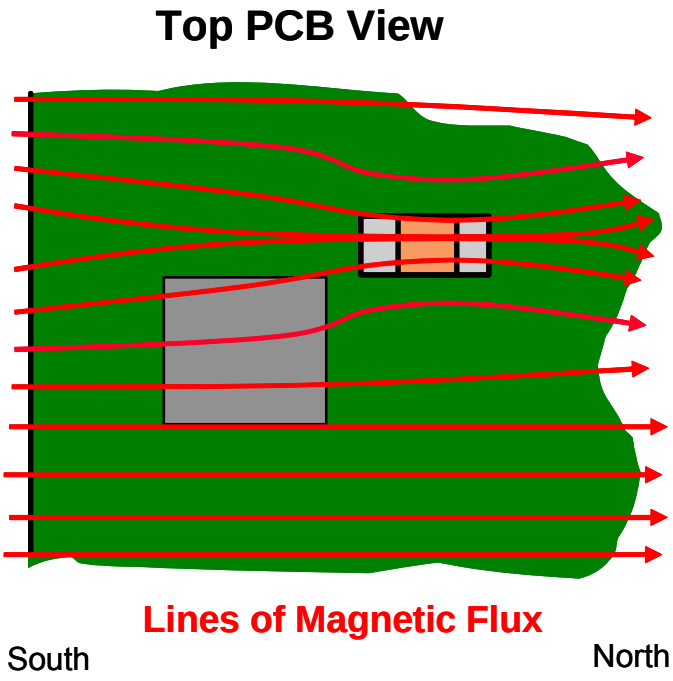


Figure 1 – Magnetic Distortion From Nickel Plating

To determine the correct amount of sensor standoff from the plating, a two-to-one rule of thumb is used. For example a 0805 resistor, like the resistor shown in Figure 1, has a 50 mil (1.27mm) wide solder end cap with a nickel under-plating causing the magnetic distortion. By placing the resistor at least 100 mil (2.54mm) away, the nickel will have less than a 1% distortion effect on the sensor IC.

Spacing Between Compass IC and High Current Wiring

Besides well foreseen magnetic distortion sources from components, high currents in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing. The HMC5843 or other magnetic sensors can not discern between earth's magnetic field and adjacent conductor generated magnetic fields, as these fields will add together; making errors in compass heading computation. Another rule of thumb is to keep currents higher than 10 milli-amperes a few millimeters further away from the sensor IC. Figure 2 depicts how circuit trace circuits circulate on a board how they flow through adjacent components.

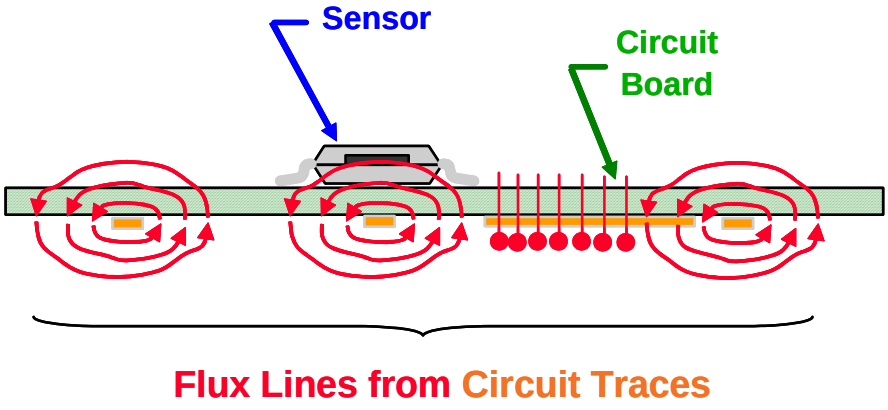


Figure 2 – Circuit Trace Magnetic Fields

Orientation of Compass IC and End Product

The HMC5843 Compass IC contains separate magnetic sensor die along with an ASIC for analog signal processing and digitization. Because compassing is a direction sensitive function, and "pointing" your product uses the compass directionality; it is convenient to orient the HMC5843 sensitive axis to the "forward" part of the end product assembly. In most cases, it means the HMC5843's X-axis will be in this forward direction. Figure 3 shows the top view of the HMC5843 and its reference sensitive axis.

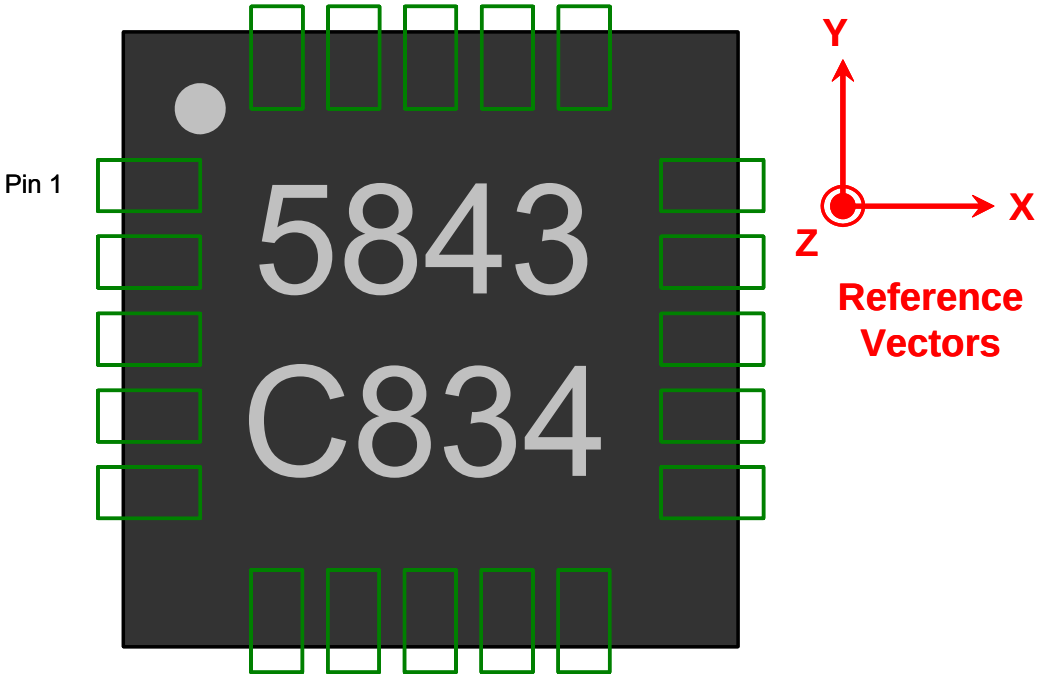


Figure 3 – Top View HMC5843

When compassing, at least two or three magnetic vectors are used to determine the forward direction of the product relative to the earth's magnetic south to north direction. When held level (Z is constant), the X and Y magnetic vectors carve out cosine and sine functions when rotated. When pointed to magnetic north the X magnetic output is at its maximum positive value in Analog-to-Digital Converter (ADC) counts, and the Y magnetic output is centered up at a near zero ADC counts. Figure 4 shows a typical swing of X and Y compass outputs with rotation.

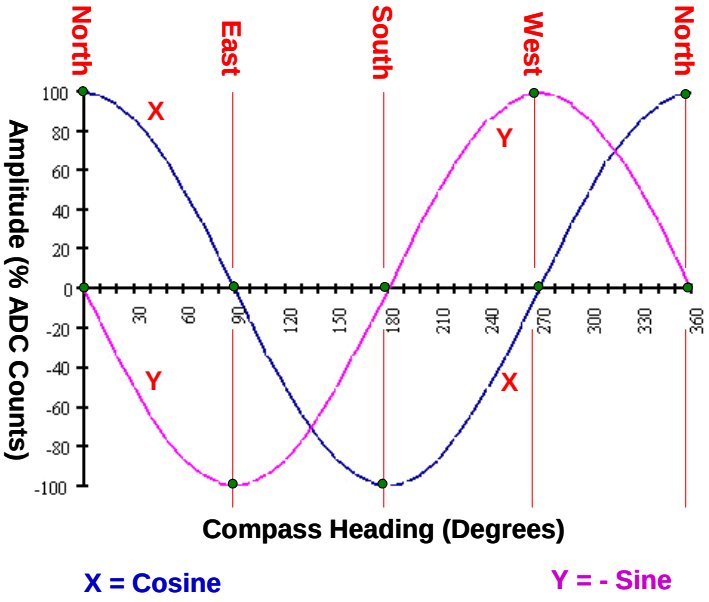


Figure 4 – Compass Curves

Because the HMC5843 magnetic sensors have the X and Y vectors flipped (X leads the Y by 90 degrees), the part does not match the compass curves shown in Figure 4. To make the match, the data from the HMC5843 Y-axis must be polarity flipped. For example a value of +89 ADC counts must become -89 counts to turn the positive sine function into the negative sine function.

To show how this works in an electrical design, Figure 5 depicts an outline of a handheld wireless phone with a single horizontal circuit board inside. By orienting the HMC5843 X-axis in forward/top end of the phone, the end customers can point the phone and receive the compass heading information via the XYZ magnetic vector data. This is the basis for Location-Based Services (LBS) and Telematics applications when used with GPS location data.

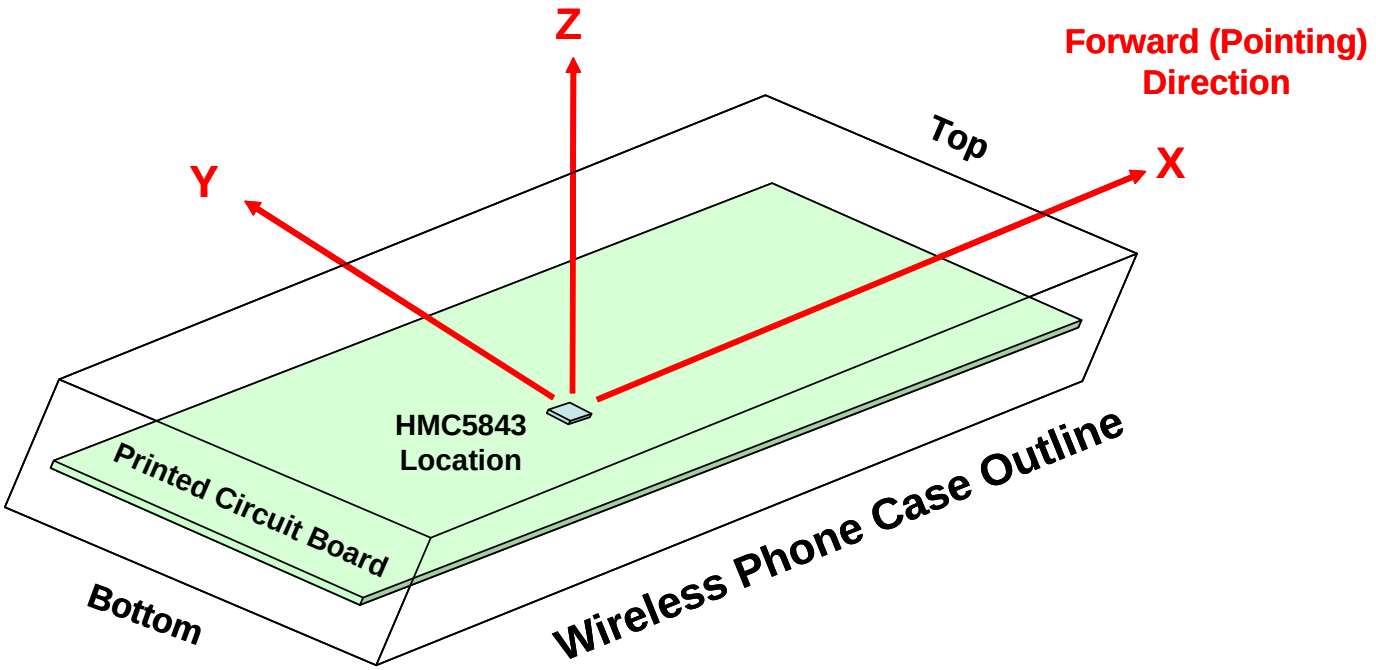
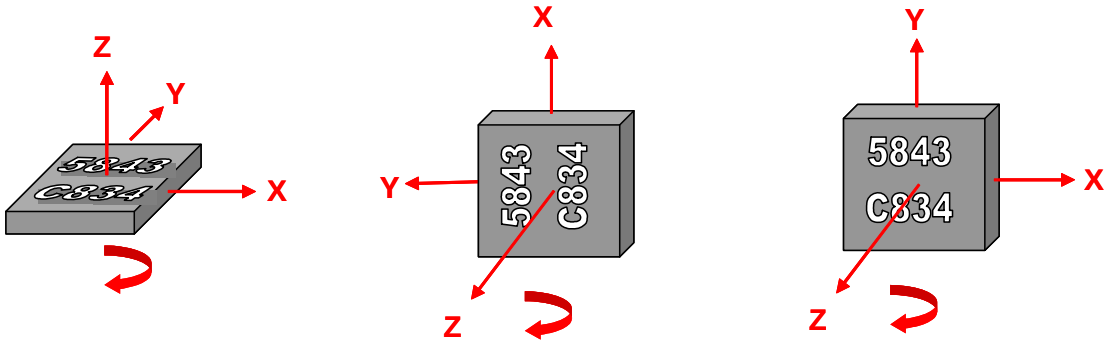


Figure 5 – Compass IC in Wireless Phone

Other axis systems maybe used when the HMC5843 can not be orientated in a horizontal orientation within the product. In fact, the alternate coordinates maybe desired when a phone is in a car holder and in an upright position. When flat, the compass is in a X-Y coordinate system, and when upright it is in an Y-Z coordinate system; with the X-axis most constant as the vehicle moves about. And a Z-X coordinate system could be used if the product is upright but in a wide (landscape) orientation. Figure 6 shows these positions.



X-Y Reference **Y-Z Reference** **Z-X Reference**

Figure 6 – HMR5843 Orientations

REFERENCE DESIGN

The HMC5843 is suitable for a lot of portable device electronic compass functions due to its low power draw characteristics and I2C serial data digital interface. Figure 7 shows a standard dual supply (digital and analog rails) reference design schematic diagram.

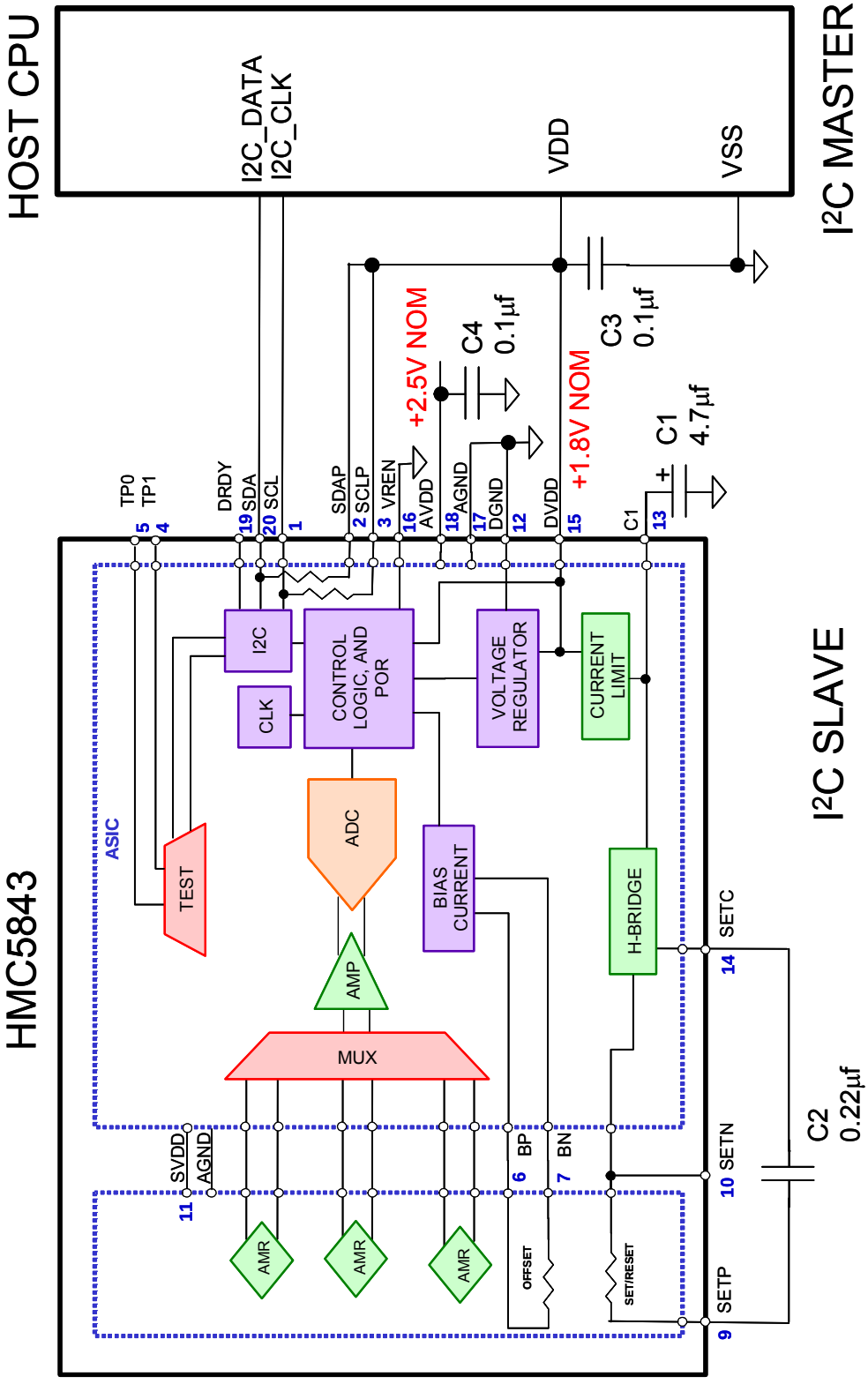


Figure 7 – Reference Design Schematic Diagram (dual supply)

Reference Design Description

Refer to Figure 7 while reading the design description. The HMC5843 in the above dual supply reference design is a single chip magnetic sensor for an electronic compass solution that measures the magnetic fields flowing over the sensor elements and converts them to amplitudes for computation into a compass heading. Three highly directional magnetic sensors take the applied magnetic field magnitude and direction and represent the information as three Cartesian amplitudes (XYZ). These amplitudes start as feeble voltages and are greatly amplified and digitized for manipulation by an external microprocessor for compassing and pointing applications..

Within the HMC5843 Integrated Circuit (IC) package, three precision Anisotropic Magneto-Resistive (AMR) sensors on silicon die convert the incident magnetic fields to balanced output voltages due to their wheatstone bridge configurations. The three AMR sensors share two sets coils (straps); one described as an offset strap, the other described as a set/reset strap. The offset strap converts current through the strap as an additional magnetic field that is used for self-test purposes, and to buck or boost the external magnetic field values for convenient measurement. The set/reset strap is another magnetic field generating coil for de-gaussing the sensors, and is used to flip the magnetic polarity of the sensors to make additional field measurements.

The remaining circuits within the HMC5843 IC package are within an Application Specific Integrated Circuit (ASIC) die. On the ASIC, a H-bridge driver circuit plus the external capacitors C1 and C2, perform a pulse shaping function to apply a set pulse followed by a reset pulse to the set/reset strap to create magnetically intense (>40 gauss) pulse fields to de-gauss the sensors and flip sensor polarities. Due to the low ohmic value of the set/reset strap, the C1 and C2 capacitors must be low-ESR (Effective Series Resistance) grade capacitors with only a hundred milli-ohms of ESR. Typically ceramic multi-layer capacitors are chosen for lowest ESR and smallest size packages.

From the AMR sensors, the ASIC provides a multiplexor circuit or MUX to switch from sensor to sensor, to sequentially connect the sensor to be measured to the amplifier and ADC. The multiplexor switches within a few micro-seconds to quickly measure the three sensors, allow the reset pulse to flip the sensor polarity, and re-measure the three sensors. This process can be programmed to happen as often as 50 times a second.

The amplifier circuit receives the balanced sensor output voltages through the multiplexor and amplifies the difference by a programmable amount before being converted to a digital number. After the amplifier, a 12-bit Analog-to-Digital Converter (ADC) circuit takes the amplified sensor voltage and creates a 12-bit digital number representation of the voltage. This number is often called ADC “counts” and has 4096 values representing the binary combinations of the 12-bits.

Typically the midpoint ADC counts location (count 2048) represents a zero field amplitude (zero gauss) with +/-700 milli-gauss span over the 0 to 4096 count span as a factory default value. Because of the plus or minus polarity representation of magnetic fields, the measured signal is converted to “two’s complement” representation over two Bytes for output register storage. This means -700 milli-gauss is 0xF800 because of the negative sign (-2048 counts) , and +700 milli-gauss is 0x7FFF (+2047 counts).

Due to the programmable amplifier settings, the HMC5843 IC has 8 ranges from +/-700 milli-gauss to +/-6.5 gauss to handle various magnetic environments. With earth’s magnetic field amplitude about +/-600 milli-gauss to be divided into the sensor’s XYZ Cartesian vector amplitudes, the lower gain settings permit stray fields from man-made sources (such as vehicle magnetization) to not clip the amplifier and ADC. Removal of some stray fields will be discussed later in the calibration section.

The power supply section of the HMC5843 IC provides functions like power-on reset for digital logic initialization, selection of an onboard voltage regulator for the digital circuits, distribution of analog and digital circuit power, and current limited supply (trickle charge) for the H-bridge pulse drive circuit. Besides the system ground reference, the ASIC is designed for single or dual supply compatibility of product power supplies. The analog supply voltage input connection (AVDD) is designed to accept a 2.4 to 3.3 volt operating range, and may diminish to zero when in dual supply mode to save energy when the IC is not used. The digital supply voltage input connection (DVDD) is only used in dual supply mode to receive a 1.62 to 1.98 volt operating range supply for energizing digital circuits. In single supply mode, the digital circuit voltage is provided by an internal linear voltage regulator that converts the AVDD voltage down to about 1.8 volts as a nominal DVDD internal supply. This internal voltage regulator is enabled via the VREN connection when connected to the AVDD

supply. Grounding the VREN connection is required to disable the internal voltage regulator for dual supply mode, to permit an external DVDD source.

The HMC5843 does require external power supply filtering capacitors in the single or dual supply modes of operation. As shown in Figure 8, each filter capacitor (C3 and C4) should be reasonably close to the HMC5843 package. Values of 0.1 to 1.0 micro-farad are recommended for supply filtering for this part.

The digital control section in the HMC5843 IC includes 2 Byte memory registers for each of the X, Y, and Z sensor output ADC count data to be transferred to master microprocessor via the I2C serial digital interface. A total of 13 memory registers are implemented in the digital control section, with the 6 Bytes of data output, 3 identification register Bytes, 2 control register Bytes, a mode register, and a status register. The configuration registers contain the information on the output data rate, measurement flow, amplifier gain setting, and measurement delay setting. The mode register allows the external microprocessor to configure the HMC5843 IC into continuous-conversion mode, single-conversion mode, idle, or sleep modes of operation. The status register shows the power supply configuration, data ready, and data register lock indications. The identification registers are fixed value Bytes indicating to the I2C master the slave is a HMC5843 device.

More detail on the registers and their interaction can be found later in this guide, and in the HMC5843 datasheet.

HMC5843 Pin Description

The following table describes the HMC5843 pins and their function:

Pin	Name	Description
1	SCL	Serial Clock – I2C Master/Slave Clock – up to 400kbps I2C Speed
2	SDAP	Serial Data Pull-up Resistor – internal 50k-ohm to SDA – tie to VDD to use.
3	SCLP	Serial Clock Pull-up Resistor – internal 50k-ohm to SCL – tie to VDD to use.
4	TP1	Test Point One – Factory Test Use Only - NC
5	TP0	Test Point Zero – Factory Test Use Only - NC
6	OFFP	Offset Strap Positive - Factory Test Use Only - NC
7	OFFN	Offset Strap Negative - Factory Test Use Only - NC
8	NC	NC - No Connection
9	SETP	Set/Reset Strap Positive – S/R Capacitor (C2) Connection – Strap Side
10	SETN	Set/Reset Strap Negative – Test Point - Factory Test Use Only - NC
11	SVDD	Sensor Supply – Test Point - Factory Test Use Only - NC
12	DGND	Digital Supply Ground/Return – Connect to System Ground
13	C1	Reservoir Capacitor (C1) Connection – 4.7uf to DGND
14	SETC	S/R Capacitor (C2) Connection – Driver Side – Connect to 0.22uf (C2)
15	DVDD	Digital Positive Supply – +1.62 to +1.98 volts input when used
16	VREN	Voltage Regulator Enable, (GND = Dual Supply, AVDD = Single Supply)
17	AGND	Analog Supply Ground/Return – Connect to System Ground
18	AVDD	Analog Positive Supply - +2.4 to +3.3 volts input
19	DRDY	Data Ready – Test Point – Stable Data in Output Registers - NC
20	SDA	Serial Data – I2C Master/Slave Data – up to 400kbps I2C Speed

Bill Of Materials (BOM)

For the complete electronic compass function, it is assumed that the HMC5843 interfaces via its I2C serial bus to a microcontroller that serves as an I2C master and converts the HMC5843 magnetic vector output data into a compass heading. The computational equation for heading also requires pitch and roll angles if the tilt compensation feature is implemented. To provide these angles relative to the downward gravity direction, a reasonable quality tilt sensor is also used with the HMC5843 to solve for the heading when the product is tilted. Specifically, a 3-Axis Micro Electro-Mechanical System (MEMS) accelerometer is used a tilt sensor (inclinometer). There are many vendors of these MEMS accels, and competition has improved inclinometer linearity while reducing costs and size.

Because a MEMS accelerometer is used often with the HMC5843, the accelerometer is likely to share the same I2C serial data interface as the HMC5843. Please take care to ensure cross-compatibility between these ICs. Things like I2C data rates and I2C slave addresses need to be checked for inclusiveness. The factory slave addresses for the HMC5843 are 0x3C (write) and 0x3D (read). The HMC5843 can support the standard I2C data rates of 400kbps and 100kbps, and can follow the Serial Clock (SCL) speed at any rate up to 400kbps.

To show an entire electronic compass system schematic, Figure 8 depicts a typical dual supply design with a MEMS accelerometer.

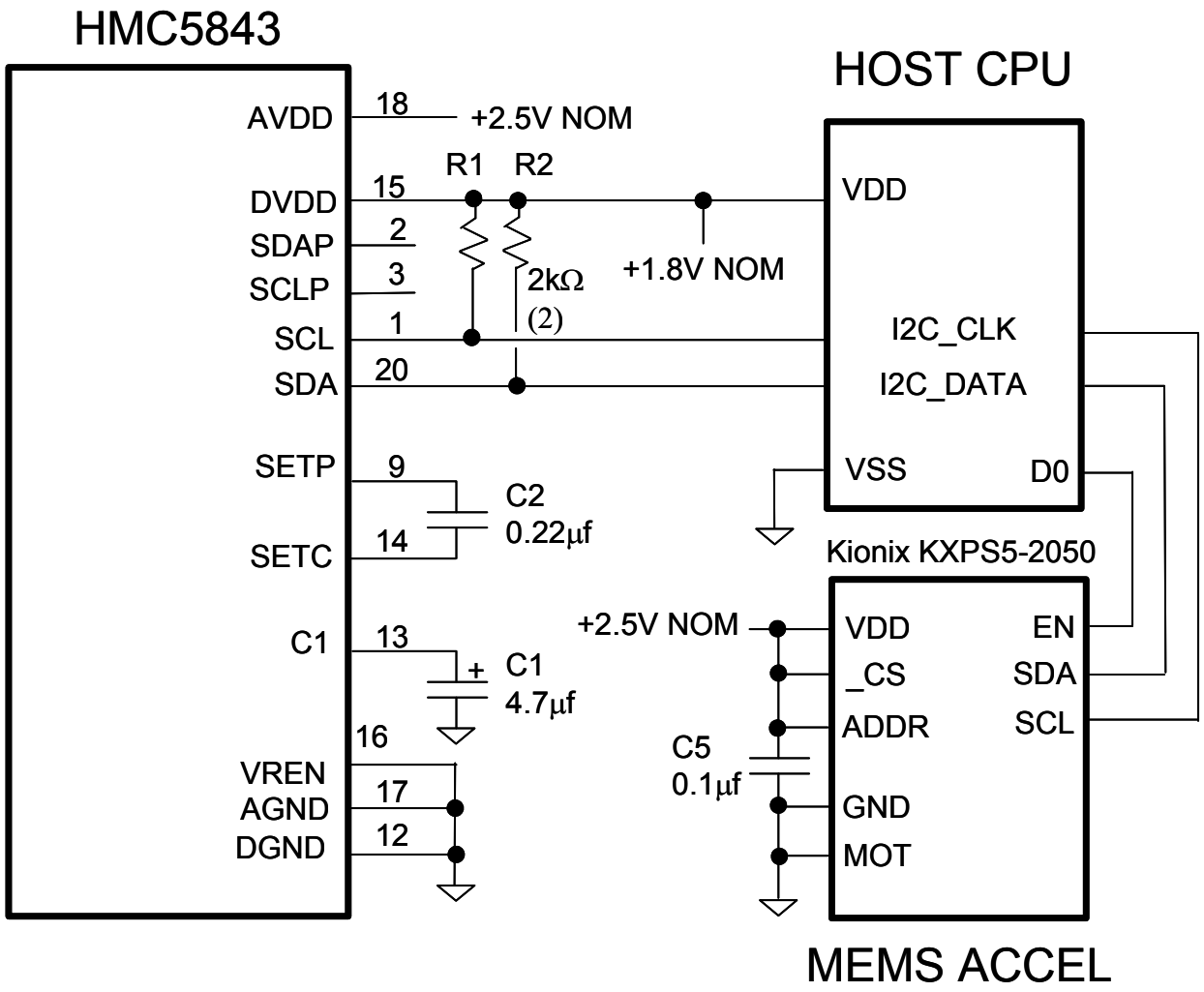


Figure 8 – Compass System Schematic Diagram

The following table is the electronic compass bill of materials:

Reference designator	Part type	Notes
HMC5843	Compass Integrated Circuit	4mm by 4mm by 1.4mm LCC, 25-pin
KXPS5-2050	MEMS Accelerometer	Chose the best MEMS accel for inclinometer application
C1	4.7uf Ceramic Capacitor	0603, Chose for lowest ESR, <200 milli-ohm
C2	0.22uf Ceramic Capacitor	0603, Chose for lowest ESR, <200 milli-ohm
C3	0.1uf Ceramic Capacitor	Supply filter capacitor for 1.8 volt rail
C4	0.1uf Ceramic Capacitor	Supply filter capacitor for 2.5 volt rail
C5	0.1uf Ceramic Capacitor	Supply filter capacitor for MEMS accelerometer
R1	2000 ohm Resistor	Serial bus clock pull-up, 2000 ohms for max data rate
R2	2000 ohm Resistor	Serial bus data pull-up, 2000 ohms for max data rate

Single Supply Operation

Many product applications do not have internal supplies with separate digital and analog supply rails for maximum power conservations. Products like GPS receivers and vehicle navigation systems may provide only a single 3 volt logic interface. The HMC5843 has an internal digital logic supply regulator to operate its digital circuitry at around 1.8 volts when the voltage regulator enable (VREN) pin is brought up to the AVDD supply level.

Also the I2C connections on the HMC5843 can now be pulled up to the AVDD supply. The DVDD pin on the HMC5843 should be jumped to C1 as the internal regulator is not designed to source external circuitry besides the internal C1 load. While popular pull-up resistor values like 2000 ohms and 10k ohms allow the higher I2C data rates (normal, fast modes) for the microprocessor master and the HMC5843 slave, the HMC5843's internal 47k ohm pull-up resistors (SDAP, SCLP) can be used as a substitute for external resistors and pulled up to AVDD in single supply operation mode. Figure 9 shows the single supply schematic for the HMC5843.

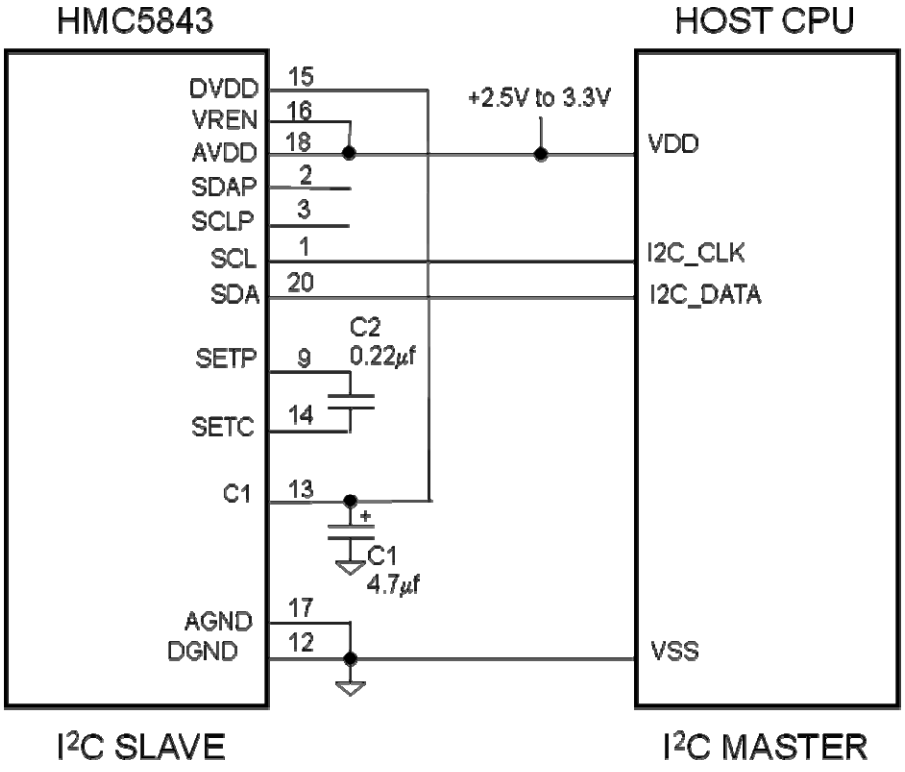


Figure 9 – Single Supply Electronic Compass Schematic

COMPASS FIRMWARE

For the HMC5843 used as an electronic compass, the firmware for extracting the magnetic data from the HMC5843 will reside inside the host microprocessor. Unlike other raw sensor outputs from other Honeywell magnetic sensor products, the HMC5843 uses internal biasing for consistent field intensity scale factors and bridge offset cancellation. Once the six Bytes of output data are transferred, the remaining computational tasks will be to incorporate the calibration offsets to each of the XYZ magnetic vectors; and then run the data into the trigonometric equations to compute heading. Figure 10 shows as a flow chart the basis of the firmware to convert the magnetic data into a usable heading output.

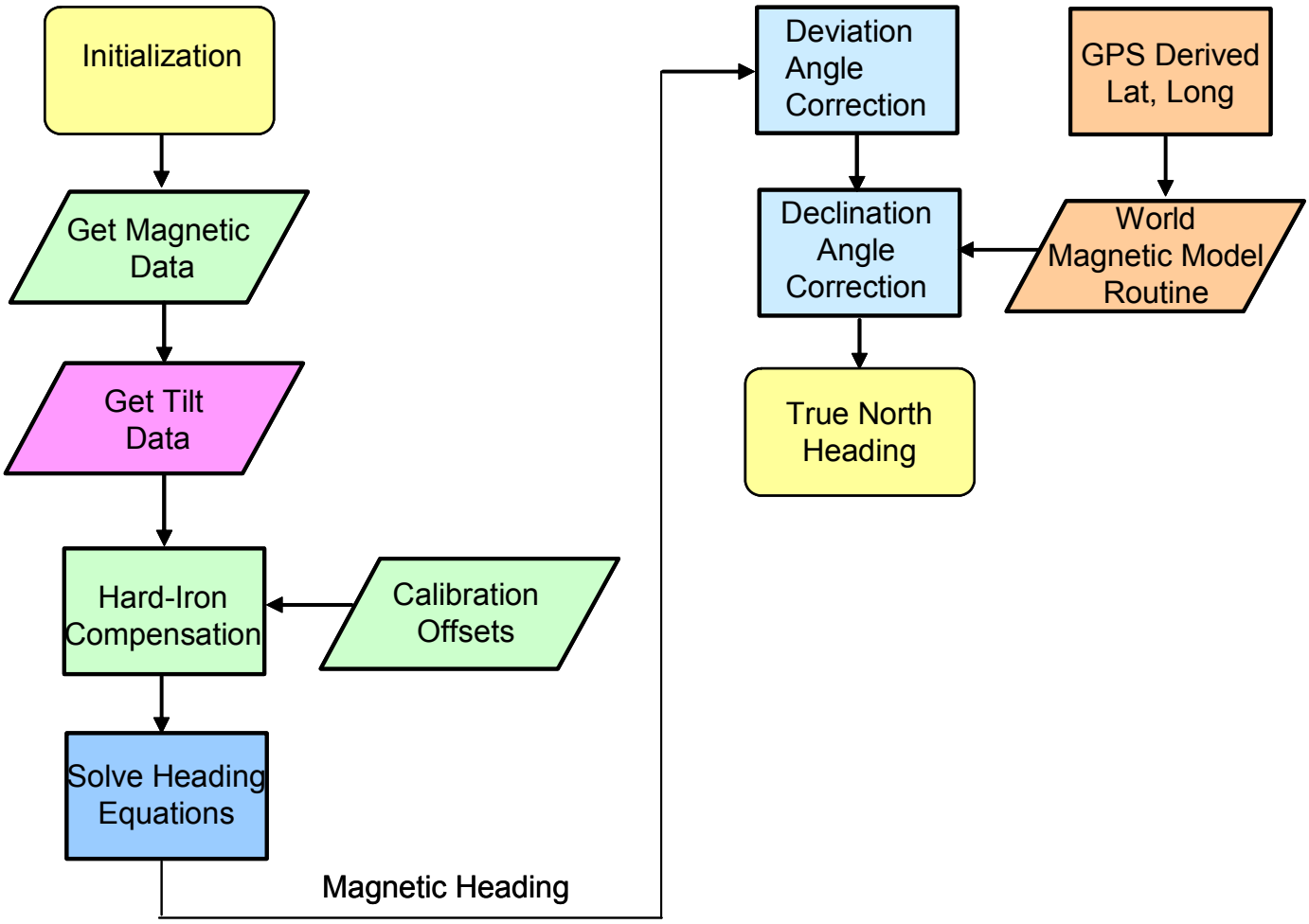


Figure 10 – Electronic Compass Flowchart

From Figure 10, the firmware is initialized and data is retrieved from the HMC5843 and the chosen MEMS accelerometer to provide the required raw XYZ magnetic vectors and the pitch and roll angles in their raw cosine angle representation (phi = ϕ = pitch, theta = θ = roll). Before the XYZ raw data can be utilized, the offset values must be added to the raw magnetic vectors to become final magnetic vectors for heading computation.

Calibration Compensation

Typically, there are two sets of offset values to be added into each magnetic vector, the first is the factory or “golden” offset that all production compasses receive based on engineering data for a nominal factory calibration of the end product (phone, GPS receiver, etc.). The second set of offsets are the customer calibration offsets; and are shipped with zero values until the user re-calibrates the compass in the end product.

Generally in handheld products, the customer should be highly discouraged from initially re-calibrating the compass as the factory calibration will likely be the best calibration for the life of the product. Re-calibration may be desired if the product is used within a cradle inside a vehicle, or inside a boat or aircraft that has a lot of magnetic interference. The

calibration routine typically involves rotation of the compass and vehicle/craft to determine new offset values. General environmental magnetic interference can not be calibrated out, if it does not rotate with the compass. Figure 11 shows typical rotational compass plots for clean (no distortion), hard-iron distortion, and soft-iron distortion.

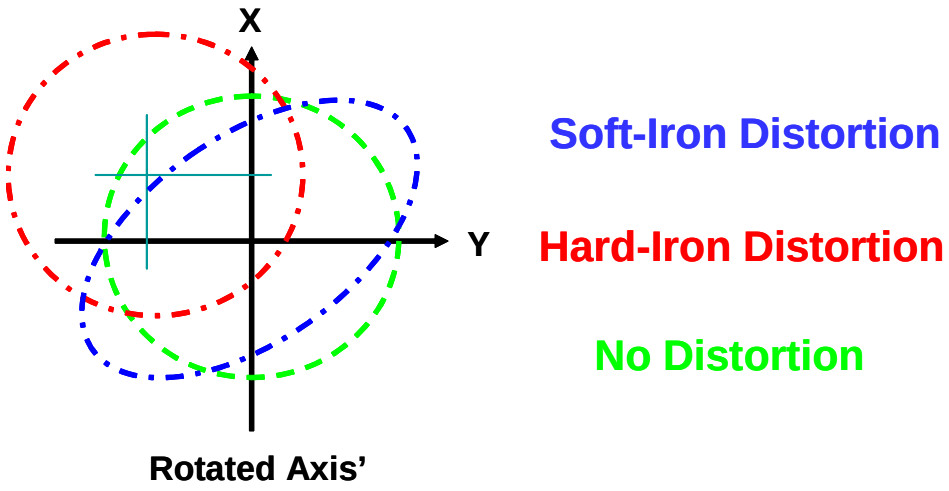


Figure 11 – Magnetic Distortions on Compass Plots

In an X-Y oriented compass, the usual calibration routine is to slowly rotate the product about the Z-axis (vertical) in a "calibration mode", in which the magnetic sensor continuously collects X, Y, and Z data. As the microprocessor gathers the inbound data, the minimum and maximum values of the XYZ vectors are continuously updated and stored until the user indicates the end of calibration mode. This single rotation is a two dimensional calibration (X and Y only), and a three dimensional calibration must include another rotated axis (pitch or roll) or at a minimum an upside down measurement. Handheld device can easily do three dimensional calibrations, but most vehicle navigation systems may only get an accurate two dimensional calibration and leave the vertical axis without an offset value.

The vast majority of electronic compass calibrations only handle hard-iron distortions of moderate intensity or less (typically <2gauss at the sensor). The rotations collect the circular data min and max values, and then determine the mean values as hard-iron distortion offsets for each magnetic vector (XYZ). By subtracting these offset to all successive magnetic vectors coming from the HMC5843, a calibrated compass heading is the result. Figure 12 shows the hard-iron offset being translated back to the origin axis for compass heading computation.

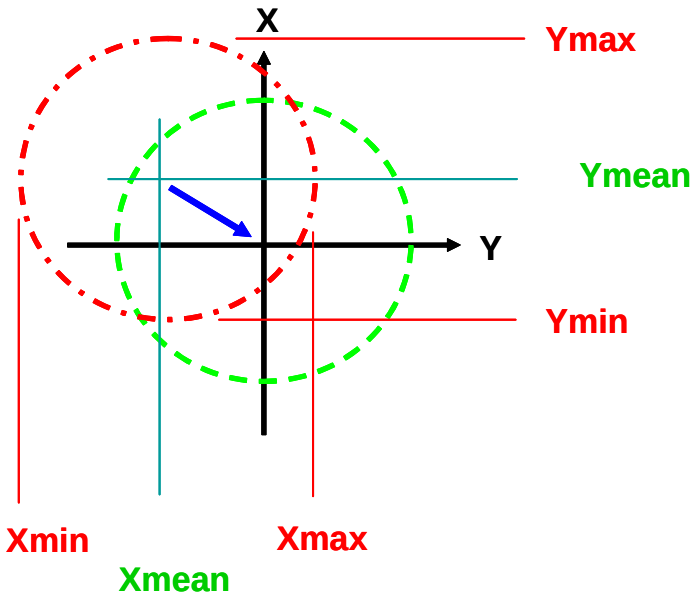


Figure 12 – Hard-Iron Distortion Translation

Honeywell provides this calibration routine in the C high level language if required.

Heading Computation

Once corrected via calibration offsets, the XYZ vectors and pitch/roll (tilt) data are plugged into two equations for tilt-compensated heading solutions. It is important to remember that X represents the forward reference direction, and Y the orthogonal "right" direction. Because orientation can be different, the XYZ variables may be reoriented for forward, right and upward variable substitutions. The following two equations are called flattening equations that turn the three-dimensional data into two-dimensional XY representation of the compass heading. These flattening equations are:

$$X' = X \cos \phi + Y \sin \theta \sin \phi - Z \cos \theta \sin \phi$$

$$Y' = Y \cos \theta + Z \sin \theta$$

With phi and θ as the pitch and roll angles from the accelerometer data. After flattening to two dimensions (X' and Y'), the basic heading equation applies:

$$\text{Heading} = \arctan (Y' / X')$$

Honeywell provides this computation routine in the C high level language if required.

Some microprocessors can not perform a direct arc-tangent function because they are lacking a floating point function. These microprocessors must then create an arc-tangent look-up table at the required compass resolution. The good news is that the arc-tangent values repeat in 90 degree segments with just polarity needing to be adjusted for each segment. So the look-up table needs only the solutions for heading over 90 degrees. For a one degree resolution compass, only 88 segment solutions plus the 4-cardinal point solutions are mapped in memory for look-up. For a 0.1 degree resolution compass, 898 arctan solutions plus the 4-cardinal point solutions are mapped.

Deviation, Declination Angle Correction

Once the magnetic north heading solution is acquired, two heading offsets can be applied for increased usefulness to customers. The first offset is the deviation angle offset, which corrects for any mechanical error from the sensor X-axis direction to the forward direction of the product. If designed well, this error may be very small or excluded completely.

The second heading offset is called the declination angle offset, which is the difference between the magnetic north and the geographic north locations. At present the magnetic north pole is biased over northern Canada and not above Greenland as where the geographic north pole is. From this polar difference, a worldwide map of declination angle offsets is created to provide "True North" indications.

To arrive with the correct declination angle offset, many approaches have been suggested, depending on the compass accuracy and the locations on earth the compass will operate. For example, a low accuracy vehicle compass used only in North America may require the customer to input a time zone (western, mountain, central, eastern) in which an approximate declination angle value will be chosen.

If magnetic north compass heading are good enough, no further declination angle offset is required. The magnetic north compass maybe the best choice; if cost is important to save on microprocessor resources, or if latitude and longitude information is not available.

For high precision compassing, a world magnetic model set of equations can be implemented to create precise declination angles given good latitude and longitude information. For example, the United States Geologic Survey (USGS) publishes new world magnetic model equations every five years on its website, with the latest update for year 2005.

With limited computing resources (no floating point processing) and modest precision compassing required, a declination angle look-up table can be formulated by allocating square lat/long locations every 5 or 10 degrees, and placing an average declination angle offset representing the location. The look-up table size can be further constrained if the product's marketing region is known, or if it to be only used on land (no ocean-only lat/longs).

HMC5843 Communication

The HMC5843 uses standard I2C protocols for communication to a host microprocessor. This HMC5843 is an I2C slave and shall be compliant with *I^2C-Bus Specification*, document number: 9398 393 40011. As an I^2C compatible device, this device has a 7-bit serial address and supports I^2C protocols. This device shall support standard and fast modes, 100kHz and 400kHz respectively, but cannot support the high speed mode (Hs). External 10k ohm pull-up resistors are required to these standard and fast speed modes.

Activities required by the master (register read and write) have priority over internal activities, such as the measurement. The purpose of this priority is to not keep the master waiting and the I^2C bus engaged for longer than necessary.

HMC5843 MODES OF OPERATION

This device has several modes whose primary purpose is power management. This section describes these modes.

Continuous-Measurement Mode

During continuous-measurement mode, the device continuously makes measurements and places measured data in data output registers. Settings in the configuration register affect the data output rate (bits DO[n]), the measurement configuration (bits MS[n]), the gain (bits GN[n]), and the delay (bits DL[n]) when in continuous-measurement mode. To conserve current between measurements, the device is placed in a state similar to idle mode, but the mode is not changed to idle mode. That is, MD[n] bits are unchanged. Data can be re-read from the data output registers if necessary; however, if the master does not ensure that the data register is accessed before the completion of the next measurement, the new measurement may be lost. All registers maintain values while in continuous-measurement mode. The I^2C bus is enabled for use by other devices on the network in while continuous-measurement mode.

Single-Measurement Mode

This is the default single supply power-up mode. In dual supply configuration this is the default mode when AVDD goes high. During single-measurement mode, the device makes a single measurement and places the measured data in data output registers. Settings in the configuration register affect the measurement configuration (bits MS[n]), the gain (bits GN[n]), and the delay (bits DL[n]) when in single-measurement mode. After the measurement is complete and output data registers are updated, the device is placed sleep mode, and the mode register *is* changed to sleep mode by setting MD[n] bits. All registers maintain values while in single-measurement mode. The I^2C bus is enabled for use by other devices on the network while in single-measurement mode.

Idle Mode

During this mode the device is accessible through the I^2C bus, but major sources of power consumption are disabled, such as, but not limited to, the ADC, the amplifier, the SVDD pin, and the sensor bias current. All registers maintain values while in idle mode. The I^2C bus is enabled for use by other devices on the network while in idle mode.

Sleep Mode

This is the default dual supply power-up mode when only DVDD goes high and AVDD remains low. During sleep mode the device functionality is limited to listening to the I^2C bus. The internal clock is not running and register values are not maintained while in sleep mode. The only functionality that exists during this mode is the device is able to recognize and execute any instructions specific to this device but does not change from sleep mode due to other traffic on the I^2C bus. The I^2C bus is enabled for use by other devices on the network while in sleep mode. This mode has two practical

differences from idle mode. First this state will create less noise on system since the clock is disabled, and secondly this state is a lower current consuming state since the clock is disabled.

Off Mode

During off mode device is off. No device functionality exists. Both AVDD and DVDD are low. The I^2C bus is enabled for use by other devices on the network in off mode. In this mode the I^2C pins shall be in a high impedance state.

HMC5843 MAGNETIC MEASUREMENTS

The measurement type is set by bits MS[n] in the configuration registers. There are two main configurations, normal measurement and bias measurement, where the self-test bias measurement can be a positive or a negative bias current on the offset strap to emulate an external magnetic field. The gain, GN[n]; the delay, DL[n]; and the data output rate, DO[n] settings are common to all measurement configurations.

In the normal measurement process, the sensor's and amplifier's differential offset are removed through differencing the sensor's output after a SET pulse and after a RESET pulse. This technique is not used during the bias measurement process. The differencing technique is completed as follows: ([Measurement after Set pulse] – [Measurement after Reset pulse])] / 2.

Normal Measurement

The normal measurement is the default measurement configuration. The normal measurement flow is shown in Figure 13.

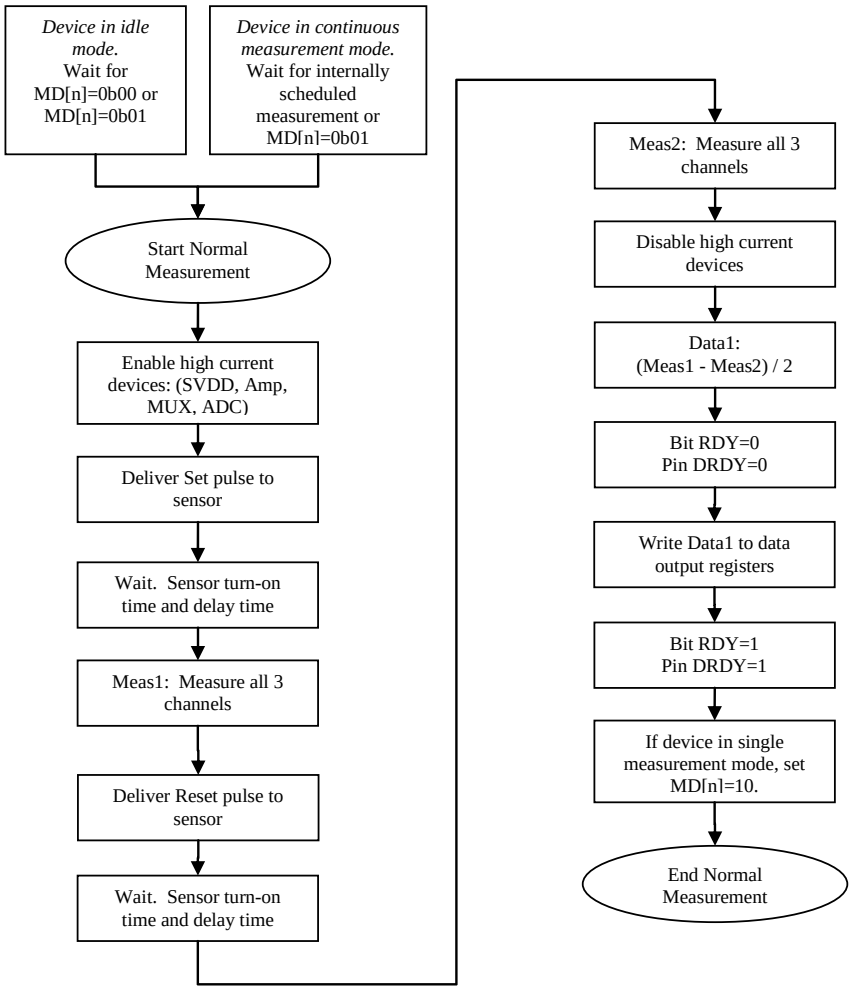


Figure 13 - Normal Measurement Flow Diagram

The timing diagram for the normal measurement is shown in Figure 14. “Normal Meas” defines the timing of the Figure 13 - **Normal Measurement Flow Diagram** below. When the device is in continuous-measurement mode, the time shown as “Idle” defines time the device is in low current state, similar to idle mode. When the device is in single-measurement mode, the time shown as “Idle” defines the time the device is in sleep mode. *Analog Turn-on* time defines the longest of these times: the sensor’s turn-on time, the amplifier turn-on time, or the ADC turn-on time. Note that after applying a reset pulse to the sensor, the device shall wait the duration of the sensor’s turn-on before making measurements, even though sensor was not powered-down between measurements. I*(R_S/R)* depicts the current through the sensor strap, $R_{S/R}$.

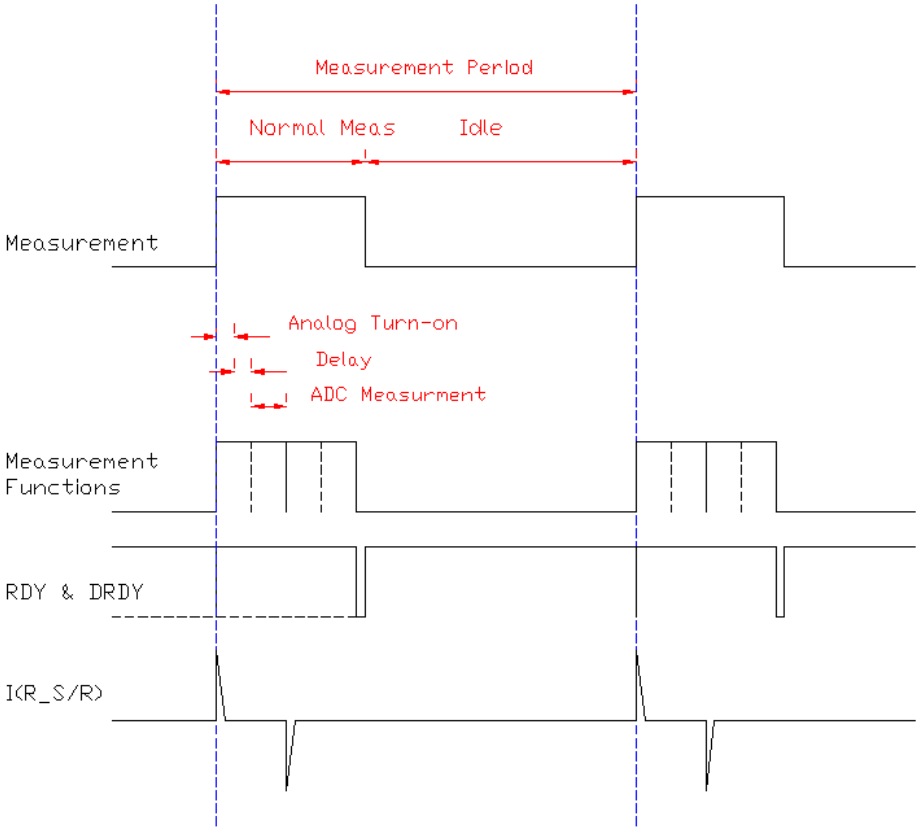


Figure 14 - Normal Measurement Timing

REGISTERS

This device is controlled and configured via a number of on-chip registers, which are described in this section. In the following descriptions, *set* implies a logic 1, and *reset* or *clear* implies a logic 0, unless stated otherwise.

Register List

The table below lists the registers and their access. All address locations are 8 bits.

Address Location	Name	Access
00	Configuration Register A	Read/Write
01	Configuration Register B	Read/Write
02	Mode Register	Read/Write
03	Data Output X MSB Register	Read
04	Data Output X LSB Register	Read
05	Data Output Y MSB Register	Read
06	Data Output Y LSB Register	Read
07	Data Output Z MSB Register	Read
08	Data Output Z LSB Register	Read
09	Status Register	Read
10	Identification Register A	Read
11	Identification Register B	Read
12	Identification Register C	Read

Register List

Register Access

This section describes the process of reading from and writing to this device. The devices uses an address pointer to indicate which register location is to be read from or written to. These pointer locations are sent from the master to this slave device and succeed the 7-bit address plus 1 bit read/write identifier.

To minimize the communication between the master and this device, the address pointer updated automatically without master intervention. This automatic address pointer update has two additional features. First when address 12 or higher is accessed the pointer updates to address 00 and secondly when address 08 is reached, the pointer rolls back to address 03. Logically, the address pointer operation functions as shown below.

If (address pointer = 08) then address pointer = 03
Else if (address pointer >= 12) then address pointer = 0
Else (address pointer) = (address pointer) + 1

The address pointer value itself cannot be read via the I^2C bus.
Any attempt to read an invalid address location returns 0's, and any write to an invalid address location or an undefined bit within a valid address location is ignored by this device.

Configuration Register A

The configuration register is used to configure the device for setting the data output rate and measurement configuration. CRA0 through CRA7 indicate bit locations, with *CRA* denoting the bits that are in the configuration register. CRA7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

CRA7	CRA6	CRA5	CRA4	CRA3	CRA2	CRA1	CRA0
(0)	(0)	(0)	DO2 (1)	DO1 (0)	DO0 (0)	MS1 (0)	MS0 (0)

Configuration Register A

Location	Name	Description
CRA7 to CRA5	0	These bits must be cleared for correct operation.
CRA4 to CRA2	DO2 to DO0	Data Output Rate Bits. These bits set the rate at which data is written to all three data output registers.
CRA1 to CRA0	MS1 to MS0	Measurement Configuration Bits. These bits define the measurement flow of the device, specifically whether or not to incorporate an applied bias to the sensor into the measurement.

Configuration Register A Bit Designations

The Table below shows minimum output data rates given PVT conditions. All three channels shall be measured within a given data rate.

DO2	DO1	DO0	Minimum Data Output Rate (Hz)
0	0	0	0.5
0	0	1	1
0	1	0	2
0	1	1	5
1	0	0	10 (default)
1	0	1	20
1	1	0	50
1	1	1	Not used

Data Output Rates

MS1	MS0	Mode
0	0	Normal measurement configuration (default). In normal measurement configuration the device follows normal measurement flow. Pins BP and BN are left floating and high impedance.
0	1	Positive bias configuration. In positive bias configuration, a positive current is forced across the resistive load on pins BP and BN.
1	0	Negative bias configuration. In negative bias configuration, a negative current is forced across the resistive load on pins BP and BN.
1	1	This configuration is not used.

Measurement Modes

Configuration Register B

The configuration register B for setting the device gain and for setting a measurement delay time. CRB0 through CRB7 indicate bit locations, with *CRB* denoting the bits that are in the configuration register. CRB7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

CRB7	CRB6	CRB5	CRB4	CRB3	CRB2	CRB1	CRB0
GN2 (0)	GN1 (0)	GN0 (1)	(0)	DL3 (0)	DL2 (0)	DL1 (0)	DL0 (0)

Configuration B Register

Location	Name	Description
CRB7 to CRB5	GN2 to GN0	Gain Configuration Bits. These bits configure the gain for the device. The gain configuration is common for all channels.
CRB4	0	This bit must be cleared for correct operation.
CRB3 to CRB0	DL3 to DL0	Delay Configuration Bits. These bits set the delay time after which pin SVDD and ADC are high before analog to digital conversion begins.

Configuration Register B Bit Designations

The table below shows nominal gain settings.

GN2	GN1	GN0	Differential Input Range	Sensor Input Field Range: Trimmed (Untrimmed)	Output Range	LSB (Input Referred)
0	0	0	±3.00mV	±0.07mT (--)	0xF800–0x07FF (-2048–2047)	1.46µV (0.059µT)
0	0	1	±3.75mV	±0.10mT (--)	0xF800–0x07FF (-2048–2047)	1.83µV (0.073µT)
0	1	0	±5.00mV	±0.15mT (--)	0xF800–0x07FF (-2048–2047)	2.44µV (0.098µT)
0	1	1	±6.25mV	±0.20mT (--)	0xF800–0x07FF (-2048–2047)	3.05µV (0.12µT)
1	0	0	±9.25mV	±0.32mT (±0.7mT)	0xF800–0x07FF (-2048–2047)	4.52µV (0.18µT)
1	0	1	±10.625mV	±0.38mT (±0.125mT)	0xF800–0x07FF (-2048–2047)	5.19µV (0.21µT)
1	1	0	±12.5mV	±0.45mT (±0.2mT)	0xF800–0x07FF (-2048–2047)	6.10µV (0.24µT)
1	1	1	±17.5mV	±0.65mT (±4.0mT)	0xF800–0x07FF (-2048–2047)	8.54µV (0.34µT)

Gain Settings

The table below shows nominal delay times settings. These values may have up to ±50% variation due to PVT.

DL3	DL2	DL1	DL0	Delay Time (ms)
0	0	0	0	0.000 (default)
0	0	0	1	0.333
0	0	1	0	0.667
0	0	1	1	1.000
0	1	0	0	1.333
0	1	0	1	1.667
0	1	1	0	2.000
0	1	1	1	2.333
1	0	0	0	2.667
1	0	0	1	3.000
1	0	1	0	3.333
1	0	1	1	3.667
1	1	0	0	4.000
1	1	0	1	4.333
1	1	1	0	4.667
1	1	1	1	5.000

Delay Times

Mode Register

The mode register is an 8-bit register from which data can be read or to which data can be written. This register is used to select the operating mode of the device. MR0 through MR7 indicate bit locations, with *MR* denoting the bits that are in the mode register. MR7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
(0)	(0)	(0)	(0)	(0)	(0)	MD1 (1)	MD0 (0)

Table 14: Mode Register

Location	Name	Description
MR7 to MR2	0	These bits must be cleared for correct operation.
MR1 to MR0	MD1 to MD0	Mode Select Bits. These bits select the operation mode of this device.

Mode Register Bit Designations

MD1	MD0	Mode
0	0	Continuous-Conversion Mode. In continuous-conversion mode, the device continuously performs conversions an places the result in the data register. RDY goes high when new data is placed in all three registers. After a power-on or a write to the mode or configuration register, the first measurement set is available from all three data output registers after a period of $2/f_{DO}$ and subsequent measurements are available at a frequency of f_{DO}, where f_{DO} is the frequency of data output.
0	1	Single-Conversion Mode. When single-conversion mode is selected, device performs a single measurement, sets RDY high and returned to sleep mode. Mode register returns to sleep mode bit values. The measurement remains in the data output register and RDY remains high until the data output register is read or another conversion is performed.
1	0	Idle Mode. Device is placed in idle mode.
1	1	Sleep Mode. Device is placed in sleep mode.

Operating Modes

Data Output X Registers A and B

The data output X registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel X. Data output X register A contains the MSB from the measurement result, and data output X register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DXRA0 through DXRA7 and DXRB0 through DXRB7 indicate bit locations, with *DXRA* and *DXRB* denoting the bits that are in the data output X registers. DXRA7 and DXRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096 in 2's complement form. This register value will clear when after the next valid measurement is made.

DXRA 7	**DXRA6**	**DXRA5**	**DXRA4**	**DXRA3**	**DXRA2**	**DXRA1**	**DXRA0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DXRB 7	**DXRB6**	**DXRB5**	**DXRB4**	**DXRB3**	**DXRB2**	**DXRB1**	**DXRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Data Output X Registers A and B

Data Output Y Registers A and B

The data output Y registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel Y. Data output Y register A contains the MSB from the measurement result, and data output Y register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DYRA0 through DYRA7 and DYRB0 through DYRB7 indicate bit locations, with *DYRA* and *DYRB* denoting the bits that are in the data output Y registers. DYRA7 and DYRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096 in 2's complement form. This register value will clear when after the next valid measurement is made.

DYRA 7	DYRA6	DYRA5	DYRA4	DYRA3	DYRA2	DYRA1	DYRA0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DYRB 7	**DYRB6**	**DYRB5**	**DYRB4**	**DYRB3**	**DYRB2**	**DYRB1**	**DYRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Data Output Y Registers A and B

Data Output Z Registers A and B

The data output Z registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel Z. Data output Z register A contains the MSB from the measurement result, and data output Z register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DZRA0 through DZRA7 and DZRB0 through DZRB7 indicate bit locations, with *DZRA* and *DZRB* denoting the bits that are in the data output Z registers. DZRA7 and DZRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096 in 2's complement form. This register value will clear when after the next valid measurement is made.

DZRA 7	DZRA6	DZRA5	DZRA4	DZRA3	DZRA2	DZRA1	DZRA0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DZRB 7	**DZRB6**	**DZRB5**	**DZRB4**	**DZRB3**	**DZRB2**	**DZRB1**	**DZRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Data Output Z Registers A and B

Data Output Register Operation

When one or more of the output registers are read, new data cannot be placed in any of the output data registers until all six data output registers are read. This requirement also impacts DRDY and RDY, which cannot be cleared until new data is placed in all the output registers.

Status Register

The status register is an 8-bit read-only register. This register is used to indicate device status. SR0 through SR7 indicate bit locations, with *SR* denoting the bits that are in the status register. SR7 denotes the first bit of the data stream.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
(0)	(0)	(0)	(0)	(0)	REN (0)	LOCK (0)	RDY(0)

Status Register

Location	Name	Description
SR7 to SR3	0	These bits must be cleared for correct operation.
SR2	REN	Regulator Enabled Bit. This bit is set when the internal voltage regulator is enabled. This bit is cleared when the internal regulator is disabled.
SR1	LOCK	Data output register lock. This bit is set when this some but not all for of the six data output registers have been read. When this bit is set, the six data output registers are locked and any new data will not be placed in these register until on of four conditions are met: one, all six have been read or the mode changed, two, a POR is issued, three, the mode is changed, or four, the measurement is changed.
SR0	RDY	Ready Bit. Set when data is written to all six data registers. Cleared when device initiates a write to the data output registers, when in off mode, and after one or more of the data output registers are written to. When RDY bit is clear it shall remain cleared for a minimum of 5 µs. DRDY pin can be used as an alternative to the status register for monitoring the device for conversion data.

Status Register Bit Designations

Identification Register A

The identification register A is used to identify the device. IRA0 through IRA7 indicate bit locations, with *IRA* denoting the bits that are in the identification register A. IRA7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

The identification value for this device is stored in this register. This is a read-only register.
Register values. ASCII value *H*

IRA7	IRA6	IRA5	IRA4	IRA3	IRA2	IRA1	IRA0
0	1	0	0	1	0	0	0

Identification Register A Default Values

Identification Register B

The identification register B is used to identify the device. IRB0 through IRB7 indicate bit locations, with *IRB* denoting the bits that are in the identification register A. IRB7 denotes the first bit of the data stream.

Register values. ASCII value *4*

IRB7	IRB6	IRB5	IRB4	IRB3	IRB2	IRB1	IRB0
0	0	1	1	0	1	0	0

Identification Register B Default Values

Identification Register C

The identification register C is used to identify the device. IRC0 through IRC7 indicate bit locations, with *IRC* denoting the bits that are in the identification register A. IRC7 denotes the first bit of the data stream.

Register values. ASCII value *3*

IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0
0	0	1	1	0	0	1	1

Identification Register C Default Values

I²C COMMUNICATION PROTOCOL

The HMC5843 communicates via a two-wire I2C bus system as a slave device. The HMC5843 uses a simple protocol with the interface protocol defined by the I2C bus specification, and by this document. The data rate is at the standard-mode 100kbps or 400kbps rates as defined in the I2C Bus Specifications. The bus bit format is an 8-bit Data/Address send and a 1-bit acknowledge bit. The format of the data bytes (payload) shall be case sensitive ASCII characters or binary data to the HMC5843 slave, and binary data returned. Negative binary values will be in two's complement form. The default (factory) HMC5843 7-bit slave address is 0x3C for write operations, or 0x3D for read operations.

The HMC5843 Serial Clock (SCL) and Serial Data (SDA) lines have optional internal pull-up resistors, but require resistive pull-ups (Rp) between the master device (usually a host microprocessor) and the HMC5843. Pull-up resistance values of about 10k ohms are recommended with a nominal 1.8-volt digital supply voltage (DVDD). Other values may be used as defined in the I2C Bus Specifications or with the internal 50k ohm pull-up resistors (SDAP, SCLP) that can be tied to DVDD.

The SCL and SDA lines in this bus specification can be connected to a host of devices. The bus can be a single master to multiple slaves, or it can be a multiple master configuration. All data transfers are initiated by the master device which is responsible for generating the clock signal, and the data transfers are 8 bit long. All devices are addressed by I2C's unique 7 bit address. After each 8-bit transfer, the master device generates a 9 th clock pulse, and releases the SDA line. The receiving device (addressed slave) will pull the SDA line low to acknowledge (ACK) the successful transfer or leave the SDA high to negative acknowledge (NACK).

Per the I2C spec, all transitions in the SDA line must occur when SCL is low. This requirement leads to two unique conditions on the bus associated with the SDA transitions when SCL is high. Master device pulling the SDA line low while the SCL line is high indicates the Start (S) condition, and the Stop (P) condition is when the SDA line is pulled high while the SCL line is high. The I2C protocol also allows for the Restart condition in which the master device issues a second start condition without issuing a stop.

All bus transactions begin with the master device issuing the start sequence followed by the slave address byte. The address byte contains the slave address; the upper 7 bits (bits7-1), and the Least Significant bit (LSb). The LSb of the address byte designates if the operation is a read (LSb=1) or a write (LSb=0). At the 9 th clock pulse, the recieving slave device will issue the ACK (or NACK). Following these bus events, the master will send data bytes for a write operation, or the slave will clock out data with a read operation. All bus transactions are terminated with the master issuing a stop sequence.

I2C bus control can be implemented with either hardware logic or in software. Typical hardware designs will release the SDA and SCL lines as appropriate to allow the slave device to manipulate these lines. In a software implementation, care must be taken to perform these tasks in code.

A HMC5843 COMMUNICATION EXAMPLE

The HMC5843 has a fairly quick stabilization time from no voltage to stable and ready for data retrieval. The nominal 5 milli-seconds with the factory default single measurement mode means that the six Bytes of magnetic data registers (DXRA, DXRB, DYRA, DYRB, DZRA, and DZRB) are filled with a valid first measurement.

To change the measurement mode to continuous measurement mode, after the 5 milli-second power-up time send the three bytes:

0x3C 0x02 0x00

This writes the 00 into the second register or mode register to switch from single to continuous measurement mode setting. With the data rate at the factory default of 10Hz updates (100 milli-seconds interval), a 100 milli-second delay should be made by the I2C master before querying the HMC5843 data registers for new measurements. To clock out the new data, send:

0x3D, and clock out DXRA, DXRB, DYRA, DYRB, DZRA, DZRB located in registers 3 through 8. The HMC5843 will automatically re-point back to register 3 for the next 0x3D query, expected 100 milli-seconds or later.