Transistors

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ITT INTERMETALL

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b	Imaginary part of y-Parameters
b_f	Imaginary part of forward transconductance y_f
b_i	Imaginary part of input admittance y_i
b_o	Imaginary part of output admittance y_o
b_r	Imaginary part of reverse transconductance y_r
B	Base connection
B_G	Imaginary part of generator (source) impedance
C	Capacitance; junction capacitance; collector connection
C_i	Input capacitance ($b_i/2\pi f$)
C_o	Output capacitance ($b_o/2\pi f$)
C_{CBO}	Collector-Base capacitance (open emitter)
C_{EBO}	Emitter-base capacitance (open collector)
C_{iss}	Input capacitance
C_r	Feedback capacitance ($b_r/2\pi f$)
E	Emitter connection
f	Frequency
f_T	Gain-bandwidth product
F	Noise figure
F_c	Noise figure in mixer stages
g	Real part of y-parameters
g_f	Real part of forward transconductance y_f
g_i	Real part of input admittance y_i
g_m	Forward transconductance
g_o	Real part of output admittance y_o
g_r	Real part of reverse transconductance y_r
g_s	Generator conductance
G_C	Current gain
G_P	Power gain
$G_{P\,av}$	Available power gain
$G_{P\,max}$	Max. available power gain
G_V	Voltage gain
h	Parameters of h- (hybrid) matrix
h_f	Small-signal current gain
h_i	Input impedance
h_o	Output admittance
h_r	Reverse voltage transfer ratio
h_{FE}	DC current gain, common emitter
I_B	Base current
I_{BM}	Peak base current
I_{B1}	Turn-on current
I_{B2}	Turn-off current
I_C	Collector current
I_{CAV}	Average collector current
I_{CBO}	Collector-base cutoff current (open emitter)
I_{CEO}	Collector-emitter cutoff current (open base)
I_{CER}	Collector-emitter cutoff current (specified resistance between base and emitter)
I_{CES}	Collector-emitter cutoff current (base short-circuited to emitter)
I_{CEV}	Collector-emitter cutoff current (specified voltage between base and emitter)
I_{CM}	Peak collector current
I_D	Drain current
I_{DSS}	Drain cutoff current
I_E	Emitter current
I_{EBO}	Emitter-base cutoff current (open collector)
I_{GSS}	Gate-body leakage current
K_V	Thermal resistance correction factor
P_{tot}	Power dissipation
P_D	Continuous power dissipation
P_I	Pulse power dissipation
$r_{b'} \cdot C_C$	Collector-base time constant
$r_{DS\,(ON)}$	Drain-source-on resistance
r_{thA}	Pulse thermal resistance junction to ambient air
r_{thC}	Pulse thermal resistance junction to case
R	Resistance; resistor
R_{BE}	Resistance between base and emitter
R_G	Generator impedance; source impedance
$R_{G\,opt}$	Optimum (matched) generator resistance
R_L	Load resistance
$R_{L\,opt}$	Optimum (matched) load resistance
R_S	Series resistance
R_{th}	Thermal resistance
R_{thA}	Thermal resistance junction to ambient air
R_{thC}	Thermal resistance junction to case resp. mounting base
$R_{thC/S}$	Thermal resistance case or mounting base to heat sink
R_{thS}	Thermal resistance heat sink to ambient air
t	Time
t_d	Delay time
t_f	Fall Time
t_{off}	Turn-off time ($t_s + t_f$)
t_{on}	Turn-on time ($t_d + t_r$)
t_p	Pulse duration
t_{pd}	Propagation delay time
t_r	Rise time
t_s	Storage time
t_{total}	Total switching time ($t_{on} + t_{off}$)
T	Temperature; duration of one period
T_{amb}	Ambient temperature
T_j	Junction temperature
T_C	Case temperature
T_S	Storage temperature
T_{SB}	Temperature of substrate backside
V	Voltage
V_{BB}	Base supply voltage
V_{BE}	Base-emitter voltage
$V_{BE\,sat}$	Base-emitter saturation voltage

$V_{(BR)CBO}$	Collector-base breakdown voltage (open emitter)
$V_{(BR)CEO}$	Collector-emitter breakdown voltage (open base)
$V_{(BR)CER}$	Collector-emitter breakdown voltage (specified resistance between base and emitter)
$V_{(BR)CES}$	Collector-emitter breakdown voltage (emitter short-circuited to base)
V_{DGS}	Drain-gate voltage
V_{DSS}	Drain-source voltage
$V_{(BR)DSS}$	Drain-source breakdown voltage
$V_{(BR)EBO}$	Emitter-base breakdown voltage (open collector)
V_{CB}	Collector-base voltage
V_{CBO}	Collector-base voltage (open emitter)
V_{CC}	Collector supply voltage
V_{CE}	Collector-emitter voltage
V_{CEO}	Collector-emitter voltage (open base)
V_{CER}	Collector-emitter voltage (specified resistance between base and emitter)
V_{CES}	Collector-emitter voltage (emitter short-circuited to base)
$V_{CE\ sat}$	Collector-emitter saturation voltage
V_{CEV}	Collector-emitter voltage (specified voltage between base and emitter)
V_{EBO}	Emitter-base voltage (open collector)
V_{EE}	Emitter supply voltage
$V_{GS(TO)}$	Gate threshold voltage
V_i	Input voltage
V_o	Output voltage
y	Parameters of y- (admittance) matrix
y_f	Forward transconductance
y_i	Input admittance
y_o	Output admittance
y_r	Reverse transconductance
y_s	Generator admittance
Z_1	Input impedance
Z_2	Output impedance
φ	Phase angle of y-parameters
τ_S	Storage time constant
ν	Duty cycle (t_p/T)

Characteristics and Maximum Ratings

The electrical performance of a semiconductor device is usually expressed in terms of its characteristics and maximum ratings.

Characteristics are those which can be measured by use of suitable measuring instruments and circuits, and provide information on the performance of the device under specified operating conditions (at a given bias, for example). Depending on requirements, they are quoted either as typical (Typ.) values or guaranteed (Min., Max.) values.

Typical values are expressed as figures or as one or more curves, and are subject to spreads. Occasionally a typical curve is accompanied by another curve, this being a 95%, or, in a few cases, a maximum spread limit curve.

Maximum Ratings give the values which cannot be exceeded without risk of damage to the device. Changes in supply voltage and in the tolerances of other components in the circuit must also be taken into consideration. No single maximum rating should ever be exceeded, even when the device is operated well within the other maximum ratings. The inclusion of the word “admissible” in a title means that the associated curve defines the maximum ratings.

An exception to this rule are data on collector current. The collector current, quoted as one of the critical transistor values, is a maximum value recommended by the manufacturer which should be noted in connection with the other characteristics valid for this collector current (e.g. collector and saturation voltages, current gain etc.) when selecting a transistor. In certain cases, the quoted collector current may be exceeded without the transistor being destroyed. The absolute limit for the collector current is determined by the maximum admissible power dissipation of the transistor.

Assembly and Soldering Instructions

To prevent transistors from being damaged during mounting, observe the following points:

All semiconductor devices are extremely sensitive to their maximum admissible junction temperature being exceeded. When planning the layout of the equipment, the distance between heat sources and semiconductor elements should be sufficiently large.

Semiconductor elements may be mounted in any desired position.

From the experience gained in soldering semiconductor elements the following rules have emerged:

For transistors in plastic case TO-92 the maximum soldering time is 8 s, at soldering temperatures between 230 and 260 °C. Here, the distance between soldered joint and case should be at least 4 mm. During soldering, the leads should not be subjected to mechanical stress.

For transistors in plastic case SOT-23 the maximum soldering time is 8 s, at maximum soldering temperatures between 230 and 260 °C.

Admissible Power Dissipation

The indicated maximum admissible junction temperature must not be exceeded because this could damage or cause the destruction of the transistor crystal. Since the user cannot measure this temperature, data sheets also reveal the maximum admissible power dissipation P_{tot} usually in the form of a derating curve (see diagram).

If power dissipation is kept within these limits the maximum junction temperature will not be exceeded. This can easily be checked by using the equation

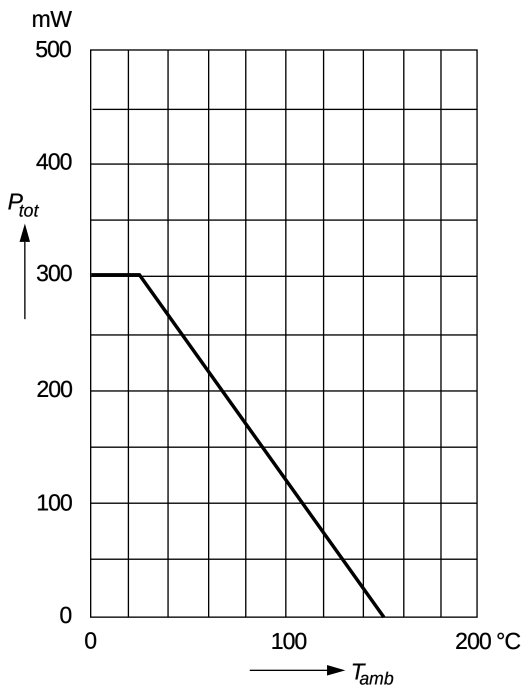
$T_j = T_{amb} + P_{tot} \cdot R_{th}$

For the thermal resistance R_{th} the junction to ambient thermal resistance R_{thA} is usually substituted in the case of small transistors (in the TO-18 or TO-92 package). In the case of power transistors (in the TO-202 or similar packages) which are usually mounted on a cooling fin or heat sink for the purpose of heat dissipation, the sum of the junction to case thermal resistance R_{thC} plus the heat sink to ambient thermal resistance R_{thS} plus – for more accurate calculations – the mounting surface to heat sink thermal resistance, is substituted for the thermal resistance in this equation. In order to keep the mounting surface to heat sink thermal resistance low, a heat conducting compound (silicone grease) is to be applied to the mounting surface before the transistor is screwed on. If a mica insulation is used, the thermal resistance of the mica washer must be added, which amounts to about 0.5 K/W.

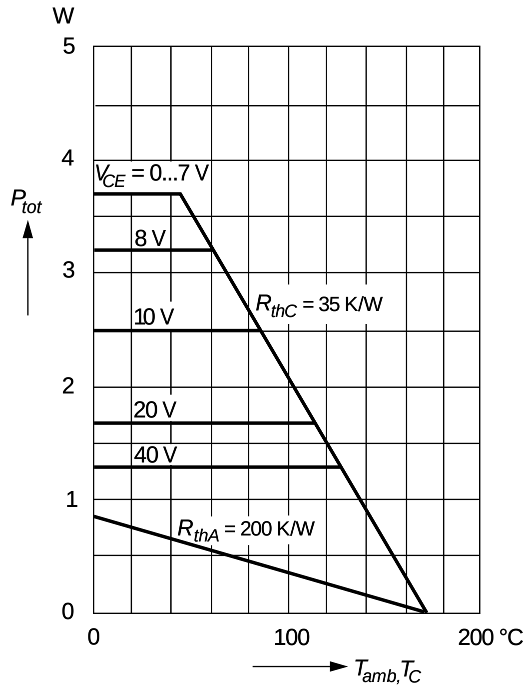
Directions for determining the thermal resistance R_{thS} for cooling fins can be found on page 11.

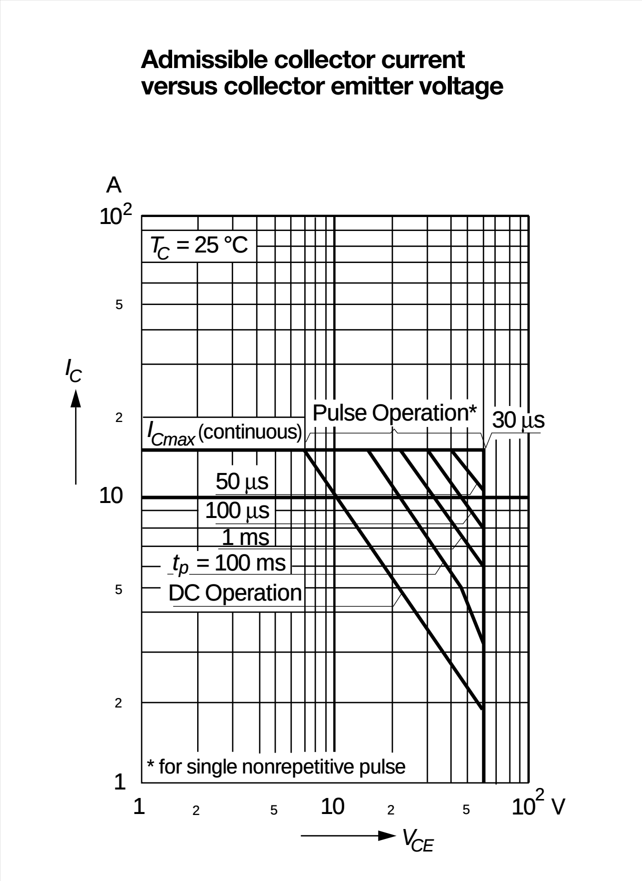
Since the distribution of heat in the transistor crystal is not uniform and depends on voltage and current, some transistors are accompanied by derating curves showing P_{tot} as a function of T_C and T_{amb} with the collector voltage V_{CE} as parameter (see diagram below).

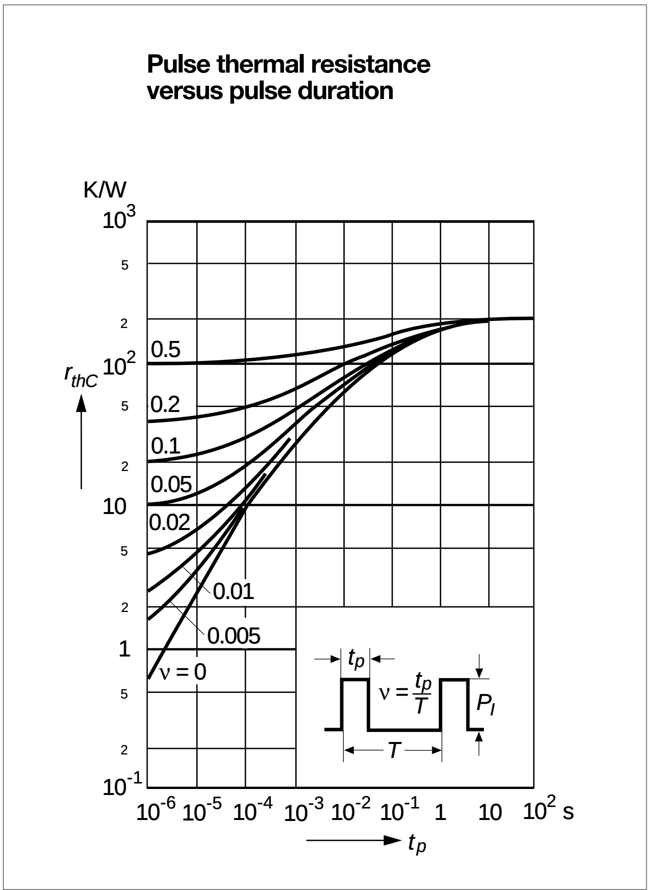
Admissible power dissipation versus ambient temperature



Admissible power dissipation versus temperature







For some power transistors the data sheets also contain a diagram giving “admissible collector current” or “permissible operating range” which gives further information on admissible power dissipation. One example is illustrated in the diagram left.

These diagrams are based on continuous power dissipation. However, pulse power dissipation may usually exceed continuous power dissipation. To ascertain maximum admissible pulse power dissipation P_I, reference is made to the pulse junction to case thermal resistance r_{thC} or the pulse junction to ambient thermal resistance r_{thA} whose value can be derived from the $r_{th} = f(t_p)$ diagram below.

Use the equation

$$T_j = T_{amb} + P_I \cdot r_{thA}$$

or, if the continuous power dissipation P_D is to be taken into consideration:

$$T_j = T_{amb} + P_D \cdot R_{thA} + P_I \cdot r_{thA}$$

If the transistor is mounted on a cooling fin then the equation becomes:

$$T_j = T_{amb} + P_{tot} \cdot R_{thS} + P_I \cdot r_{thC}$$

wherein P_{tot} is the mean value of the pulse power dissipation P_I. Where continuous power dissipation must be considered in addition, the equation is expanded accordingly:

$$T_j = T_{amb} + P_{tot} \cdot R_{thS} + P_D \cdot R_{thC} + P_I \cdot r_{thC}$$

wherein P_{tot} is the mean value of the total power dissipation.

The thermal resistance and pulse thermal resistance values derived from the data sheets apply without limitation only to small collector-emitter voltages V_{CE}, between about 5 and 10 V. For higher voltages these thermal resistance values have to be multiplied by a correction factor K_V which has to be calculated from the previously mentioned derating curves. The admissible power dissipation $P_{tot\ max}$, applicable to low collector voltages, must be divided by the admissible power dissipation $P_{tot\ V}$ for the higher collector voltage V:

$$K_v = \frac{P_{tot\ max}}{P_{tot\ V}}$$

The complete equation for T_j then reads:

$$T_j = T_{amb} + P_{tot} \cdot R_{thS} + P_D \cdot K_V \cdot R_{thC} + P_I \cdot K_V \cdot r_{thC}$$

Heat Removal from Transistors

The operation of any semiconductor device involves the dissipation of power with a consequent rise in junction temperature. Because the maximum admissible junction temperature must not be exceeded, careful circuit design with due regard not only to the electrical, but also the thermal performance of a semiconductor circuit, is essential.

If the dissipated power is low, then sufficient heat is radiated from the surface of the case; if the dissipation is high, however, additional steps may have to be taken to promote this process by reducing the thermal resistance between the junction and the ambient air. This can be achieved either by pushing a star- or flag-shaped heat dissipator over the case, or by bolting the semiconductor device to a heat sink.

P, the power to be dissipated, T_j the junction temperature, and T_{amb}, the ambient temperature are related by the formula

$$P = \frac{T_j - T_{amb}}{R_{thA}} = \frac{T_j - T_{amb}}{R_{thC} + R_{thS}}$$

where R_{thA} is the total thermal resistance between junction and ambient air. The total thermal resistance in turn comprises an internal thermal resistance R_{thC} between the junction and the mounting base, and an outer thermal resistance R_{thS} between the case and the surrounding air (or any other cooling medium). It should be noted that only the outer thermal resistance is affected by the design of the heat sink. To determine the size of the heat sink required to meet given operating conditions, proceed as follows: First calculate the outer thermal resistance by use of the formula

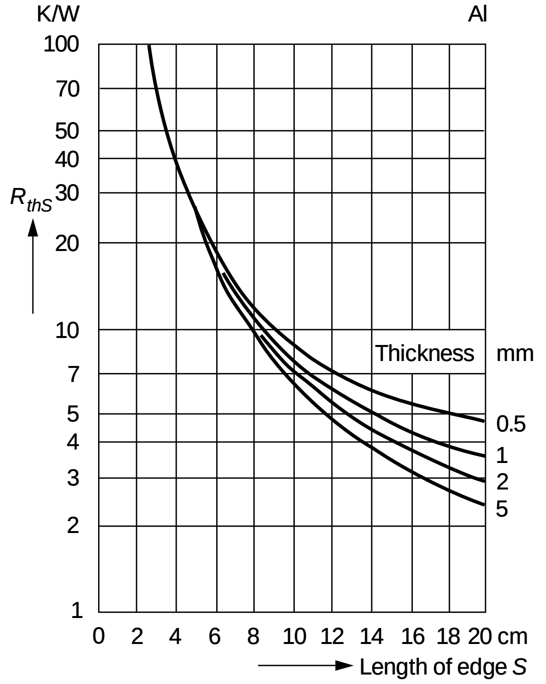
$$R_{thS} < \frac{T_j - T_{amb}}{P} - R_{thC}$$

and then, by use of the diagrams, determine the size of the heat sink which provides the calculated R_{thS}-value. To determine the maximum admissible device dissipation and ambient temperature limit for a given heat sink, proceed in the reverse order to that described above.

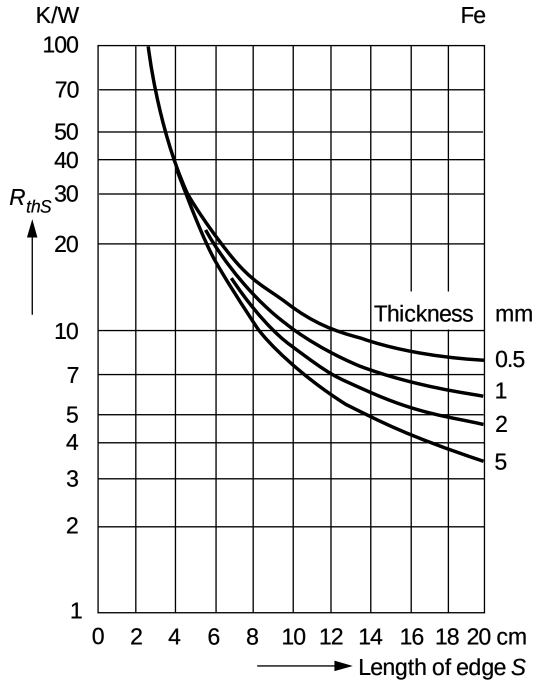
The calculations are based on the following assumptions: Use of a squareshaped heat sink without any finish, mounted in a vertical position; semiconductor device located in the centre of the sink; heat sink operated in still air and not subjected to any additional heat radiation. The calculated area should be increased by a factor of 1.3 if the sink is mounted horizontally, and can be reduced by a factor of approximately 0.7 if a black finish is used.

The curves give the thermal to ambient resistance of square vertical heat sinks as a function of side length. It is assumed that the heat is applied at the center of the square.

Aluminium Cooling Fin

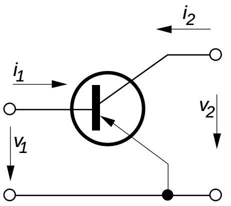


Steel Cooling Fin

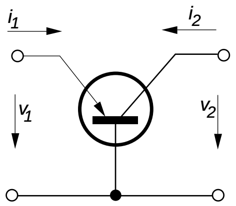


Basic Circuits

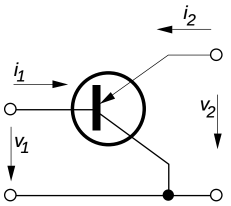
There are three basic transistor circuits. They are called according to that electrode (emitter, base, collector) which is common to both input and output circuit.



Common Emitter



Common Base



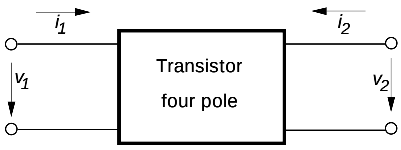
Common Collector

Properties of the three basic circuits:

	Common Emitter	Common Base	Common Collector
Input impedance	medium	small	high
Output impedance	medium	high	small
Current gain	high	less than 1	high
Upper frequency limit	low	high	low

Four-Pole-Symbols of h-Matrix

A transistor can be considered as an active four-pole network. When driven with small low-frequency signals its properties can be described by the four characteristic values of the h- (hybrid) matrix, which are assumed to be real.



$$v_1 = h_i \cdot i_1 + h_r \cdot v_2$$

$$i_2 = h_f \cdot i_1 + h_o \cdot v_2$$

If expressed this in matrix form we obtain:

$$\begin{pmatrix} v_1 \\ i_2 \end{pmatrix} = (h)\begin{pmatrix} i_1 \\ v_2 \end{pmatrix} \qquad (h) = \begin{pmatrix} h_i & h_r \\ h_f & h_o \end{pmatrix}$$

Explanation of h-Parameters

Input impedance (shorted output, $v_2 = 0$):

$$h_i = \frac{v_1}{i_1}$$

Reverse voltage transfer ratio (open input, $i_1 = 0$):

$$h_r = \frac{v_1}{v_2}$$

Small-signal current gain (shorted output, $v_2 = 0$):

$$h_f = \frac{i_2}{i_1}$$

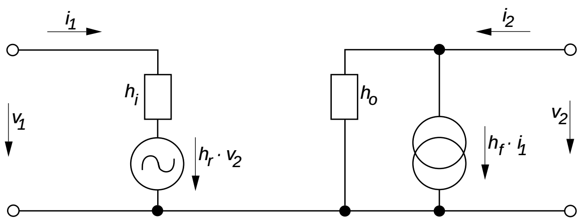
Output admittance (open input, $i_1 = 0$):

$$h_o = \frac{i_2}{v_2}$$

A frequently used abbreviation is the determinant:

$\Delta h = h_i \cdot h_o - h_r \cdot h_f$

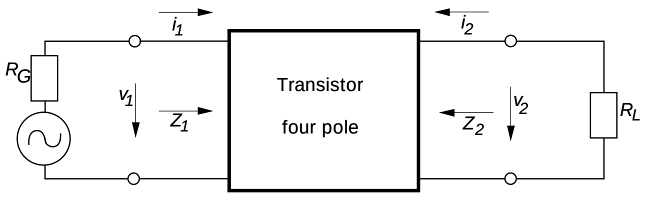
For all three basic circuit configurations the circuit illustrated below represents the equivalent four-pole circuit using h-parameters.



In the transistor data sheets the h-parameters are usually quoted for the common emitter configuration and for a given operating point (bias). The latter is determined by the collector voltage, the emitter or collector current and by the ambient temperature. For different operating points, correction factors are needed which can be gathered from the relevant curves. For common base or common collector transistor stage calculations, the appropriate h-parameters are ascertained from those of the common emitter configuration by using the following conversion formulas.

	Common Emitter	Common Base	Common Collector
Input impedance	h_{ie}	$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$	$h_{ic} = h_{ie}$
Reverse voltage transfer ratio	h_{re}	$h_{rb} = \frac{h_{ie} \cdot h_{oe}}{1 + h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re}$
Small-signal current gain	h_{fe}	$h_{fb} = -\frac{h_{fe}}{1 + h_{fe}}$	$-h_{fc} = 1 + h_{fe}$
Output admittance	h_{oe}	$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$	$h_{oc} = h_{oe}$

Calculation of a Transistor Stage



Input impedance

$$Z_1 = \frac{v_1}{i_1} = \frac{h_i + R_L \cdot \Delta h}{1 + h_o \cdot R_L}$$

Output impedance

$$Z_2 = \frac{v_2}{i_2} = \frac{h_i + R_G}{\Delta h + h_o \cdot R_G}$$

Current gain

$$G_c = \frac{i_2}{i_1} = \frac{h_f}{1 + h_o \cdot R_L}$$

Voltage gain

$$G_v = \frac{v_2}{v_1} = \frac{-h_f \cdot R_L}{h_i + R_L \cdot \Delta h}$$

Power gain

$$G_p = \frac{v_2 \cdot i_2}{v_1 \cdot i_1} = \frac{h_f^2 \cdot R_L}{(1 + h_o \cdot R_L)(h_i + R_L \cdot \Delta h)}$$

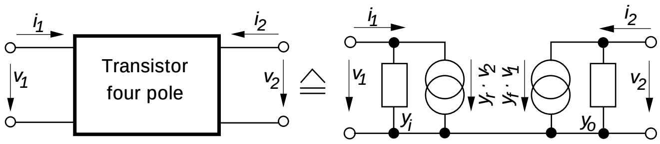
Max. available power gain, input and output matched with $R_{G\,opt}$ resp. $R_{L\,opt}$

$$G_{p\,max} = \left(\frac{h_f}{\sqrt{\Delta h} + \sqrt{h_i \cdot h_o}}\right)^2$$

$$R_{G\,opt} = \sqrt{\frac{h_i \cdot \Delta h}{h_o}} \qquad R_{L\,opt} = \sqrt{\frac{h_i}{h_o \cdot \Delta h}}$$

Four-Pole Symbols of y-Matrix

Whereas the network behaviour of of low-frequency transistors could be described by using the h- (hybrid) matrix, the y- (admittance) matrix is usually employed for high frequency transistors.



$$i_1 = y_i \cdot v_1 + y_r \cdot v_2$$

$$i_2 = y_f \cdot v_1 + y_o \cdot v_2$$

In matrix form we obtain:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = (y) \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \qquad (y) = \begin{pmatrix} y_i & y_r \\ y_f & y_o \end{pmatrix}$$

The y-parameters are complex values which can be expressed as

$y_{ik} = g_{ik} + jb_{ik}$ with $b_{ik} = \omega C_{ik}$ or with $b_{ik} = -\frac{1}{\omega L_{ik}}$

Often, the following notation is expedient:

$y_{ik} = | y_{ik} | \exp j\varphi_{ik}$

By adding the suffix e, b, or c it is possible to indicate to which of the three basic circuit configurations the parameters are valid.

Explanation of y-Parameters

Input admittance (shorted output, $v_2 = 0$)

$$y_i = \frac{i_1}{v_1}$$

Reverse transconductance (shorted input, $v_1 = 0$)

$$y_r = \frac{i_1}{v_2}$$

Forward transconductance (shorted output, $v_2 = 0$)

$$y_f = \frac{i_2}{v_1}$$

Output admittance (shorted input, $v_1 = 0$)

$$y_o = \frac{i_2}{v_2}$$

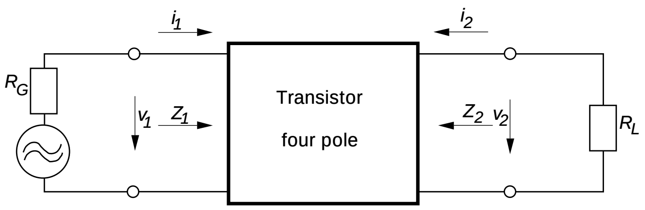
The determinant reads $\Delta y = y_i \cdot y_o - y_r \cdot y_f$

Conversion from y-Parameters to h-Parameters

$$h_i = \frac{1}{y_i} \qquad h_r = -\frac{y_r}{y_i} \qquad \Delta h = \frac{y_o}{y_i}$$

$$h_f = \frac{y_f}{y_i} \qquad h_o = \frac{\Delta y}{y_i}$$

Calculation of a Transistor Stage



Input impedance

$$Z_1 = \frac{v_1}{i_1} = \frac{1 + y_o \cdot R_L}{y_i + \Delta y \cdot R_L}$$

Output impedance

$$Z_2 = \frac{v_2}{i_2} = \frac{1 + y_i \cdot R_G}{y_o + \Delta y \cdot R_G}$$

Current gain

$$G_c = \frac{i_2}{i_1} = \frac{y_f}{y_i + \Delta y \cdot R_L}$$

Voltage gain

$$G_v = \frac{v_2}{v_1} = \frac{-y_f \cdot R_L}{1 + y_o \cdot R_L}$$

Power gain

$$G_p = \frac{v_2 \cdot i_2}{v_1 \cdot i_1} = \frac{|y_f|^2 \cdot R_L}{(1 + y_o \cdot R_L)(y_i + \Delta y \cdot R_L)}$$

Available power gain, input matched with $R_{G\,opt}$

$$G_{p\,av} = \frac{4 \cdot y_f^2 \cdot R_G \cdot R_L}{[(y_1 + \Delta y \cdot R_L) \cdot R_G + 1 + y_o \cdot R_L]^2}$$

Max. available power gain, input and output matched with $R_{G\,opt}$ resp. $R_{L\,opt}$

$$G_{p\,max} = \left(\frac{y_f}{\sqrt{\Delta y} + \sqrt{y_i \cdot y_o}} \right)^2$$

Max. available power gain will be attained if input and output are matched, where:

$$R_{L\,opt} = \sqrt{\frac{y_o}{y_i} \cdot \frac{1}{\Delta y}}$$

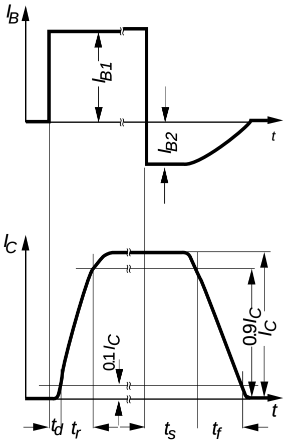
$$R_{G\,opt} = \sqrt{\frac{y_i}{y_o} \cdot \frac{1}{\Delta y}}$$

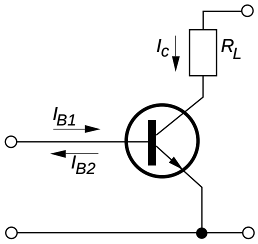
and:

$\Delta y = y_i \cdot y_o - y_r \cdot y_f$

Switching Times

Definitions for the various times which make up the total switching time can be gathered from the diagram below in which the switching characteristic of a transistor in common-emitter configuration is illustrated.



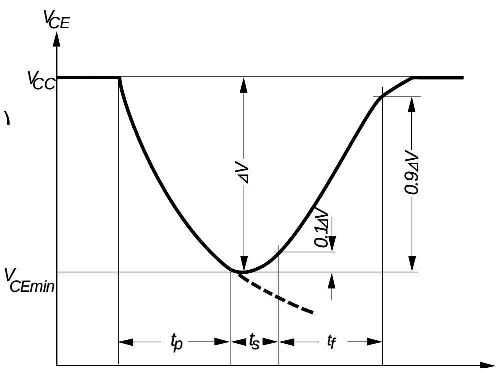


t_d	Delay time
t_r	Rise time
t_s	Storage time
t_f	Fall time
$t_{on} = t_d + t_r$	Turn-on time
$t_{off} = t_s + t_f$	Turn-off time

The duration of the switching times depends upon the transistor type and very much on the circuit arrangement.

With increasing saturation of the transistor the turn-on time decreases and the turn-off time increases. An increase of the turn-off current I_{B2} shortens the turn-off time.

The switching times depend on the duration of the turn-on pulse. It is only when the duration of this pulse is a multiple of the switching times that the latter remain constant. If the pulse is shorter, especially the storage time decreases. With a pulse duration in the region of the turn-on time the transistor is no longer fully saturated. The collector voltage then exhibits a characteristic such as is qualitatively represented in the diagram below.



ITT INTERMETALL's Quality Assurance and Reliability System

Our View of Quality and Reliability

ITT INTERMETALL gives the highest priority to developing, manufacturing, and delivering products that satisfy all our customers with respect to product performance, quality, reliability, on-time delivery, and competitive prices. Therefore, ITT INTERMETALL has implemented quality and reliability assurance activities in all phases of the product cycle from business development through product design, mass production, shipment, and marketing. Each department is responsible for the quality of its output and also each individual for the quality of his/her work. The quality system is based on the ISO 9000 concept. The system and the processes are continuously improved so that a steady progress in product quality can be achieved.

Quality Assurance during Product Development

The quality and reliability of a product are "built-in" during the product development and design phase. In IC development, functional simulations, design rule checks, and detailed resource planning are performed to get good quality products to the market in time.
Design reviews control the progress of development projects by measuring performance data against the targeted specification. The product release for production is determined by the results of extensive product performance evaluation as well as quality and reliability testing on prototypes.

Quality Assurance during Mass Production

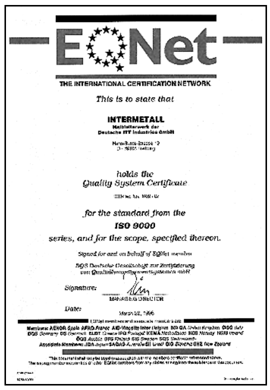
In a manufacturing line, processes are controlled by monitoring the relevant process parameters (SPC). Variations in processes are continuously reduced to increase yield, product performance, quality, and reliability. State-of-the-art production equipment and stable processes are essential for good quality products at competitive prices.
In order to achieve these goals, a wide variety of design and process changes are made after production release. Detailed qualification procedures ensure that these changes maintain or improve the quality and reliability of the products.

Quality Control of Outgoing Products

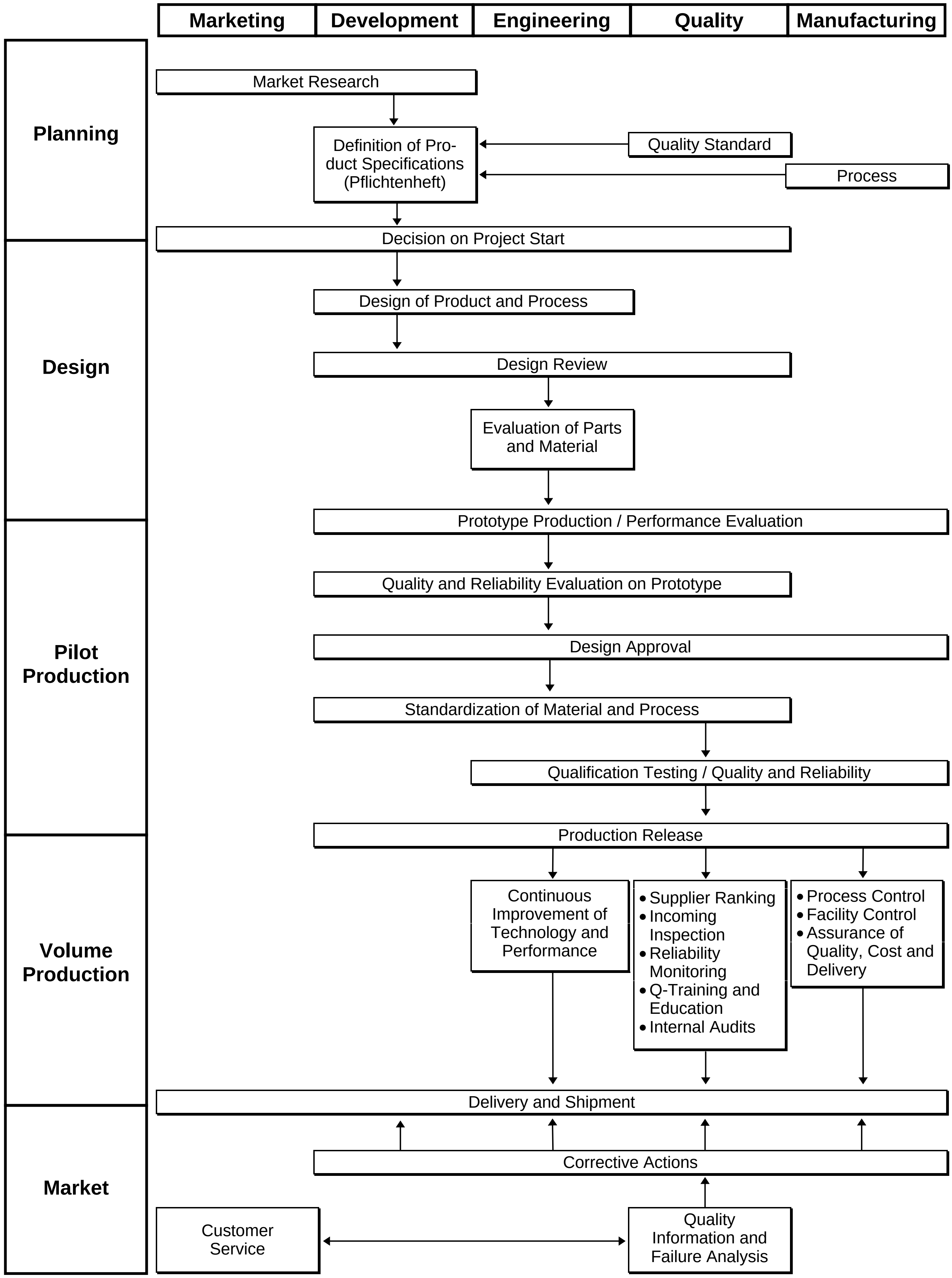
Although the quality and reliability is "built into" the products during products development and production, it is also verified by inspections.
Outgoing inspection of samples generates quality data that is fed back to previous processes for corrective actions.
A reliability monitoring program is installed to verify product reliability. Failure analysis is performed to find the root cause. The documented information is fed back to development and production departments for further product improvements. Reliability data is also used to predict product lifetime under specific environmental conditions.

Quality Control in the Market

Close contacts with key customers enable ITT INTERMETALL to collect quality information from the market. If a customer returns a failing product, it is subjected to detailed failure analysis until root causes are found. The history of the product, the results of the failure analysis, and the root causes are entered into a Quality Data Base (QDB). The evaluation of the data base is used to prioritize corrective action programs in all departments.



Product Quality and Assurance System

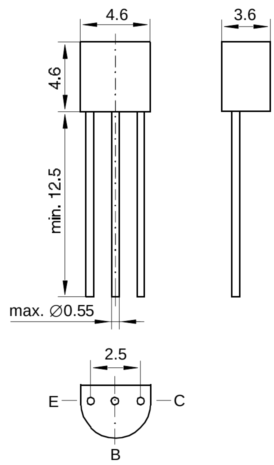


Small-Signal Transistors (NPN)

NPN Silicon Epitaxial Planar Transistor
for switching and amplifier applications.

As complementary type, the PNP transistor 2N3906 is recommended.

On special request, this transistor is also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	60	V
Collector-Emitter Voltage	V_{CEO}	40	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	100	mA
Peak Collector Current	I_{CM}	200	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	500[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = 1 V, I_C = 0.1 mA at V_{CE} = 1 V, I_C = 1 mA at V_{CE} = 1 V, I_C = 10 mA at V_{CE} = 1 V, I_C = 50 mA at V_{CE} = 1 V, I_C = 100 mA	 h_{FE} h_{FE} h_{FE} h_{FE} h_{FE}	 40 70 100 60 30	 – – – – –	 – – 300 – –	 – – – – –
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	250[1)]	K/W
Collector Saturation Voltage at I_C = 10 mA, I_B = 1 mA at I_C = 50 mA, I_B = 5 mA	 V_{CEsat} V_{CEsat}	 – –	 – –	 0.2 0.3	 V V
Base Saturation Voltage at I_C = 10 mA, I_B = 1 mA at I_C = 50 mA, I_B = 5 mA	 V_{BEsat} V_{BEsat}	 – –	 – –	 0.85 0.95	 V V
Collector-Emitter Cutoff Current V_{EB} = 3 V, V_{CE} = 30 V	I_{CEV}	–	–	50	nA
Emitter-Base Cutoff Current V_{EB} = 3 V, V_{CE} = 30 V	I_{EBV}	–	–	50	nA
Collector-Base Breakdown Voltage at I_C = 10 µA, I_E = 0	$V_{(BR)CBO}$	60	–	–	V
Collector-Emitter Breakdown Voltage at I_C = 1 mA, I_B = 0	$V_{(BR)CEO}$	40	–	–	V
Emitter-Base Breakdown Voltage at I_E = 10 µA, I_C = 0	$V_{(BR)EBO}$	6	–	–	V
Gain-Bandwidth Product at V_{CE} = 20 V, I_C = 10 mA, f = 100 MHz	f_T	300	–	–	MHz
Collector-Base Capacitance at V_{CB} = 5 V, f = 100 kHz	C_{CBO}	–	–	4	pF
Emitter-Base Capacitance at V_{EB} = 0.5 V, f = 100 kHz	C_{EBO}	–	–	8	pF
Input Impedance at V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	h_{ie}	1	–	10	kΩ
Voltage Feedback Ratio at V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	h_{re}	$0.5 \cdot 10^{-4}$	–	$8 \cdot 10^{-4}$	–
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case					

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Small-Signal Current Gain at V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	h_{fe}	100	–	400	–
Output Admittance at V_{CE} = 1 V, I_C = 1 mA, f = 1 kHz	h_{oe}	1	–	40	µS
Noise Figure at V_{CE} = 5 V, I_C = 100 µA, R_G = 1 kΩ, f = 10…15000 Hz	–	–	–	5	dB
Delay Time (see Fig. 1) at I_{B1} = 1 mA, I_C = 10 mA	t_d	–	–	35	ns
Rise Time (see Fig. 1) at I_{B1} = 1 mA, I_C = 10 mA	t_r	–	–	35	ns
Storage Time (see Fig. 2) at $-I_{B1} = I_{B2}$ = 1 mA, I_C = 10 mA	t_s	–	–	200	ns
Fall Time (see Fig. 2) at $-I_{B1} = I_{B2}$ = 1 mA, I_C = 10 mA	t_f	–	–	50	ns

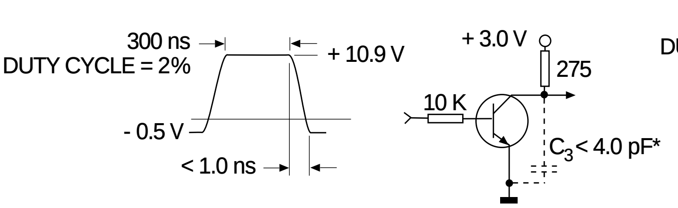


Fig. 1: Test circuit for delay and rise time

* total shunt capacitance of test jig and connectors

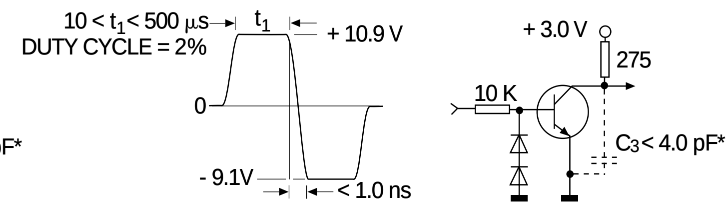
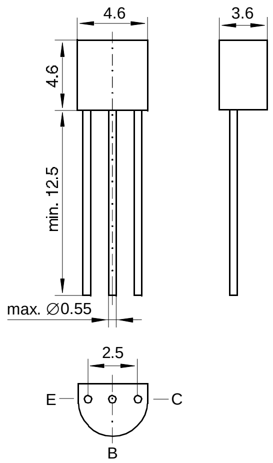


Fig. 2: Test circuit for storage and fall time

* total shunt capacitance of test jig and connectors

NPN Silicon Epitaxial Transistor
for switching and amplifier applications.
Especially suitable for AF-driver and
low-power output stages.

As complementary type, the PNP transistor 2N4126 is recommended.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	V
Collector-Base Voltage	V_{CBO}	30	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	200	mA
Peak Collector Current	I_{CM}	800	mA
Base Current	I_B	50	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	625[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

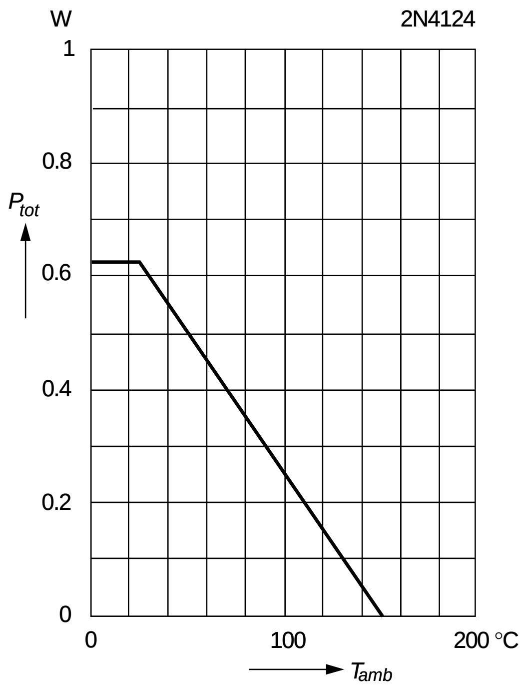
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = 1 V, I_C = 2.0 mA at V_{CE} = 1 V, I_C = 50 mA	 h_{FE} h_{FE}	 120 –	 – 60	 360 –	 – –
Collector-Base Cutoff Current at V_{CB} = 20 V	I_{CBO}	–	–	50	nA
Emitter-Base Cutoff Current at V_{EB} = 3 V	I_{EBO}	–	–	50	nA
Collector Saturation Voltage at I_C = 50 mA, I_B = 5 mA	V_{CESAT}	–	–	0.3	V
Base Saturation Voltage at I_C = 50 mA, I_B = 5 mA	V_{BESAT}	–	–	0.95	V
Collector-Emitter Breakdown Voltage at I_C = 1 mA	$V_{(BR)CEO}$	25	–	–	V
Collector-Base Breakdown Voltage at I_C = 10 µA	$V_{(BR)CBO}$	30	–	–	V
Emitter-Base Breakdown Voltage at I_E = 10 µA	$V_{(BR)EBO}$	5	–	–	V
Gain-Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz	f_T	–	200	–	MHz
Collector-Base Capacitance at V_{CB} = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	200[1)]	K/W

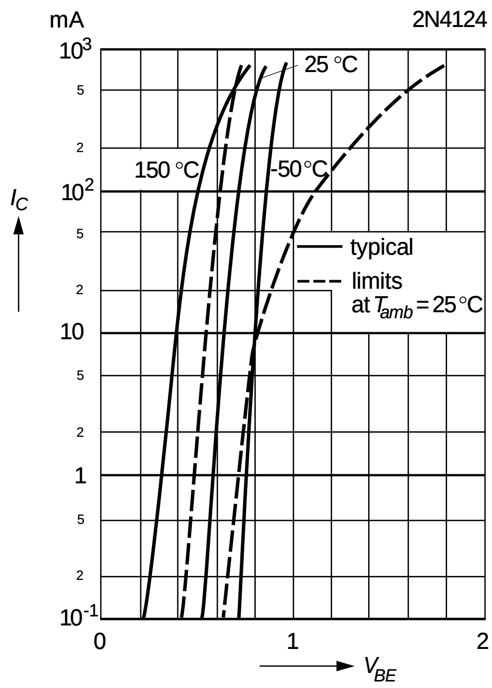
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

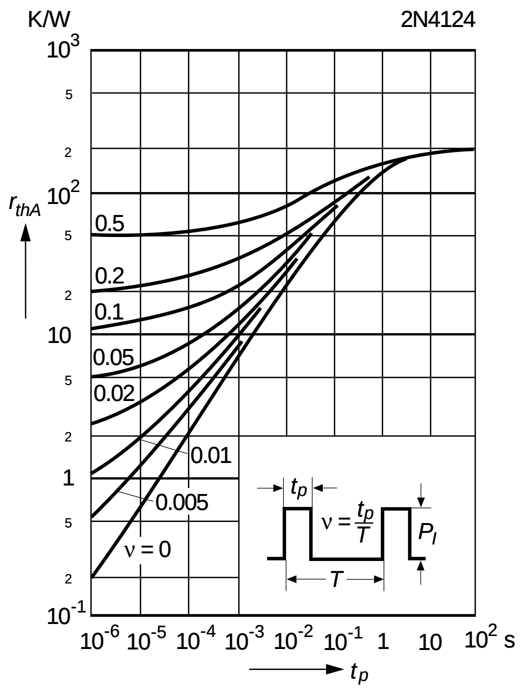


Collector current versus base-emitter voltage

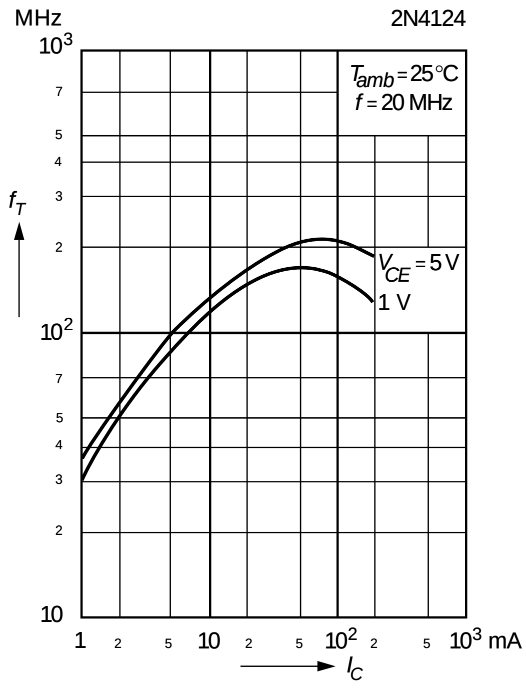


Pulse thermal resistance versus pulse duration

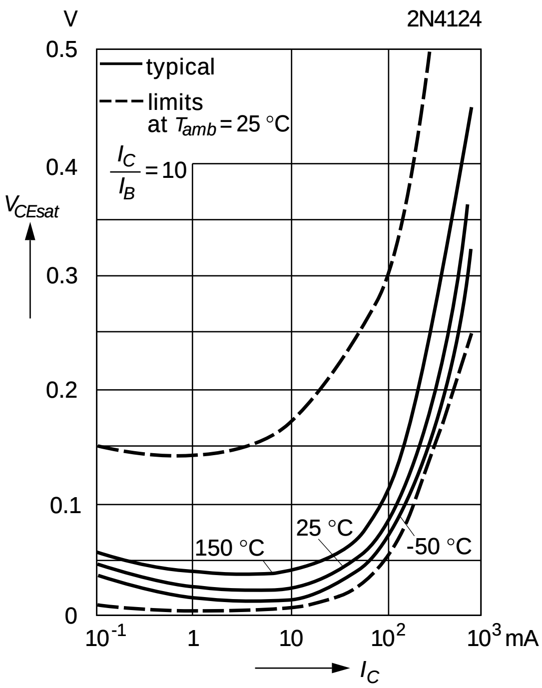
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



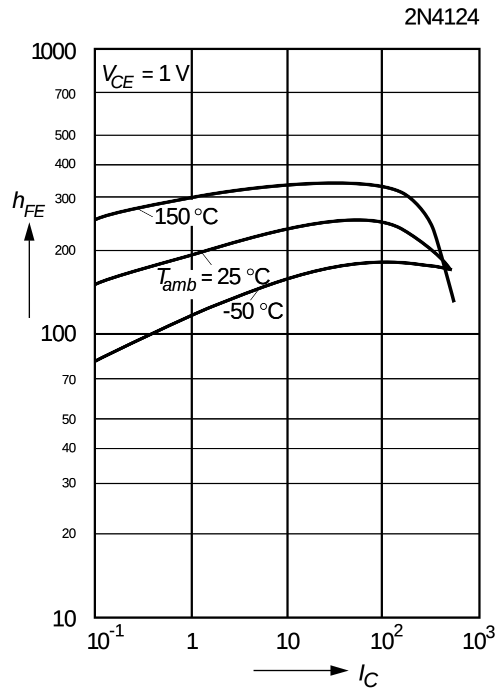
Gain-bandwidth product versus collector current



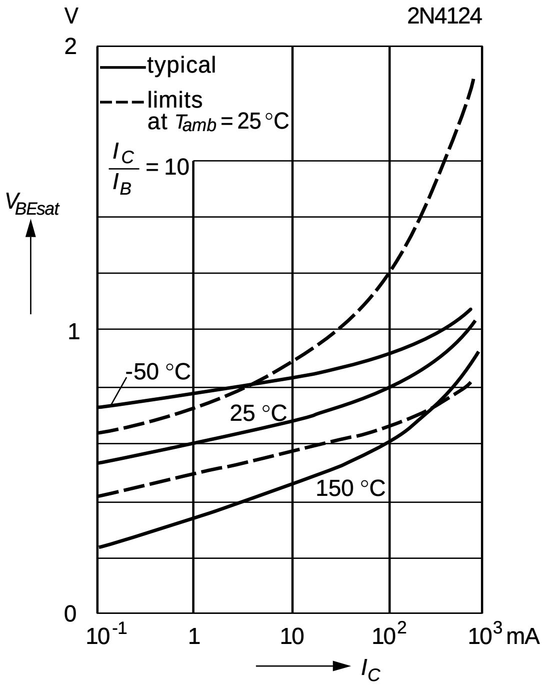
Collector saturation voltage versus collector current



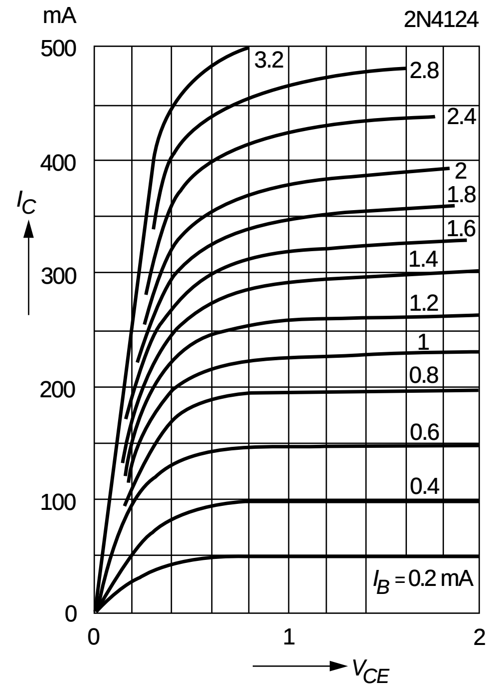
DC current gain versus collector current

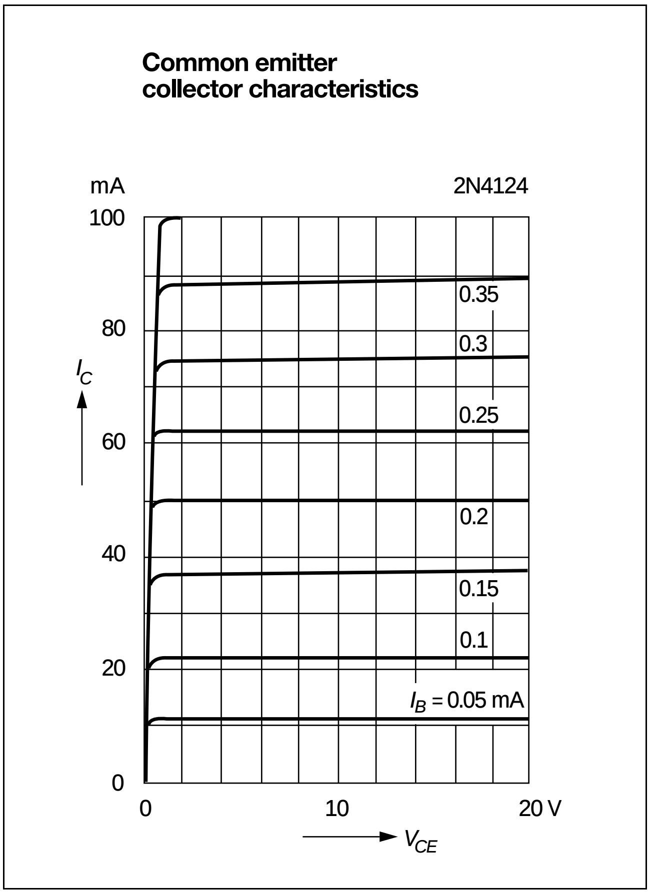


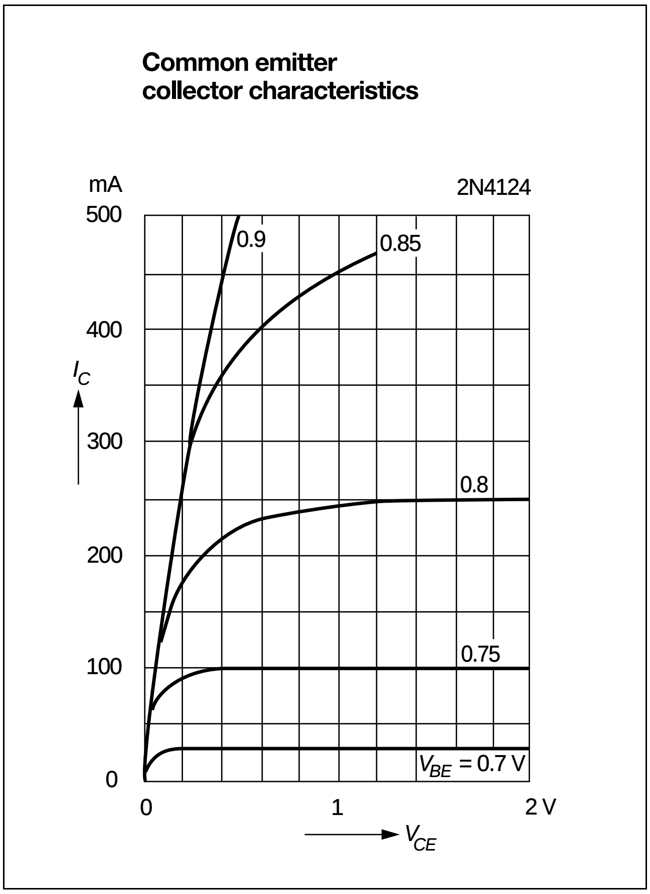
Base saturation voltage versus collector current



Common emitter collector characteristics



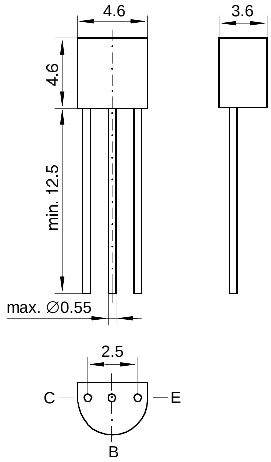

Common emitter
collector characteristics
mA
2N4124
100
80
60
40
20
0
I_C
0.35
0.3
0.25
0.2
0.15
0.1
I_B = 0.05 mA
0
10
20 V
V_{CE}


Common emitter
collector characteristics
mA
2N4124
500
400
300
200
100
0
I_C
0.9
0.85
0.8
0.75
V_{BE} = 0.7 V
0
1
2 V
V_{CE}

NPN Silicon Epitaxial Planar Transistors
for switching and amplifier applications. Especially suitable for AF-driver stages and low power output stages.

These types are also available subdivided into three groups -16, -25, and -40, according to their DC current gain. As complementary types, the PNP transistors BC327 and BC328 are recommended.

On special request, these transistors are also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Emitter Voltage	**BC337** **BC338**	V_{CES} V_{CES}	50 30	V V
Collector-Emitter Voltage	**BC337** **BC338**	V_{CEO} V_{CEO}	45 25	V V
Emitter-Base Voltage		V_{EBO}	5	V
Collector Current		I_C	800	mA
Peak Collector Current		I_{CM}	1	A
Base Current		I_B	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65 to +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case				

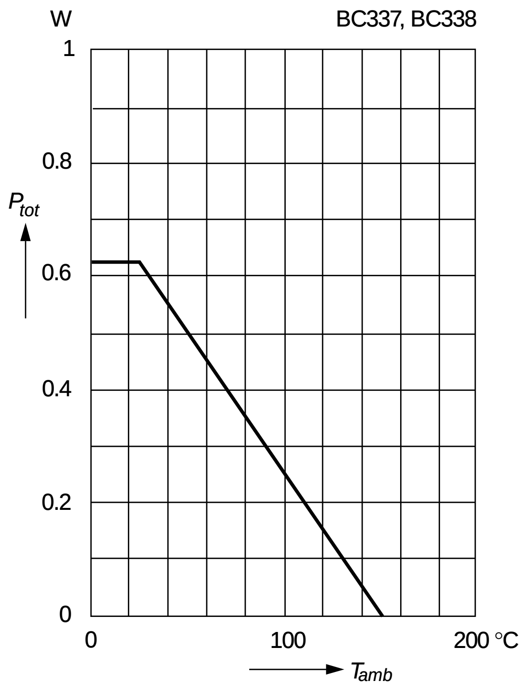
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = 1 V, I_C = 100 mA **Current Gain Group -16** **-25** **-40**	 h_{FE} h_{FE} h_{FE}	 100 160 250	 160 250 400	 250 400 630	 – – –
at V_{CE} = 1 V, I_C = 300 mA **Current Gain Group -16** **-25** **-40**	 h_{FE} h_{FE} h_{FE}	 60 100 170	 130 200 320	 – – –	 – – –
Collector-Emitter Cutoff Current at V_{CE} = 45 V **BC337** at V_{CE} = 25 V **BC338** at V_{CE} = 45 V, T_{amb} = 125 °C **BC337** at V_{CE} = 25 V, T_{amb} = 125 °C **BC338**	 I_{CES} I_{CES} I_{CES} I_{CES}	 – – – –	 2 2 – –	 100 100 10 10	 nA nA µA µA
Collector-Emitter Breakdown Voltage at I_C = 10 mA **BC338** **BC337**	 $V_{(BR)CEO}$ $V_{(BR)CEO}$	 20 45	 – –	 – –	 V V
Collector-Emitter Breakdown Voltage at I_C = 0.1 mA **BC338** **BC337**	 $V_{(BR)CES}$ $V_{(BR)CES}$	 30 50	 – –	 – –	 V V
Emitter-Base Breakdown Voltage at I_E = 0.1 mA	$V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at I_C = 500 mA, I_B = 50 mA	V_{CEsat}	–	–	0.7	V
Base-Emitter Voltage at V_{CE} = 1 V, I_C = 300 mA	V_{BE}	–	–	1.2	V
Gain-Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector-Base Capacitance at V_{CB} = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	200[1)]	K/W

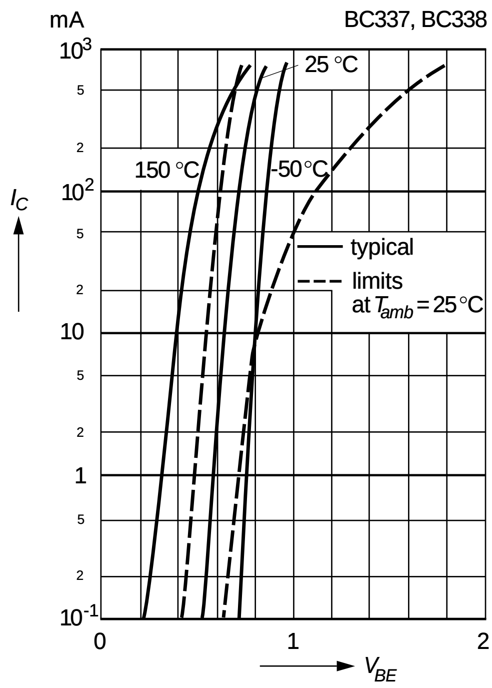
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

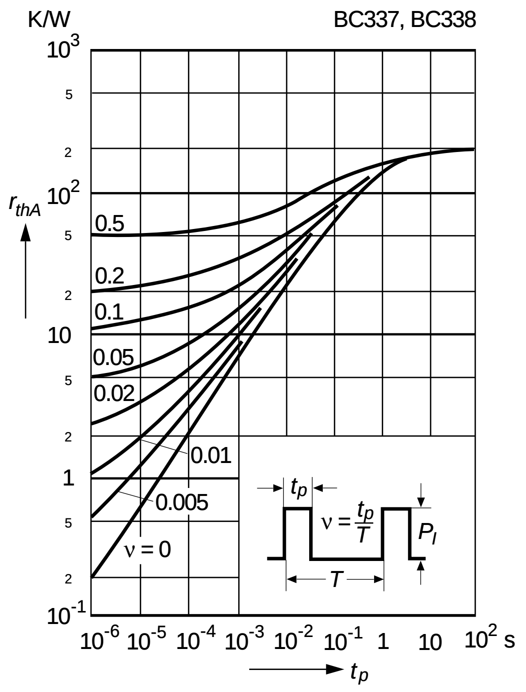


Collector current versus base-emitter voltage

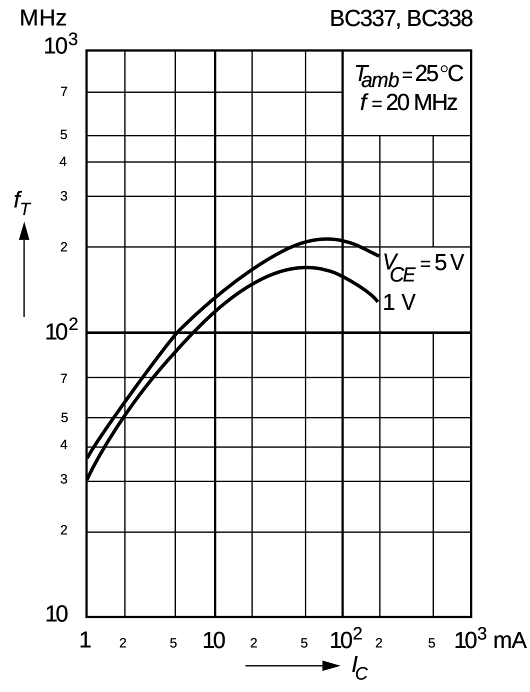


Pulse thermal resistance versus pulse duration

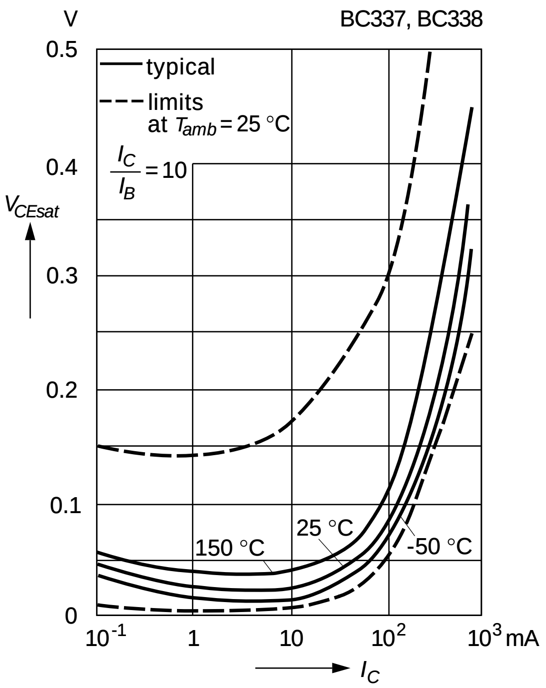
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



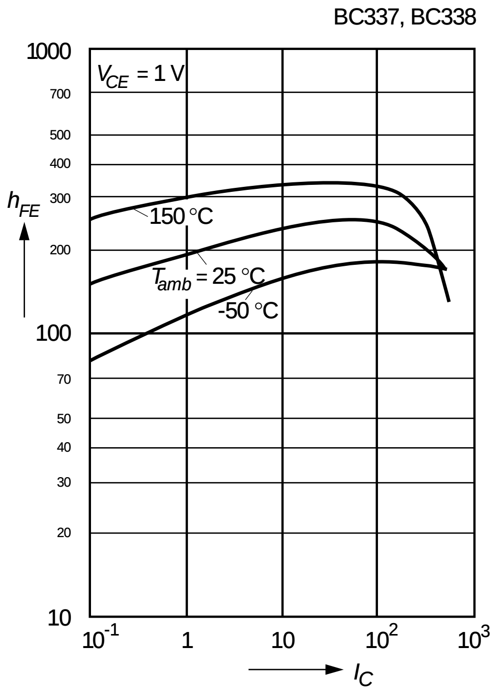
Gain-bandwidth product versus collector current



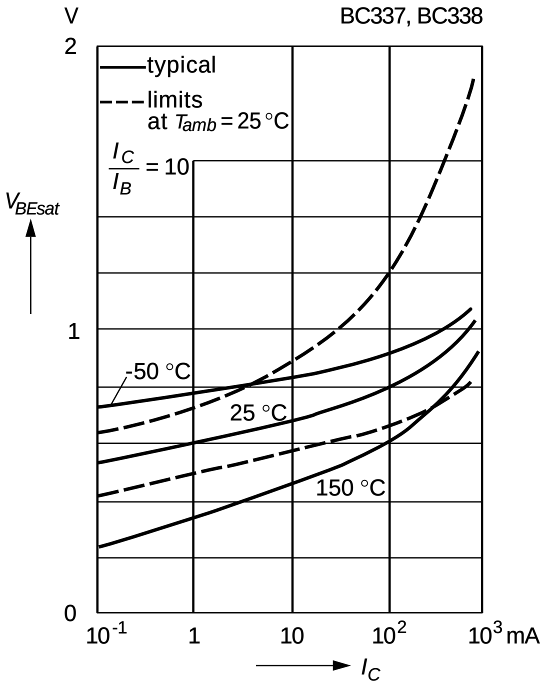
Collector saturation voltage versus collector current



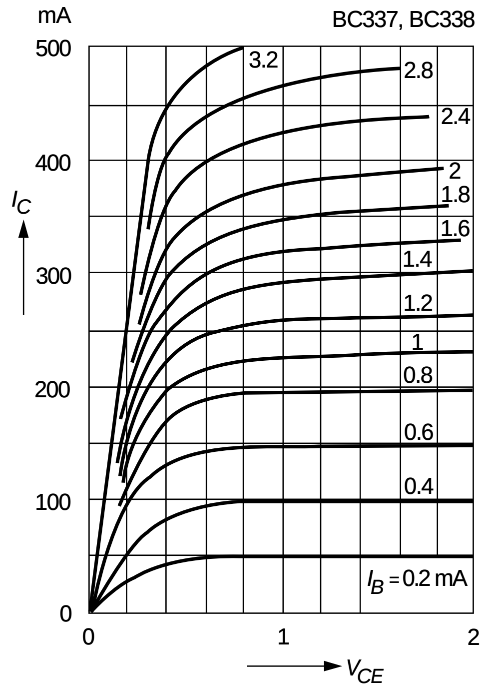
DC current gain versus collector current

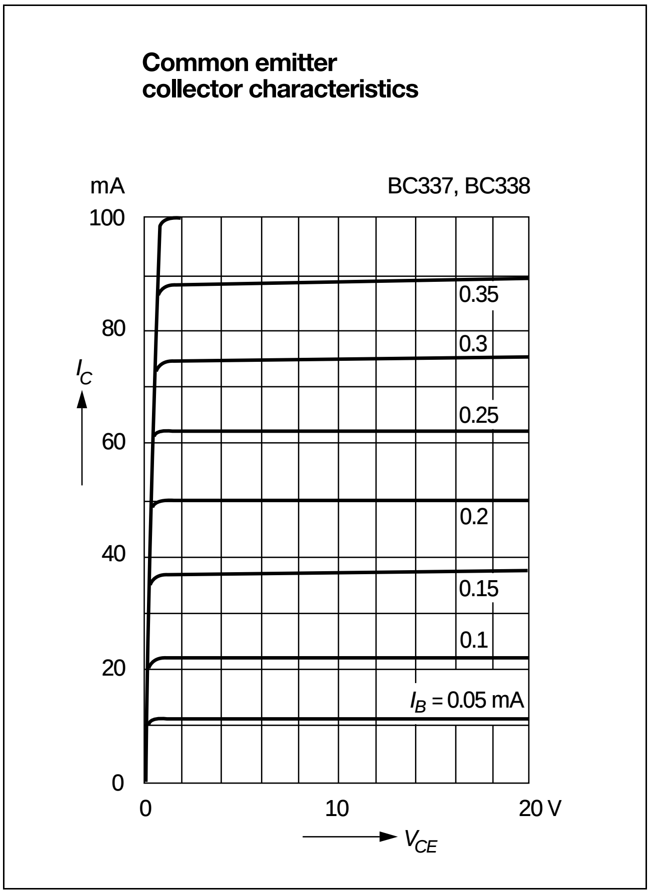


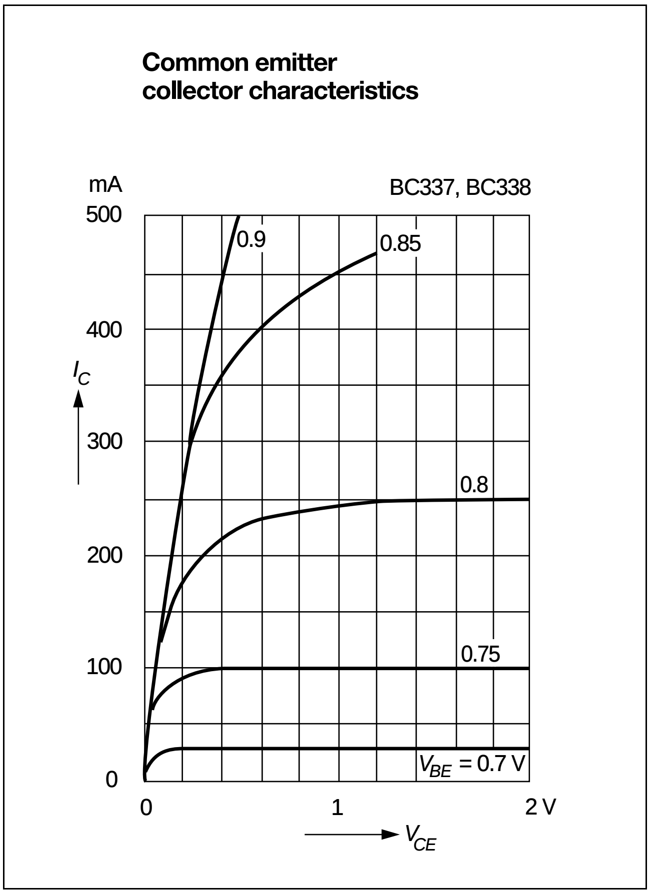
Base saturation voltage versus collector current



Common emitter collector characteristics



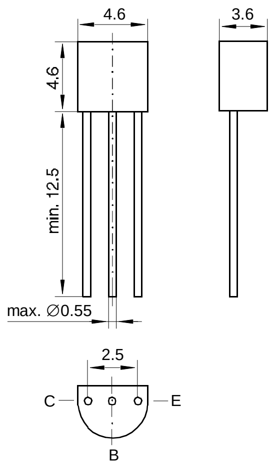

Common emitter
collector characteristics
BC337, BC338
mA
100
80
60
40
20
0
I_C
0
10
20 V
V_{CE}
0.35
0.3
0.25
0.2
0.15
0.1
I_B = 0.05 mA


Common emitter
collector characteristics
BC337, BC338
mA
500
400
300
200
100
0
I_C
0
1
2 V
V_{CE}
0.9
0.85
0.8
0.75
V_{BE} = 0.7 V

NPN Silicon Epitaxial Planar Transistors

These transistors are subdivided into three groups A, B and C according to their current gain. The type BC546 is available in groups A and B, however, the types BC547 and BC548 can be supplied in all three groups. The BC549 is a low-noise type and available in groups B and C. As complementary types, the PNP transistors BC556 … BC559 are recommended.

On special request, these transistors are also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Base Voltage	**BC546** **BC547** **BC548, BC549**	V_{CBO} V_{CBO} V_{CBO}	80 50 30	V V V
Collector-Emitter Voltage	**BC546** **BC547** **BC548, BC549**	V_{CES} V_{CES} V_{CES}	80 50 30	V V V
Collector-Emitter Voltage	**BC546** **BC547** **BC548, BC549**	V_{CEO} V_{CEO} V_{CEO}	65 45 30	V V V
Emitter-Base Voltage	**BC546, BC547** **BC548, BC549**	V_{EBO} V_{EBO}	6 5	V V
Collector Current		I_C	100	mA
Peak Collector Current		I_{CM}	200	mA
Peak Base Current		I_{BM}	200	mA
Peak Emitter Current		$-I_{EM}$	200	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
h-Parameters at V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz, Small Signal Current Gain					
Current Gain Group A	h_{fe}	–	220	–	–
B	h_{fe}	–	330	–	–
C	h_{fe}	–	600	–	–
Input Impedance **Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
B	h_{ie}	3.2	4.5	8.5	kΩ
C	h_{ie}	6	8.7	15	kΩ
Output Admittance **Current Gain Group A**	h_{oe}	–	18	30	µS
B	h_{oe}	–	30	60	µS
C	h_{oe}	–	60	110	µS
Reverse Voltage Transfer Ratio					
Current Gain Group A	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain at V_{CE} = 5 V, I_C = 10µA					
Current Gain Group A	h_{FE}	–	90	–	–
B	h_{FE}	–	150	–	–
C	h_{FE}	–	270	–	–
at V_{CE} = 5 V, I_C = 2 mA					
Current Gain Group A	h_{FE}	110	180	220	–
B	h_{FE}	200	290	450	–
C	h_{FE}	420	500	800	–
at V_{CE} = 5 V, I_C = 100 mA					
Current Gain Group A	h_{FE}	–	120	–	–
B	h_{FE}	–	200	–	–
C	h_{FE}	–	400	–	–
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	250[1)]	K/W
Collector Saturation Voltage					
at I_C = 10 mA, I_B = 0.5 mA	V_{CEsat}	–	80	200	mV
at I_C = 100 mA, I_B = 5 mA	V_{CEsat}	–	200	600	mV
Base Saturation Voltage					
at I_C = 10 mA, I_B = 0.5 mA	V_{BEsat}	–	700	–	mV
at I_C = 100 mA, I_B = 5 mA	V_{BEsat}	–	900	–	mV
Base-Emitter Voltage					
at V_{CE} = 5 V, I_C = 2 mA	V_{BE}	580	660	700	mV
at V_{CE} = 5 V, I_C = 10 mA	V_{BE}	–	–	720	mV
Collector-Emitter Cutoff Current					
at V_{CE} = 80 V **BC546**	I_{CES}	–	0.2	15	nA
at V_{CE} = 50 V **BC547**	I_{CES}	–	0.2	15	nA
at V_{CE} = 30 V **BC548, BC549**	I_{CES}	–	0.2	15	nA
at V_{CE} = 80 V, T_j = 125 °C **BC546**	I_{CES}	–	–	4	µA
at V_{CE} = 50 V, T_j = 125 °C **BC547**	I_{CES}	–	–	4	µA

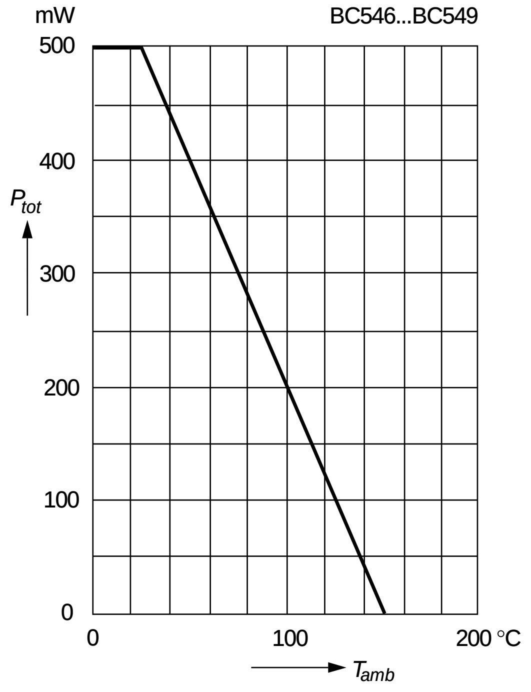
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
at V_{CE} = 30 V, T_j = 125 °C **BC548, BC549**	I_{CES}	–	–	4 4	µA µA
Gain-Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz	f_T	–	300	–	MHz
Collector-Base Capacitance at V_{CB} = 10 V, f = 1 MHz	C_{CBO}	–	3.5	6	pF
Emitter-Base Capacitance at V_{EB} = 0.5 V, f = 1 MHz	C_{EBO}	–	9	–	pF
Noise Figure at V_{CE} = 5 V, I_C = 200 µA, R_G = 2 kΩ, f = 1 kHz, Δf = 200 Hz **BC546, BC547**	F	–	2	10	dB
BC548 **BC549**	F	–	1.2	4	dB
at V_{CE} = 5 V, I_C = 200 µA, R_G = 2 kΩ, f = 30…15000 Hz **BC549**	F	–	1.4	4	dB

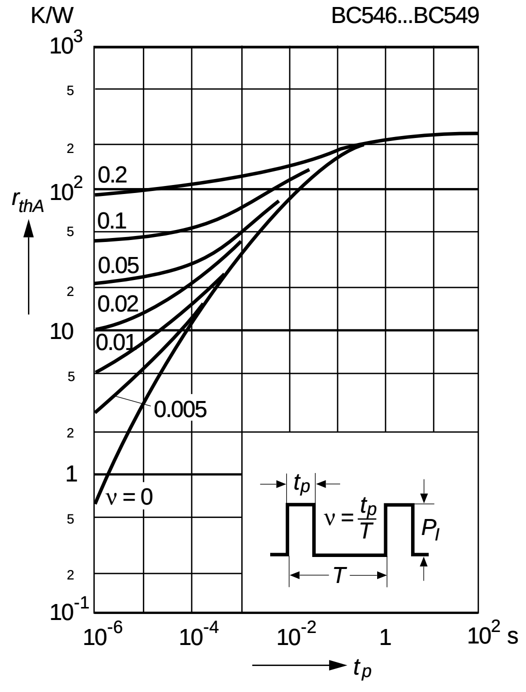
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

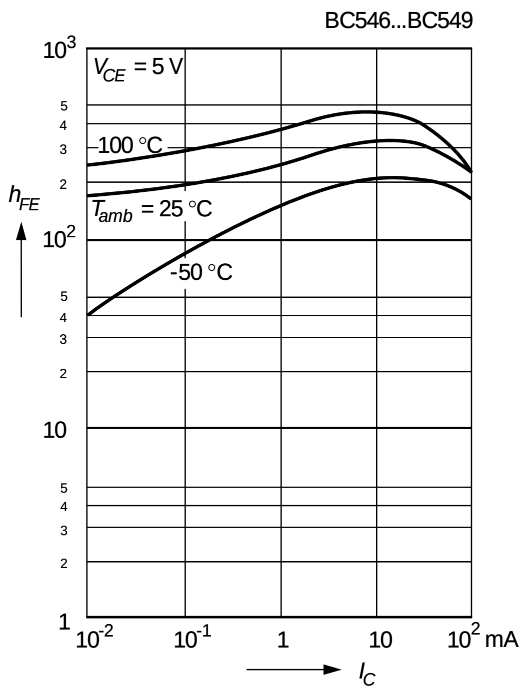


Pulse thermal resistance versus pulse duration

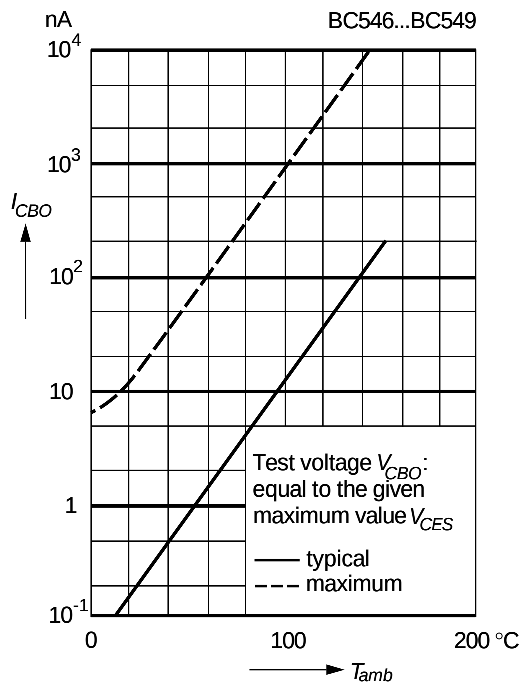
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



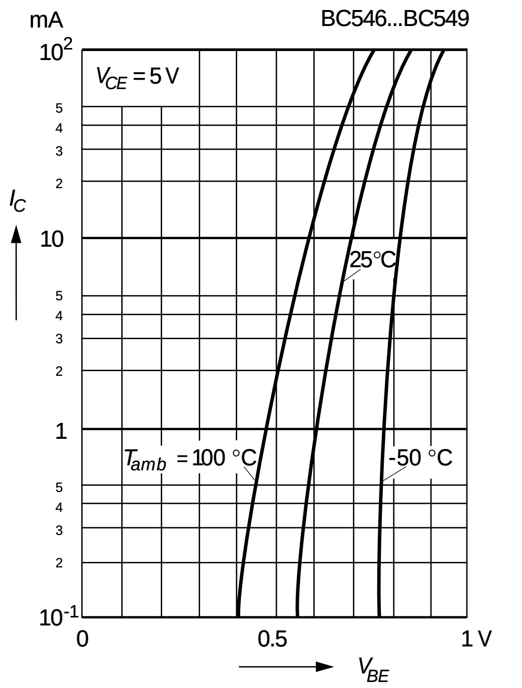
DC current gain versus collector current



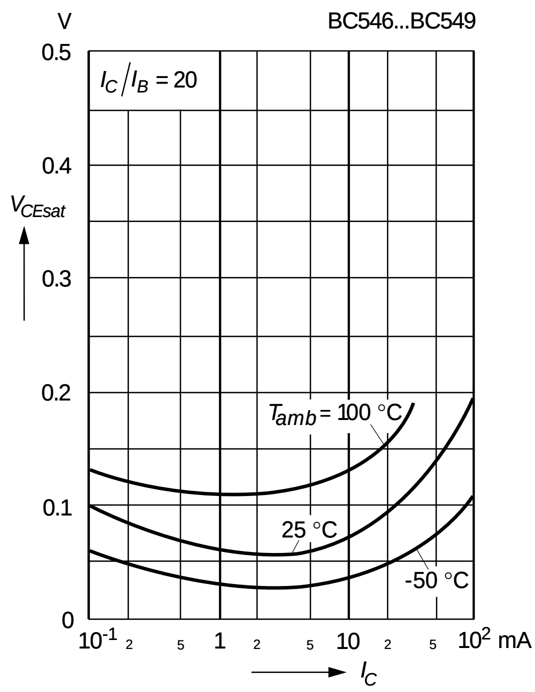
Collector-base cutoff current versus ambient temperature



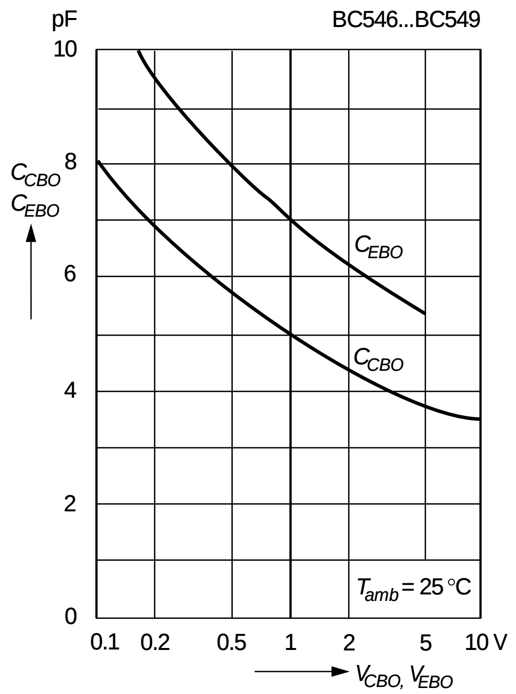
Collector current versus base-emitter voltage



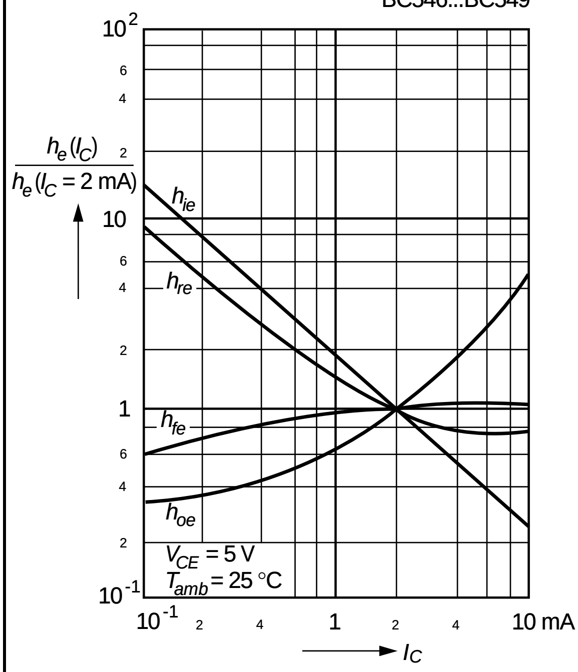
Collector saturation voltage versus collector current



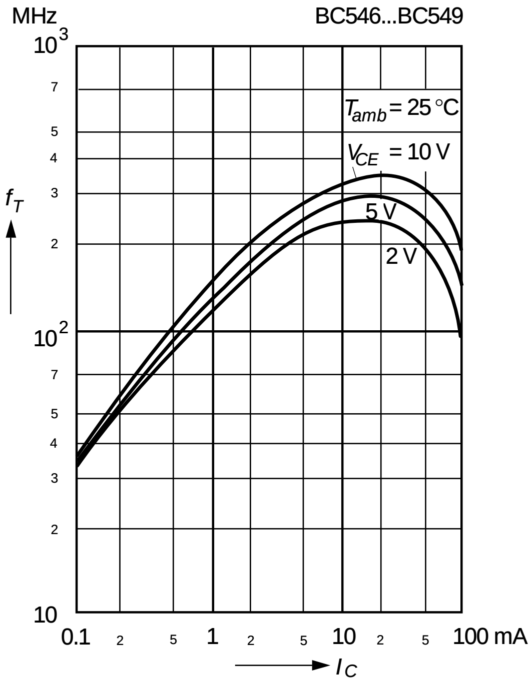
Collector-base capacitance, Emitter-base capacitance versus reverse bias voltage



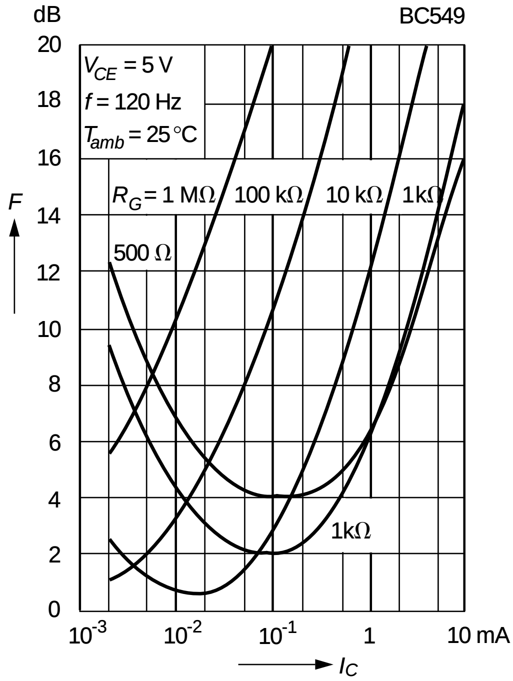
Relative h-parameters versus collector current



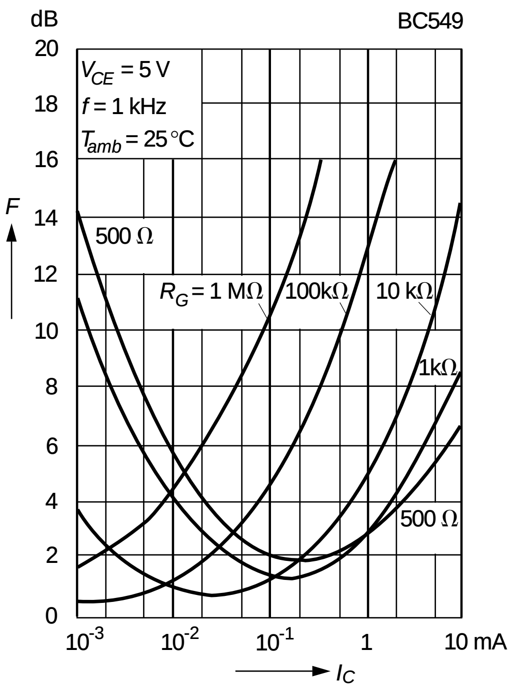
Gain-bandwidth product versus collector current



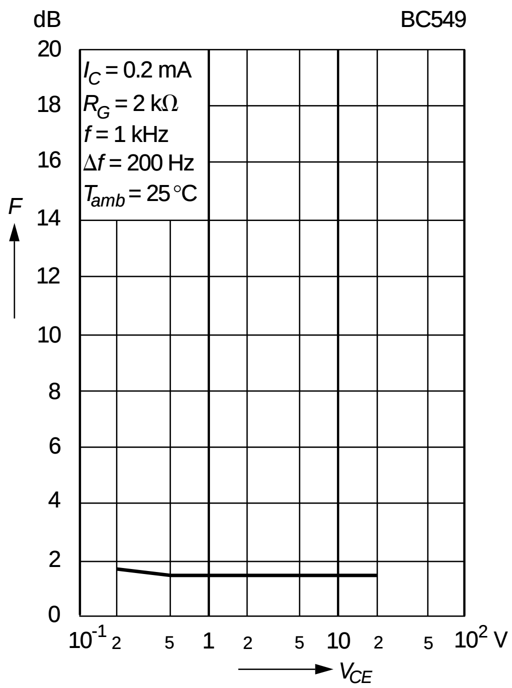
Noise figure versus collector current



Noise figure versus collector current



Noise figure versus collector emitter voltage



NPN Silicon Epitaxial Planar Transistors
for switching, AF driver and amplifier applications.

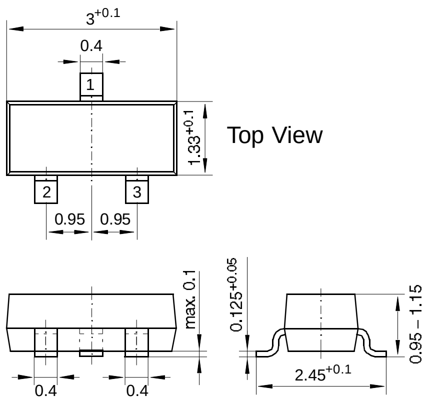
Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors are subdivided into three groups -16, -25 and -40 according to their current gain.
As complementary types, the PNP transistors BC807 and BC808 are recommended.

Pin configuration
1 = Collector, 2 = Base, 3 = Emitter.

Marking code

Type	Marking
BC817-16	6A
-25	6B
-40	6C
BC818-16	6E
-25	6F
-40	6G



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

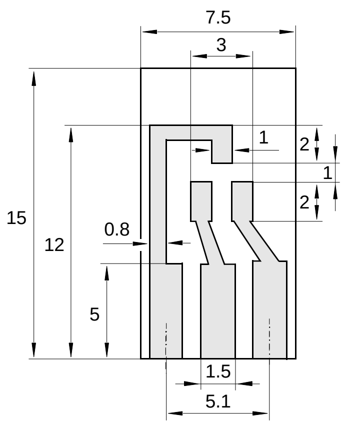
		Symbol	Value	Unit
Collector-Emitter Voltage	**BC817** **BC818**	V_{CES} V_{CES}	50 30	V V
Collector-Emitter Voltage	**BC817** **BC818**	V_{CEO} V_{CEO}	45 25	V V
Emitter-Base Voltage		V_{EBO}	5	V
Collector Current		I_C	800	mA
Peak Collector Current		I_{CM}	1000	mA
Peak Base Current		I_{BM}	200	mA
Peak Emitter Current		$-I_{EM}$	1000	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Device on fiberglass substrate, see layout

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = 1 V, I_C = 100 mA **Current Gain Group-16** **-25** **-40** at V_{CE} = 1 V, I_C = 300 mA **-16** **-25** **-40**	 h_{FE} h_{FE} h_{FE} h_{FE} h_{FE} h_{FE}	 100 160 250 60 100 170	 – – – – – –	 250 400 600 – – –	 – – – – – –
Thermal Resistance Junction Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Collector Saturation Voltage at I_C = 500 mA, I_B = 50 mA	V_{CEsat}	–	–	0.7	V
Base-Emitter Voltage at V_{CE} = 1 V, I_C = 300 mA	V_{BE}	–	–	1.2	V
Collector-Emitter Cutoff Current at V_{CE} = 45 V **BC817** at V_{CE} = 25 V **BC818** at V_{CE} = 25 V, T_j = 150 °C	 I_{CES} I_{CES} I_{CES}	 – – –	 – – –	 100 100 5	 nA nA µA
Emitter-Base Cutoff Current at V_{EB} = 4 V	I_{EBO}	–	–	100	nA
Gain-Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector-Base Capacitance at V_{CB} = 10 V, f = 1 MHz	C_{CBO}	–	12		pF

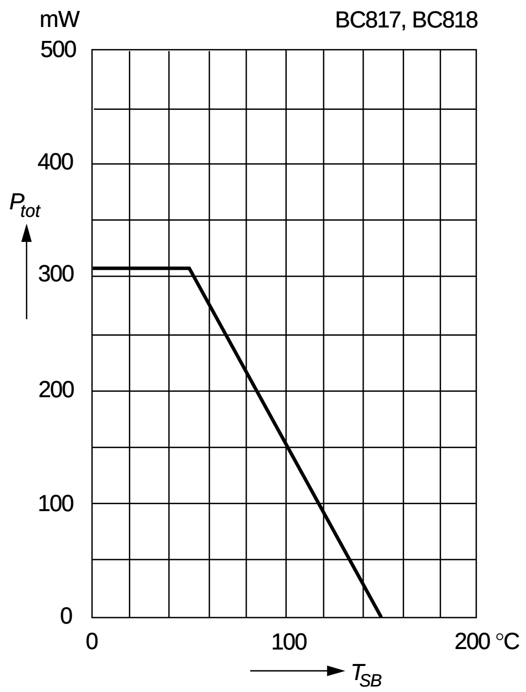
1) Device on fiberglass substrate, see layout



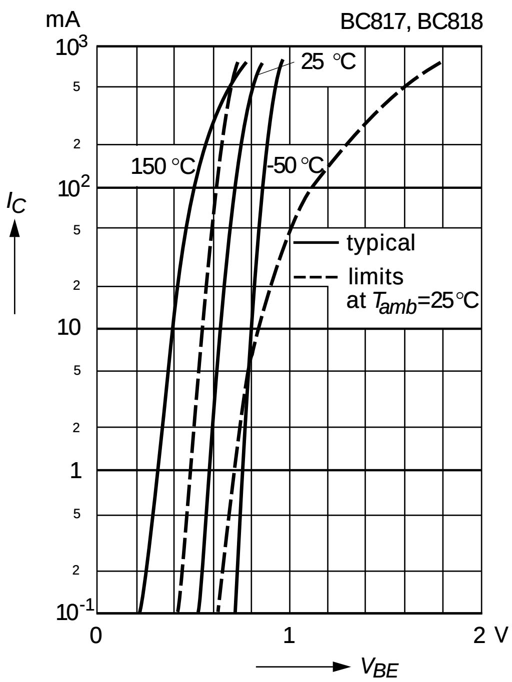
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout

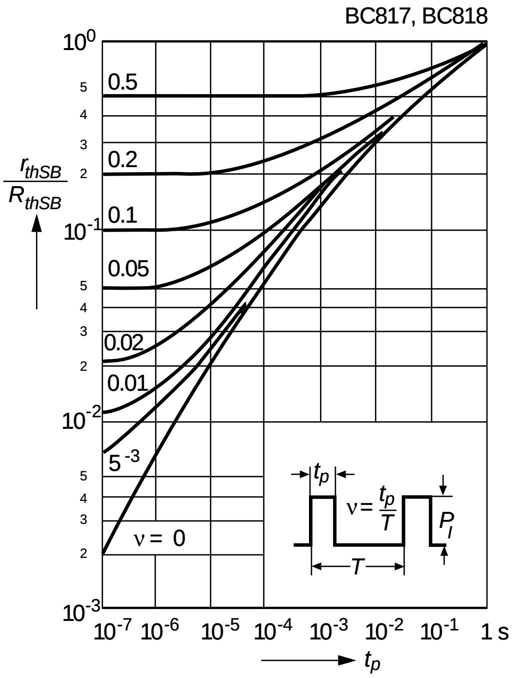


Collector current versus base-emitter voltage

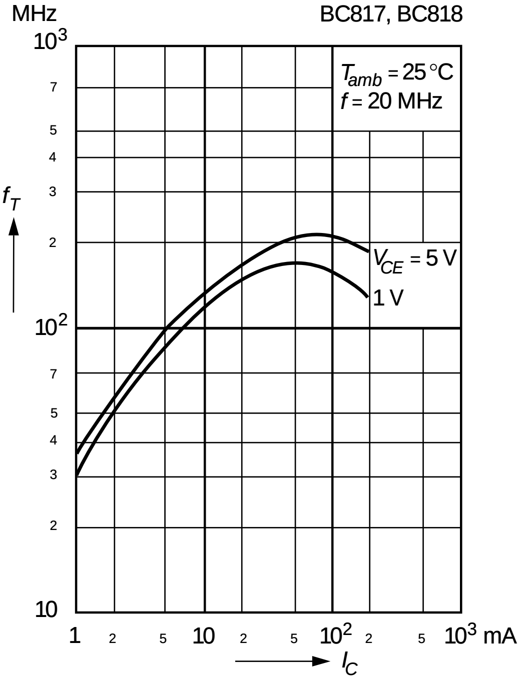


Pulse thermal resistance versus pulse duration (normalized)

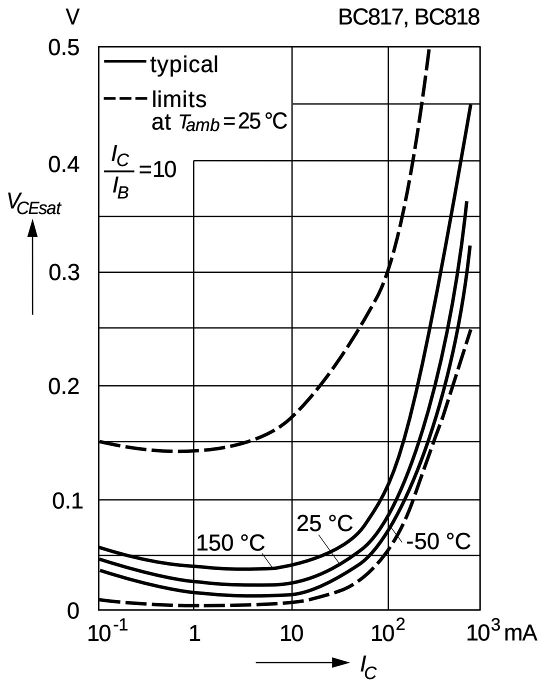
Device on fiberglass substrate, see layout



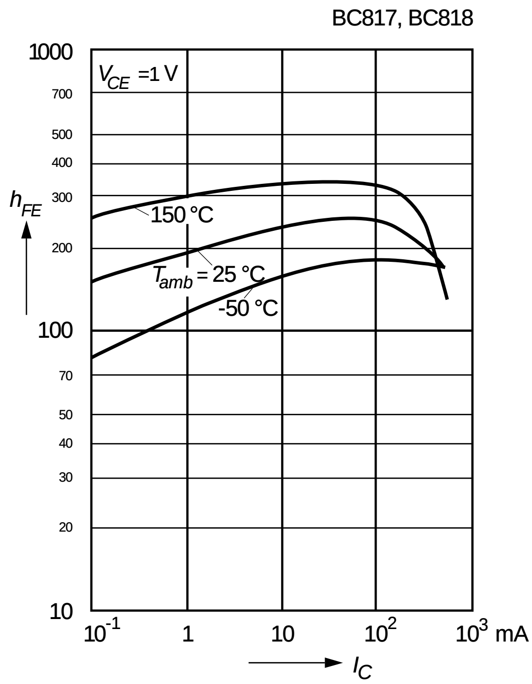
Gain-bandwidth product versus collector current



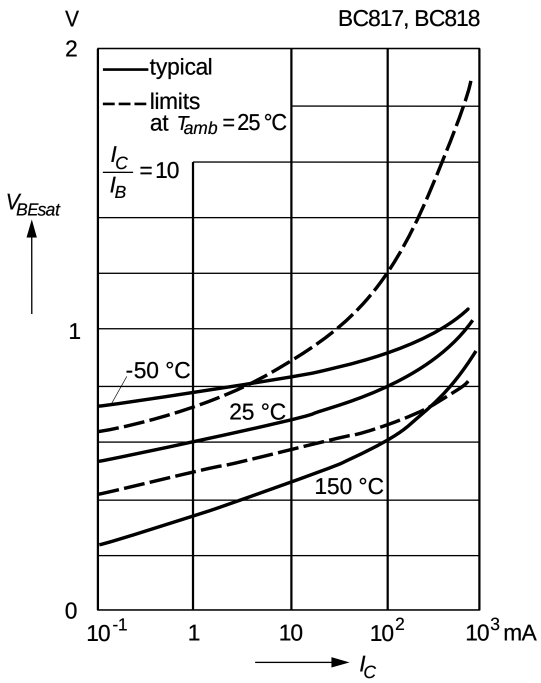
Collector saturation voltage versus collector current



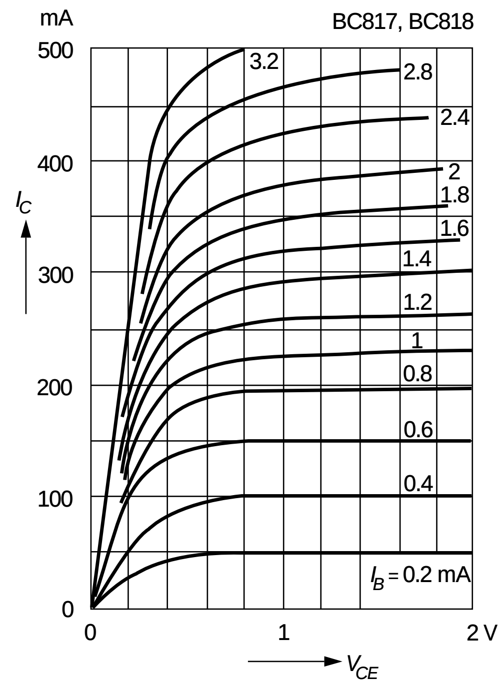
DC current gain versus collector current

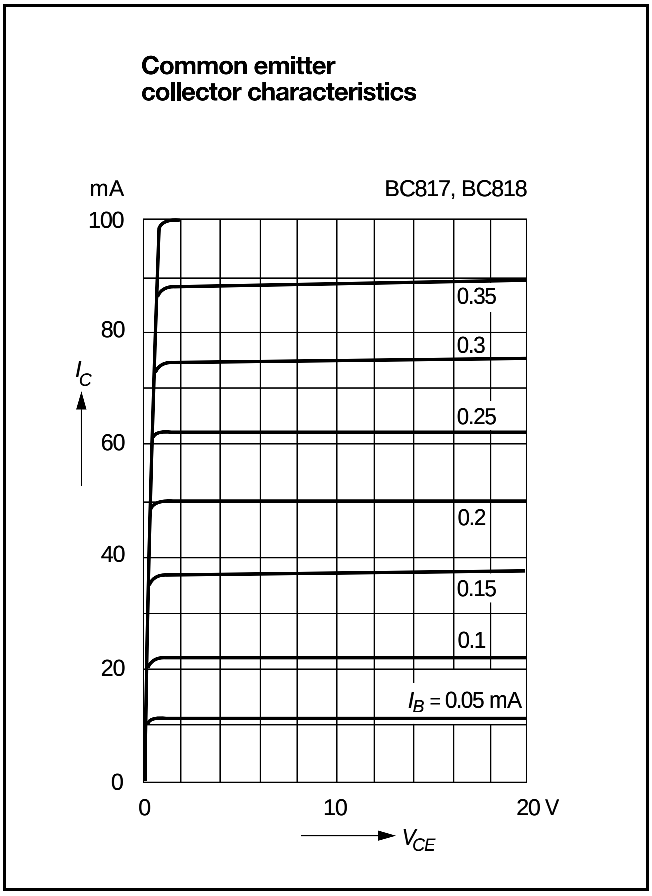


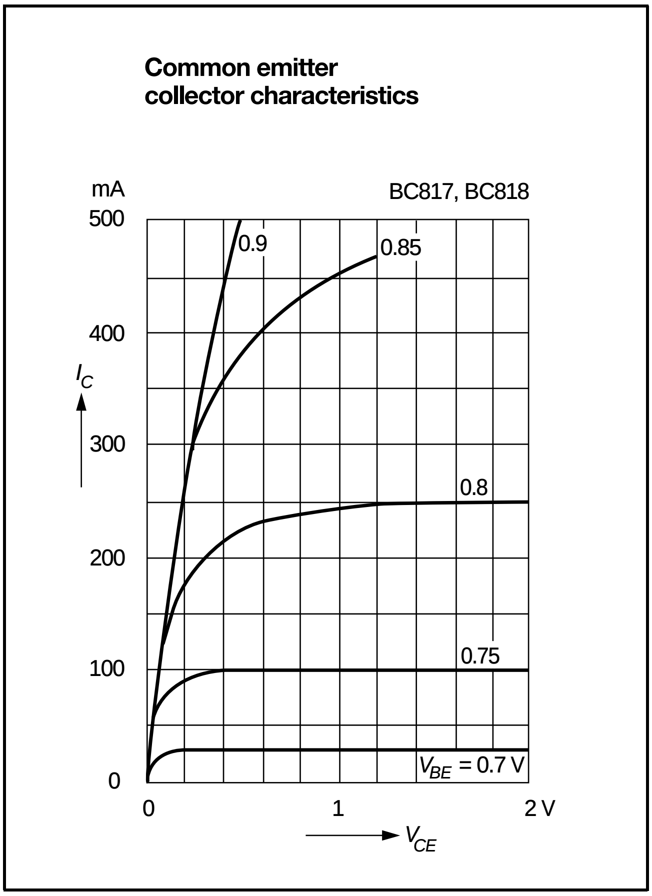
Base saturation voltage versus collector current



Common emitter collector characteristics



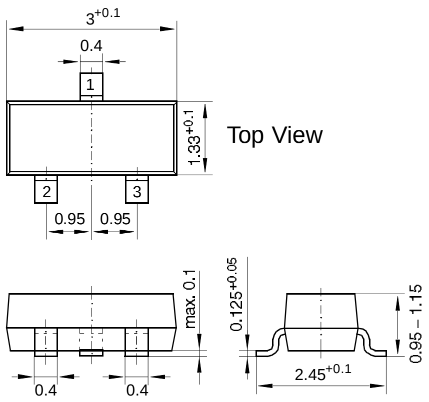

Common emitter
collector characteristics
mA
BC817, BC818
100
80
60
40
20
0
I_C
0.35
0.3
0.25
0.2
0.15
0.1
I_B = 0.05 mA
0
10
20 V
V_{CE}


Common emitter
collector characteristics
mA
BC817, BC818
500
400
300
200
100
0
I_C
0.9
0.85
0.8
0.75
V_{BE} = 0.7 V
0
1
2 V
V_{CE}

NPN Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors are subdivided into three groups A, B and C according to their current gain. The type BC846 is available in groups A and B, however, the types BC847 and BC848 can be supplied in all three groups. The BC849 is a low noise type available in groups B and C. As complementary types, the PNP transistors BC856…BC859 are recommended.



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Pin configuration
1 = Collector, 2 = Base, 3 = Emitter.

Marking code

Type	Marking	Type	Marking
BC846A	1A	BC848A	1J
B	1B	B	1K
BC847A	1E	C	1L
B	1F	BC849B	2B
C	1G	C	2C

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Base Voltage	**BC846**	V_{CBO}	80	V
	BC847	V_{CBO}	50	V
	BC848, BC849	V_{CBO}	30	V
Collector-Emitter Voltage	**BC846**	V_{CES}	80	V
	BC847	V_{CES}	50	V
	BC848, BC849	V_{CES}	30	V
Collector-Emitter Voltage	**BC846**	V_{CEO}	65	V
	BC847	V_{CEO}	45	V
	BC848, BC849	V_{CEO}	30	V
Emitter-Base Voltage	**BC846, BC847**	V_{EBO}	6	V
	BC848, BC849	V_{EBO}	5	V
Collector Current		I_C	100	mA
Peak Collector Current		I_{CM}	200	mA
Peak Base Current		I_{BM}	200	mA
Peak Emitter Current		$-I_{EM}$	200	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Device on fiberglass substrate, see layout

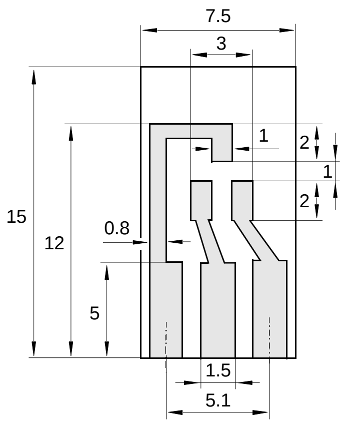
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
h-Parameters at V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz,					
Small-Signal Current Gain **Current Gain Group A**	h_{fe}	–	220	–	–
B	h_{fe}	–	330	–	–
C	h_{fe}	–	600	–	–
Input Impedance **Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
B	h_{ie}	3.2	4.5	8.5	kΩ
C	h_{ie}	6	8.7	15	kΩ
Output Admittance **Current Gain Group A**	h_{oe}	–	18	30	µS
B	h_{oe}	–	30	60	µS
C	h_{oe}	–	60	110	µS
Reverse Voltage Transfer Ratio **Current Gain Group A**	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain at V_{CE} = 5 V, I_C = 10 µA **Current Gain Group A**	h_{FE}	–	90	–	–
B	h_{FE}	–	150	–	–
C	h_{FE}	–	270	–	–
at V_{CE} = 5 V, I_C = 2 mA **Current Gain Group A**	h_{FE}	110	180	220	–
B	h_{FE}	200	290	450	–
C	h_{FE}	420	520	800	–
Thermal Resistance Junction to Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Collector Saturation Voltage at I_C = 10 mA, I_B = 0.5 mA	V_{CEsat}	–	90	250	mV
at I_C = 100 mA, I_B = 5 mA	V_{CEsat}	–	200	600	mV
Base Saturation Voltage at I_C = 10 mA, I_B = 0.5 mA	V_{BEsat}	–	700	–	mV
at I_C = 100 mA, I_B = 5 mA	V_{BEsat}	–	900	–	mV
Base-Emitter Voltage at V_{CE} = 5 V, I_C = 2 mA	V_{BE}	580	660	700	mV
at V_{CE} = 5 V, I_C = 10 mA	V_{BE}	–	–	720	mV
Collector-Emitter Cutoff Current at V_{CE} = 80 V **BC846**	I_{CES}	–	0.2	15	nA
at V_{CE} = 50 V **BC847**	I_{CES}	–	0.2	15	nA
at V_{CE} = 30 V **BC848, BC849**	I_{CES}	–	0.2	15	nA
at V_{CE} = 80 V, T_j = 125 °C **BC846**	I_{CES}	–	–	4	µA
at V_{CE} = 50 V, T_j = 125 °C **BC847**	I_{CES}	–	–	4	µA
at V_{CE} = 30 V, T_j = 125 °C **BC848, BC849**	I_{CES}	–	–	4	µA
Gain-Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz	f_T	–	300	–	MHz

[1)] Device on fiberglass substrate, see layout

Characteristics, continuation

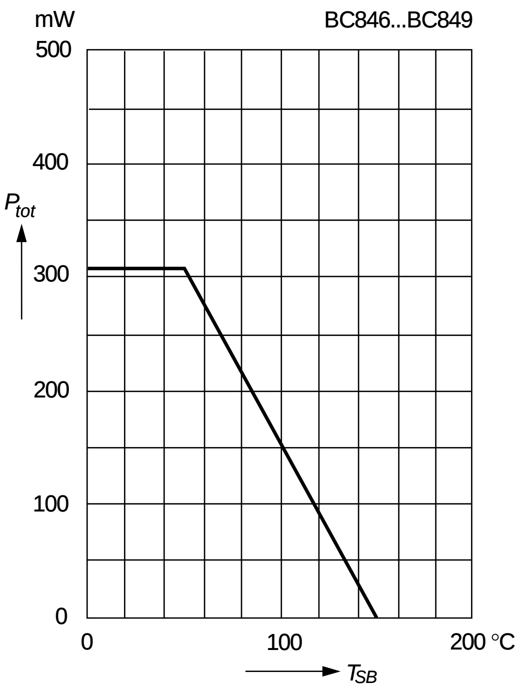
	Symbol	Min.	Typ.	Max.	Unit
Collector-Base Capacitance at V_{CB} = 10 V, f = 1 MHz	C_{CBO}	–	3.5	6	pF
Emitter-Base Capacitance at V_{EB} = 0.5 V, f = 1 MHz	C_{EBO}	–	9	–	pF
Noise Figure at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 1 kHz, Δf = 200 Hz **BC846, BC847, BC848** **BC849**	 F F	 – –	 2 1.2	 10 4	 dB dB
at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 30…15000 Hz **BC849**	F	–	1.4	4	dB



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

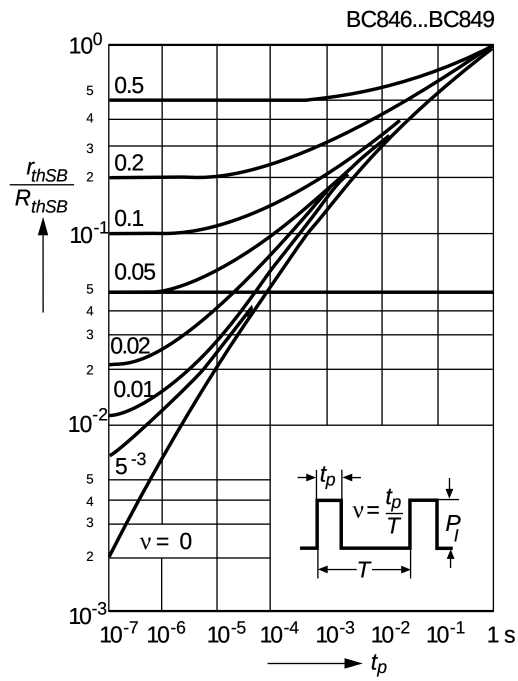
Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout

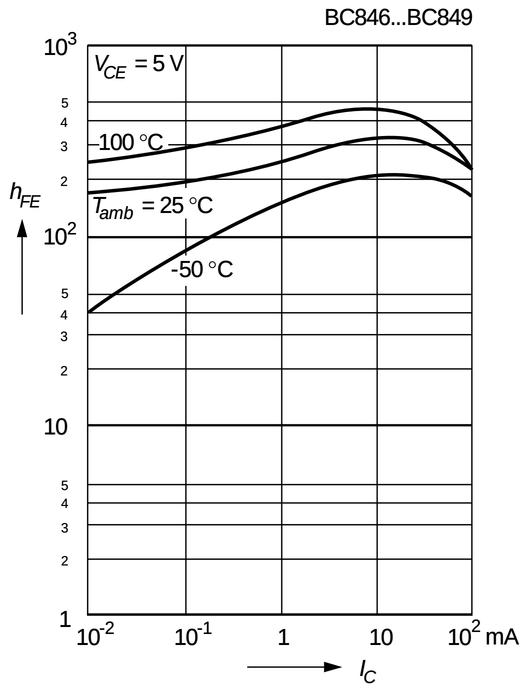


Pulse thermal resistance versus pulse duration (normalized)

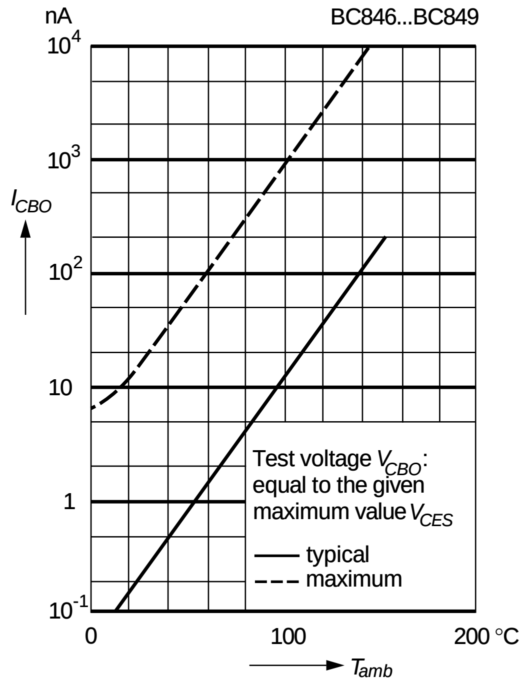
Device on fiberglass substrate, see layout



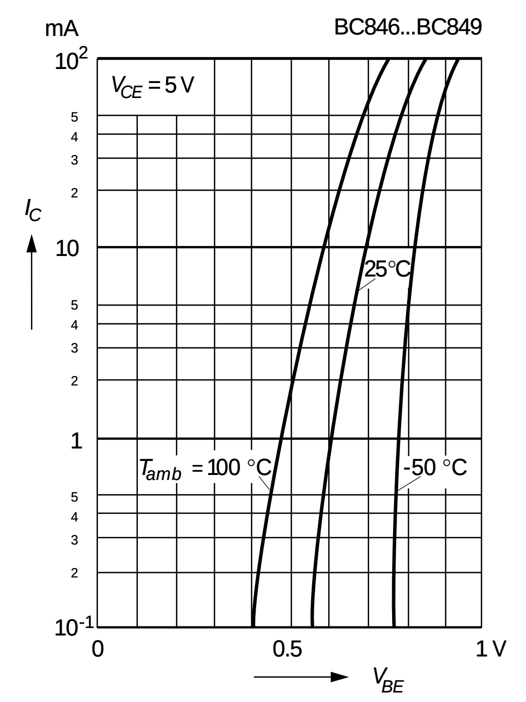
DC current gain versus collector current



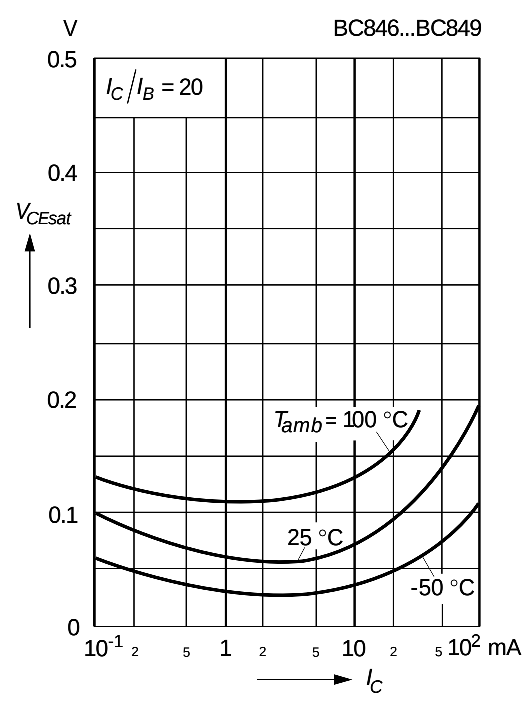
Collector-Base cutoff current versus ambient temperature



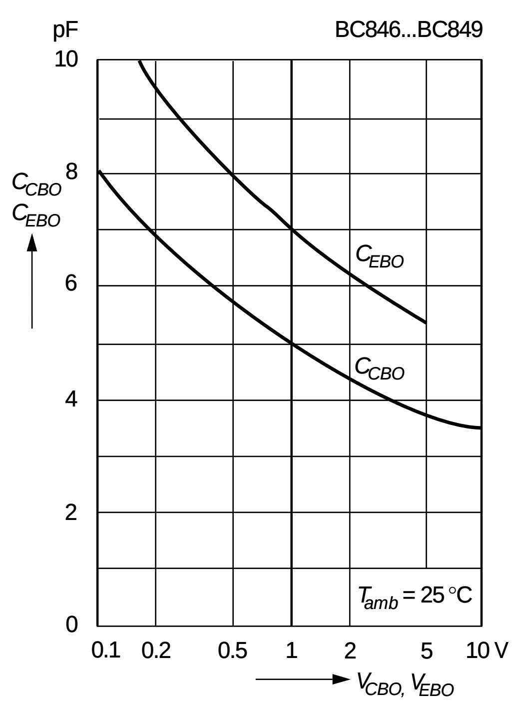
Collector current versus base-emitter voltage



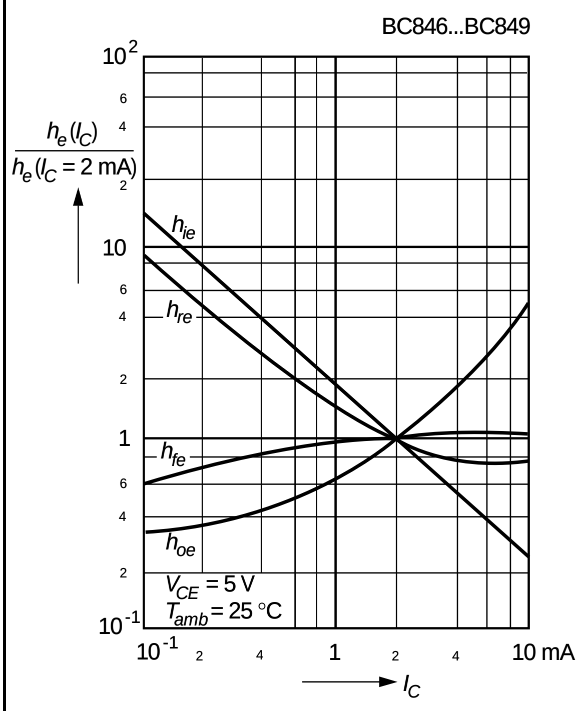
Collector saturation voltage versus collector current



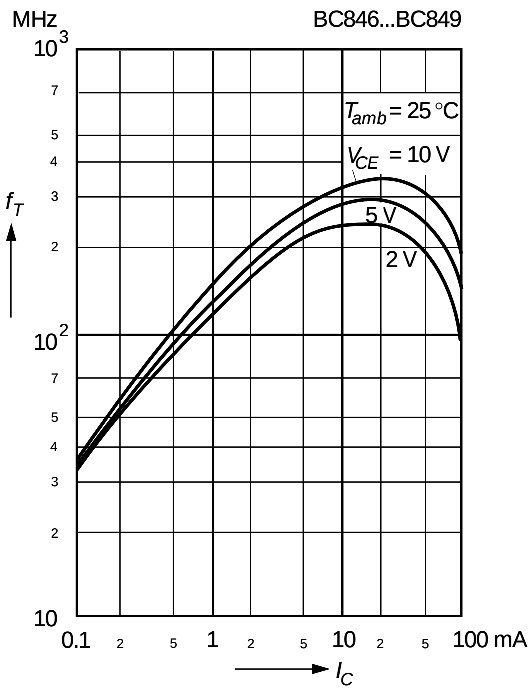
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



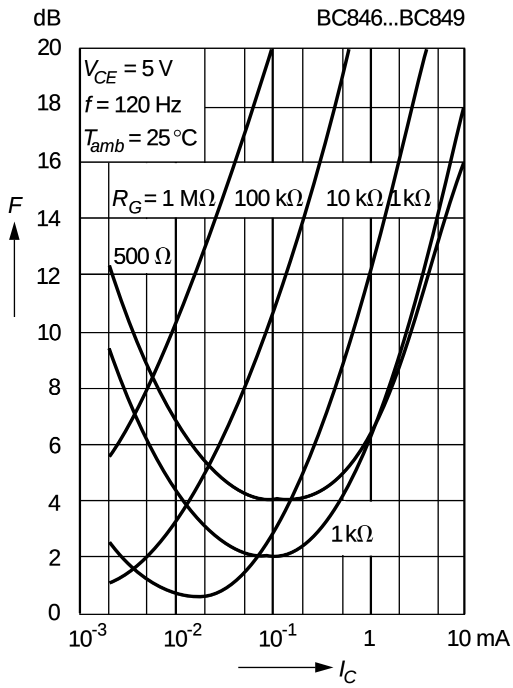
Relative h-parameters versus collector current



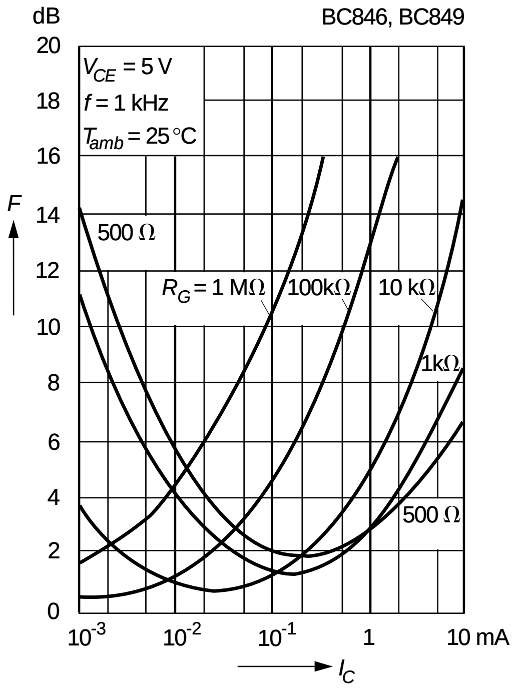
Gain-bandwidth product versus collector current



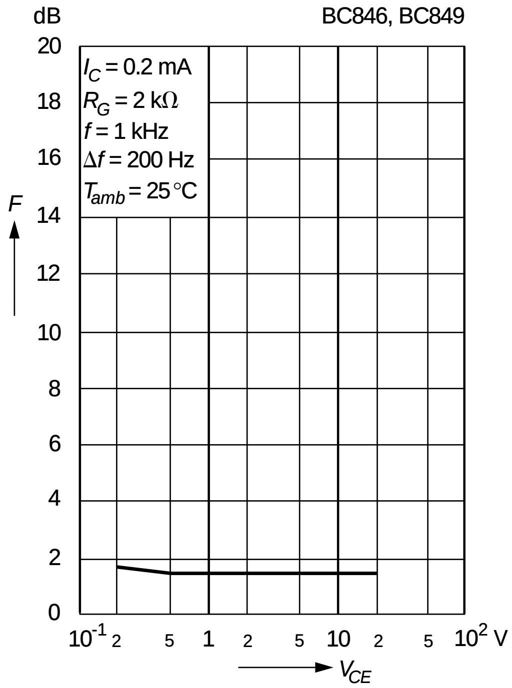
Noise figure versus collector current



Noise figure versus collector current

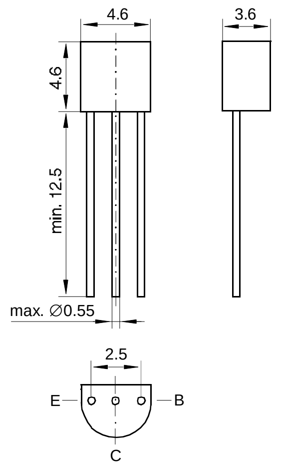


Noise figure versus collector emitter voltage



NPN Silicon Epitaxial Planar Transistors
especially suited for application in class-B video output stages of TV receivers and monitors.

As complementary types, the PNP transistors BF421 and BF423 are recommended



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Base Voltage	**BF420** **BF422**	V_{CBO} V_{CBO}	300 250	V V
Collector-Emitter Voltage	**BF422**	V_{CEO}	250	V
Collector-Emitter Voltage	**BF420**	V_{CER}	300	V
Emitter-Base Voltage		V_{EBO}	5	V
Collector Current		I_C	50	mA
Peak Collector Current		I_{CM}	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	830[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics at T_{amb} = 25 °C

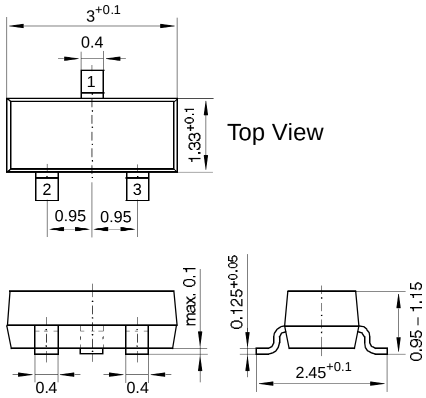
	Symbol	Min.	Typ.	Max.	Unit
Collector-Base Breakdown Voltage **BF420** at I_C = 100 µA, I_B = 0 **BF422**	$V_{(BR)CBO}$ $V_{(BR)CBO}$	300 250	– –	– –	V V
Collector-Emitter Breakdown Voltage **BF422** at I_C = 10 mA, I_E = 0	$V_{(BR)CEO}$	250	–	–	V
Collector-Emitter Breakdown Voltage **BF420** at R_{BE} = 2.7 kΩ, I_C = 10 mA	$V_{(BR)CER}$	300	–	–	V
Emitter-Base Breakdown Voltage at I_E = 100 µA, I_B = 0	$V_{(BR)EBO}$	5	–	–	V
Collector-Base Cutoff Current at V_{CB} = 200 V, I_E = 0	I_{CBO}	–	–	10	nA
Collector-Emitter Cutoff Current at R_{BE} = 2.7 kΩ, V_{CE} = 250 V at R_{BE} = 2.7 kΩ, V_{CE} = 200 V, T_j = 150 °C	 I_{CER} I_{CER}			 50 10	 nA µA
Collector Saturation Voltage at I_C = 30 mA, I_B = 5 mA	V_{CEsat}	–	–	0.6	V
DC Current Gain at V_{CE} = 20 V, I_C = 25 mA	h_{FE}	50	–	–	–
Gain-Bandwidth Product at V_{CE} = 10 V, I_C = 10 mA	f_T	60	–	–	MHz
Feedback Capacitance at V_{CE} = 30 V, I_C = 0, f = 1 MHz	C_{re}	–	–	1.6	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case					

NPN Silicon Epitaxial Planar Transistors
especially suited for application in class-B video output stages of TV receivers and monitors.

As complementary types, the PNP transistors BF821 and BF823 are recommended.

Pin configuration
1 = Collector, 2 = Base, 3 = Emitter.

Marking code
BF820 = 1V
BF822 = 1X



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

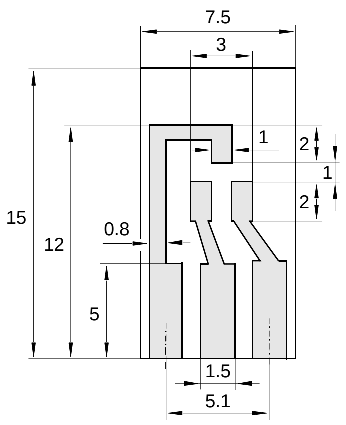
		Symbol	Value	Unit
Collector-Base Voltage	**BF820** **BF822**	V_{CBO} V_{CBO}	300 250	V V
Collector-Emitter Voltage	**BF822**	V_{CEO}	250	V
Collector-Emitter Voltage	**BF820**	V_{CER}	300	V
Emitter-Base Voltage		V_{EBO}	5	V
Collector Current		I_C	50	mA
Peak Collector Current		I_{CM}	100	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	300[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Device on fiberglass substrate, see layout

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Collector-Base Breakdown Voltage at I_C = 100 μA, I_B = 0 **BF820** / **BF822**	$V_{(BR)CBO}$ $V_{(BR)CBO}$	300 250	– –	– –	V V
Collector-Emitter Breakdown Voltage at I_C = 10 mA, I_E = 0 **BF822**	$V_{(BR)CEO}$	250	–	–	V
Collector-Emitter Breakdown Voltage at R_{BE} = 2.7 kΩ, I_C = 10 mA **BF820**	$V_{(BR)CER}$	300	–	–	V
Emitter-Base Breakdown Voltage at I_E = 100 μA, I_B = 0	$V_{(BR)EBO}$	5	–	–	V
Collector-Base Cutoff Current at V_{CB} = 200 V, I_E = 0	I_{CBO}	–	–	10	nA
Collector-Emitter Cutoff Current at R_{BE} = 2.7 kΩ, V_{CE} = 250 V at R_{BE} = 2.7 kΩ, V_{CE} = 200 V, T_j = 150 °C	 I_{CER} I_{CER}			 50 10	 nA μA
Collector Saturation Voltage at I_C = 30 mA, I_B = 5 mA	V_{CEsat}	–	–	0.6	V
DC Current Gain at V_{CE} = 20 V, I_C = 25 mA	h_{FE}	50	–	–	–
Gain-Bandwidth Product at V_{CE} = 10 V, I_C = 10 mA	f_T	60	–	–	MHz
Feedback Capacitance at V_{CE} = 30 V, I_C = 0, f = 1 MHz	C_{re}	–	–	1.6	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	430[1)]	K/W

[1)] Device on fiberglass substrate, see layout



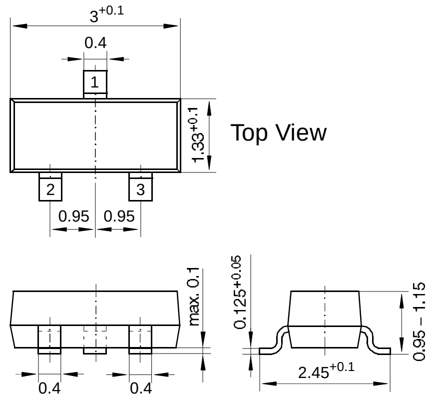
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

NPN Silicon Epitaxial Planar Transistor
for switching and amplifier applications.

As complementary type, the PNP transistor MMBT3906 is recommended.

Pin configuration
1 = Collector, 2 = Base, 3 = Emitter.

Marking code
1N



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	60	V
Collector-Emitter Voltage	V_{CEO}	40	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	100	mA
Peak Collector Current	I_{CM}	200	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	310[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C

1) Device on fiberglass substrate, see layout

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain					
at V_{CE} = 1 V, I_C = 0.1 mA	h_{FE}	40	–	–	–
at V_{CE} = 1 V, I_C = 1 mA	h_{FE}	70	–	–	–
at V_{CE} = 1 V, I_C = 10 mA	h_{FE}	100	–	300	–
at V_{CE} = 1 V, I_C = 50 mA	h_{FE}	60	–	–	–
at V_{CE} = 1 V, I_C = 100 mA	h_{FE}	30	–	–	–
Thermal Resistance Junction to Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Collector Saturation Voltage					
at I_C = 10 mA, I_B = 1 mA	V_{CEsat}	–	–	0.2	V
at I_C = 50 mA, I_B = 5 mA	V_{CEsat}	–	–	0.3	V
Base Saturation Voltage					
at I_C = 10 mA, I_B = 1 mA	V_{BEsat}	–	–	0.85	V
at I_C = 50 mA, I_B = 5 mA	V_{BEsat}	–	–	0.95	V
Collector-Emitter Cutoff Current V_{EB} = 3 V, V_{CE} = 30 V	I_{CEV}	–	–	50	nA
Emitter-Base Cutoff Current V_{EB} = 3 V, V_{CE} = 30 V	I_{EBV}	–	–	50	nA
Collector-Base Breakdown Voltage at I_C = 10 µA, I_E = 0	$V_{(BR)CBO}$	60	–	–	V
Collector-Emitter Breakdown Voltage at I_C = 1 mA, I_B = 0	$V_{(BR)CEO}$	40	–	–	V
Emitter-Base Breakdown Voltage at I_E = 10 µA, I_C = 0	$V_{(BR)EBO}$	6	–	–	V
Gain-Bandwidth Product at V_{CE} = 20 V, I_C = 10 mA, f = 100 MHz	f_T	300	–	–	MHz
Collector-Base Capacitance at V_{CB} = 5 V, f = 100 kHz	C_{CBO}	–	–	4	pF
Emitter-Base Capacitance at V_{EB} = 0.5 V, f = 100 kHz	C_{EBO}	–	–	8	pF
Input Impedance at V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	h_{ie}	1	–	10	kΩ

[1)] Device on fiberglass substrate, see layout

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Voltage Feedback Ratio at V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	h_{re}	$0.5 \cdot 10^{-4}$	–	$8 \cdot 10^{-4}$	–
Small-Signal Current Gain at V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	h_{fe}	100	–	400	–
Output Admittance at V_{CE} = 1 V, I_C = 1 mA, f = 1 kHz	h_{oe}	1	–	40	µS
Noise Figure at V_{CE} = 5 V, I_C = 100 µA, R_G = 1 kΩ, f = 10…15000 Hz	–	–	–	5	dB
Delay Time (see Fig. 1) at I_{B1} = 1 mA, I_C = 10 mA	t_d	–	–	35	ns
Rise Time (see Fig. 1) at I_{B1} = 1 mA, I_C = 10 mA	t_r	–	–	35	ns
Storage Time (see Fig. 2) at $-I_{B1}$ = I_{B2} = 1 mA, I_C = 10 mA	t_s	–	–	200	ns
Fall Time (see Fig. 2) at $-I_{B1}$ = I_{B2} = 1 mA, I_C = 10 mA	t_f	–	–	50	ns

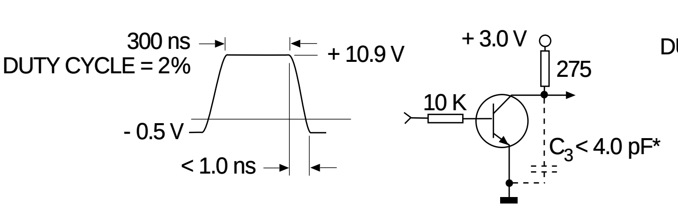


Fig. 1: Test circuit for delay and rise time

* total shunt capacitance of test jig and connectors

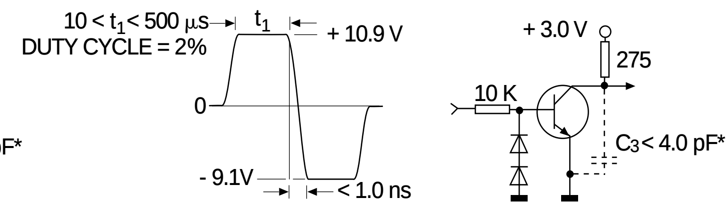
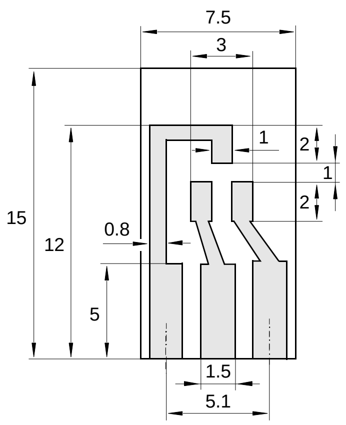


Fig. 2: Test circuit for storage and fall time

* total shunt capacitance of test jig and connectors



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

NPN Silicon Epitaxial Planar Transistors
especially suited as line switch in telephone subsets and in video output stages of TV receivers and monitors.

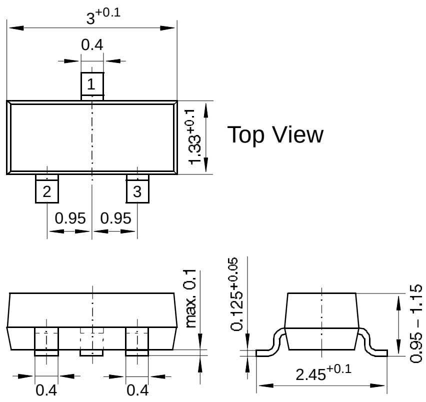
As complementary types, the PNP transistors MMBTA92 and MMBTA93 are recommended.

Pin Configuration

1 = Collector, 2 = Base, 3 = Emitter

Marking Code

MMBTA42 = 1D
MMBTA43 = 1E



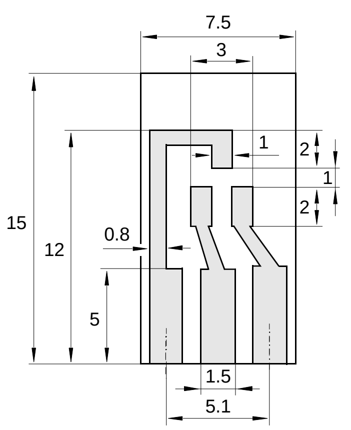
SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Emitter Voltage	**MMBTA42** **MMBTA43**	V_{CEO} V_{CEO}	300 200	V V
Collector-Base Voltage	**MMBTA42** **MMBTA43**	V_{CBO} V_{CBO}	300 200	V V
Emitter-Base Voltage		V_{EBO}	6	V
Collector Current		I_C	500	mA
Power Dissipation[1)] at T_{SB} = 50 °C		P_{tot}	300[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C
[1)] Device on fiberglass substrate, see layout				

Characteristics at T_{amb} = 25 °C

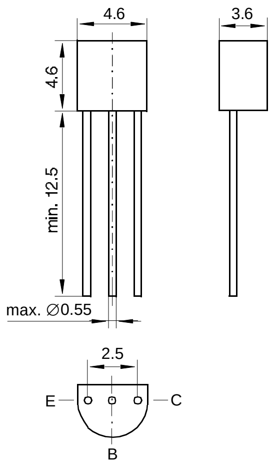
	Symbol	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage **MMBTA42** I_C = 10 mA, I_B = 0 **MMBTA43**	$V_{(BR)CEO}$ $V_{(BR)CEO}$	300 200	– –	– –	V V
Collector-Base Breakdown Voltage **MMBTA42** I_C = 100 µA, I_E = 0 **MMBTA43**	$V_{(BR)CBO}$ $V_{(BR)CBO}$	300 200	– –	– –	V V
Emitter-Base Breakdown Voltage I_E = 100 µA, I_C = 0	$V_{(BR)EBO}$	6	–	–	V
Collector-Base Cutoff Current V_{CB} = 200 V, I_E = 0 **MMBTA42** V_{CB} = 160 V, I_E = 0 **MMBTA43**	I_{CBO} I_{CBO}	– –	– –	100 100	nA nA
Emitter-Base Cutoff Current V_{EB} = 6 V, I_C = 0 **MMBTA42** V_{EB} = 4 V, I_C = 0 **MMBTA43**	I_{EBO} I_{EBO}	– –	– –	100 100	nA nA
DC Current Gain I_C = 1 mA, V_{CE} = 10 V I_C = 10 mA, V_{CE} = 10 V I_C = 30 mA, V_{CE} = 10 V	h_{FE} h_{FE} h_{FE}	25 40 40	– – –	– – –	– – –
Collector-Emitter Saturation Voltage I_C = 20 mA, I_B = 2 mA	V_{CEsat}	–	–	500	mV
Base-Emitter Saturation Voltage I_C = 20 mA, I_B = 2 mA	V_{BEsat}	–	–	900	mV
Gain-Bandwidth Product I_E = 10 mA, V_{CE} = 20 V, f = 100 MHz	f_T	50	–	–	MHz
Collector-Base Capacitance **MMBTA42** V_{CB} = 20 V, I_E = 0, f = 1 MHz **MMBTA43**	C_{CBO} C_{CBO}	– –	– –	3 4	pF pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	430[1)]	K/W
[1)] Device on fiberglass substrate, see layout					



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

NPN Silicon Epitaxial Planar Transistors
especially suited as line switch in telephone subsets and in video output stages of TV receivers and monitors.

As complementary types, the PNP transistors MPSA92 and MPSA93 are recommended.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Emitter Voltage	**MPSA42** **MPSA43**	V_{CEO} V_{CEO}	300 200	V V
Collector-Base Voltage	**MPSA42** **MPSA43**	V_{CBO} V_{CBO}	300 200	V V
Emitter-Base Voltage		V_{EBO}	6	V
Collector Current		I_C	500	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage I_C = 10 mA, I_B = 0	**MPSA42** **MPSA43**	$V_{(BR)CEO}$ $V_{(BR)CEO}$	300 200	– –	– –	V V
Collector-Base Breakdown Voltage I_C = 100 µA, I_E = 0	**MPSA42** **MPSA43**	$V_{(BR)CBO}$ $V_{(BR)CBO}$	300 200	– –	– –	V V
Emitter-Base Breakdown Voltage I_E = 100 µA, I_C = 0		$V_{(BR)EBO}$	6	–	–	V
Collector-Base Cutoff Current V_{CB} = 200 V, I_E = 0 V_{CB} = 160 V, I_E = 0	 **MPSA42** **MPSA43**	 I_{CBO} I_{CBO}	 – –	 – –	 100 100	 nA nA
Emitter-Base Cutoff Current V_{EB} = 6 V, I_C = 0 V_{EB} = 4 V, I_C = 0	 **MPSA42** **MPSA43**	 I_{EBO} I_{EBO}	 – –	 – –	 100 100	 nA nA
DC Current Gain I_C = 1 mA, V_{CE} = 10 V I_C = 10 mA, V_{CE} = 10 V I_C = 30 mA, V_{CE} = 10 V		 h_{FE} h_{FE} h_{FE}	 25 40 40	 – – –	 – – –	 – – –
Collector-Emitter Saturation Voltage I_C = 20 mA, I_B = 2 mA		V_{CEsat}	–	–	500	mV
Base-Emitter Saturation Voltage I_C = 20 mA, I_B = 2 mA		V_{BEsat}	–	–	900	mV
Gain-Bandwidth Product I_E = 10 mA, V_{CE} = 20 V, f = 100 MHz		f_T	50	–	–	MHz
Collector-Base Capacitance V_{CB} = 20 V, I_E = 0, f = 1 MHz	**MPSA42** **MPSA43**	C_{CBO} C_{CBO}	– –	– –	3 4	pF pF
Thermal Resistance Junction to Ambient Air		R_{thA}	–	–	200[1)]	K/W

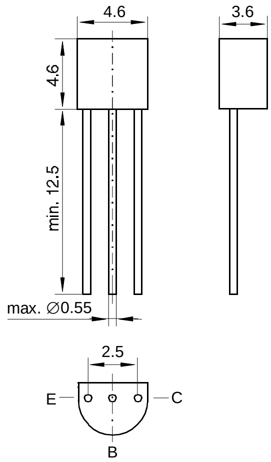
[1)] Valid provided that lead are kept at ambient temperature at a distance of 2 mm from case.

Small-Signal Transistors (PNP)

PNP Silicon Epitaxial Planar Transistor
for switching and amplifier applications.

As complementary type, the NPN transistor 2N3904 is recommended.

On special request, this transistor is also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector-Base Voltage	$-V_{CBO}$	40	V
Collector-Emitter Voltage	$-V_{CEO}$	40	V
Emitter-Base Voltage	$-V_{EBO}$	5	V
Collector Current	$-I_C$	100	mA
Peak Collector Current	$-I_{CM}$	200	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	500[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C

1) Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $-V_{CE}$ = 1 V, $-I_C$ = 0.1 mA at $-V_{CE}$ = 1 V, $-I_C$ = 1 mA at $-V_{CE}$ = 1 V, $-I_C$ = 10 mA at $-V_{CE}$ = 1 V, $-I_C$ = 50 mA at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA	 h_{FE} h_{FE} h_{FE} h_{FE} h_{FE}	 60 80 100 60 30	 – – – – –	 – – 300 – –	 – – – – –
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	250[1)]	K/W
Collector Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 1 mA at $-I_C$ = 50 mA, $-I_B$ = 5 mA	 $-V_{CEsat}$ $-V_{CEsat}$	 – –	 – –	 0.25 0.4	 V V
Base Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 1 mA at $-I_C$ = 50 mA, $-I_B$ = 5 mA	 $-V_{BEsat}$ $-V_{BEsat}$	 – –	 – –	 0.85 0.95	 V V
Collector-Emitter Cutoff Current at $-V_{EB}$ = 3 V, $-V_{CE}$ = 30 V	$-I_{CEV}$	–	–	50	nA
Emitter-Base Cutoff Current at $-V_{EB}$ = 3 V, $-V_{CE}$ = 30 V	$-I_{EBV}$	–	–	50	nA
Collector-Base Breakdown Voltage at $-I_C$ = 10 µA, I_E = 0	$-V_{(BR)CBO}$	40	–	–	V
Collector-Emitter Breakdown Voltage at $-I_C$ = 1 mA, I_B = 0	$-V_{(BR)CEO}$	40	–	–	V
Emitter-Base Breakdown Voltage at $-I_E$ = 10 µA, I_C = 0	$-V_{(BR)EBO}$	5	–	–	V
Gain-Bandwidth Product at $-V_{CE}$ = 20 V, $-I_C$ = 10 mA, f = 100 MHz	f_T	250	–	–	MHz
Collector-Base Capacitance at $-V_{CB}$ = 5 V, f = 100 kHz	C_{CBO}	–	–	4.5	pF
Emitter-Base Capacitance at $-V_{EB}$ = 0.5 V, f = 100 kHz	C_{EBO}	–	–	10	pF
Input Impedance at $-V_{CE}$ = 10 V, $-I_C$ = 1 mA, f = 1 kHz	h_{ie}	1	–	10	kΩ
Voltage Feedback Ratio at $-V_{CE}$ = 10 V, $-I_C$ = 1 mA, f = 1 kHz	h_{re}	$0.5 \cdot 10^{-4}$	–	$8 \cdot 10^{-4}$	–

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Small-Signal Current Gain at $-V_{CE}$ = 10 V, $-I_C$ = 1 mA, f = 1 kHz	h_{fe}	100	–	400	–
Output Admittance at $-V_{CE}$ = 1 V, $-I_C$ = 1 mA, f = 1 kHz	h_{oe}	1	–	40	µS
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 100 µA, R_G = 1 kΩ, f = 10 … 15000 Hz	F	–	–	4	dB
Delay Time (see Fig. 1) at $-I_{B1}$ = 1 mA, $-I_C$ = 10 mA	t_d	–	–	35	ns
Rise Time (see Fig. 1) at $-I_{B1}$ = 1 mA, $-I_C$ = 10 mA	t_r	–	–	35	ns
Storage Time (see Fig. 2) at $I_{B1} = -I_{B2}$ = 1 mA, $-I_C$ = 10 mA	t_s	–	–	225	ns
Fall Time (see Fig. 2) at $I_{B1} = -I_{B2}$ = 1 mA, $-I_C$ = 10 mA	t_f	–	–	75	ns

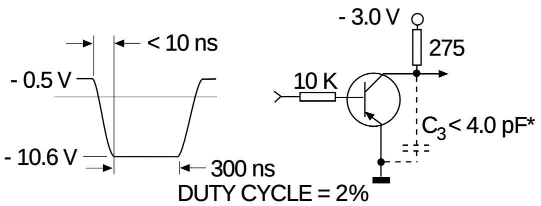


Fig. 1: Test circuit for delay and rise time

* total shunt capacitance of test jig and connectors

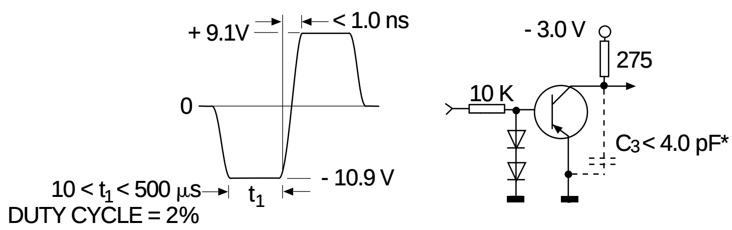
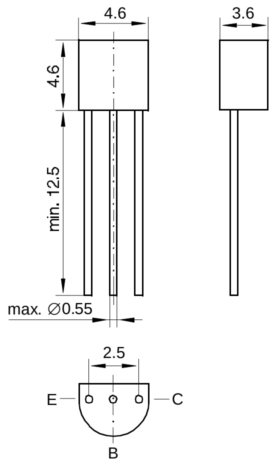


Fig. 2: Test circuit for storage and fall time

* total shunt capacitance of test jig and connectors

PNP Silicon Epitaxial Transistor
for switching and amplifier applications. Especially suitable for AF-driver and low-power output stages.

As complementary type, the NPN transistor 2N4124 is recommended.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector-Emitter Voltage	$-V_{CEO}$	25	V
Collector-Base Voltage	$-V_{CBO}$	25	V
Emitter-Base Voltage	$-V_{EBO}$	4	V
Collector Current	$-I_C$	200	mA
Peak Collector Current	$-I_{CM}$	800	mA
Base Current	$-I_B$	50	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	625[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

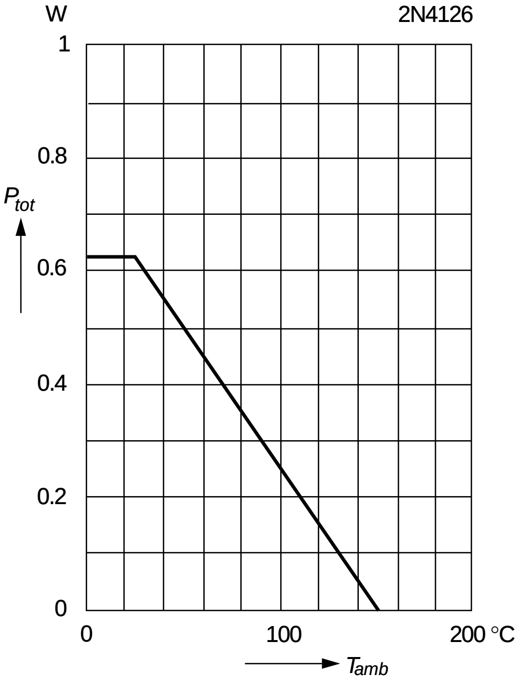
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = –1 V, I_C = –2.0 mA at V_{CE} = –1 V, I_C = –50 mA	 h_{FE} h_{FE}	 120 –	 – 60	 360 –	 – –
Collector Cutoff Current at V_{CB} = –20 V	$-I_{CBO}$	–	–	50	nA
Emitter Cutoff Current at V_{EB} = –3 V	$-I_{EBO}$	–	–	50	nA
Collector Saturation Voltage at I_C = –50 mA, I_B = –5 mA	$-V_{CESAT}$	–	–	0.4	V
Base Saturation Voltage at I_C = –50 mA, I_B = –5 mA	$-V_{BESAT}$	–	–	0.95	V
Collector-Emitter Breakdown Voltage at I_C = –1 mA	$-V_{(BR)CEO}$	25	–	–	V
Collector-Base Breakdown Voltage at I_C = –10 µA	$-V_{(BR)CBO}$	25	–	–	V
Emitter-Base Breakdown Voltage at I_E = –10 µA	$-V_{(BR)EBO}$	4	–	–	V
Gain-Bandwidth Product at V_{CE} = –5 V, I_C = –10 mA, f = 50 MHz	f_T	–	200	–	MHz
Collector-Base Capacitance at V_{CB} = –10 V, f = 1 MHz	C_{CBO}	–	12	–	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	200[1)]	K/W

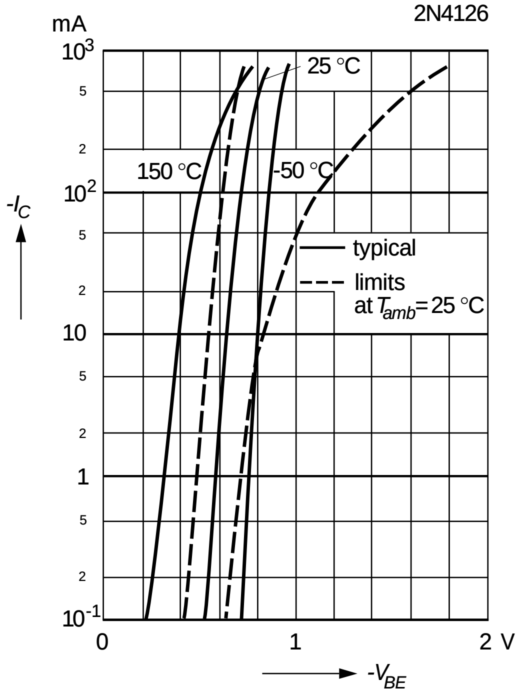
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

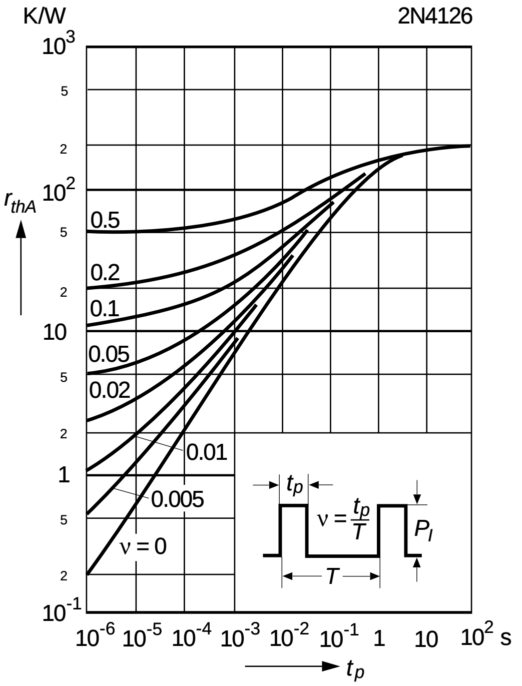


Collector current versus base-emitter voltage

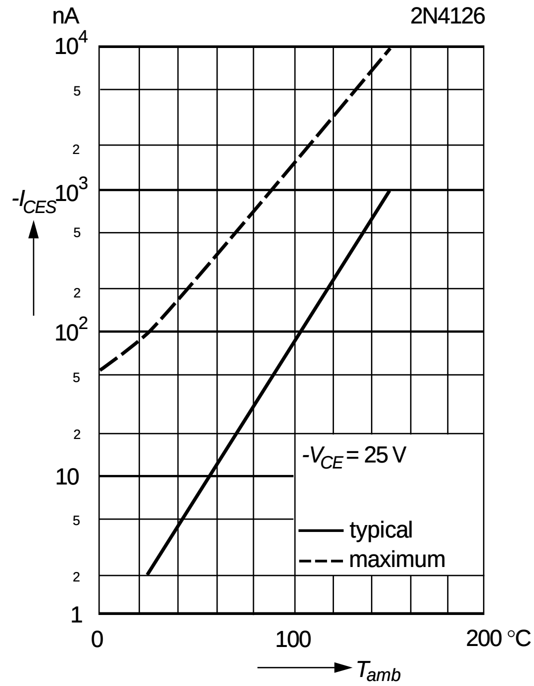


Pulse thermal resistance versus pulse duration

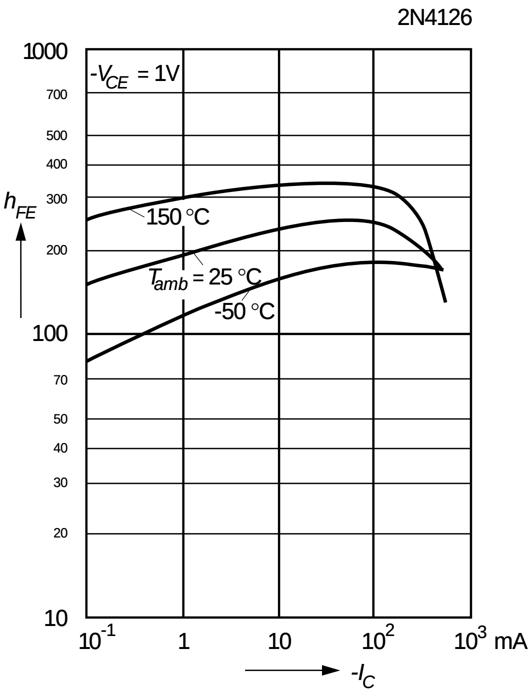
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



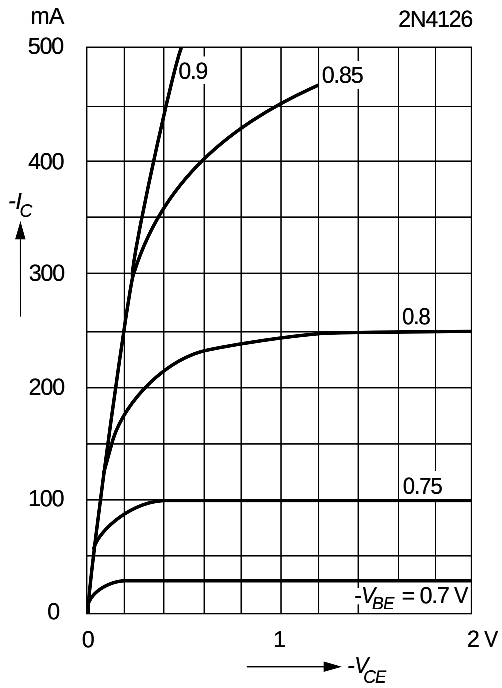
Collector-emitter cutoff current versus ambient temperature



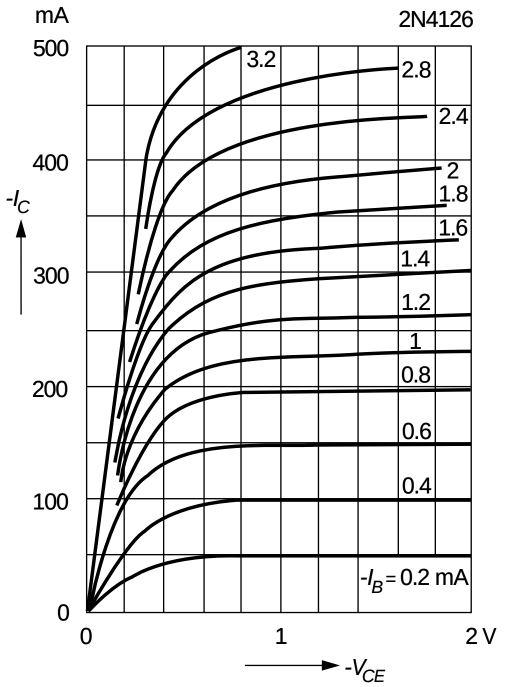
DC current gain versus collector current



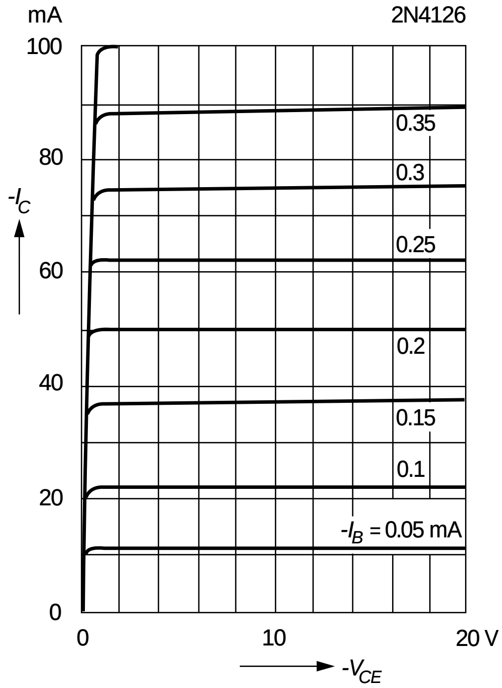
Common emitter collector characteristics



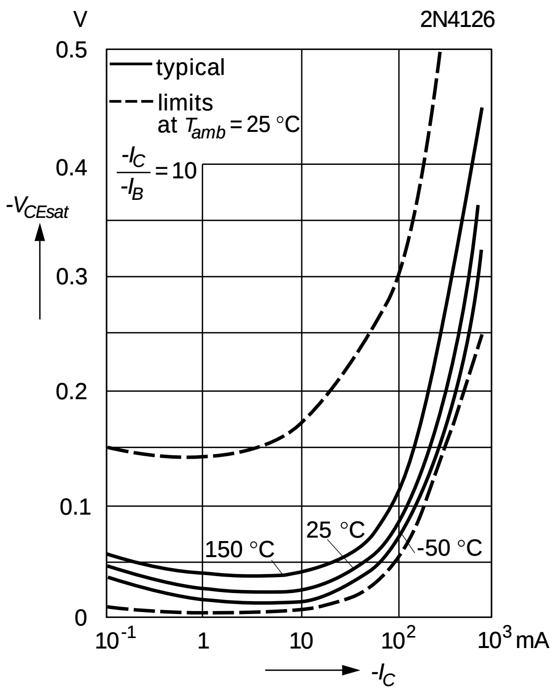
Common emitter collector characteristics



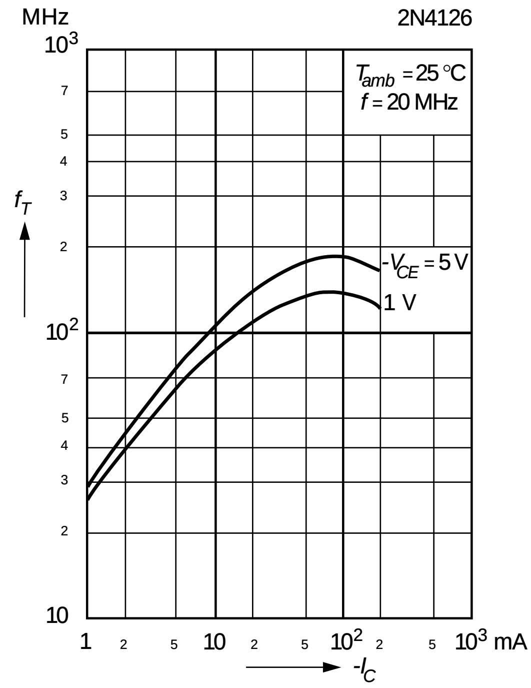
Common emitter collector characteristics



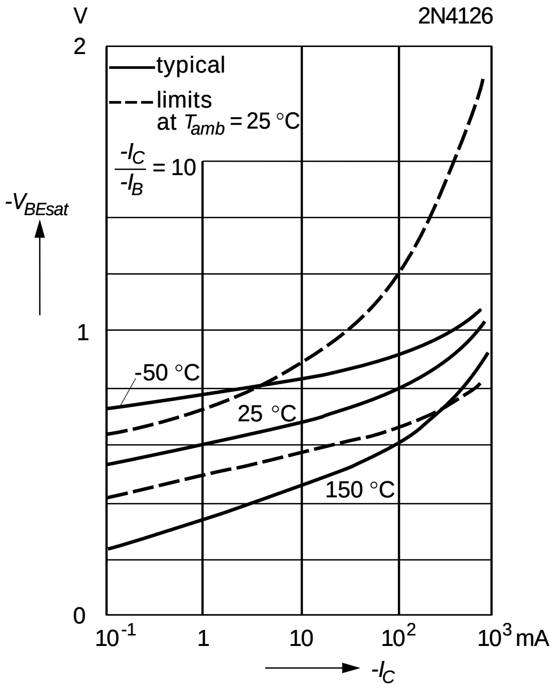
Collector saturation voltage versus collector current



Gain-bandwidth product versus collector current



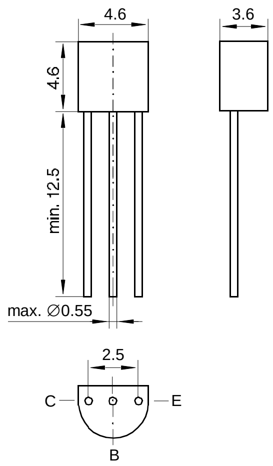
Base saturation voltage versus collector current



PNP Silicon Epitaxial Planar Transistors
for switching and amplifier applications. Especially suitable for AF-driver stages and low-power output stages.

These types are also available subdivided into three groups -16, -25, and -40, according to their DC current gain. As complementary types, the NPN transistors BC337 and BC338 are recommended.

On special request, these transistors are also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Emitter Voltage	**BC327** **BC328**	$-V_{CES}$ $-V_{CES}$	50 30	V V
Collector-Emitter Voltage	**BC327** **BC328**	$-V_{CEO}$ $-V_{CEO}$	45 25	V V
Emitter-Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	800	mA
Peak Collector Current		$-I_{CM}$	1	A
Base Current		$-I_B$	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

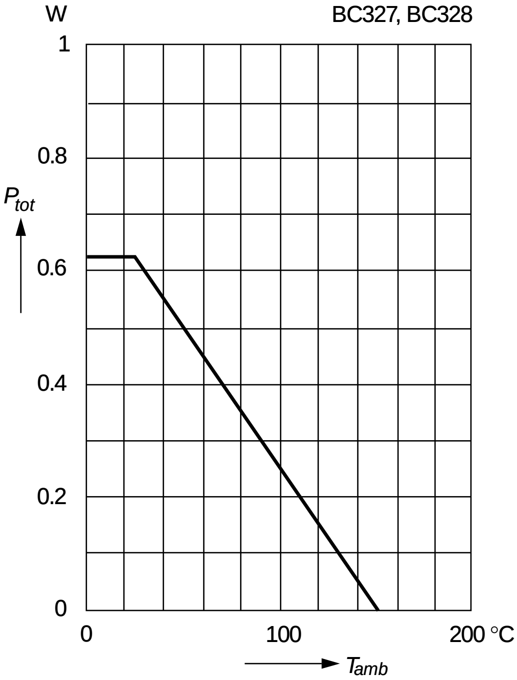
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA					
Current Gain Group-16	h_{FE}	100	160	250	–
-25	h_{FE}	160	250	400	–
-40	h_{FE}	250	400	630	–
at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA					
Current Gain Group-16	h_{FE}	60	130	–	–
-25	h_{FE}	100	200	–	–
-40	h_{FE}	170	320	–	–
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	200[1)]	K/W
Collector-Emitter Cutoff Current					
at $-V_{CE}$ = 45 V **BC327**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 25 V **BC328**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 45 V, T_{amb} = 125 °C **BC327**	$-I_{CES}$	–	–	10	µA
at $-V_{CE}$ = 25 V, T_{amb} = 125 °C **BC328**	$-I_{CES}$	–	–	10	µA
Collector-Emitter Breakdown Voltage					
at $-I_C$ = 10 mA **BC327**	$-V_{(BR)CEO}$	45	–	–	V
BC328	$-V_{(BR)CEO}$	25	–	–	V
Collector-Emitter Breakdown Voltage					
at $-I_C$ = 0.1 mA **BC327**	$-V_{(BR)CES}$	50	–	–	V
BC328	$-V_{(BR)CES}$	30	–	–	V
Emitter-Base Breakdown Voltage at $-I_E$ = 0.1 mA	$-V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at $-I_C$ = 500 mA, $-I_B$ = 50 mA	$-V_{CEsat}$	–	–	0.7	V
Base-Emitter Voltage at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA	$-V_{BE}$	–	–	1.2	V
Gain-Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector-Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF

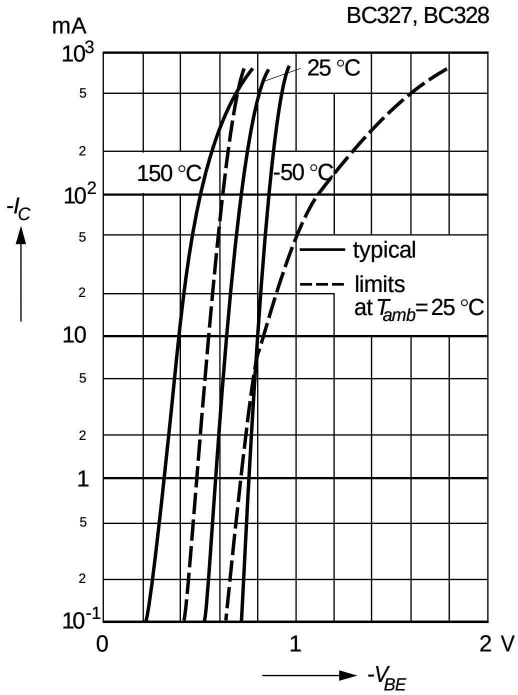
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

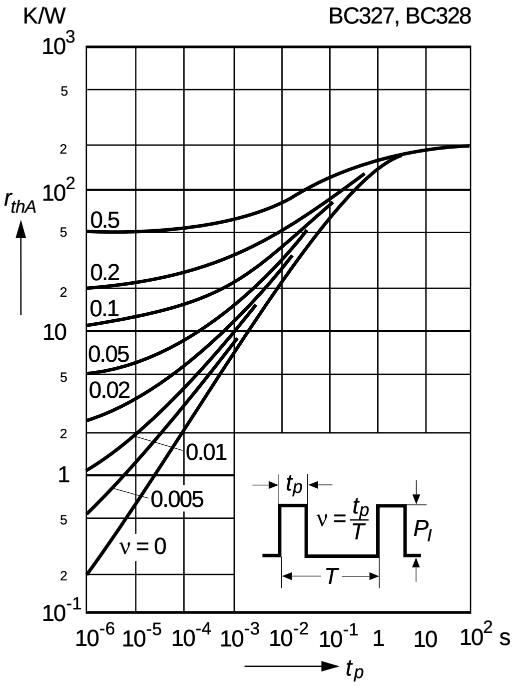


Collector current versus base-emitter voltage

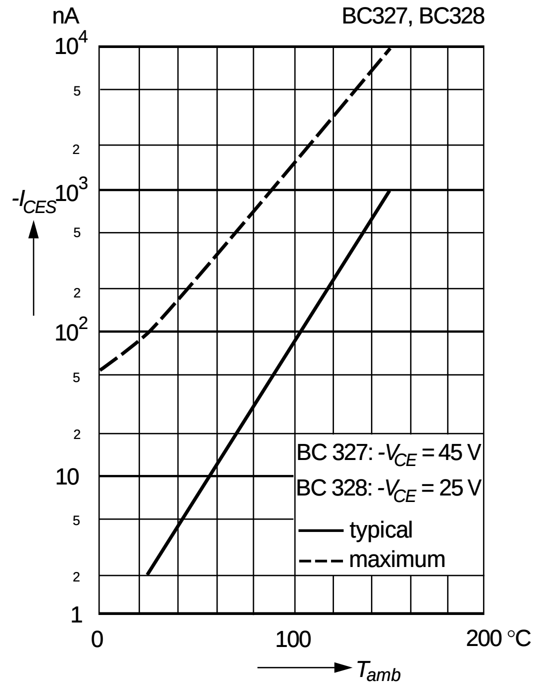


Pulse thermal resistance versus pulse duration

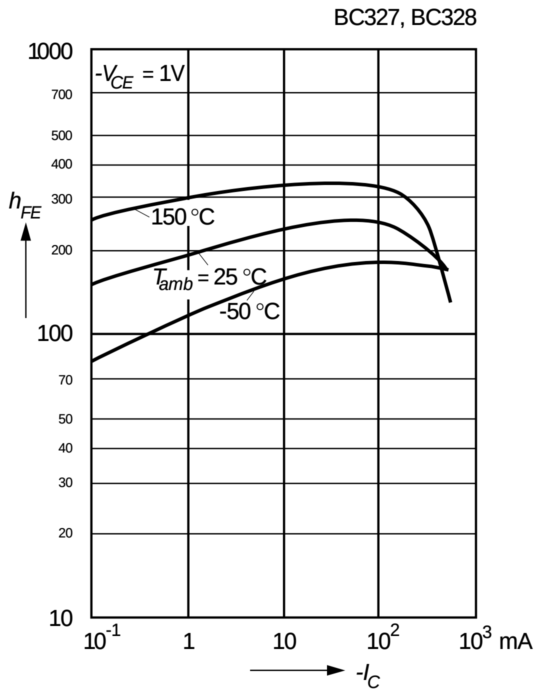
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



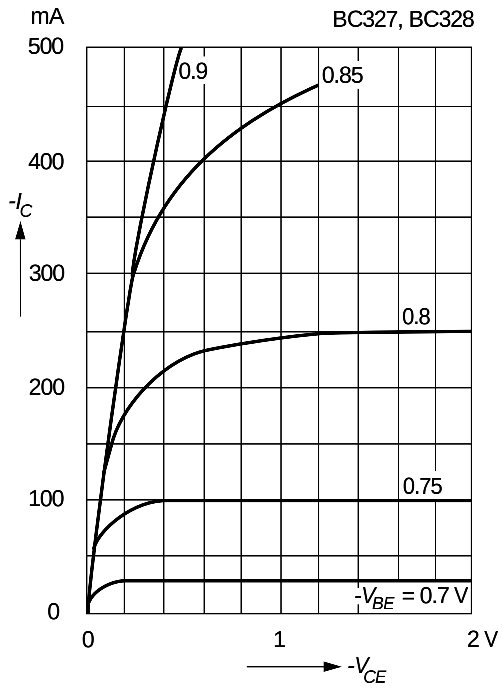
Collector-emitter cutoff current versus ambient temperature



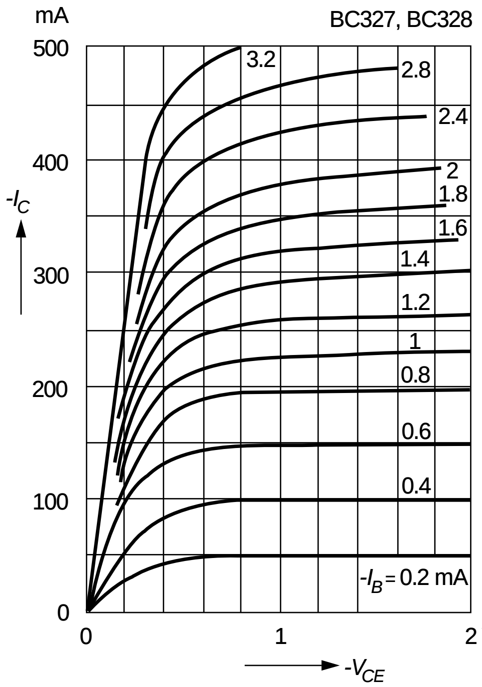
DC current gain versus collector current



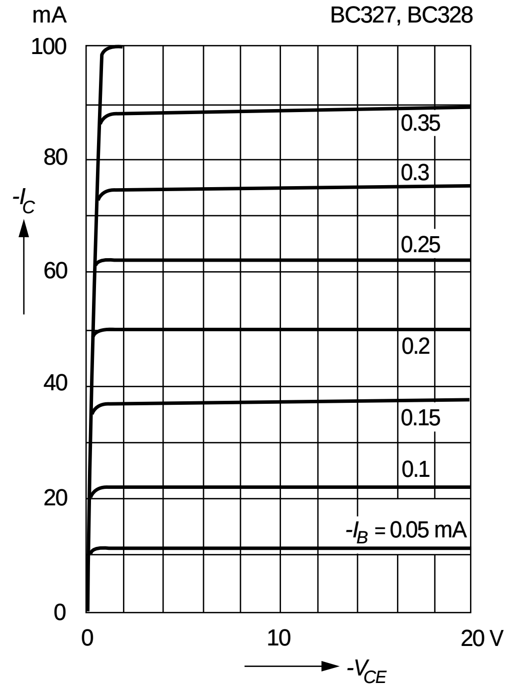
Common emitter collector characteristics



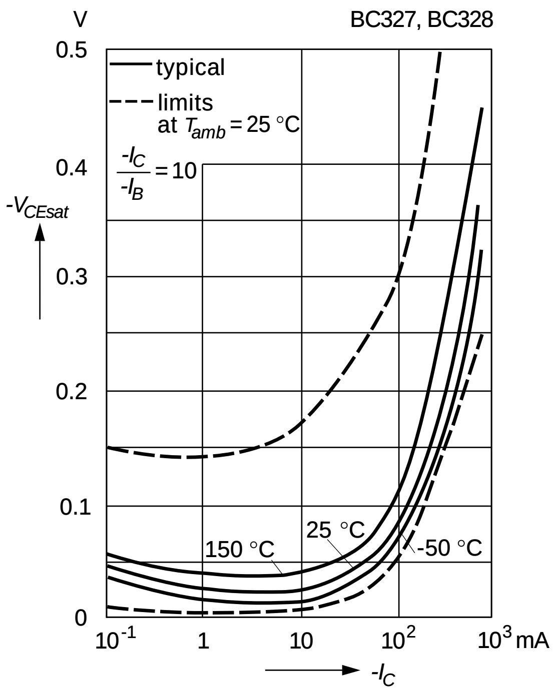
Common emitter collector characteristics



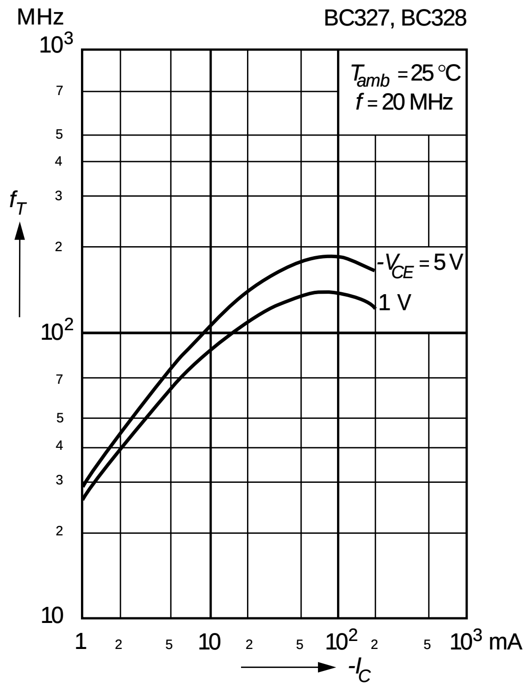
Common emitter collector characteristics



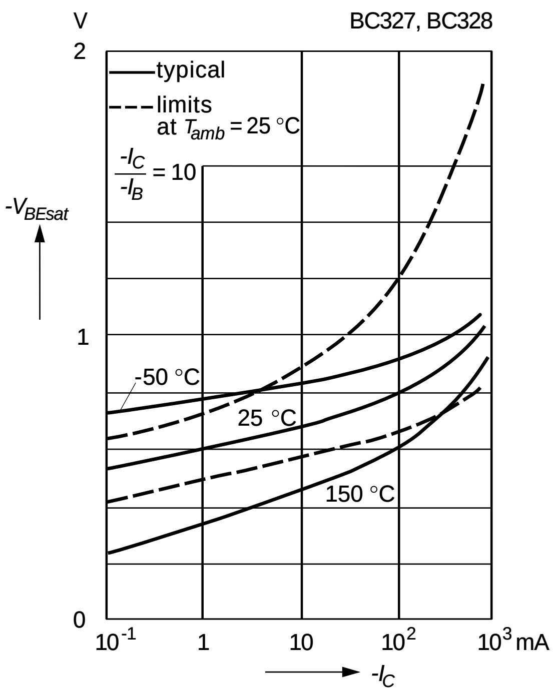
Collector saturation voltage versus collector current



Gain-bandwidth product versus collector current



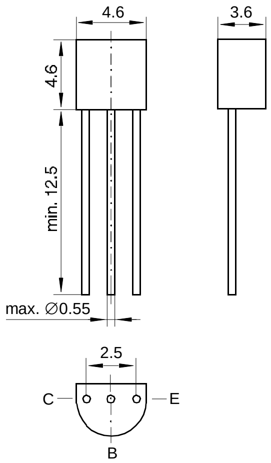
Base saturation voltage versus collector current



PNP Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

These transistors are subdivided into three groups A, B and C according to their current gain. The type BC556 is available in groups A and B, however, the types BC557 and BC558 can be supplied in all three groups. The BC559 is a low-noise type available in all three groups. As complementary types, the NPN transistors BC546 … BC549 are recommended.

On special request, these transistors are also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Base Voltage	**BC556** **BC557** **BC558, BC559**	$-V_{CBO}$ $-V_{CBO}$ $-V_{CBO}$	80 50 30	V V V
Collector-Emitter Voltage	**BC556** **BC557** **BC558, BC559**	$-V_{CES}$ $-V_{CES}$ $-V_{CES}$	80 50 30	V V V
Collector-Emitter Voltage	**BC556** **BC557** **BC558, BC559**	$-V_{CEO}$ $-V_{CEO}$ $-V_{CEO}$	65 45 30	V V V
Emitter-Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	100	mA
Peak Collector Current		$-I_{CM}$	200	mA
Peak Base Current		$-I_{BM}$	200	mA
Peak Emitter Current		I_{EM}	200	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
h-Parameters at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA, f = 1 kHz					
Current Gain **Current Gain Group A**	h_{fe}	–	220	–	–
B	h_{fe}	–	330	–	–
C	h_{fe}	–	600	–	–
Input Impedance **Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
B	h_{ie}	3.2	4.5	8.5	kΩ
C	h_{ie}	6	8.7	15	kΩ
Output Admittance **Current Gain Group A**	h_{oe}	–	18	30	µS
B	h_{oe}	–	30	60	µS
C	h_{oe}	–	60	110	µS
Reverse Voltage Transfer Ratio **Current Gain Group A**	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain at $-V_{CE}$ = 5 V, $-I_C$ = 10 µA **Current Gain Group A**	h_{FE}	–	90	–	–
B	h_{FE}	–	150	–	–
C	h_{FE}	–	270	–	–
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA **Current Gain Group A**	h_{FE}	110	180	220	–
B	h_{FE}	200	290	450	–
C	h_{FE}	420	500	800	–
at $-V_{CE}$ = 5 V, $-I_C$ = 100 mA **Current Gain Group A**	h_{FE}	–	120	–	–
B	h_{FE}	–	200	–	–
C	h_{FE}	–	400	–	–
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	250[1)]	K/W
Collector Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA	$-V_{CEsat}$	–	80	300	mV
at $-I_C$ = 100 mA, $-I_B$ = 5 mA	$-V_{CEsat}$	–	250	650	mV
Base Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA	$-V_{BEsat}$	–	700	–	mV
at $-I_C$ = 100 mA, $-I_B$ = 5 mA	$-V_{BEsat}$	–	900	–	mV
Base-Emitter Voltage at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA	$-V_{BE}$	600	660	750	mV
at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA	$-V_{BE}$	–	–	800	mV
Collector-Emitter Cutoff Current at $-V_{CE}$ = 80 V **BC556**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 50 V **BC557**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 30 V **BC558**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 80 V, T_j = 125 °C **BC556**	$-I_{CES}$	–	–	4	µA
at $-V_{CE}$ = 50 V, T_j = 125 °C **BC557**	$-I_{CES}$	–	–	4	µA
at $-V_{CE}$ = 30 V, T_j = 125 °C **BC558, BC559**	$-I_{CES}$	–	–	4	µA

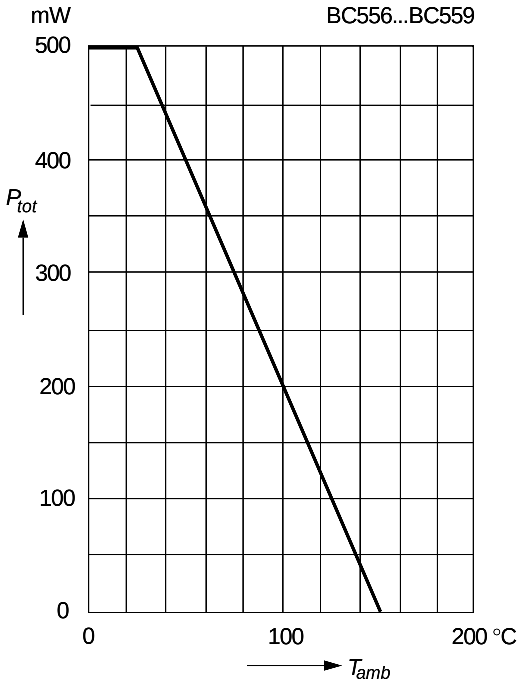
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Gain-Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 100 MHz	f_T	–	150	–	MHz
Collector-Base Capacitance at $-V_{CB}$ = 10V, f = 1 MHz	C_{CBO}	–	–	6	pF
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 200 µA, R_G = 2 kΩ, f = 1 kHz, Δf = 200 Hz **BC556, BC557, BC558** **BC559**	 F F	 – –	 2 1	 10 4	 dB dB
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 200 µA, R_G = 2 kΩ, f = 30…15000 Hz **BC559**	 F	 –	 1.2	 4	 dB

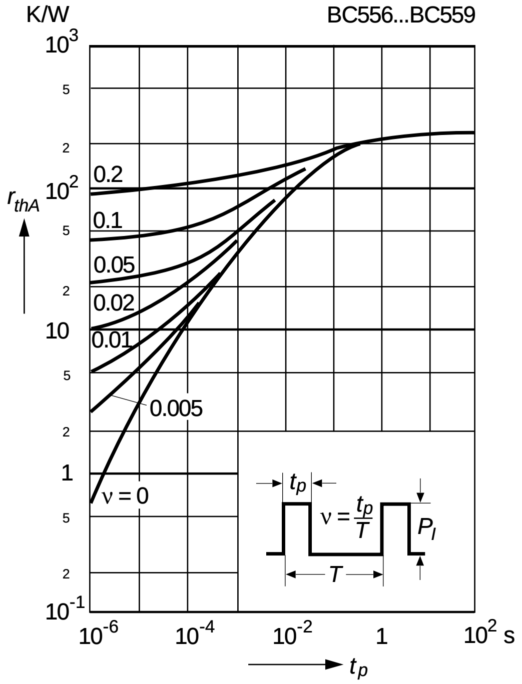
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

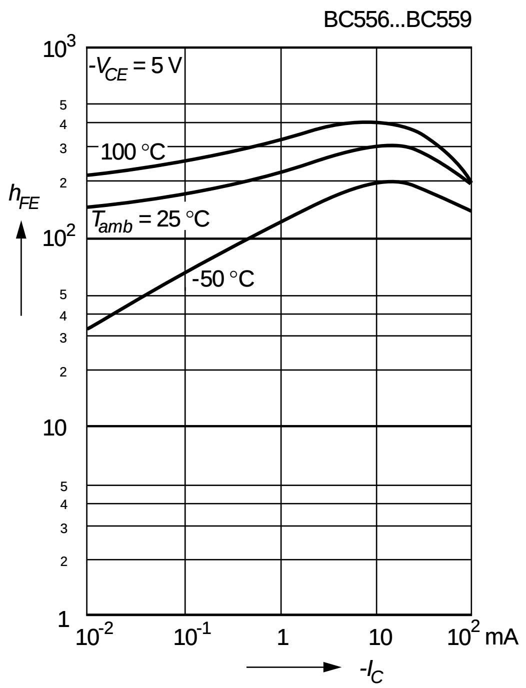


Pulse thermal resistance versus pulse duration

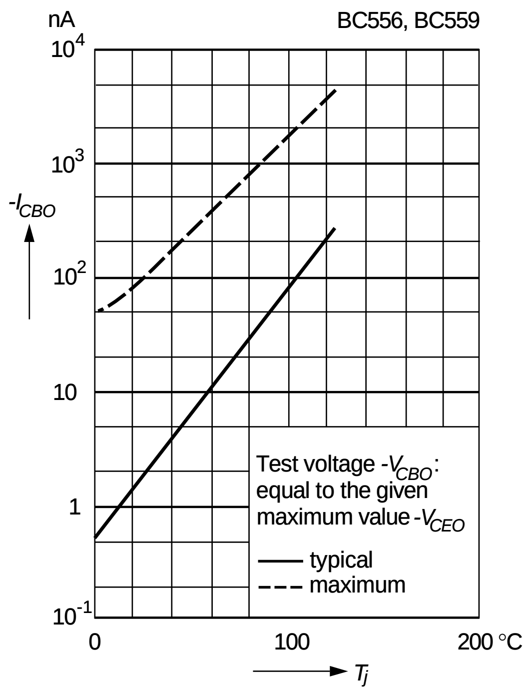
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



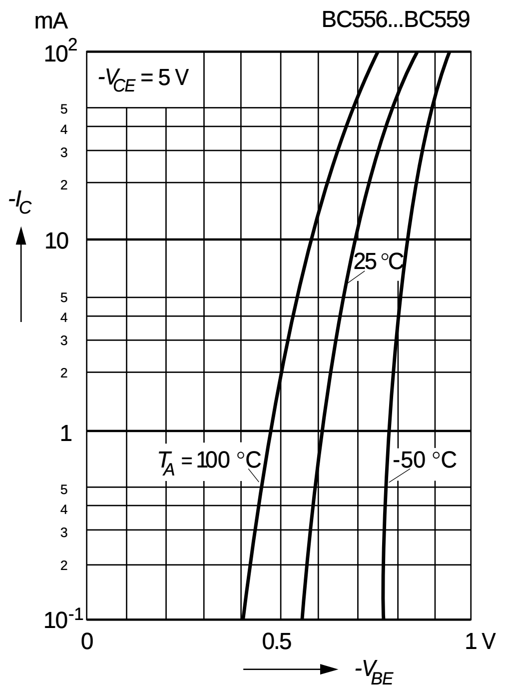
DC current gain versus collector current



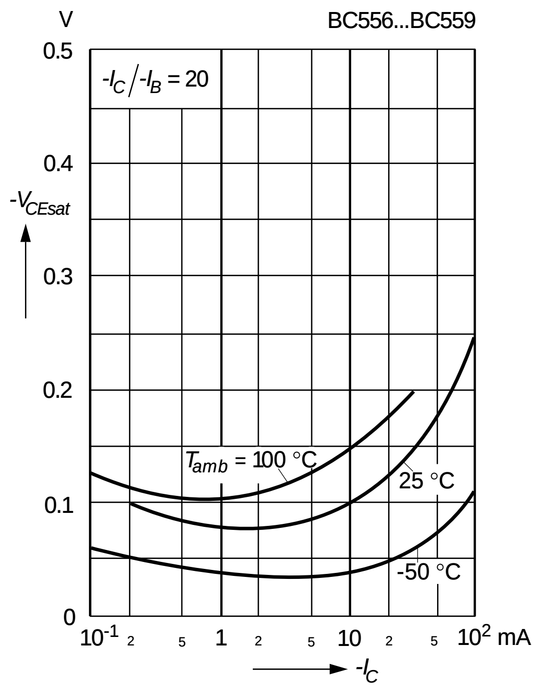
Collector-base cutoff current versus junction temperature



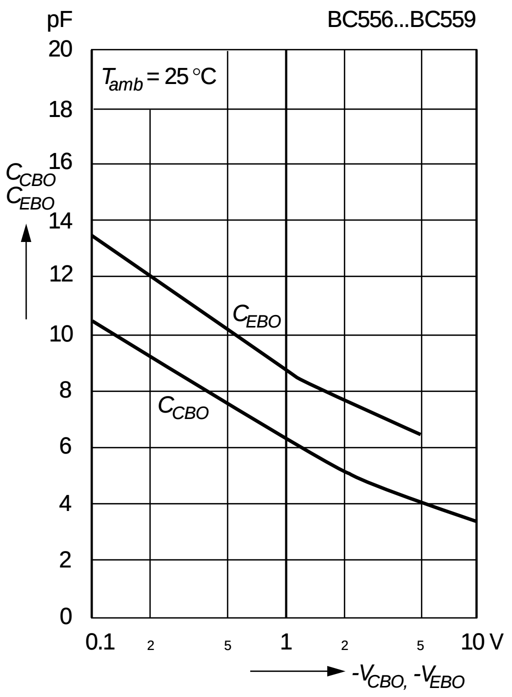
Collector current versus base-emitter voltage



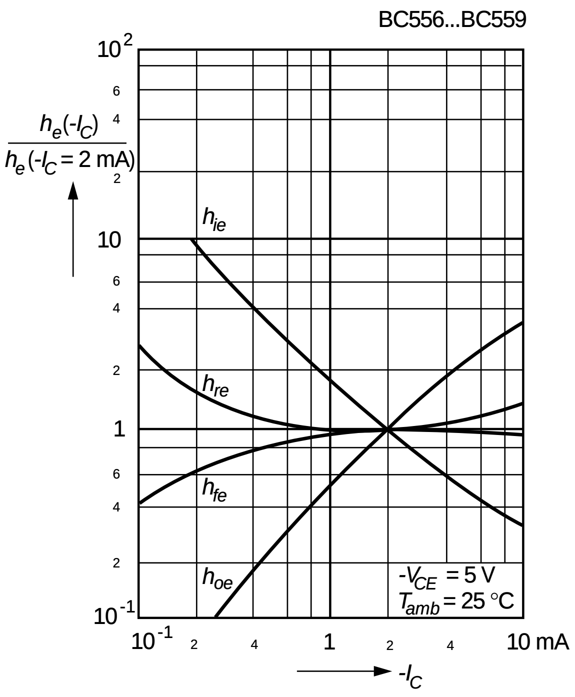
Collector saturation voltage versus collector current



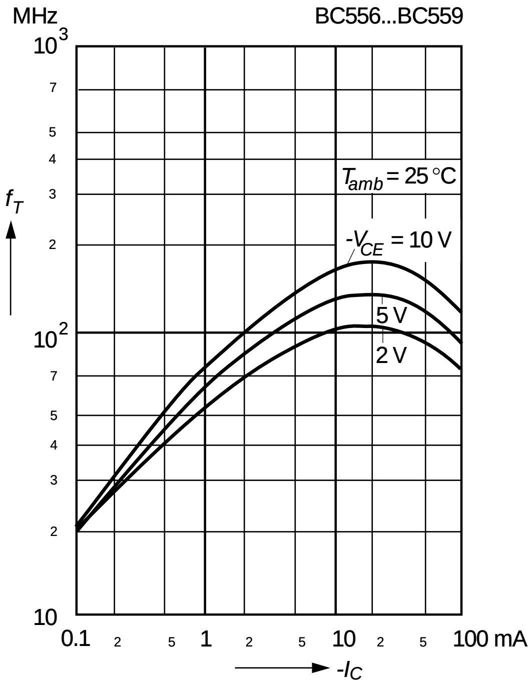
Collector-base capacitance, Emitter-base capacitance versus reverse bias voltage



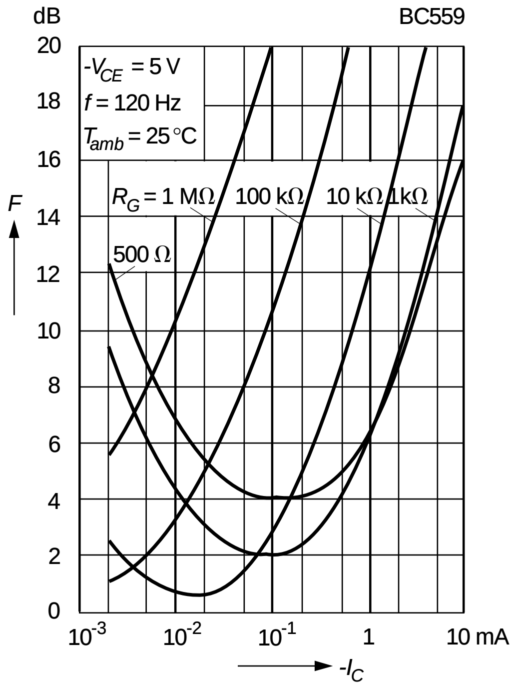
Relative h-parameters versus collector current

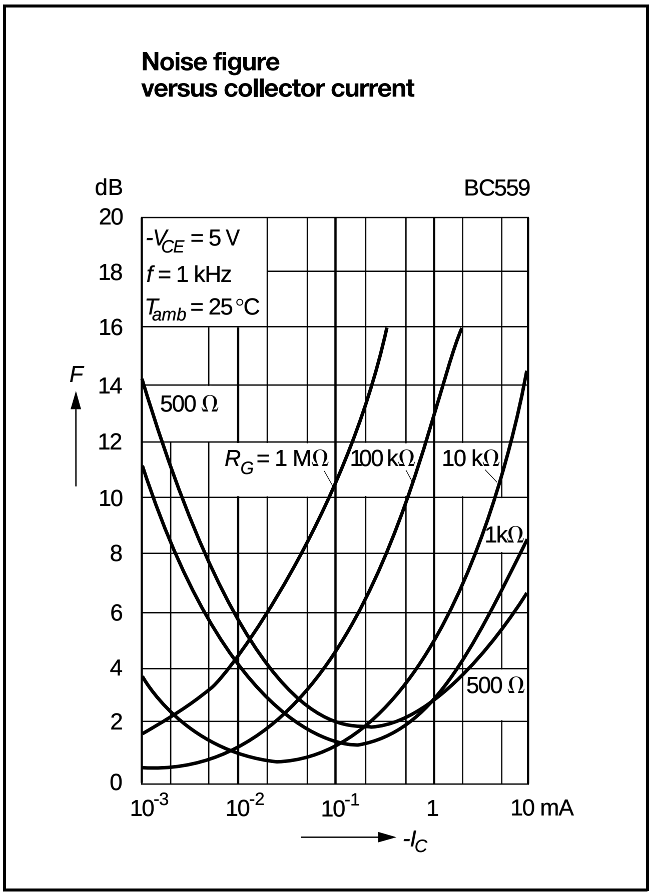


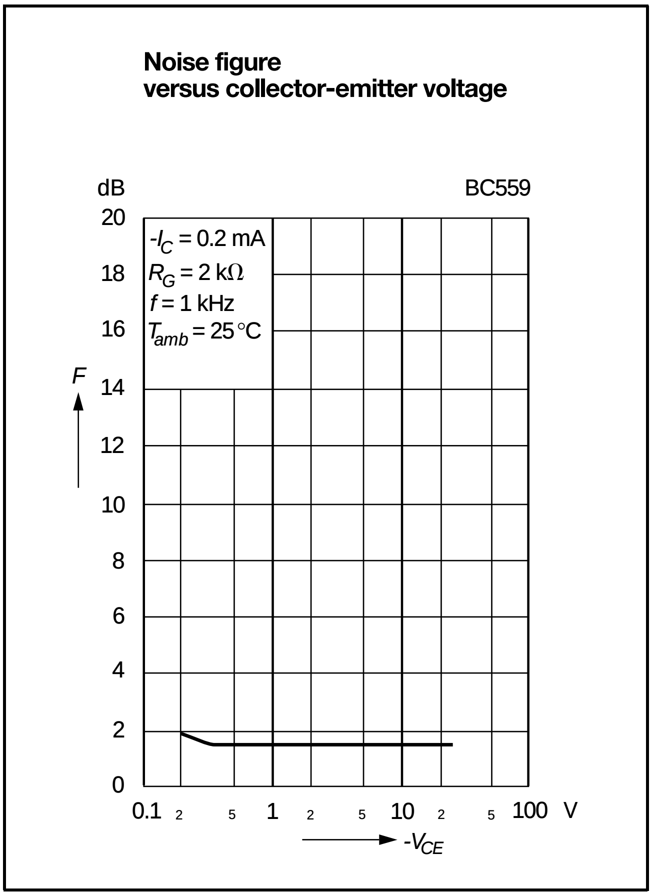
Gain-bandwidth product versus collector current



Noise figure versus collector current




Noise figure
versus collector current
dB
BC559
-VCE = 5 V
f = 1 kHz
Tamb = 25 °C
F
500 Ω
RG = 1 MΩ
100 kΩ
10 kΩ
1kΩ
500 Ω
20
18
16
14
12
10
8
6
4
2
0
10-3
10-2
10-1
1
10 mA
-IC


Noise figure
versus collector-emitter voltage
dB
BC559
-IC = 0.2 mA
RG = 2 kΩ
f = 1 kHz
Tamb = 25 °C
F
20
18
16
14
12
10
8
6
4
2
0
0.1
2
5
1
2
5
10
2
5
100 V
-VCE

PNP Silicon Epitaxial Planar Transistors
for switching, AF driver and amplifier applications.

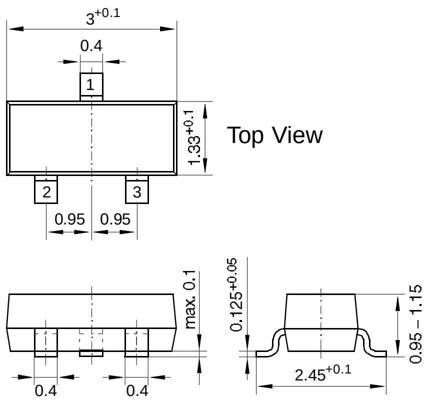
Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors are subdivided into three groups -16, -25 and -40 according to their current gain.
As complementary types, the NPN transistors BC817 and BC818 are recommended.

Pin configuration
1 = Collector, 2 = Base, 3 = Emitter.

Marking code

Type	Marking
BC807-16	5A
-25	5B
-40	5C
BC808-16	5E
-25	5F
-40	5G



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

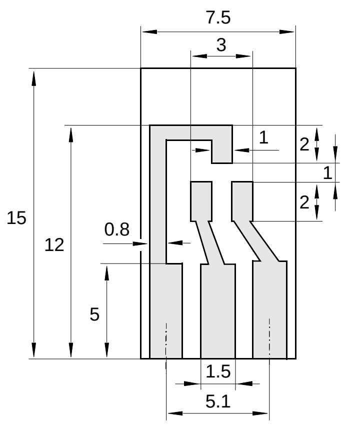
Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Emitter Voltage	**BC807** **BC808**	$-V_{CES}$ $-V_{CES}$	50 30	V V
Collector-Emitter Voltage	**BC807** **BC808**	$-V_{CEO}$ $-V_{CEO}$	45 25	V V
Emitter-Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	500	mA
Peak Collector Current		$-I_{CM}$	1000	mA
Peak Base Current		$-I_{BM}$	200	mA
Peak Emitter Current		I_{EM}	1000	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

1) Device on fiberglass substrate, see layout

Characteristics at T_{amb} = 25 °C

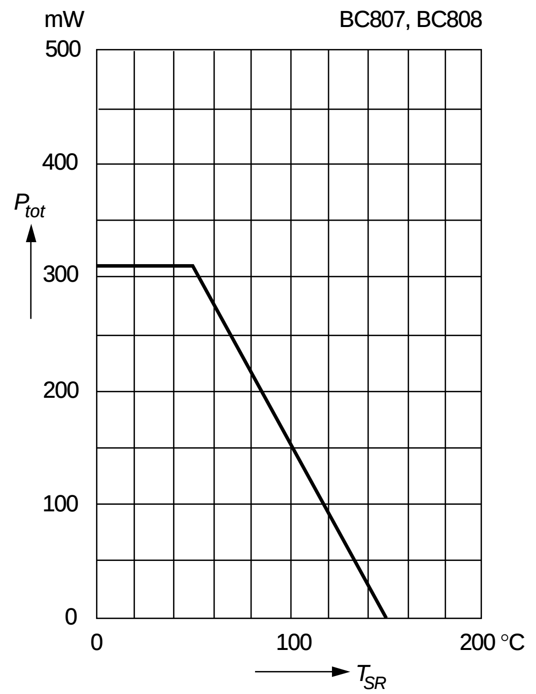
	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA **Current Gain Group-16** **-25** **-40** at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA **-16** **-25** **-40**	 h_{FE} h_{FE} h_{FE} h_{FE} h_{FE} h_{FE}	 100 160 250 60 100 170	 – – – – – –	 250 400 600 – – –	 – – – – – –
Thermal Resistance Junction Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Collector Saturation Voltage at $-I_C$ = 500 mA, $-I_B$ = 50 mA	$-V_{CEsat}$	–	–	0.7	V
Base-Emitter Voltage at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA	$-V_{BE}$	–	–	1.2	V
Collector-Emitter Cutoff Current at $-V_{CE}$ = 45 V **BC807** at $-V_{CE}$ = 25 V **BC808** at $-V_{CE}$ = 25 V, T_j = 150 °C	 $-I_{CES}$ $-I_{CES}$ $-I_{CES}$	 – – –	 – – –	 100 100 5	 nA nA µA
Emitter-Base Cutoff Current at $-V_{EB}$ = 4 V	$-I_{EBO}$	–	–	100	nA
Gain-Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector-Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz	C_{CBO}		12		pF
[1)] Device on fiberglass substrate, see layout					



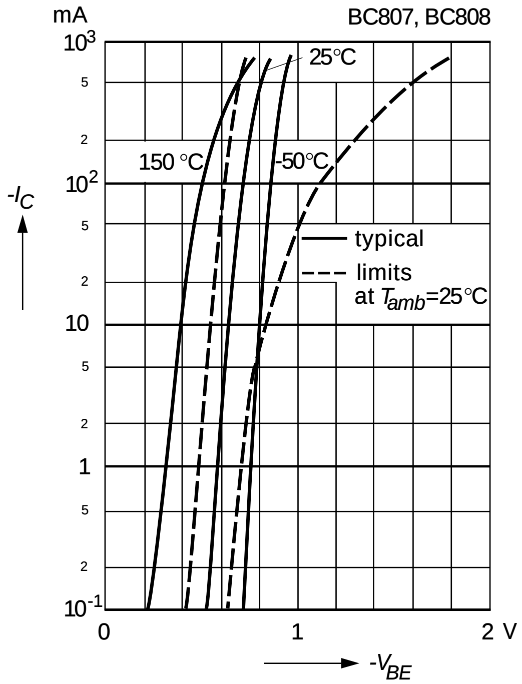
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout

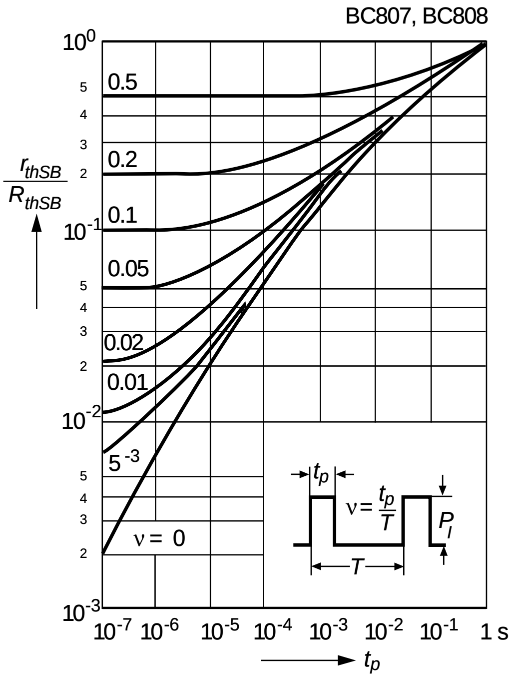


Collector current versus base-emitter voltage

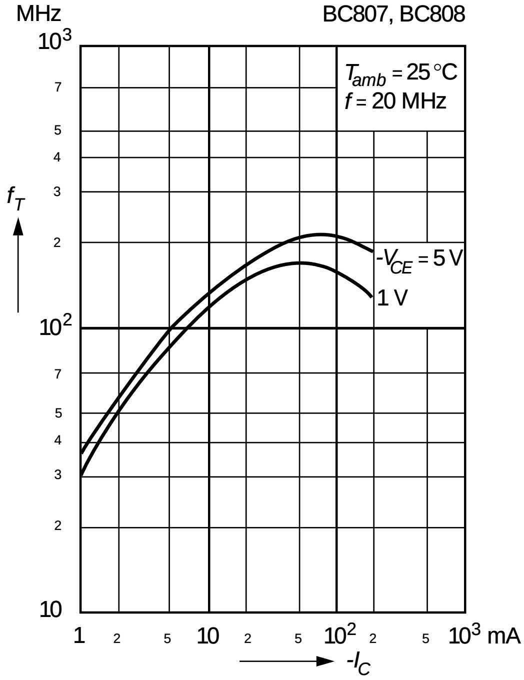


Pulse thermal resistance versus pulse duration (normalized)

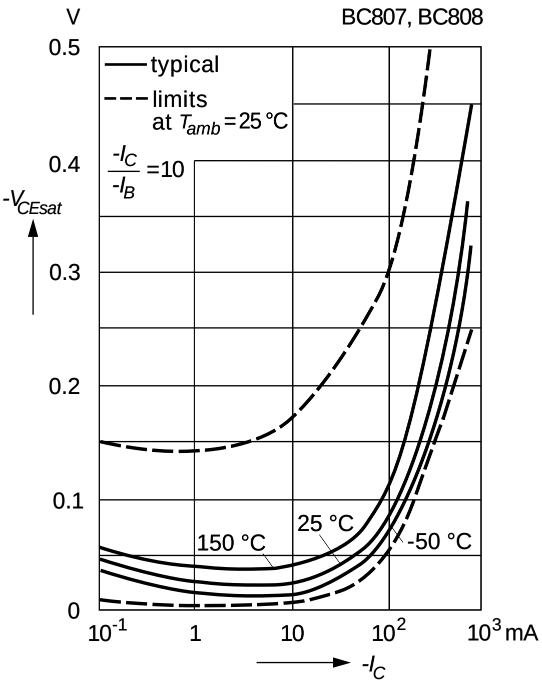
Device on fiberglass substrate, see layout



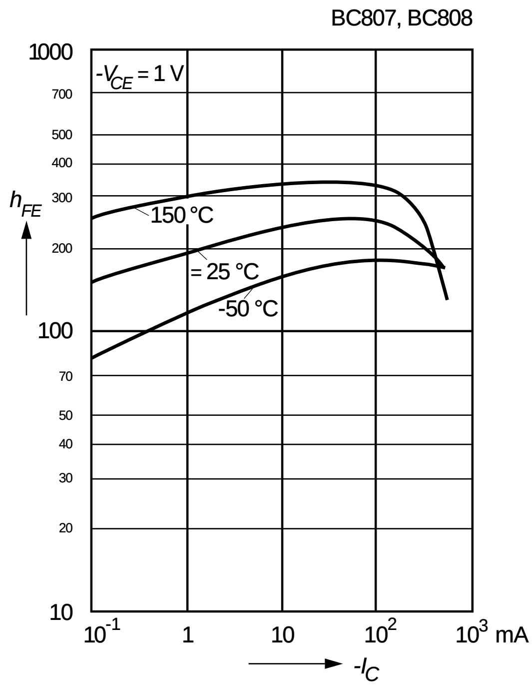
Gain-bandwidth product versus collector current



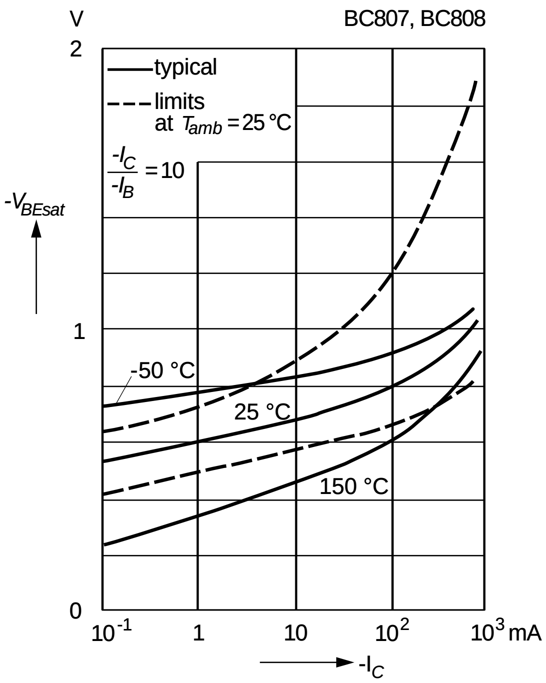
Collector saturation voltage versus collector current



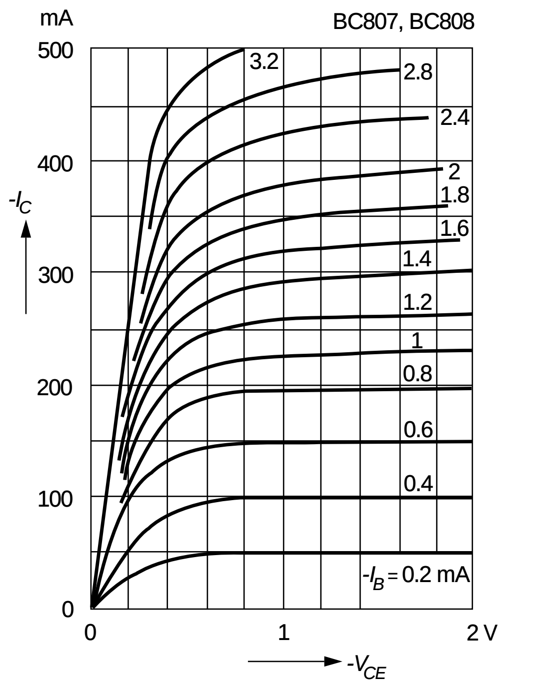
DC current gain versus collector current

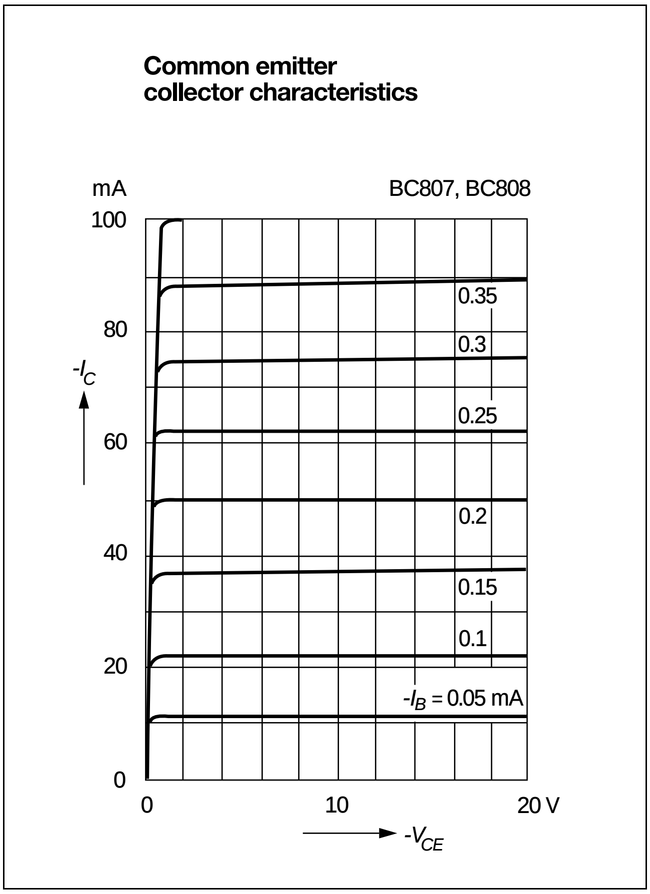


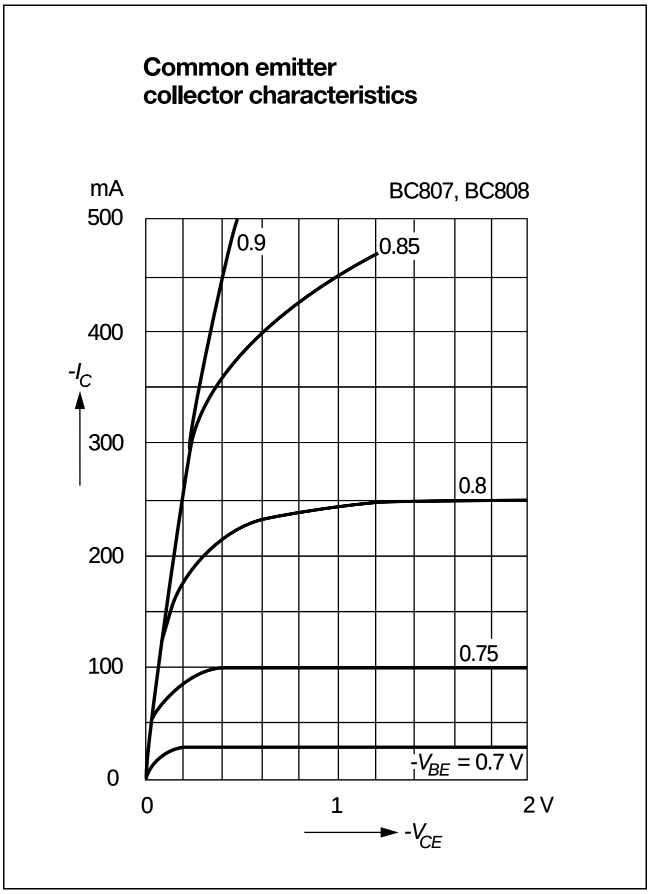
Base saturation voltage versus collector current



Common emitter collector characteristics




Common emitter
collector characteristics
BC807, BC808
mA
100
80
60
40
20
0
-IC
0
10
20 V
-VCE
0.35
0.3
0.25
0.2
0.15
0.1
-IB = 0.05 mA


Common emitter
collector characteristics
BC807, BC808
mA
500
400
300
200
100
0
-IC
0
1
2 V
-VCE
0.9
0.85
0.8
0.75
-VBE = 0.7 V

PNP Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

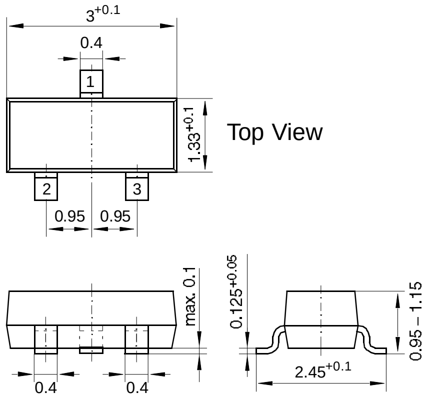
Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors are subdivided into three groups A, B and C according to their current gain. The type BC856 is available in groups A and B, however, the types BC857, BC858 and BC859 can be supplied in all three groups. The BC859 is a low noise type. As complementary types, the NPN transistors BC846 … BC849 are recommended.

Pin configuration
1 = Collector, 2 = Base, 3 = Emitter.

Marking code

Type	Marking	Type	Marking
BC856A	3A	BC859A	4A
B	3B	B	4B
BC857A	3E	C	4C
B	3F		
C	3G		
BC858A	3J		
B	3K		
C	3L		



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Base Voltage	**BC856** **BC857** **BC858, BC859**	$-V_{CBO}$ $-V_{CBO}$ $-V_{CBO}$	80 50 30	V V V
Collector-Emitter Voltage	**BC856** **BC857** **BC858, BC859**	$-V_{CES}$ $-V_{CES}$ $-V_{CES}$	80 50 30	V V V
Collector-Emitter Voltage	**BC856** **BC857** **BC858, BC859**	$-V_{CEO}$ $-V_{CEO}$ $-V_{CEO}$	65 45 30	V V V
Emitter-Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	100	mA
Peak Collector Current		$-I_{CM}$	200	mA
Peak Base Current		$-I_{BM}$	200	mA
Peak Emitter Current		I_{EM}	200	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65 … +150	°C

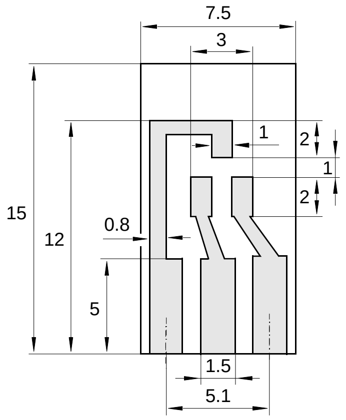
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
h-Parameters at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA, f = 1 kHz					
Current Gain **Current Gain Group A**	h_{fe}	–	220	–	–
B	h_{fe}	–	330	–	–
C	h_{fe}	–	600	–	–
Input Impedance **Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
B	h_{ie}	3.2	4.5	8.5	kΩ
C	h_{ie}	6	8.7	15	kΩ
Output Admittance **Current Gain Group A**	h_{oe}	–	18	30	µS
B	h_{oe}	–	30	60	µS
C	h_{oe}	–	60	110	µS
Reverse Voltage Transfer Ratio **Current Gain Group A**	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain at $-V_{CE}$ = 5 V, $-I_C$ = 10 µA **Current Gain Group A**	h_{FE}	–	90	–	–
B	h_{FE}	–	150	–	–
C	h_{FE}	–	270	–	–
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA **Current Gain Group A**	h_{FE}	110	180	220	–
B	h_{FE}	200	290	450	–
C	h_{FE}	420	520	800	–
Thermal Resistance Junction to Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Collector Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA	$-V_{CEsat}$	–	90	300	mV
at $-I_C$ = 100 mA, $-I_B$ = 5 mA	$-V_{CEsat}$	–	250	650	mV
Base Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA	$-V_{BEsat}$	–	700	–	mV
at $-I_C$ = 100 mA, $-I_B$ = 5 mA	$-V_{BEsat}$	–	900	–	mV
Base-Emitter Voltage at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA	$-V_{BE}$	600	660	750	mV
at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA	$-V_{BE}$	–	–	800	mV
Collector-Emitter Cutoff Current at $-V_{CE}$ = 80 V **BC856**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 50 V **BC857**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 30 V **BC858, BC859**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 80 V, T_j = 125 °C **BC856**	$-I_{CES}$	–	–	4	µA
at $-V_{CE}$ = 50 V, T_j = 125 °C **BC857**	$-I_{CES}$	–	–	4	µA
at $-V_{CE}$ = 30 V, T_j = 125 °C **BC858, BC859**	$-I_{CES}$	–	–	4	µA
at $-V_{CB}$ = 30 V	$-I_{CBO}$	–	–	15	nA
at $-V_{CB}$ = 30 V, T_j = 150 °C	$-I_{CBO}$	–	–	5	µA
Gain-Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 100 MHz	f_T	–	150	–	MHz

[1)] Device on fiberglass substrate, see layout

Characteristics, continuation

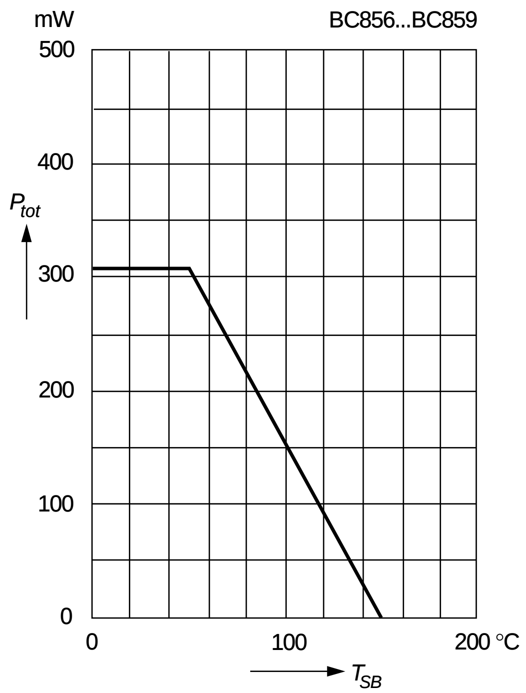
	Symbol	Min.	Typ.	Max.	Unit
Collector-Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz	C_{CBO}	–	–	6	pF
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 200 µA, R_G = 2 kΩ, f = 1 kHz, Δf = 200 Hz **BC856, BC857, BC858** **BC859**	 F F	 – –	 2 1	 10 4	 dB dB
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 200 µA, R_G = 2 kΩ, f = 30…15000 Hz **BC859**	F	–	1.2	4	dB



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

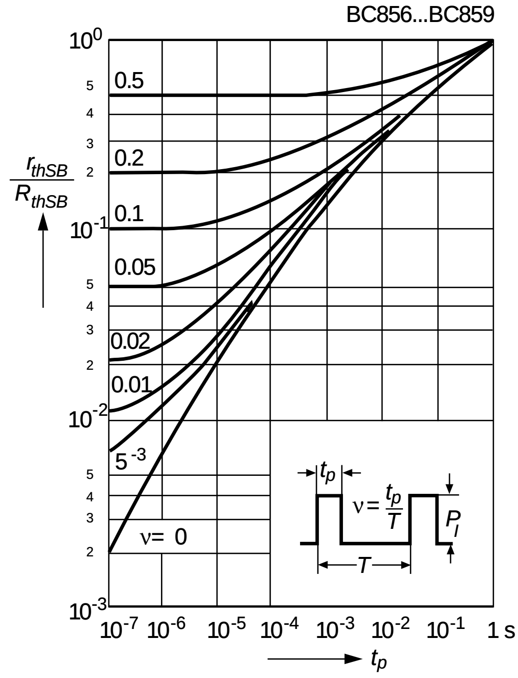
Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout

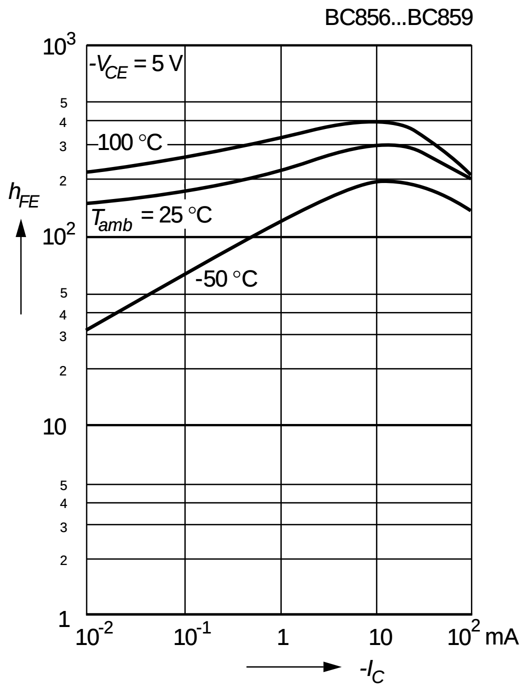


Pulse thermal resistance versus pulse duration (normalized)

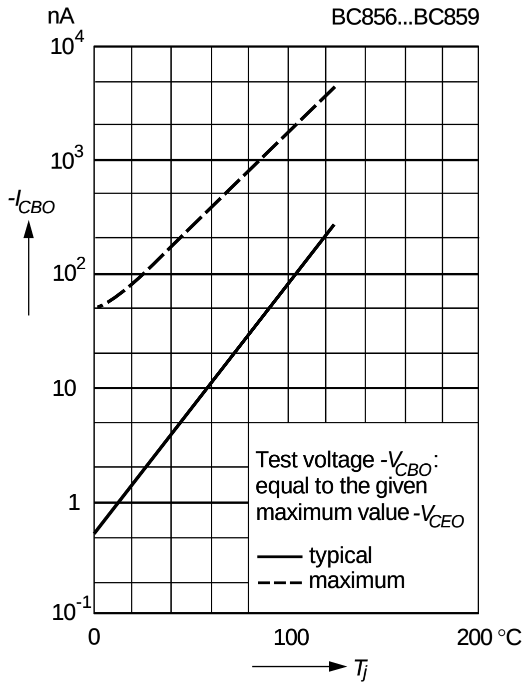
Device on fiberglass substrate, see layout



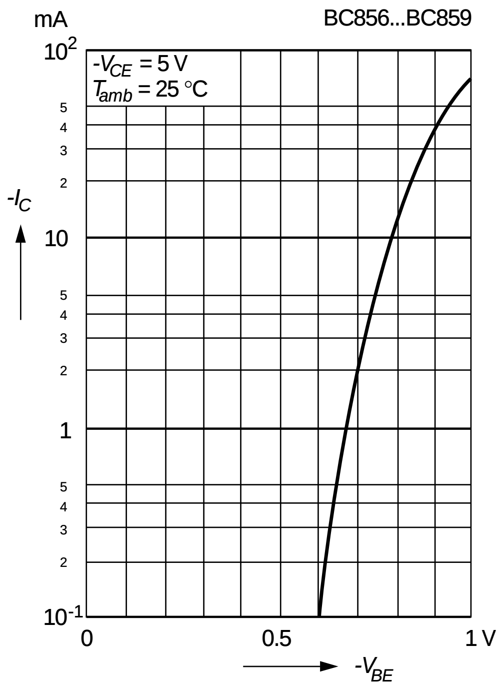
DC current gain versus collector current



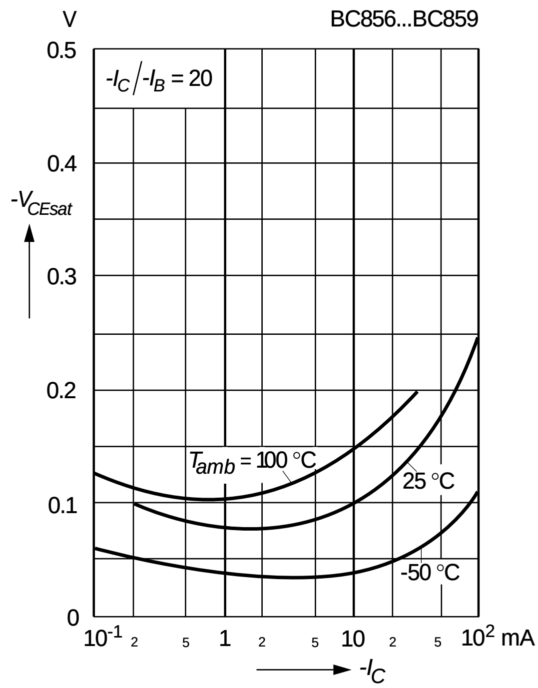
Collector-base cutoff current versus junction temperature



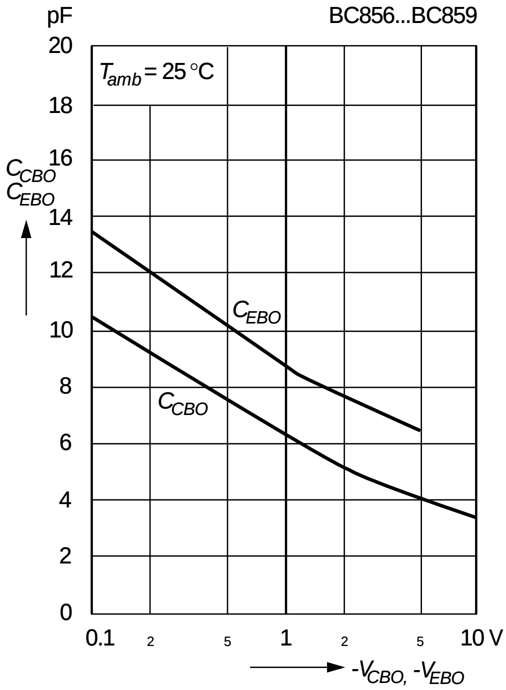
Collector current versus base-emitter voltage



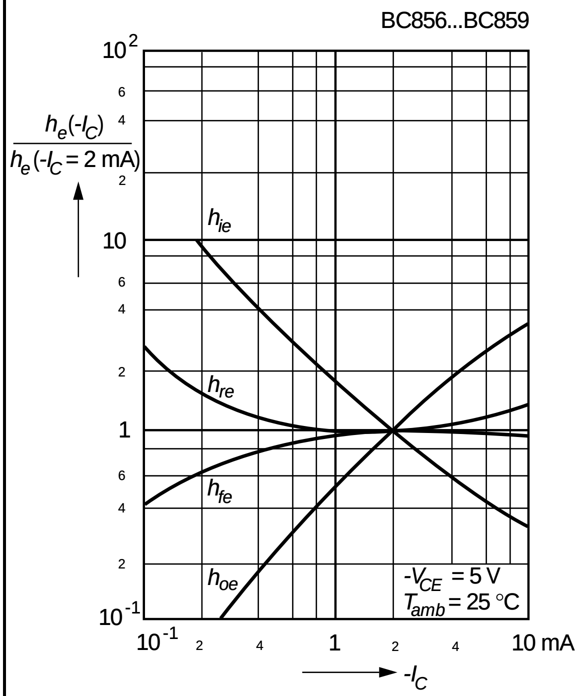
Collector saturation voltage versus collector current



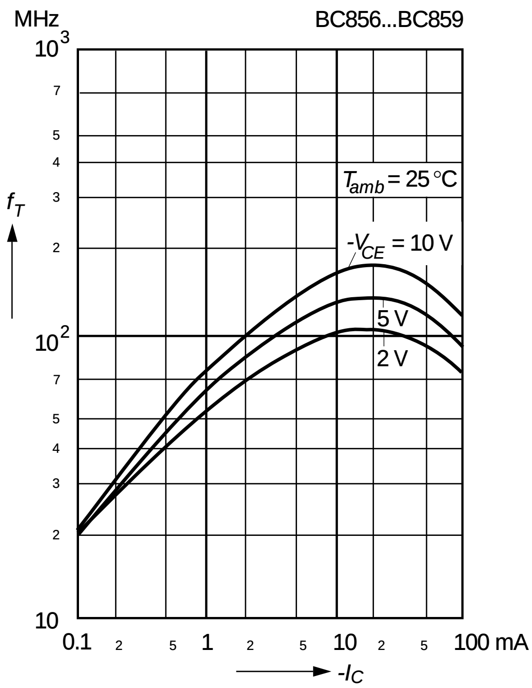
Collector-base capacitance, Emitter-base capacitance versus reverse bias voltage



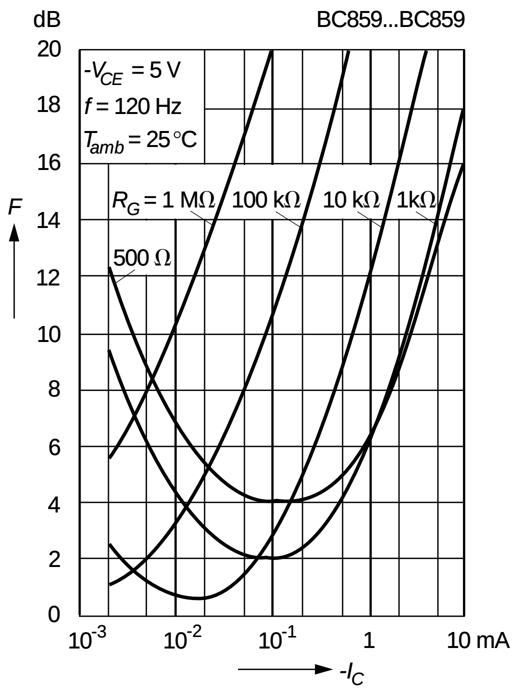
Relative h-parameters versus collector current



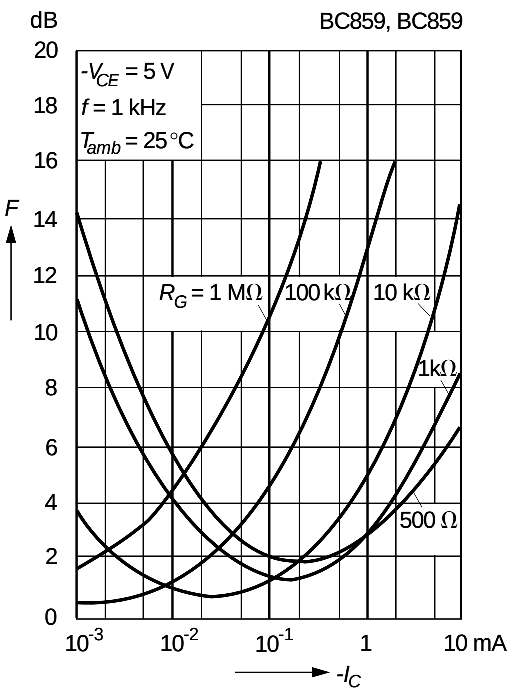
Gain-bandwidth product versus collector current



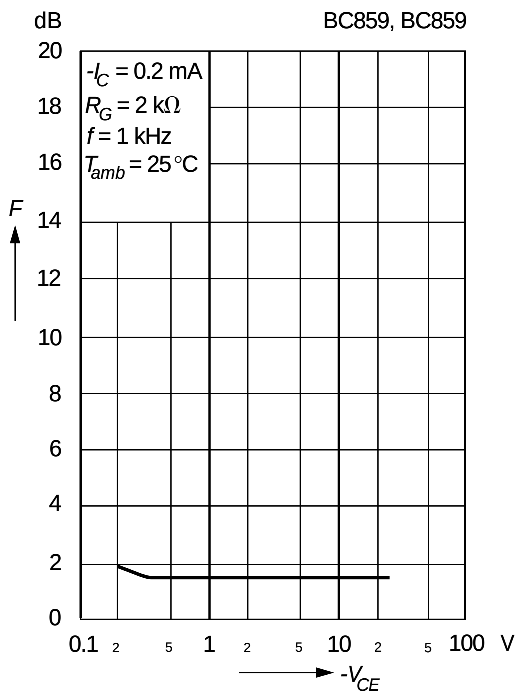
Noise figure versus collector current



Noise figure versus collector current

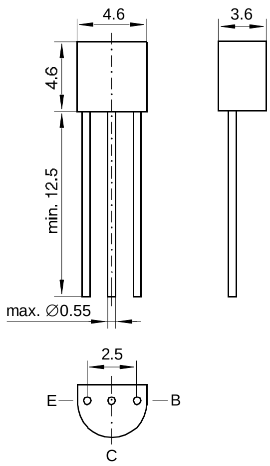


Noise figure versus collector-emitter voltage



PNP Silicon Epitaxial Transistors
especially suited for application in class-B video output stages of TV receivers and monitors.

As complementary types, the NPN transistors BF420 and BF422 are recommended.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Base Voltage	**BF421** **BF423**	$-V_{CBO}$ $-V_{CBO}$	300 250	V V
Collector-Emitter Voltage	**BF423**	$-V_{CEO}$	250	V
Collector-Emitter Voltage	**BF421**	$-V_{CER}$	300	V
Emitter-Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	50	mA
Peak Collector Current		$-I_{CM}$	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	830[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

1) Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Collector-Base Breakdown Voltage at $-I_C$ = 100 µA, I_E = 0 **BF421** **BF423**	$-V_{(BR)CBO}$ $-V_{(BR)CBO}$	300 250	– –	– –	V V
Collector-Emitter Breakdown Voltage **BF423** at $-I_C$ = 10 mA, I_B = 0	$-V_{(BR)CEO}$	250	–	–	V
Collector-Emitter Breakdown Voltage **BF421** at R_{BE} = 2.7 kΩ, at $-I_C$ = 10 mA	$-V_{(BR)CER}$	300	–	–	V
Emitter-Base Breakdown Voltage at $-I_E$ = 100 µA, I_C = 0	$-V_{(BR)EBO}$	5	–	–	V
Collector-Base Cutoff Current at $-V_{CB}$ = 200 V, I_E = 0	$-I_{CBO}$	–	–	10	nA
Collector-Emitter Cutoff Current at R_{BE} = 2.7 kΩ, $-V_{CE}$ = 250 V at R_{BE} = 2.7 kΩ, $-V_{CE}$ = 200 V, T_j = 150 °C	 $-I_{CER}$ $-I_{CER}$			 50 10	 nA µA
Collector Saturation Voltage at $-I_C$ = 30 mA, $-I_B$ = 5 mA	$-V_{CEsat}$	–	–	0.8	V
DC Current Gain at $-V_{CE}$ = 20 V, $-I_C$ = 25 mA	h_{FE}	50	–	–	–
Gain-Bandwidth Product at $-V_{CE}$ = 10 V, $-I_C$ = 10 mA	f_T	60	–	–	MHz
Feedback Capacitance at $-V_{CE}$ = 30 V, $-I_C$ = 0, f = 1 MHz	C_{re}	–	–	1.6	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W

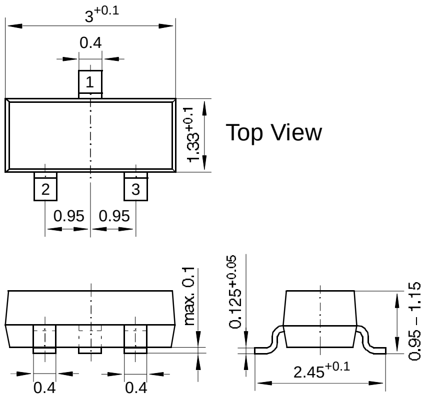
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

PNP Silicon Epitaxial Planar Transistors
especially suited for application in class-B video output stages of TV receivers and monitors.

As complementary types, the NPN transistors BF820 and BF822 are recommended.

Pin Configuration
1 = Collector, 2 = Base, 3 = Emitter.

Marking code
BF821 = 1W
BF823 = 1Y



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

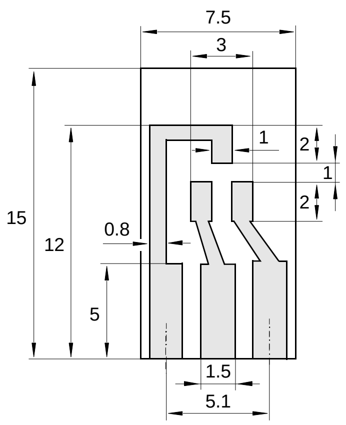
Absolute Maximum Ratings

	Symbol	Value	Unit
Collector-Base Voltage **BF821** **BF823**	$-V_{CBO}$ $-V_{CBO}$	300 250	V V
Collector-Emitter Voltage **BF823**	$-V_{CEO}$	250	V
Collector-Emitter Voltage **BF821**	$-V_{CER}$	300	V
Emitter-Base Voltage	$-V_{EBO}$	5	V
Collector Current	$-I_C$	50	mA
Peak Collector Current	$-I_{CM}$	100	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	300[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C
1) Device on fiberglass substrate, see layout			

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
Collector-Base Breakdown Voltage at $-I_C$ = 100 µA, I_E = 0	**BF821** **BF823**	$-V_{(BR)CBO}$ $-V_{(BR)CBO}$	300 250	– –	– –	V V
Collector-Emitter Breakdown Voltage at $-I_C$ = 10 mA, I_B = 0	**BF823**	$-V_{(BR)CEO}$	250	–	–	V
Collector-Emitter Breakdown Voltage at R_{BE} = 2.7 kΩ, $-I_C$ = 10 mA	**BF821**	$-V_{(BR)CER}$	300	–	–	V
Emitter-Base Breakdown Voltage at $-I_E$ = 100 µA, I_C = 0		$-V_{(BR)EBO}$	5	–	–	V
Collector-Base Cutoff Current at $-V_{CB}$ = 200 V, I_E = 0		$-I_{CBO}$	–	–	10	nA
Collector-Emitter Cutoff Current at R_{BE} = 2.7 kΩ, $-V_{CE}$ = 250 V at R_{BE} = 2.7 kΩ, $-V_{CE}$ = 200 V, T_j = 150 °C		$-I_{CER}$ $-I_{CER}$			50 10	nA µA
Collector Saturation Voltage at $-I_C$ = 30 mA, $-I_B$ = 5 mA		$-V_{CEsat}$	–	–	0.8	V
DC Current Gain at $-V_{CE}$ = 20 V, $-I_C$ = 25 mA		h_{FE}	50	–	–	–
Gain-Bandwidth Product at $-V_{CE}$ = 10 V, $-I_C$ = 10 mA		f_T	60	–	–	MHz
Feedback Capacitance at $-V_{CE}$ = 30 V, $-I_C$ = 0, f = 1 MHz		C_{re}	–	–	1.6	pF
Thermal Resistance Junction to Ambient Air		R_{thA}	–	–	430[1)]	K/W

[1)] Device on fiberglass substrate, see layout



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

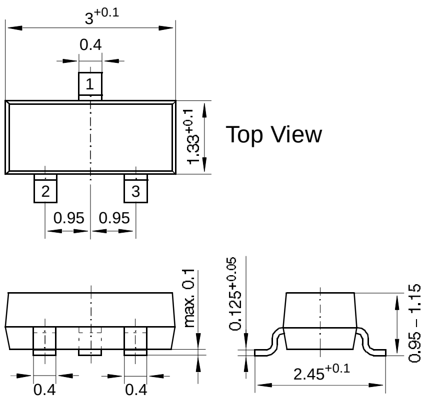
MMBT3906

PNP Silicon Epitaxial Planar Transistor
for switching and amplifier applications.

As complementary type, the NPN transistor MMBT3904 is recommended.

Pin Configuration
1 = Collector, 2 = Base, 3 = Emitter.

Marking code
3N



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector-Base Voltage	$-V_{CBO}$	40	V
Collector-Emitter Voltage	$-V_{CEO}$	40	V
Emitter-Base Voltage	$-V_{EBO}$	5	V
Collector Current	$-I_C$	100	mA
Peak Collector Current	$-I_{CM}$	200	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	310[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–55…+150	°C

[1)] Device on fiberglass subtrate, see layout

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $-V_{CE}$ = 1 V, $-I_C$ = 0.1 mA at $-V_{CE}$ = 1 V, $-I_C$ = 1 mA at $-V_{CE}$ = 1 V, $-I_C$ = 10 mA at $-V_{CE}$ = 1 V, $-I_C$ = 50 mA at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA	 h_{FE} h_{FE} h_{FE} h_{FE} h_{FE}	 60 80 100 60 30	 – – – – –	 – – 300 – –	 – – – –
Thermal Resistance Junction to Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Collector Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 1 mA at $-I_C$ = 50 mA, $-I_B$ = 5 mA	 $-V_{CEsat}$ $-V_{CEsat}$	 – –	 – –	 0.25 0.4	 V V
Base Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 1 mA at $-I_C$ = 50 mA, $-I_B$ = 5 mA	 $-V_{BEsat}$ $-V_{BEsat}$	 – –	 – –	 0.85 0.95	 V V
Collector-Emitter Cutoff Current at $-V_{EB}$ = 3 V, $-V_{CE}$ = 30 V	$-I_{CEV}$	–	–	50	nA
Emitter-Base Cutoff Current at $-V_{EB}$ = 3 V, $-V_{CE}$ = 30 V	$-I_{EBV}$	–	–	50	nA
Collector-Base Breakdown Voltage at $-I_C$ = 10 µA, I_E = 0	$-V_{(BR)CBO}$	40	–	–	V
Collector-Emitter Breakdown Voltage at $-I_C$ = 1 mA, I_B = 0	$-V_{(BR)CEO}$	40	–	–	V
Emitter-Base Breakdown Voltage at $-I_E$ = 10 µA, I_C = 0	$-V_{(BR)EBO}$	5	–	–	V
Gain-Bandwidth Product at $-V_{CE}$ = 20 V, $-I_C$ = 10 mA, f = 100 MHz	f_T	250	–	–	MHz
Collector-Base Capacitance at $-V_{CB}$ = 5 V, f = 100 kHz	C_{CBO}	–	–	4.5	pF
Emitter-Base Capacitance at $-V_{EB}$ = 0.5 V, f = 100 kHz	C_{EBO}	–	–	10	pF
Input Impedance at $-V_{CE}$ = 10 V, $-I_C$ = 1 mA, f = 1 kHz	h_{ie}	1	–	10	kΩ

[1)] Device on fiberglass substrate, see layout

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Voltage Feedback Ratio at $-V_{CE}$ = 10 V, $-I_C$ = 1 mA, f = 1 kHz	h_{re}	$0.5 \cdot 10^{-4}$	–	$8 \cdot 10^{-4}$	–
Small-Signal Current Gain at $-V_{CE}$ = 10 V, $-I_C$ = 1 mA, f = 1 kHz	h_{fe}	100	–	400	–
Output Admittance at $-V_{CE}$ = 1 V, $-I_C$ = 1 mA, f = 1 kHz	h_{oe}	1	–	40	µS
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 100 µA, R_G = 1 kΩ, f = 10…15 000 Hz	F	–	–	4	dB
Delay Time (see Fig. 1) at $-I_{B1}$ = 1 mA, $-I_C$ = 10 mA	t_d	–	–	35	ns
Rise Time (see Fig. 1) at $-I_{B1}$ = 1 mA, $-I_C$ = 10 mA	t_r	–	–	35	ns
Storage Time (see Fig. 2) at $I_{B1} = -I_{B2}$ = 1 mA, $-I_C$ = 10 mA	t_s	–	–	225	ns
Fall Time (see Fig. 2) at $I_{B1} = -I_{B2}$ = 1 mA, $-I_C$ = 10 mA	t_f	–	–	75	ns

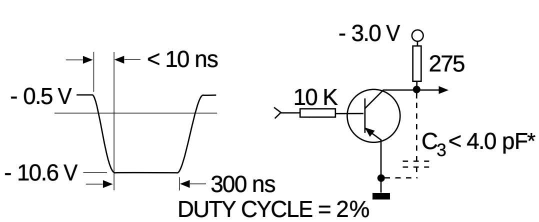


Fig. 1: Test circuit for delay and rise time

* total shunt capacitance of test jig and connectors

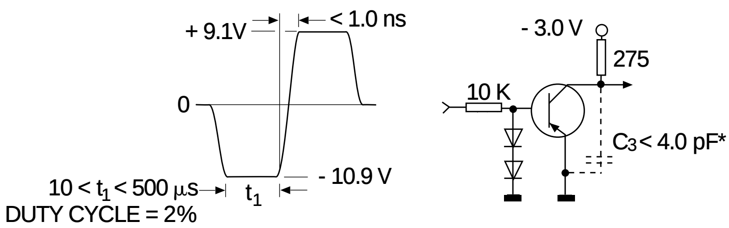
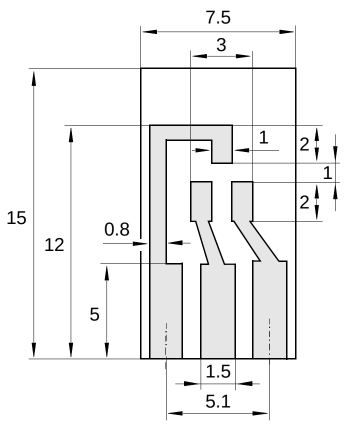


Fig. 2: Test circuit for storage and fall time

* total shunt capacitance of test jig and connectors



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

PNP Silicon Epitaxial Planar Transistors
especially suited as line switch in telephone subsets and in video output stages of TV receivers and monitors.

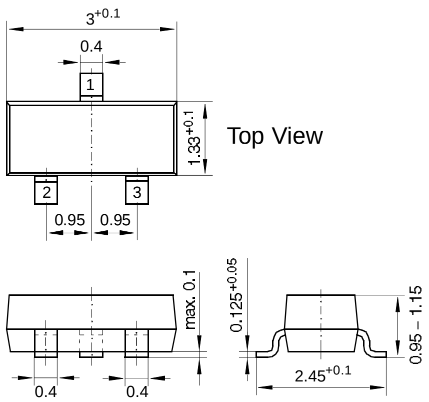
As complementary types, the PNP transistors MMBTA42 and MMBTA43 are recommended.

Pin Configuration

1 = Collector, 2 = Base, 3 = Emitter

Marking Code

MMBTA92 = 2D
MMBTA93 = 2E



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

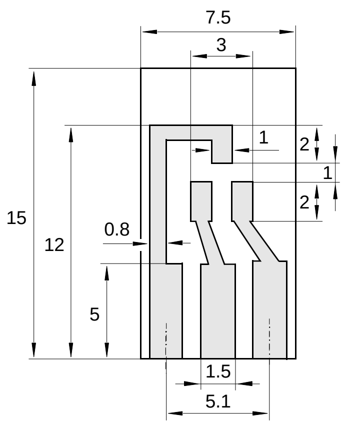
Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Emitter Voltage	**MMBTA92** **MMBTA93**	$-V_{CEO}$ $-V_{CEO}$	300 200	V V
Collector-Base Voltage	**MMBTA92** **MMBTA93**	$-V_{CBO}$ $-V_{CBO}$	300 200	V V
Emitter-Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	500	mA
Power Dissipation[1)] at T_{SB} = 50 °C		P_{tot}	300[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Device on fiberglass substrate, see layout

Characteristics at T_{amb} = 25 °C

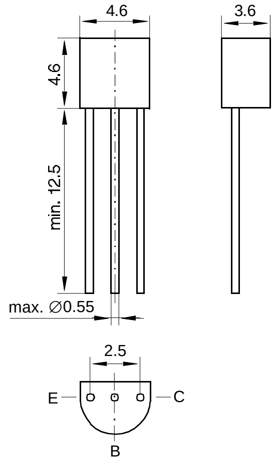
	Symbol	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage **MMBTA92** $-I_C$ = 10 mA, I_B = 0 **MMBTA93**	$-V_{(BR)CEO}$ $-V_{(BR)CEO}$	300 200	– –	– –	V V
Collector-Base Breakdown Voltage **MMBTA92** $-I_C$ = 100 µA, I_E = 0 **MMBTA93**	$-V_{(BR)CBO}$ $-V_{(BR)CBO}$	300 200	– –	– –	V V
Emitter-Base Breakdown Voltage $-I_E$ = 100 µA, I_C = 0	$-V_{(BR)EBO}$	5	–	–	V
Collector-Base Cutoff Current $-V_{CB}$ = 200 V, I_E = 0 **MMBTA92** $-V_{CB}$ = 160 V, I_E = 0 **MMBTA93**	$-I_{CBO}$ $-I_{CBO}$	– –	– –	250 250	nA nA
Emitter-Base Cutoff Current $-V_{EB}$ = 3 V, I_C = 0	$-I_{EBO}$	–	–	100	nA
DC Current Gain $-I_C$ = 1 mA, $-V_{CE}$ = 10 V $-I_C$ = 10 mA, $-V_{CE}$ = 10 V $-I_C$ = 30 mA, $-V_{CE}$ = 10 V	h_{FE} h_{FE} h_{FE}	25 40 25	– – –	– – –	– – –
Collector-Emitter Saturation Voltage $-I_C$ = 20 mA, $-I_B$ = 2 mA	$-V_{CEsat}$	–	–	500	mV
Base-Emitter Saturation Voltage $-I_C$ = 20 mA, $-I_B$ = 2 mA	$-V_{BEsat}$	–	–	900	mV
Gain-Bandwidth Product $-I_C$ = 10 mA, $-V_{CE}$ = 20 V, f = 100 MHz	f_T	50	–	–	MHz
Collector-Base Capacitance $-V_{CB}$ = 20 V, I_E = 0, f = 1 MHz **MMBTA92** **MMBTA93**	C_{CBO} C_{CBO}	– –	– –	6 8	pF pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	430[1)]	K/W
[1)] Device on fiberglass substrate, see layout					



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

PNP Silicon Epitaxial Planar Transistors
especially suited as line switch in telephone subsets and in video output stages of TV receivers and monitors.

As complementary types, the PNP transistors MPSA42 and MPSA43 are recommended.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector-Emitter Voltage	**MPSA92** **MPSA93**	$-V_{CEO}$ $-V_{CEO}$	300 200	V V
Collector-Base Voltage	**MPSA92** **MPSA93**	$-V_{CBO}$ $-V_{CBO}$	300 200	V V
Emitter-Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	500	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65…+150	°C

[1)] Valid provided that lead are kept at ambient temperature at a distance of 2 mm from case.

Characteristics at T_{amb} = 25 °C

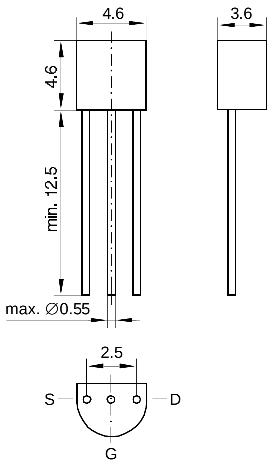
	Symbol	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage **MPSA92** $-I_C$ = 10 mA, I_B = 0 **MPSA93**	$-V_{(BR)CEO}$ $-V_{(BR)CEO}$	300 200	– –	– –	V V
Collector-Base Breakdown Voltage **MPSA92** $-I_C$ = 100 µA, I_E = 0 **MPSA93**	$-V_{(BR)CBO}$ $-V_{(BR)CBO}$	300 200	– –	– –	V V
Emitter-Base Breakdown Voltage $-I_E$ = 100 µA, I_C = 0	$-V_{(BR)EBO}$	5	–	–	V
Collector-Base Cutoff Current $-V_{CB}$ = 200 V, I_E = 0 **MPSA92** $-V_{CB}$ = 160 V, I_E = 0 **MPSA93**	$-I_{CBO}$ $-I_{CBO}$	– –	– –	250 250	nA nA
Emitter-Base Cutoff Current $-V_{EB}$ = 3 V, I_C = 0	$-I_{EBO}$	–	–	100	nA
DC Current Gain $-I_C$ = 1 mA, $-V_{CE}$ = 10 V $-I_C$ = 10 mA, $-V_{CE}$ = 10 V $-I_C$ = 30 mA, $-V_{CE}$ = 10 V	h_{FE} h_{FE} h_{FE}	25 40 25	– – –	– – –	– – –
Collector-Emitter Saturation Voltage $-I_C$ = 20 mA, $-I_B$ = 2 mA	$-V_{CEsat}$	–	–	500	mV
Base-Emitter Saturation Voltage $-I_C$ = 20 mA, $-I_B$ = 2 mA	$-V_{BEsat}$	–	–	900	mV
Gain-Bandwidth Product $-I_C$ = 10 mA, $-V_{CE}$ = 20 V, f = 100 MHz	f_T	50	–	–	MHz
Collector-Base Capacitance $-V_{CB}$ = 20 V, I_E = 0, f = 1 MHz **MPSA92** **MPSA93**	C_{CBO} C_{CBO}	– –	– –	6 8	pF pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	200[1)]	K/W
[1)] Valid provided that lead are kept at ambient temperature at a distance of 2 mm from case.					

DMOS Transistors (N-Channel)

N-Channel Enhancement Mode DMOS Transistor

Features

– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGS}	60	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	I_D	300	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	830[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.			

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	500	mA
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.5 A, T_j = 25 °C	V_F	850	mV

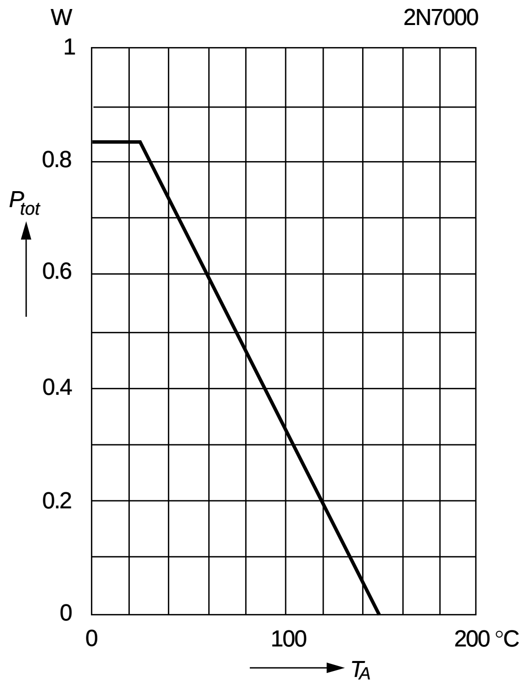
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0 V	$V_{(BR)DSS}$	60	90	–	V
Gate-Body Leakage Current, Forward at V_{GSF} = 20 V, V_{DS} = 0 V	I_{GSSF}	–	–	10	nA
Gate-Body Leakage Current, Reverse at V_{GSR} = –20 V, V_{DS} = 0 V	I_{GSSR}	–	–	–10	nA
Drain Cutoff Current at V_{DS} = 48 V, V_{GS} = 0 V	I_{DSS}	–	–	1	µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, I_D = 1.0 mA	$V_{GS(th)}$	0.8	1.5	3	V
Drain-Source ON Resistance at V_{GS} = 10 V, I_D = 500 mA	$R_{DS(ON)}$	–	3.5	5.0	Ω
Capacitance at V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rSS}	 – – –	 60 25 5	 – – –	 pF pF pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 10 10	 – –	 ns ns
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

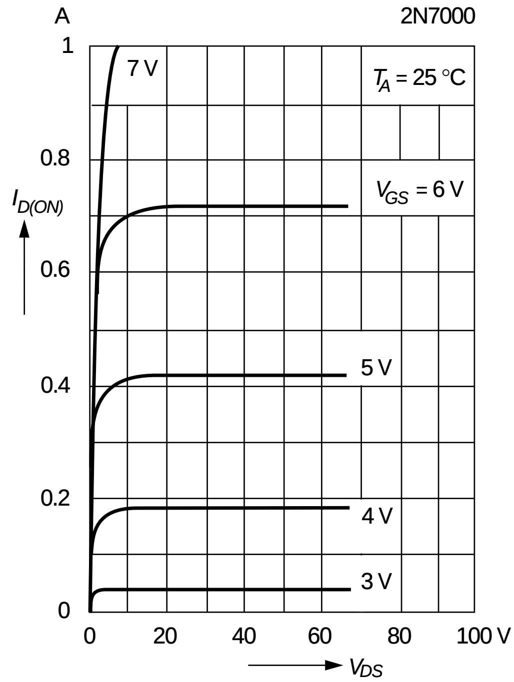
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



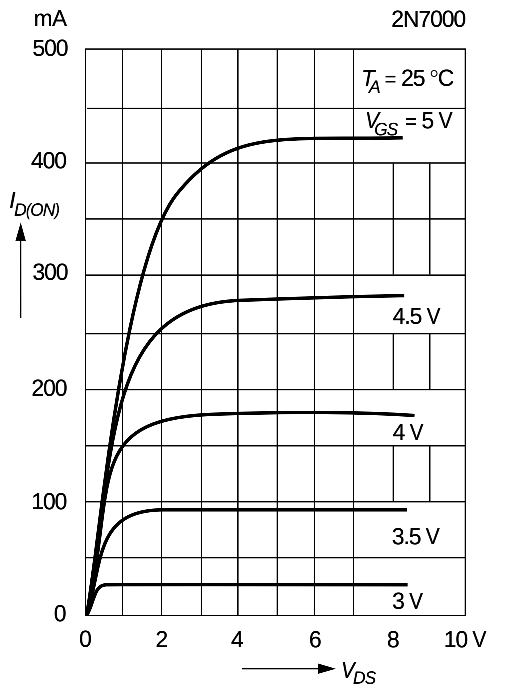
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%.

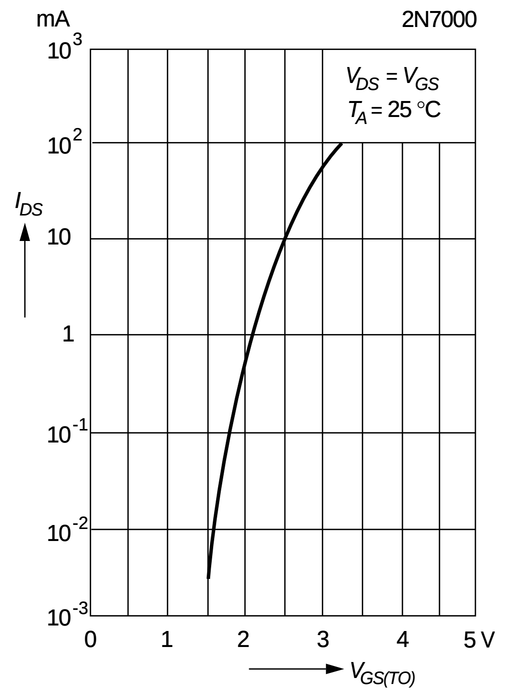


Saturation characteristics

Pulse test width 80 µs; pulse duty factor 1%.

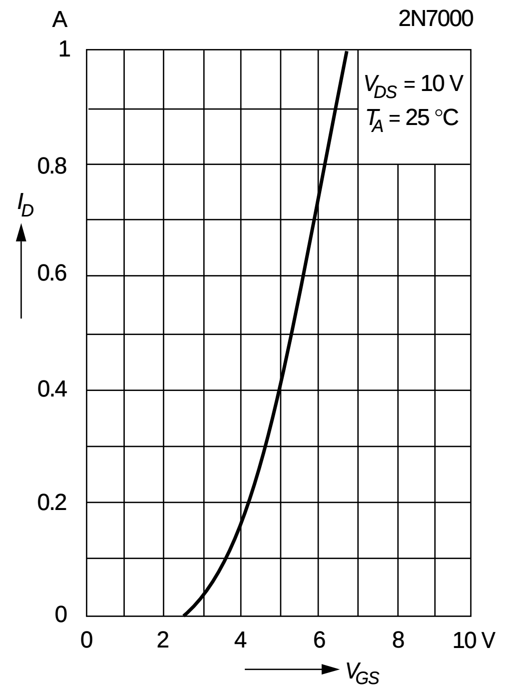


Drain-source current versus gate threshold voltage

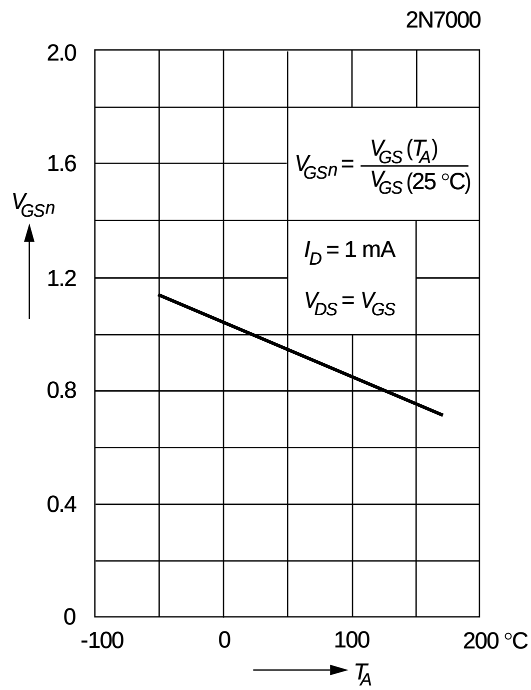


Drain current versus gate-source voltage

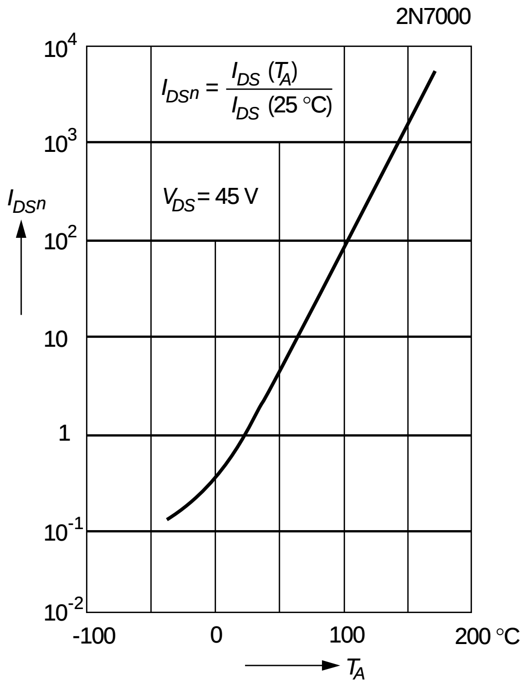
Pulse test width 80 µs; pulse duty factor 1%.



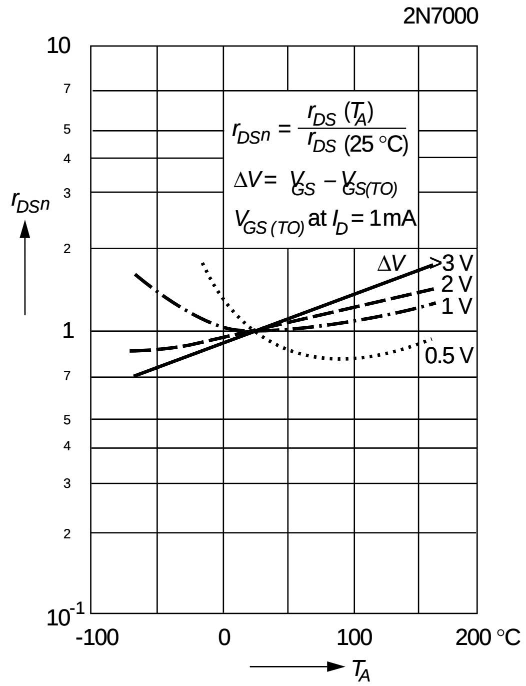
Normalized gate-source voltage versus temperature



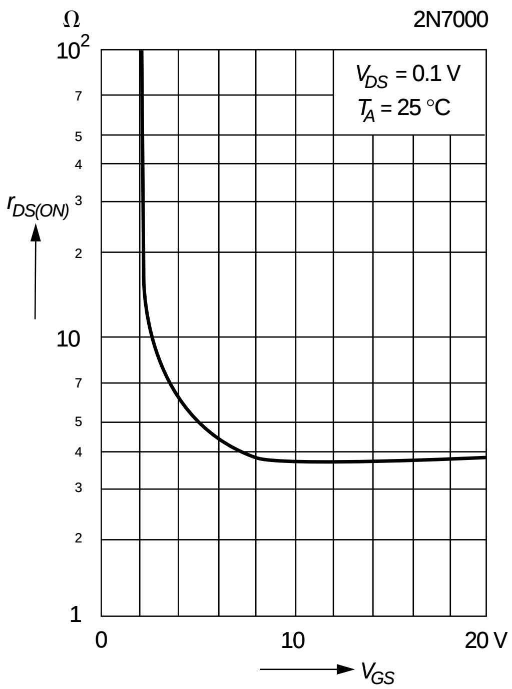
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

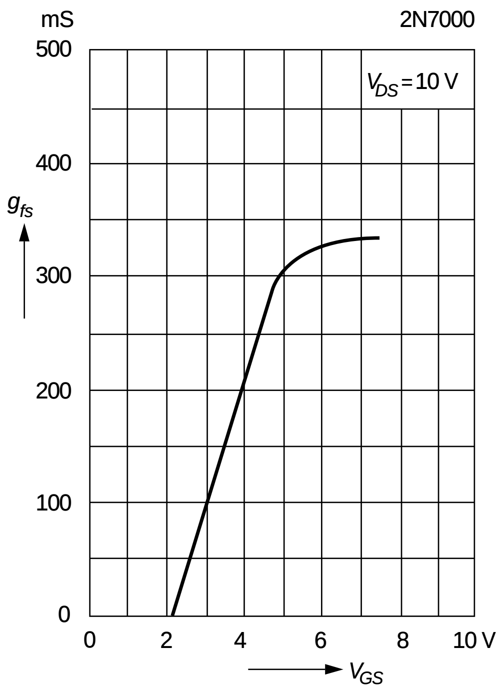


Drain-source resistance versus gate-source voltage



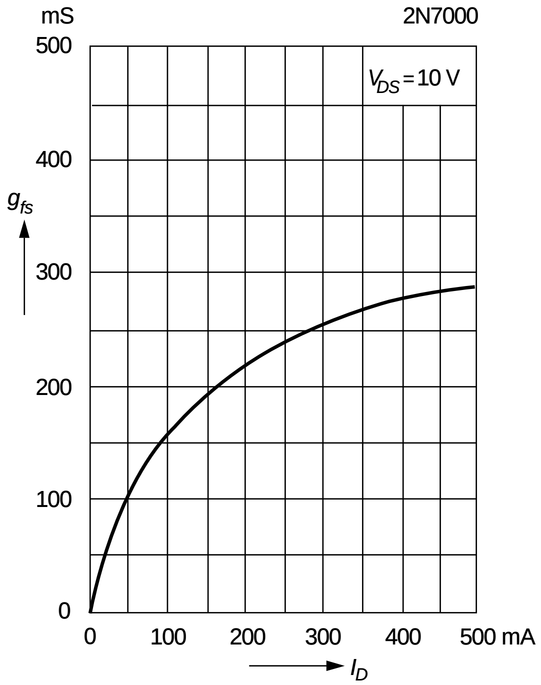
Transconductance versus gate-source voltage

Pulse test width 80 µs; pulse duty factor 1%

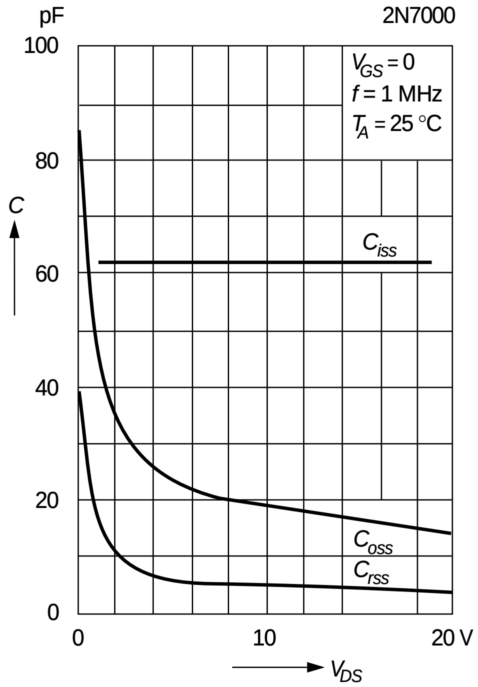


Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%



Capacitance versus drain-source voltage



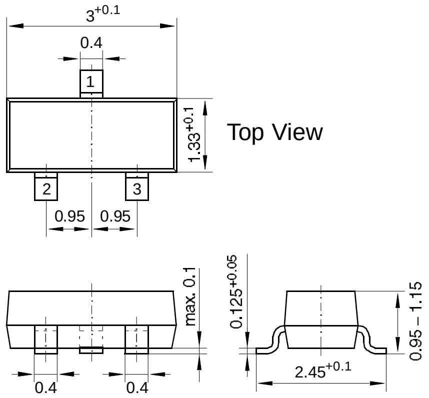
2N7002

N-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

Pin configuration
1 = Drain, 2 = Gate, 3 = Source.

Marking
S72



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGS}	60	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	I_D	250	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	0.310[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C
[1)] Device on fiberglass substrate, see layout			

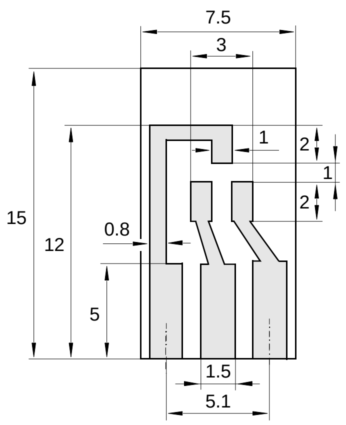
Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.3	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.3 A, T_j = 25 °C	V_F	0.85	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0	$V_{(BR)DSS}$	60	90	–	V
Gate Threshold Voltage at V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(TO)}$	–	2	2.5	V
Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0	I_{GSS}	–	–	10	nA
Drain Cutoff Current at V_{DS} = 25 V, V_{GS} = 0	I_{DSS}	–	–	0.5	µA
Drain-Source ON Resistance at V_{GS} = 10 V, I_D = 500 mA	$r_{DS(ON)}$	–	5	7.5	Ω
Thermal Resistance Junction to Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Forward Transconductance at V_{DS} = 10 V, I_D = 200 mA, f = 1 MHz	g_m	–	200	–	mS
Input Capacitance at V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	C_{iss}	–	60	–	pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 5 25	 – –	 ns ns

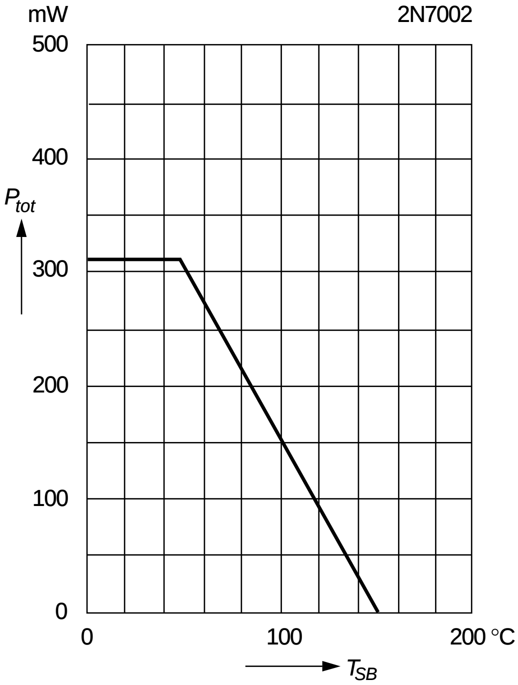
[1)] Device on fiberglass substrate, see layout



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

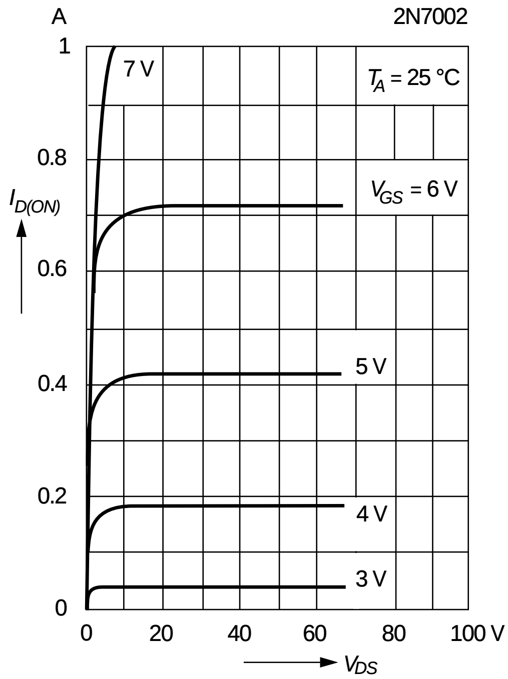
Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout



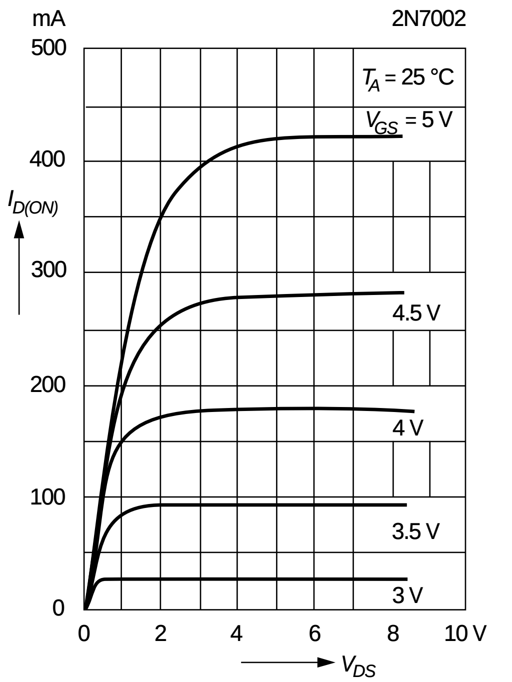
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%.

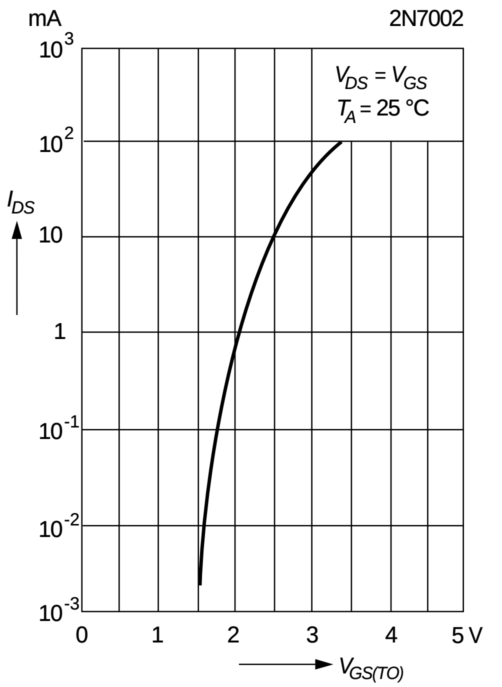


Saturation characteristics

Pulse test width 80 µs; pulse duty factor 1%.

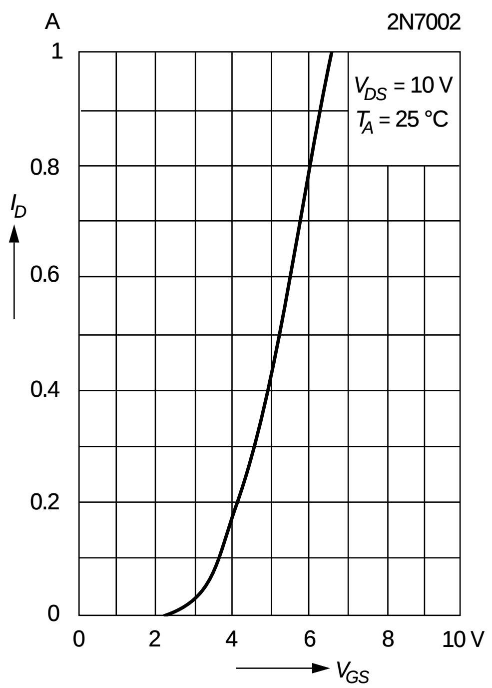


Drain-source current versus gate threshold voltage

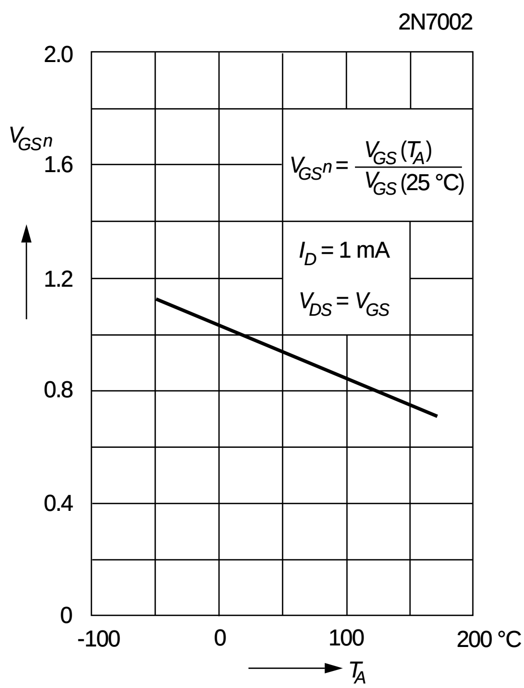


Drain current versus gate-source voltage

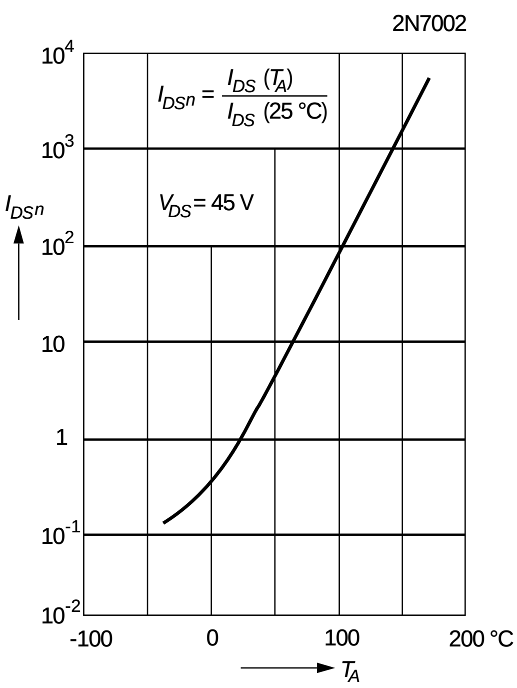
Pulse test width 80 µs; pulse duty factor 1%.



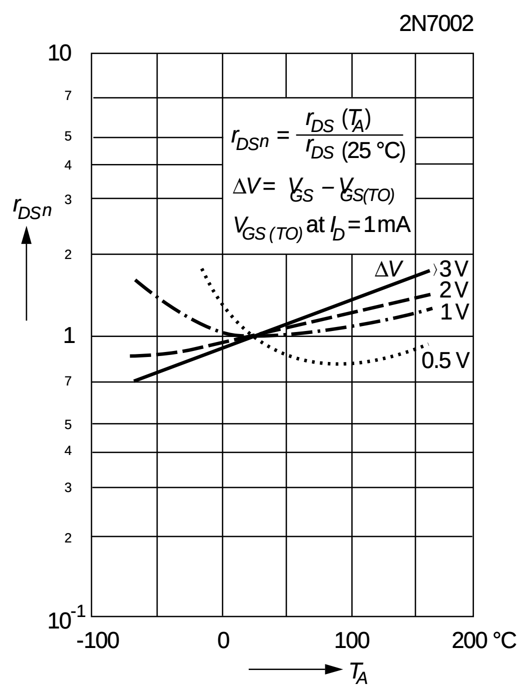
Normalized gate-source voltage versus temperature



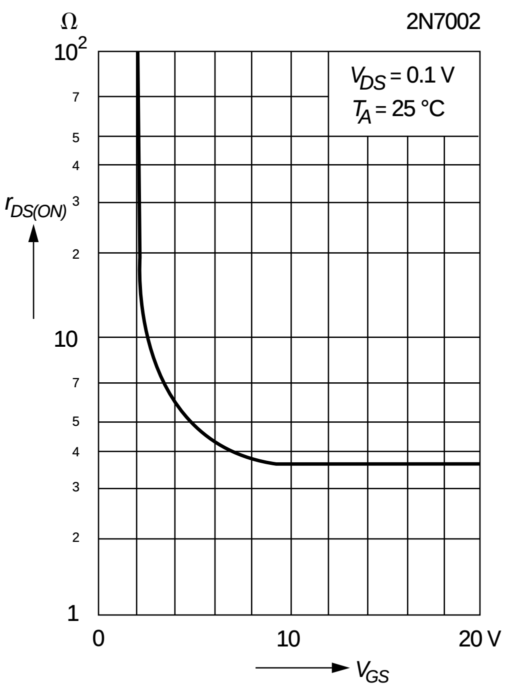
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

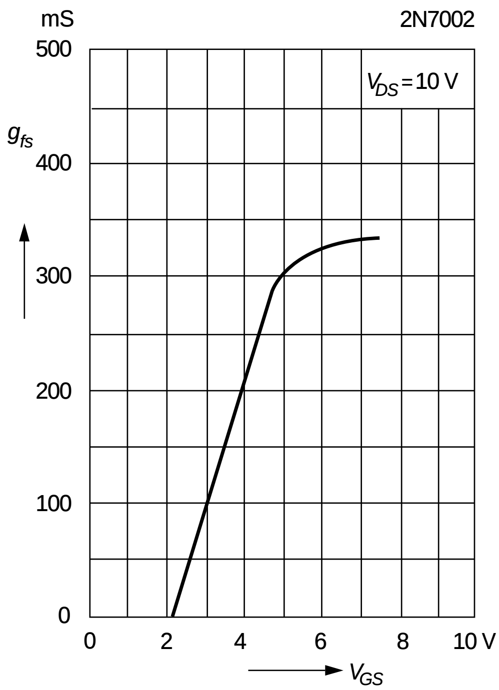


Drain-source resistance versus gate-source voltage



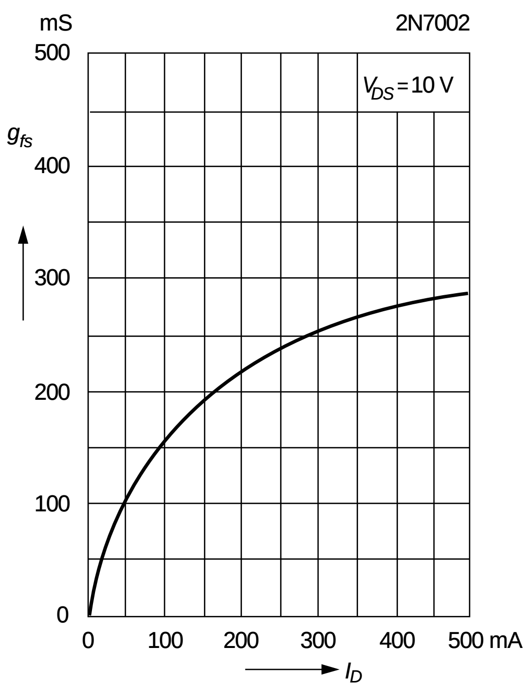
Transconductance versus gate-source voltage

Pulse test width 80 µs; pulse duty factor 1%

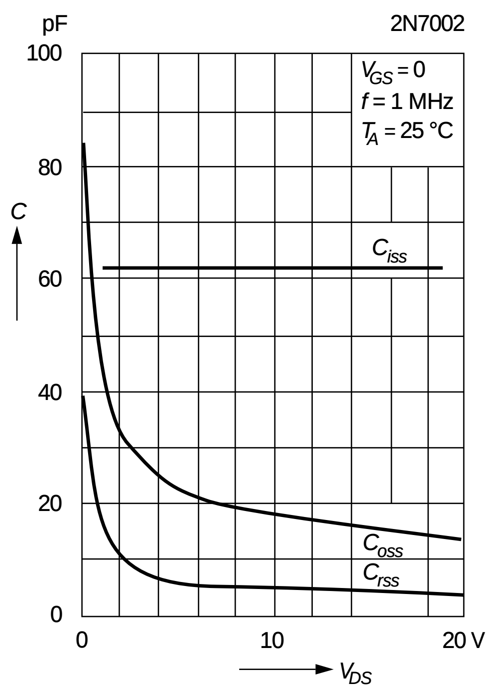


Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%



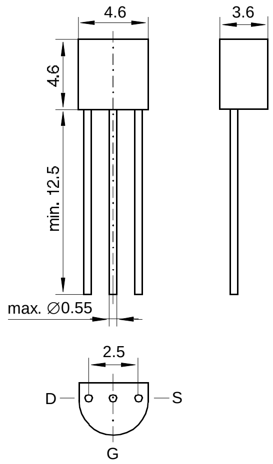
Capacitance versus drain-source voltage



N-Channel Enhancement Mode DMOS Transistor

Features
– high breakdown voltage
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown
– specially suited for telephone subsets

On special request, this transistor is also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	240	V
Drain-Gate Voltage	V_{DGS}	240	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous)	I_D	230	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Inverse Diode

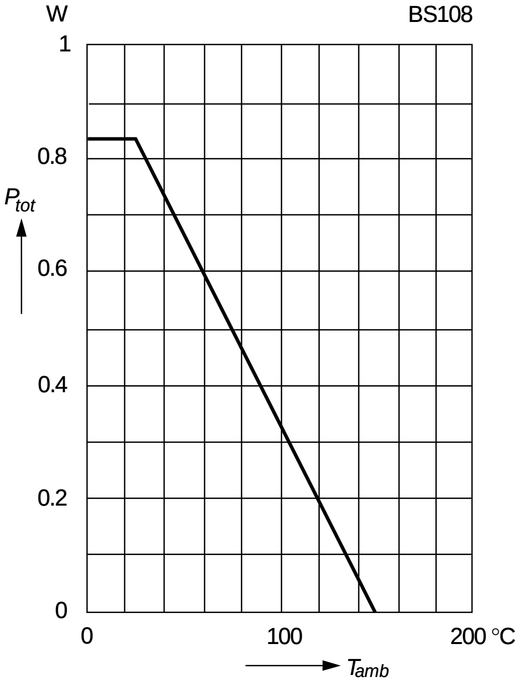
	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.75	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0	$V_{(BR)DSS}$	240	250	–	V
Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0	I_{GSS}	–	–	10	nA
Drain Cutoff Current at V_{DS} = 130 V, V_{GS} = 0 at V_{DS} = 70 V, V_{GS} = 0.2 V	 I_{DSS} I_{DSX}	 – –	 – –	 1 25	 µA µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(TO)}$	0.8	1.5	2.5	V
Drain-Source ON Resistance at V_{GS} = 2.8 V, I_D = 100 mA	$R_{DS(ON)}$	–	5.5	8	Ω
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
Capacitance at V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rSS}	 – – –	 80 20 5	 – – –	 pF pF pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 5 50	 – –	 ns ns
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case					

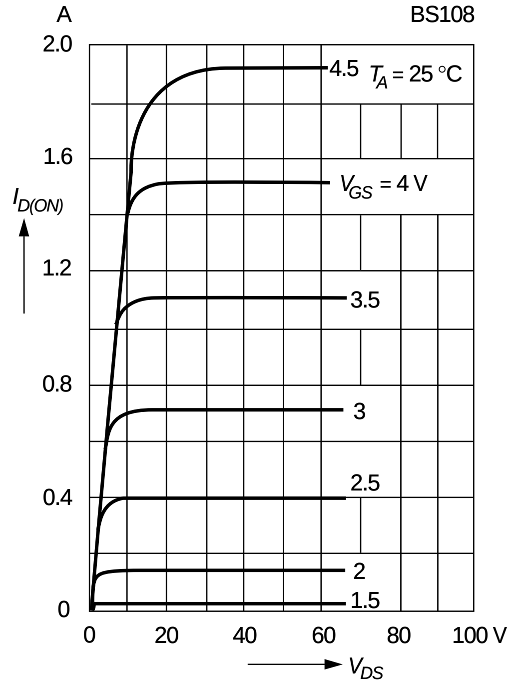
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



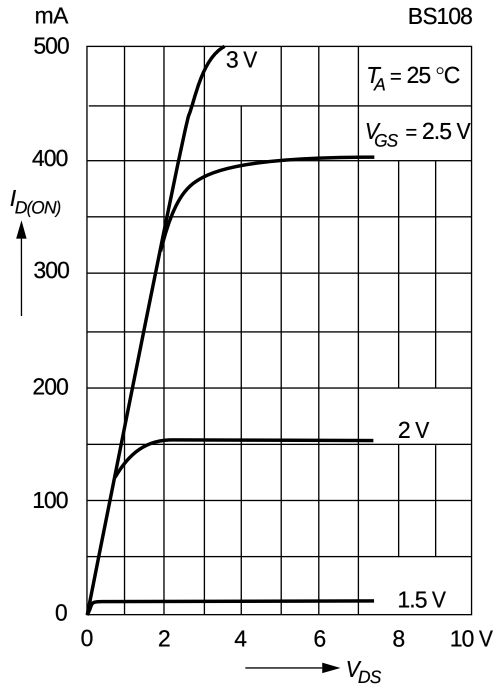
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%

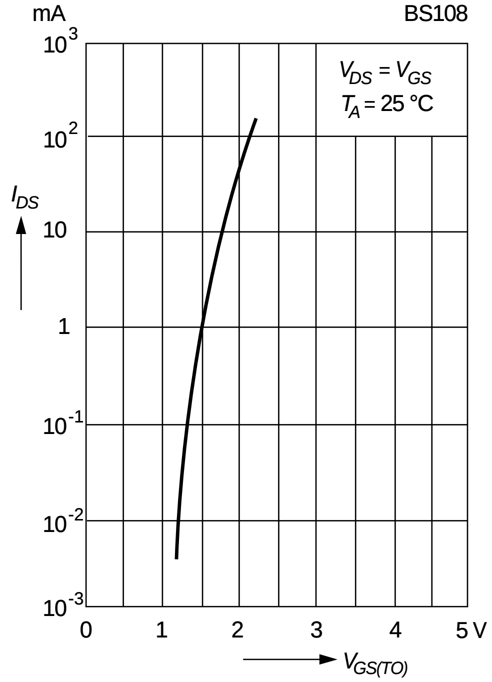


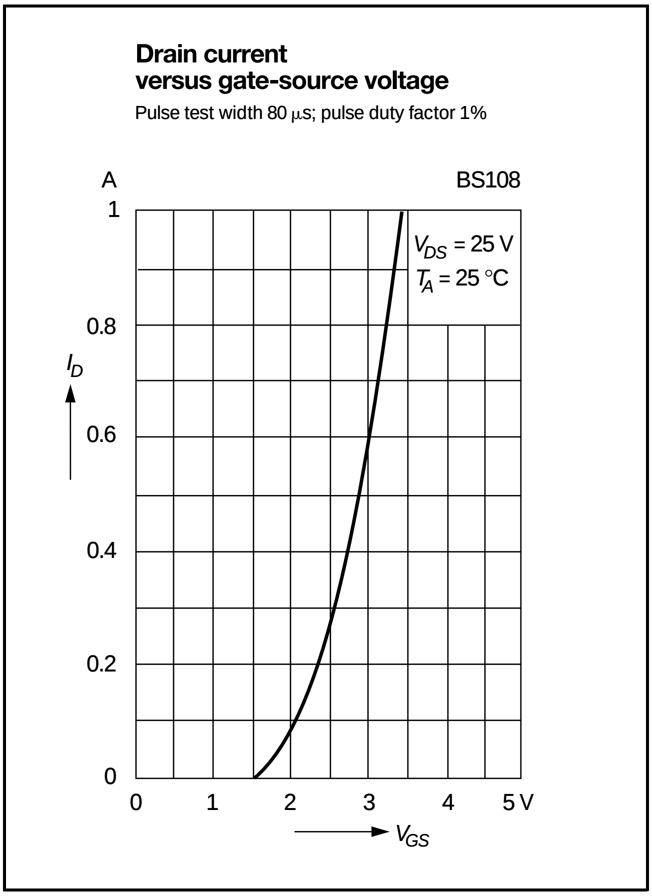
Saturation characteristics

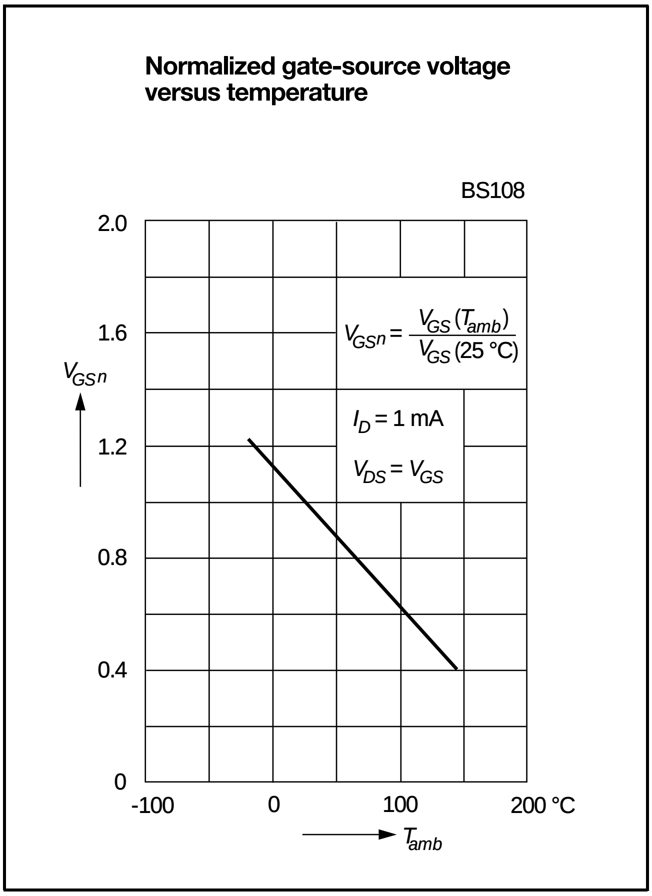
Pulse test width 80 µs; pulse duty factor 1%

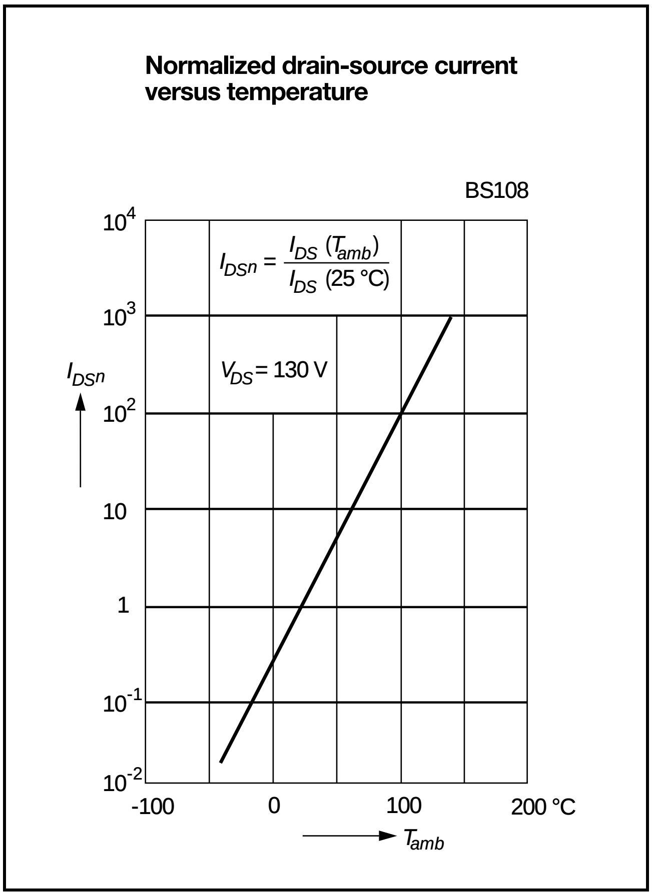


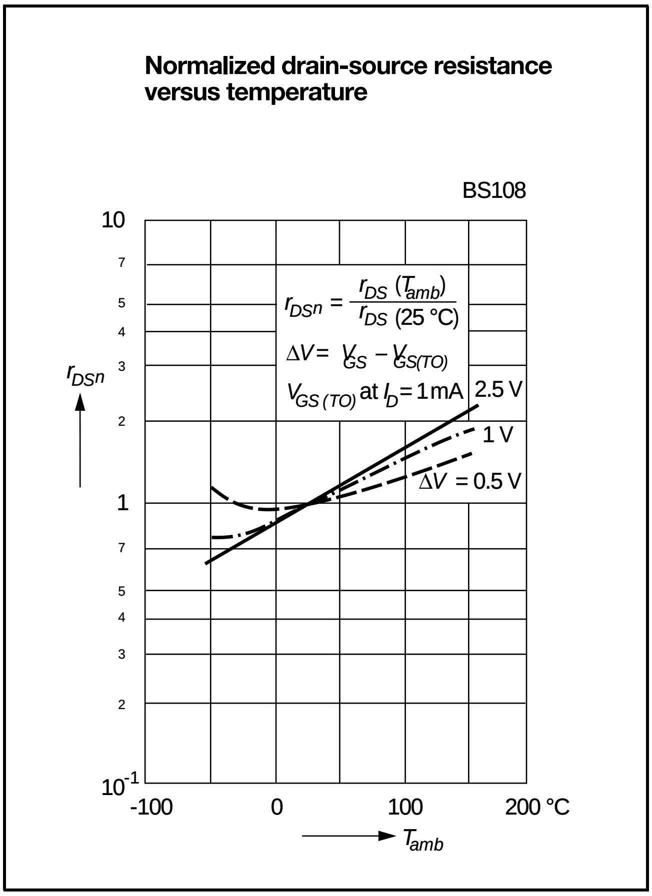
Drain-source current versus gate threshold voltage



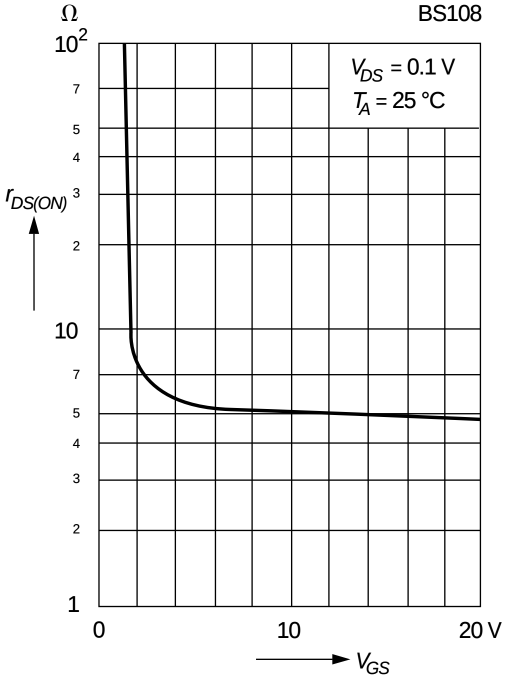

Drain current
versus gate-source voltage
Pulse test width 80 µs; pulse duty factor 1%
A
BS108
V_{DS} = 25 V
T_A = 25 °C
I_D
V_{GS}
0 1 2 3 4 5 V
0 0.2 0.4 0.6 0.8 1


Normalized gate-source voltage
versus temperature
BS108
$V_{GSn} = \frac{V_{GS}(T_{amb})}{V_{GS}(25\ °C)}$
I_D = 1 mA
$V_{DS} = V_{GS}$
V_{GSn}
T_{amb}
-100 0 100 200 °C
0 0.4 0.8 1.2 1.6 2.0


Normalized drain-source current
versus temperature
BS108
$I_{DSn} = \frac{I_{DS}(T_{amb})}{I_{DS}(25\ °C)}$
V_{DS} = 130 V
I_{DSn}
T_{amb}
-100 0 100 200 °C
10^{-2} 10^{-1} 1 10 10^2 10^3 10^4

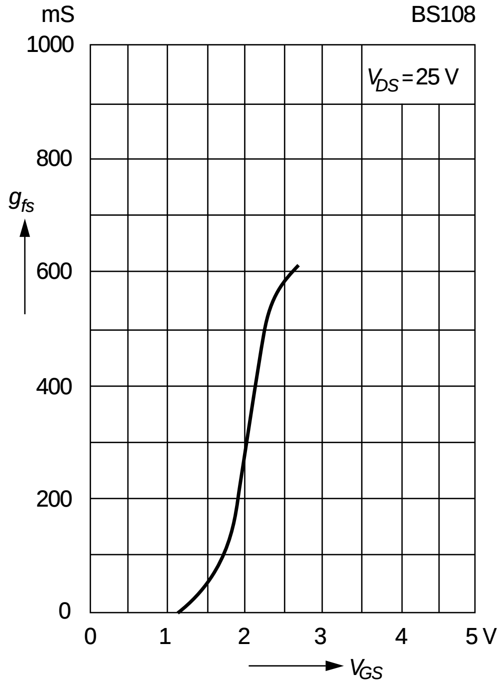

Normalized drain-source resistance
versus temperature
BS108
$r_{DSn} = \frac{r_{DS}(T_{amb})}{r_{DS}(25\ °C)}$
$\Delta V = V_{GS} - V_{GS(TO)}$
$V_{GS(TO)}$ at I_D = 1 mA
2.5 V
1 V
ΔV = 0.5 V
r_{DSn}
T_{amb}
-100 0 100 200 °C
10^{-1} 2 3 4 5 7 1 2 3 4 5 7 10

Drain-source resistance versus gate-source voltage



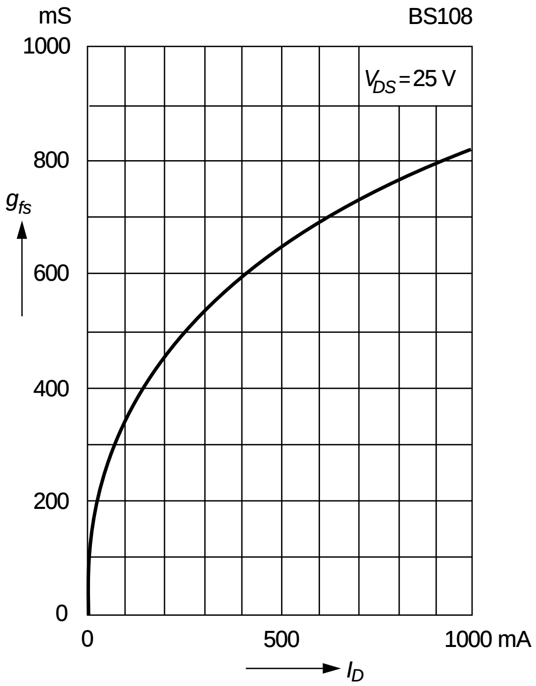
Transconductance versus gate-source voltage

Pulse test width 80 µs; pulse duty factor 1%



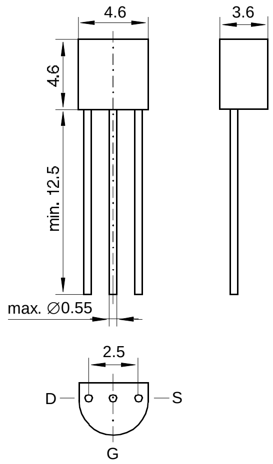
Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%



N-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	400	V
Drain-Gate Voltage	V_{DGS}	400	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous) at T_{amb} = 25 °C	I_D	120	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	830[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.			

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	400	mA
Forward Voltage Drop (typ.) at V_{GS} = 0 V, I_F = 400 mA, T_j = 25 °C	V_F	1.0	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0 V	$V_{(BR)DSS}$	400	430	–	V
Gate-Body Leakage Current, Forward at V_{GSF} = 20 V, V_{DS} = 0 V	I_{GSSF}	–	–	100	nA
Gate-Body Leakage Current, Reverse at V_{GSR} = 20 V, V_{DS} = 0 V	I_{GSSR}	–	–	100	nA
Drain Cutoff Current at V_{DS} = 400 V, V_{GS} = 0 V	I_{DSS}	–	–	500	nA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, I_D = 250 µA	$V_{GS(th)}$	1	1.5	2.5	V
Drain-Source ON Resistance at V_{GS} = 10 V, I_D = 120 mA	$R_{DS(on)}$	–	16	22	Ω
Capacitance at V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rSS}	 – – –	 80 20 10	 – – –	 pF pF pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 10 50	 – –	 ns ns
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

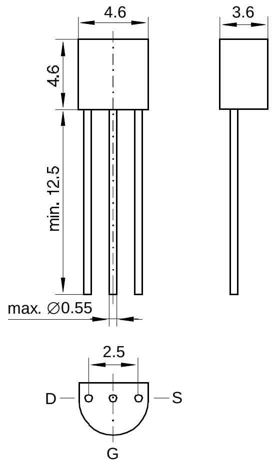
N-Channel Enhancement Mode DMOS Transistors

Features
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

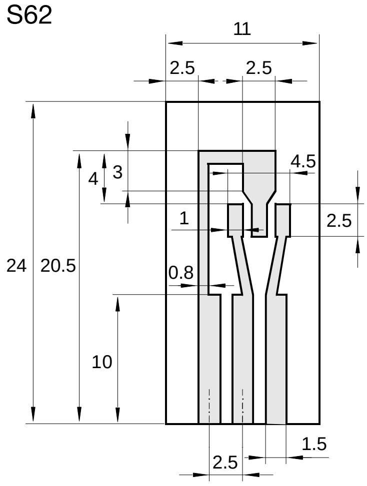
Packages
– TO-92 (BS123)
– SOT-89A (BS623)

Pin configuration (BS623)
1 = Source, 2 = Gate, 3 = Drain

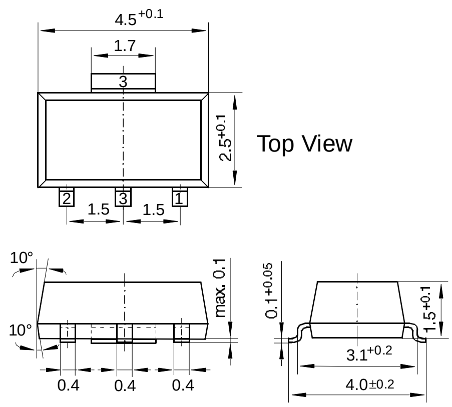
Marking (BS623)
S62



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm



SOT-89A Plastic Package
Weight approx. 0.04 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGS}	60	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous) at T_{amb}[1] = 25 °C, at T_{SB}[2] = 50 °C	I_D	1.1	A
Power Dissipation at T_{amb}[1] = 25 °C, at T_{SB}[2] = 50 °C	P_{tot}	830[1], 600[2]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case (for TO-92).
[2] Device on fiberglass substrate, see layout (for SOT-89A).

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	1.1	A
Forward Voltage Drop (typ.) at V_{GS} = 0 V, I_F = 1.1 A, T_j = 25 °C	V_F	1	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0 V	$V_{(BR)DSS}$	60	80	–	V
Gate-Body Leakage Current, Forward at V_{GSF} = 20 V, V_{DS} = 0 V	I_{GSSF}	–	–	500	nA
Gate-Body Leakage Current, Reverse at V_{GSR} = 20 V, V_{DS} = 0 V	I_{GSSR}	–	–	500	nA
Drain Cutoff Current at V_{DS} = 60 V, V_{GS} = 0 V	I_{DSS}	–	–	250	µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, I_D = 250 µA	$V_{GS(th)}$	1	1.5	3	V
Drain-Source ON Resistance at V_{GS} = 10 V, I_D = 600 mA	$R_{DS(on)}$	–	0.3	0.4	Ω
Capacitance at V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz					
Input Capacitance	C_{iSS}	–	350	–	pF
Output Capacitance	C_{OSS}	–	150	–	pF
Feedback Capacitance	C_{rSS}	–	35	–	pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω					
Turn-On Time	t_{on}	–	40	–	ns
Turn-Off Time	t_{off}	–	100	–	ns
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
	R_{thA}	–	–	200[2)]	K/W

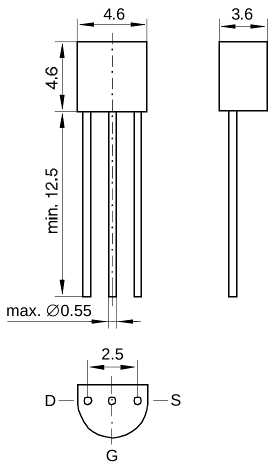
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case (for TO-92).
[2)] Device on fiberglass substrate, see layout (for SOT-89A).

N-Channel Enhancement Mode DMOS Transistor

Features

– high input impedance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

On special request, this transistor is also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGS}	60	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	I_D	300	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.			

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.5	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.5 A, T_j = 25 °C	V_F	0.85	V

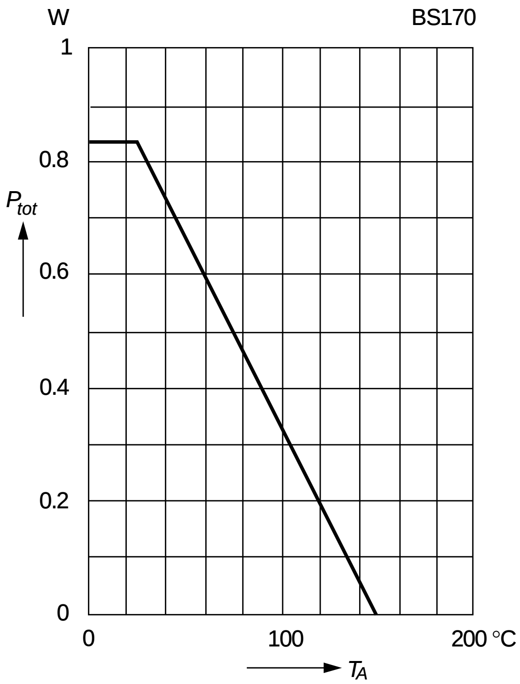
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0	$V_{(BR)DSS}$	60	80	–	V
Gate Threshold Voltage at V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(TO)}$	1.0	2	3.0	V
Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0	I_{GSS}	–	–	10	nA
Drain Cutoff Current at V_{DS} = 25 V, V_{GS} = 0	I_{DSS}	–	–	0.5	µA
Drain-Source ON Resistance at V_{GS} = 10 V, I_D = 0.2 A	$r_{DS(ON)}$	–	3.5	5.0	Ω
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
Forward Transconductance at V_{DS} = 10 V, I_D = 0.2 A, f = 1 MHz	g_m	–	200	–	mS
Input Capacitance at V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	C_{iss}	–	30	–	pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω					
Turn-On Time	t_{on}	–	5	–	ns
Turn-Off Time	t_{off}	–	15	–	ns

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

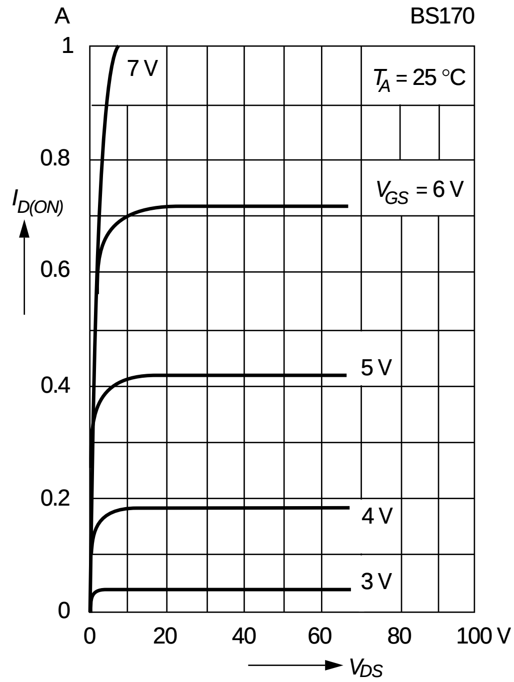
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



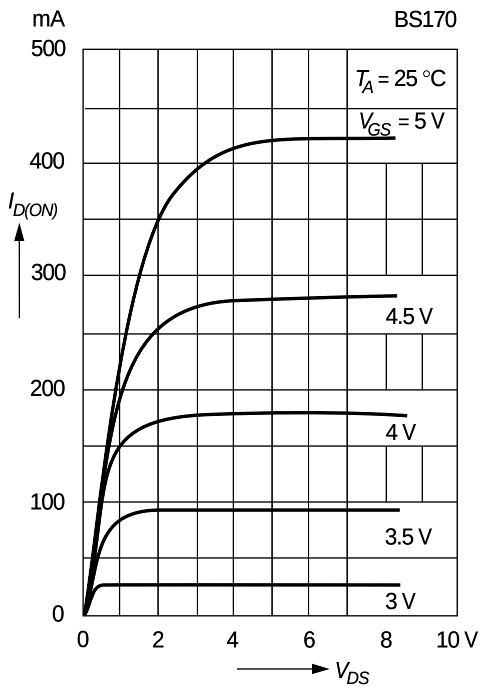
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%

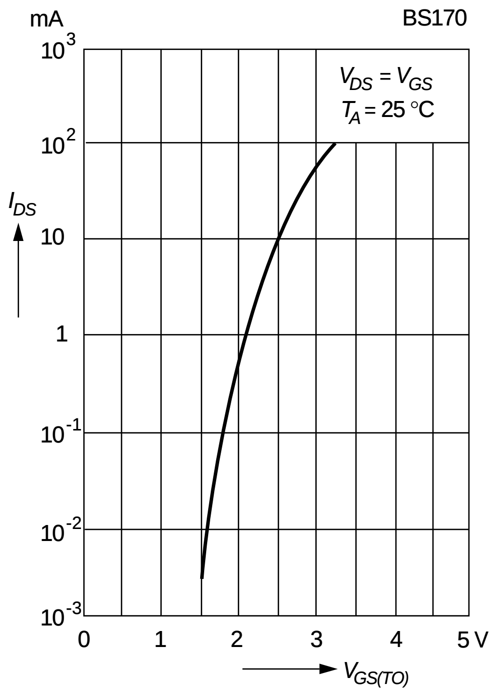


Saturation characteristics

Pulse test width 80 µs; pulse duty factor 1%

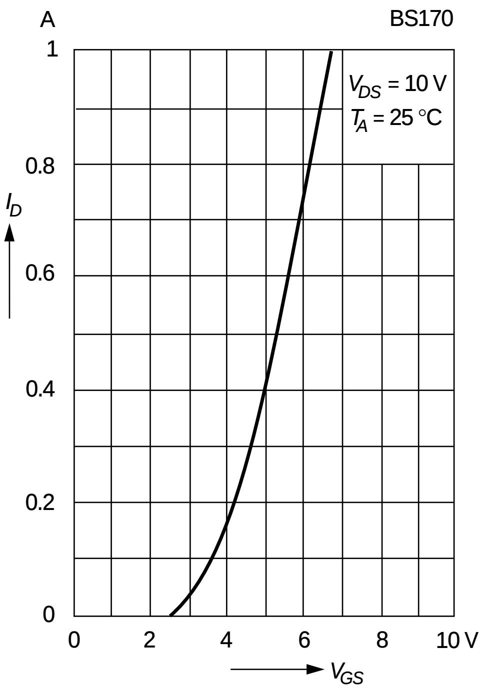


Drain-source current versus gate threshold voltage

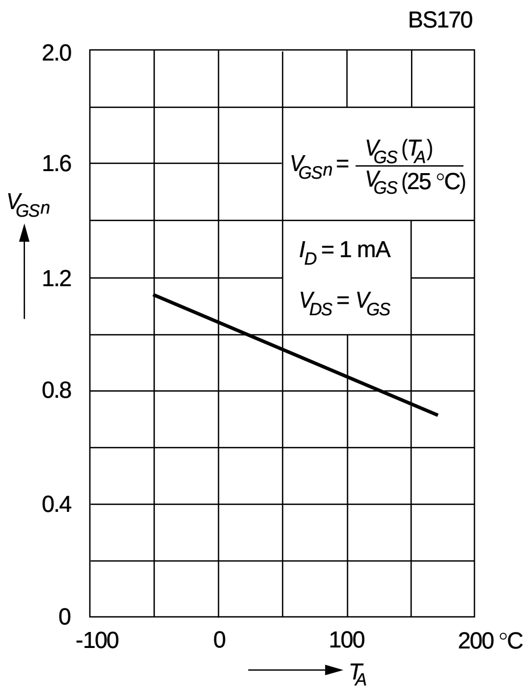


Drain current versus gate-source voltage

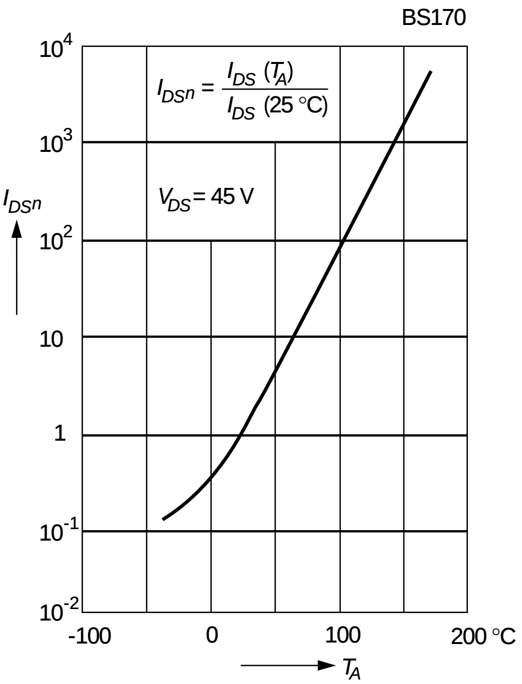
Pulse test width 80 µs; pulse duty factor 1%



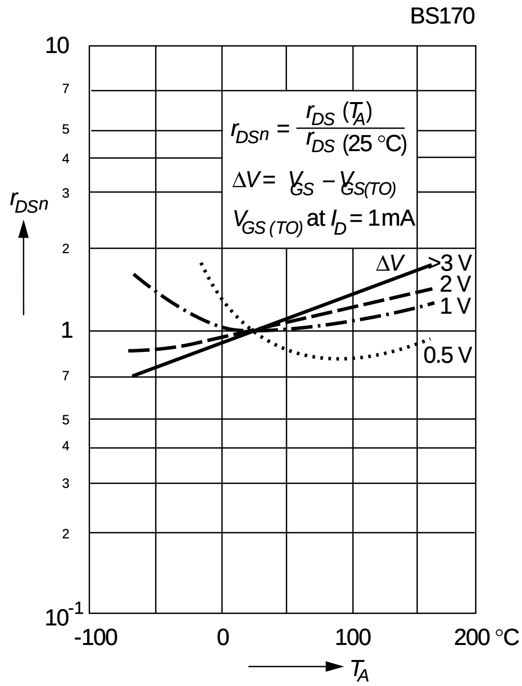
Normalized gate-source voltage versus temperature



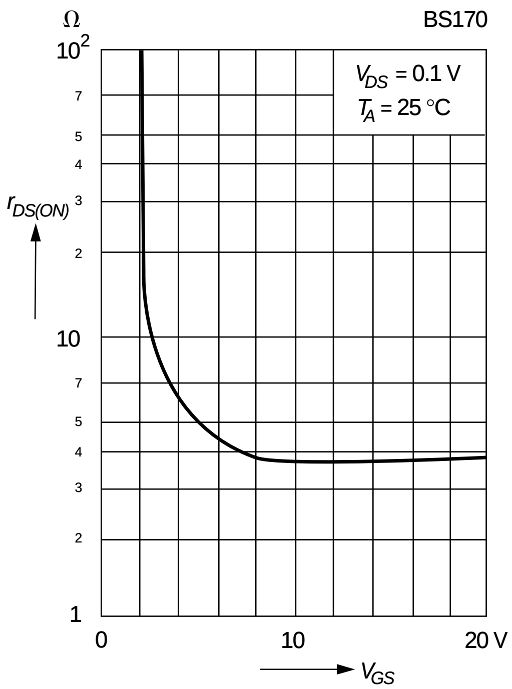
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

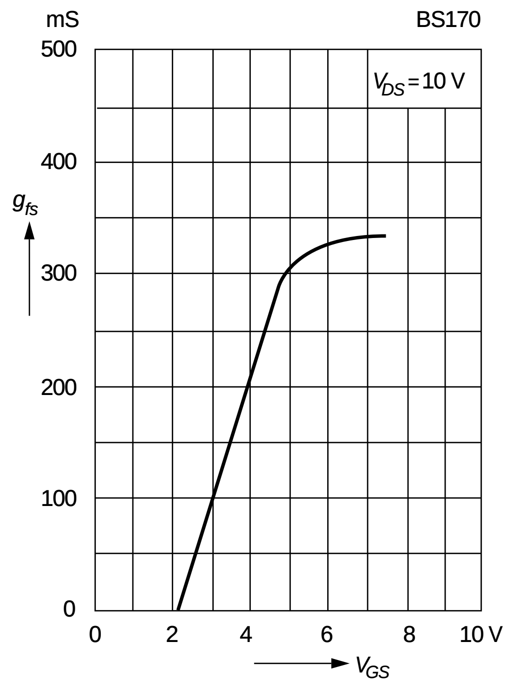


Drain-source resistance versus gate-source voltage



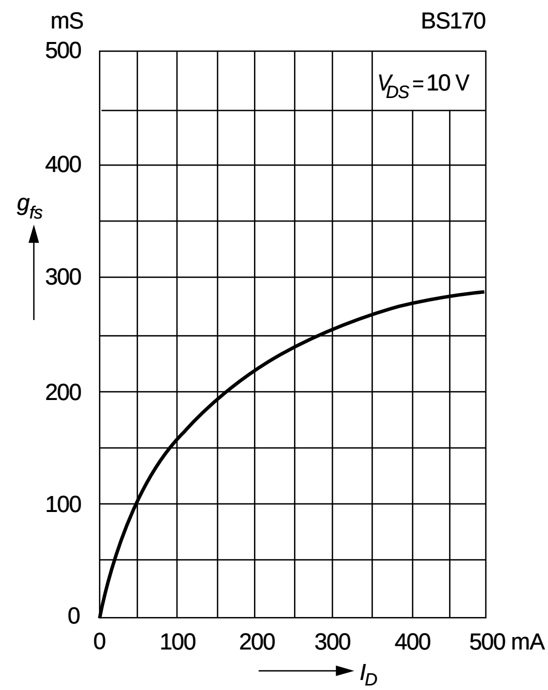
Transconductance versus gate-source voltage

Pulse test width 80 µs; pulse duty factor 1%

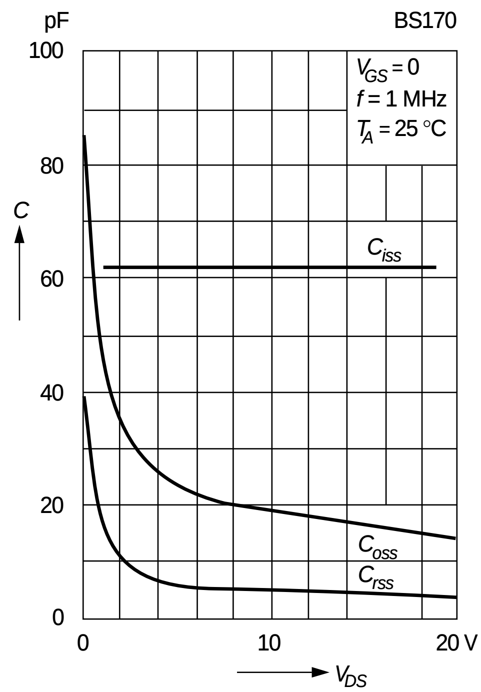


Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%



Capacitance versus drain-source voltage

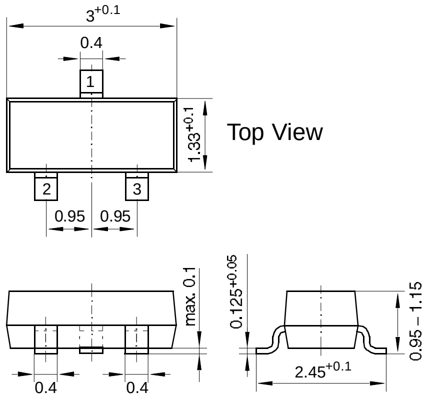


N-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

Pin Configuration
1 = Drain, 2 = Gate, 3 = Source

Marking
S09



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	400	V
Drain-Gate Voltage	V_{DGS}	400	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous) at T_{SB} = 50 °C	I_D	100	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	310[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C
[1)] Device on fiberglass substrate, see layout			

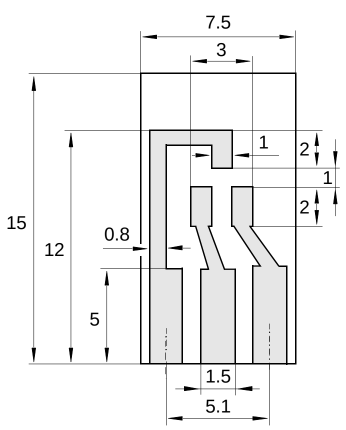
Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	300	mA
Forward Voltage Drop (typ.) at V_{GS} = 0 V, I_F = 300 mA, T_j = 25 °C	V_F	1.0	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0 V	$V_{(BR)DSS}$	400	430	–	V
Gate-Body Leakage Current, Forward at V_{GSF} = 20 V, V_{DS} = 0 V	I_{GSSF}	–	–	100	nA
Gate-Body Leakage Current, Reverse at V_{GSR} = 20 V, V_{DS} = 0 V	I_{GSSR}	–	–	100	nA
Drain Cutoff Current at V_{DS} = 400 V, V_{GS} = 0 V	I_{DSS}	–	–	500	nA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, I_D = 250 µA	$V_{GS(th)}$	1	1.5	2.5	V
Drain-Source ON Resistance at V_{GS} = 5 V, I_D = 100 mA	$R_{DS(on)}$	–	18	22	Ω
Capacitances at V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rS}	 – – –	 80 20 10	 – – –	 pF pF pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 10 50	 – –	 ns ns
Thermal Resistance Junction to Substrate Backside	R_{thSB}			320[1)]	
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W

[1)] Device on fiberglass substrate, see layout



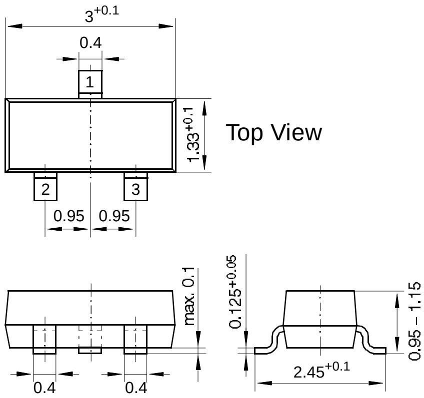
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

N-Channel Enhancement Mode DMOS Transistor

Features
– high breakdown voltage
– high input impedance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown
– specially suited for telephone subsets

Pin configuration
1 = Drain, 2 = Gate, 3 = Source.

Marking
S28



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

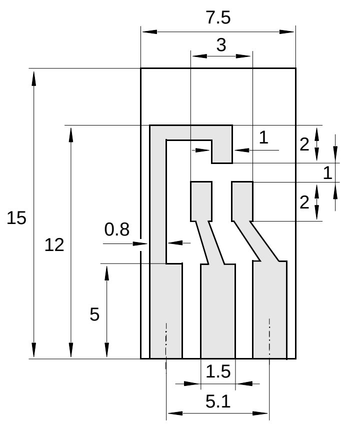
	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	240	V
Drain-Gate Voltage	V_{DGS}	240	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	I_D	230	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	0.310[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C
[1)] Device on fiberglass substrate, see layout			

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.3	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.3 A, T_j = 25 °C	V_F	0.85	V

Characteristics at T_{amb} = 25 °C

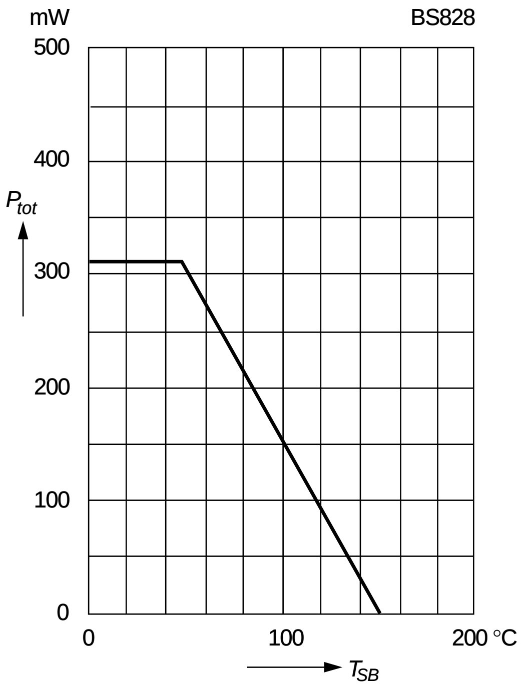
	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0	$V_{(BR)DSS}$	240	250	–	V
Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0	I_{GSS}	–	–	10	nA
Drain Cutoff Current at V_{DS} = 130 V, V_{GS} = 0 at V_{DS} = 70 V, V_{GS} = 0.2 V	 I_{DSS} I_{DSX}	 – –	 – –	 1 25	 µA µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(TO)}$	–	1.5	2.5	V
Drain-Source ON Resistance at V_{GS} = 2.8 V, I_D = 100 mA	$r_{DS(ON)}$	–	5.5	8	Ω
Thermal Resistance Junction to Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Capacitances at V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 80 20 5	 – – –	 pF pF pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 5 50	 – –	 ns ns
[1)] Device on fiberglass substrate, see layout					



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

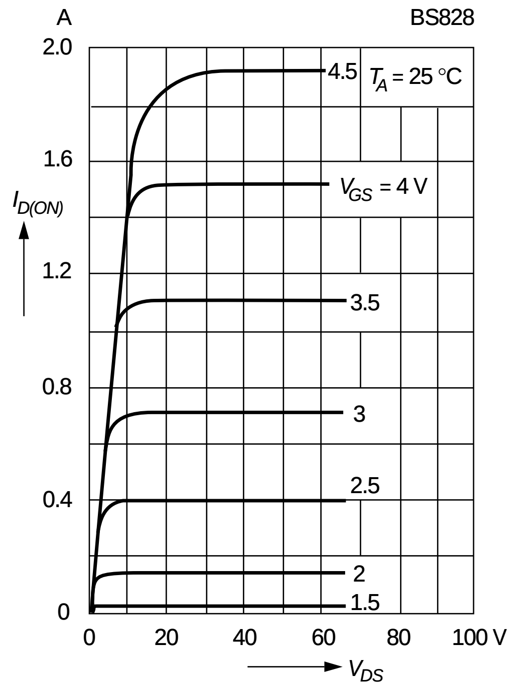
Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout



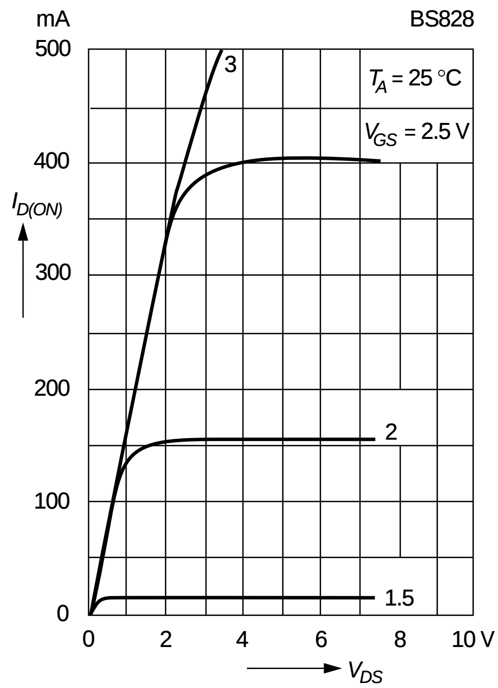
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%

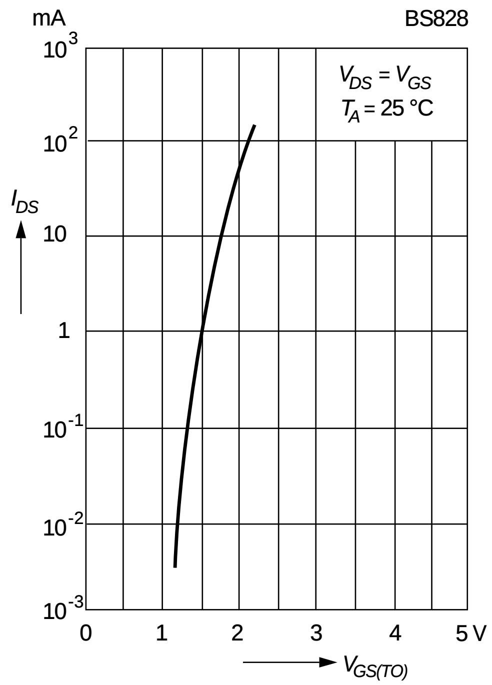


Saturation characteristics

Pulse test width 80 µs; pulse duty factor 1%

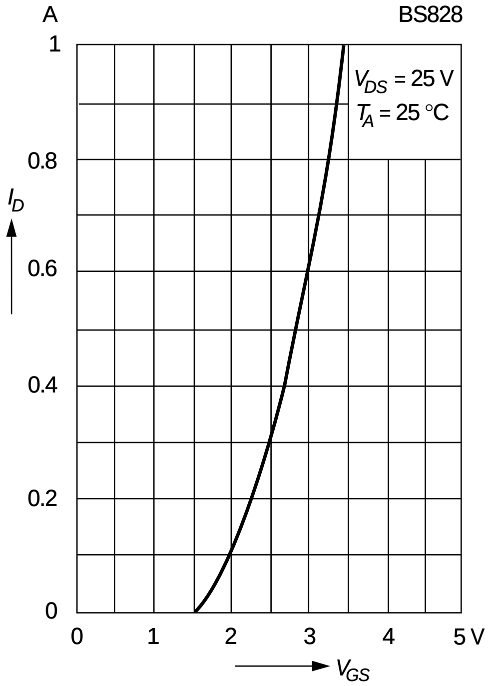


Drain-source current versus gate threshold voltage

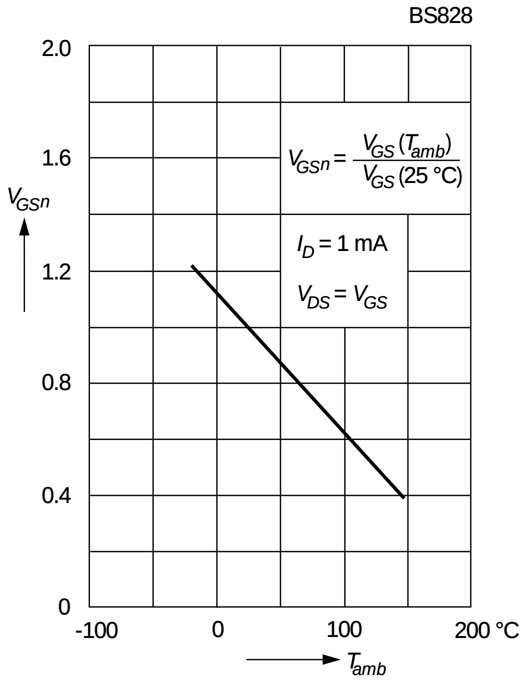


Drain current versus gate-source voltage

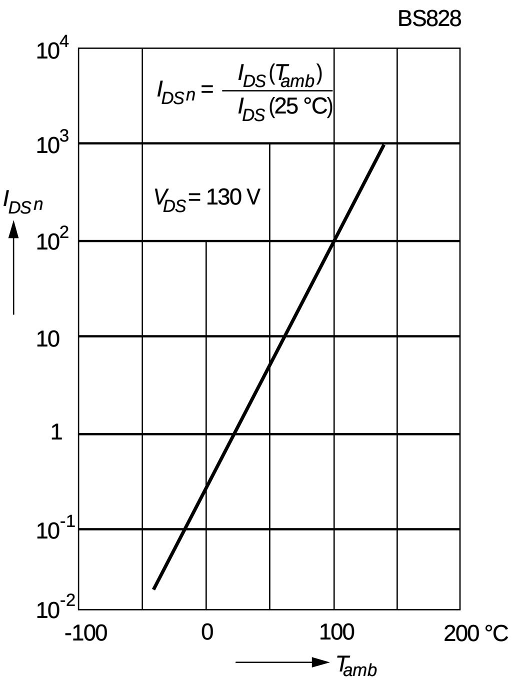
Pulse test width 80 µs; pulse duty factor 1%



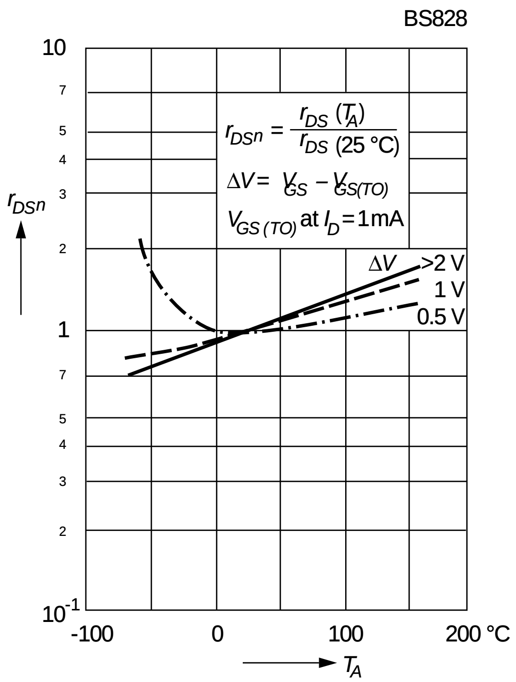
Normalized gate-source voltage versus temperature



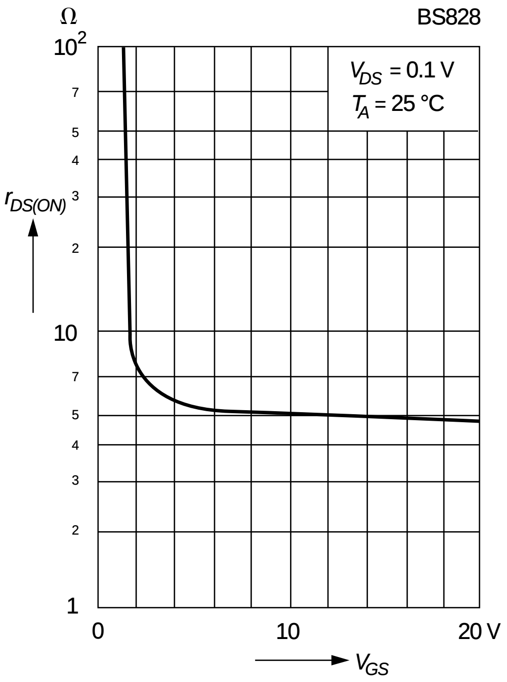
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

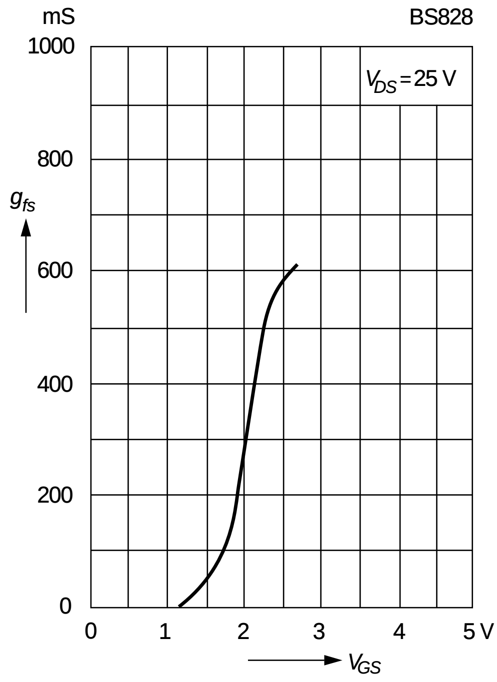


Drain-source resistance versus gate-source voltage



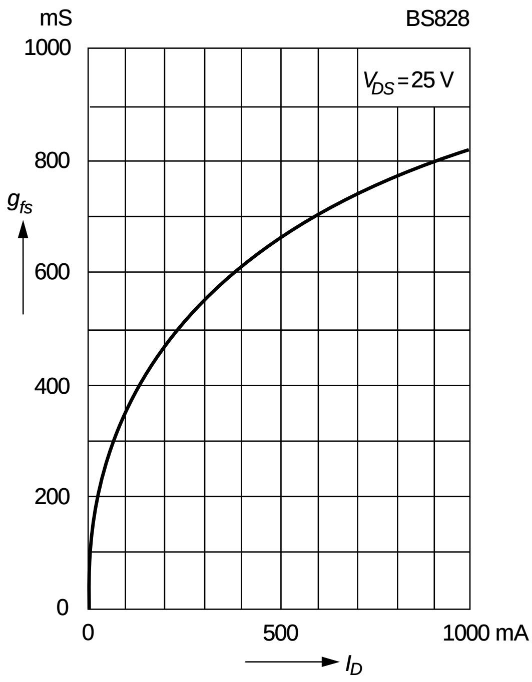
Transconductance versus gate-source voltage

Pulse test width 80 µs; pulse duty factor 1%



Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%

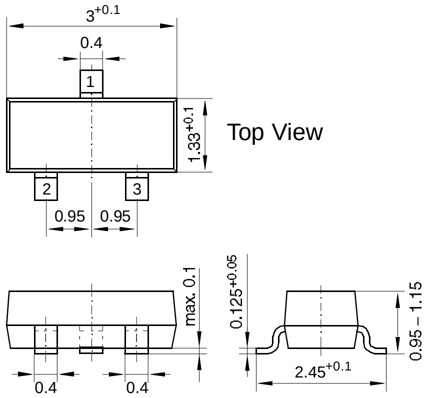


N-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

Pin configuration
1 = Drain, 2 = Gate, 3 = Source.

Marking
S70



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGS}	60	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	I_D	250	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	0.310[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C
[1)] Device on fiberglass substrate, see layout			

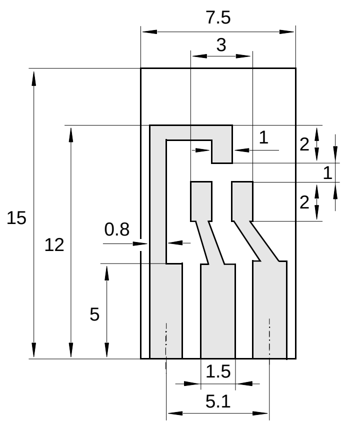
Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.3	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.3 A, T_j = 25 °C	V_F	0.85	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at I_D = 100 µA, V_{GS} = 0	$V_{(BR)DSS}$	60	80	–	V
Gate Threshold Voltage at V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(TO)}$	1.0	2	3.0	V
Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0	I_{GSS}	–	–	10	nA
Drain Cutoff Current at V_{DS} = 25 V, V_{GS} = 0	I_{DSS}	–	–	0.5	µA
Drain-Source ON Resistance at V_{GS} = 10 V, I_D = 200 mA	$r_{DS(ON)}$	–	3.5	5.0	Ω
Thermal Resistance Junction to Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Forward Transconductance at V_{DS} = 10 V, I_D = 200 mA, f = 1 MHz	g_m	–	200	–	mS
Input Capacitance at V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	C_{iss}	–	30	–	pF
Switching Times at V_{GS} = 10 V, V_{DS} = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 5 25	 – –	 ns ns

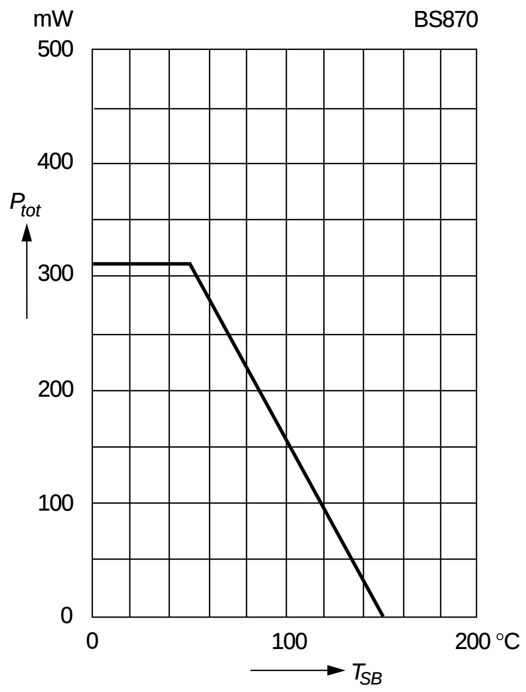
[1)] Device on fiberglass substrate, see layout



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

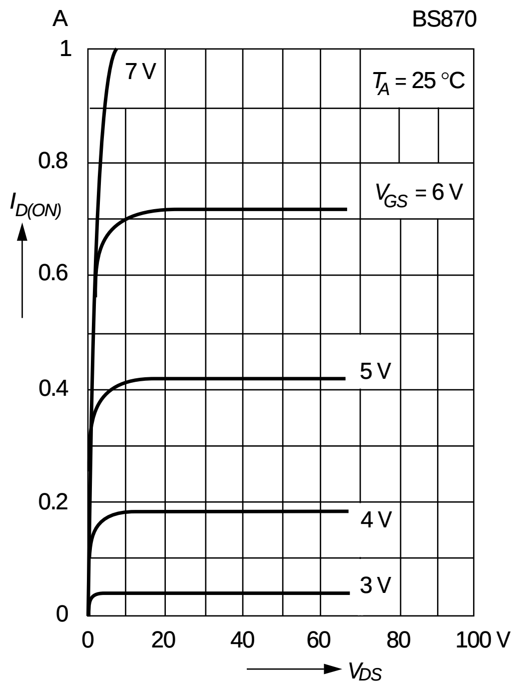
Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout



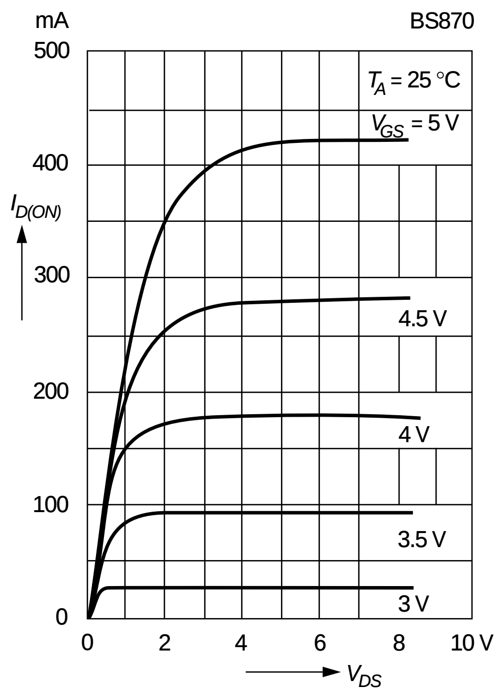
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%

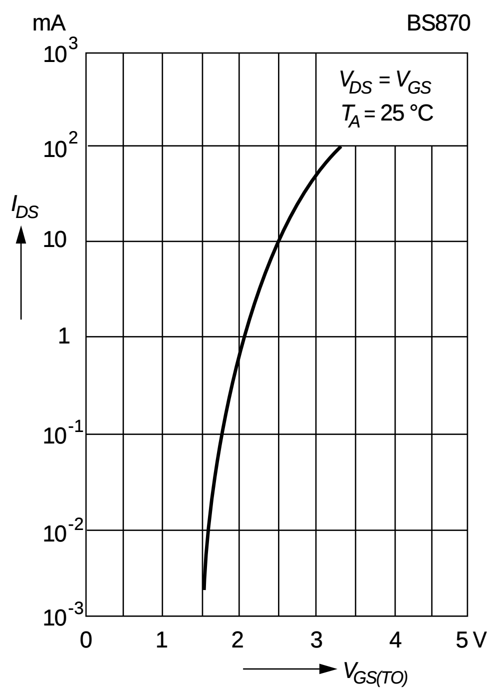


Saturation characteristics

Pulse test width 80 µs; pulse duty factor 1%

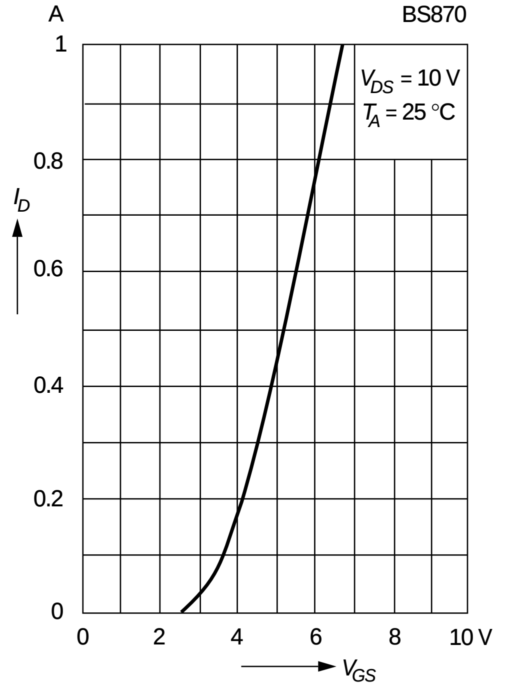


Drain-source current versus gate threshold voltage

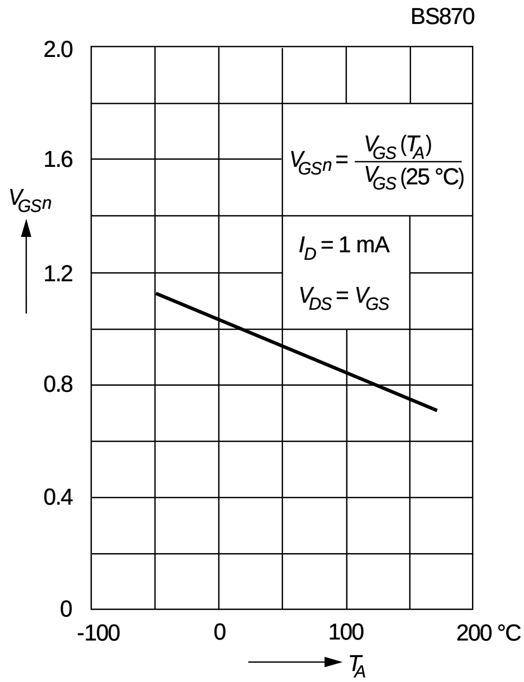


Drain current versus gate-source voltage

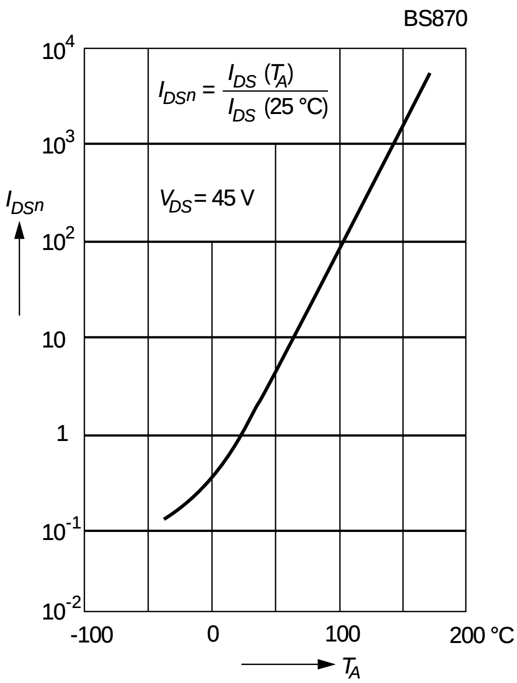
Pulse test width 80 µs; pulse duty factor 1%



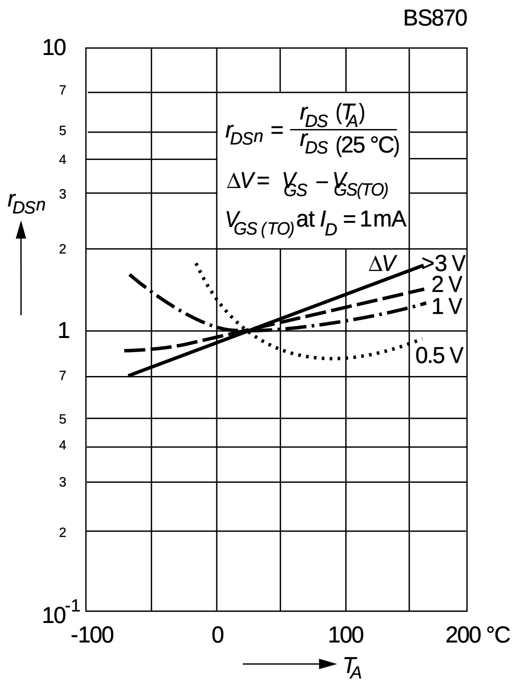
Normalized gate-source voltage versus temperature



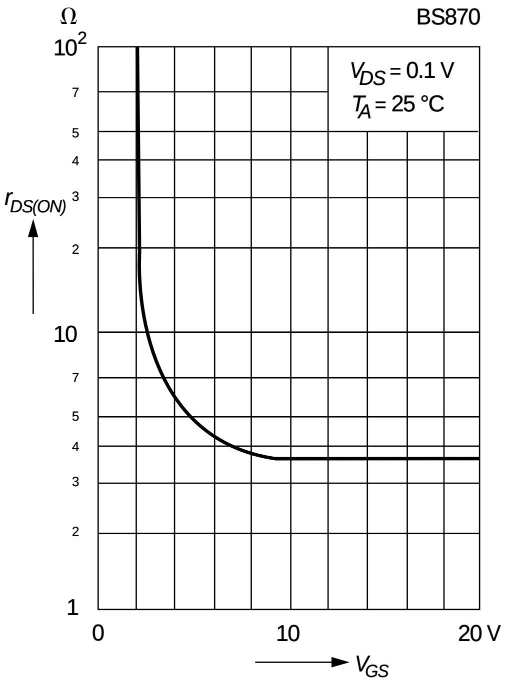
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

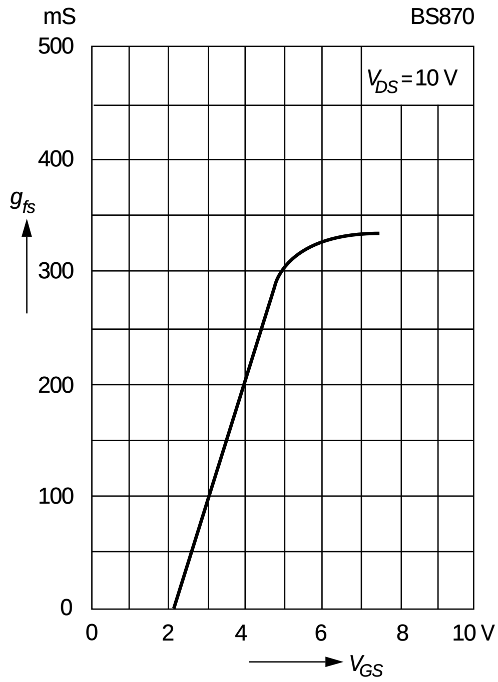


Drain-source resistance versus gate-source voltage



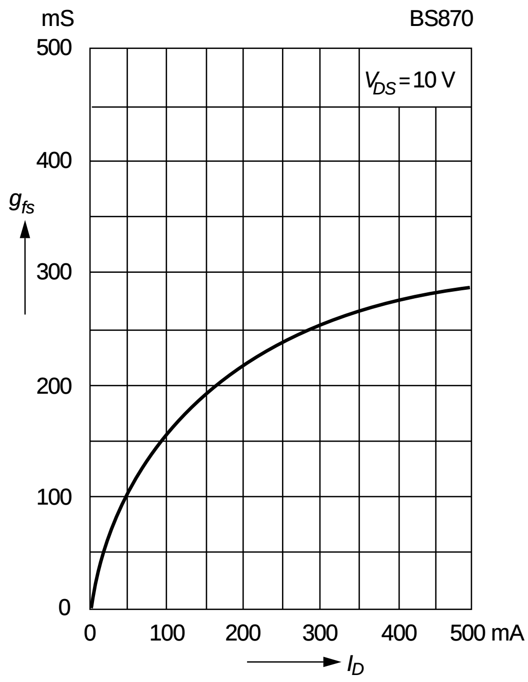
Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%

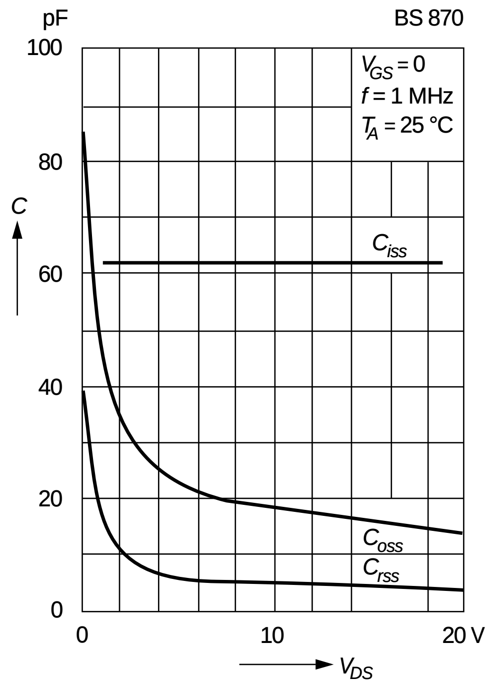


Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%



Capacitance versus drain-source voltage



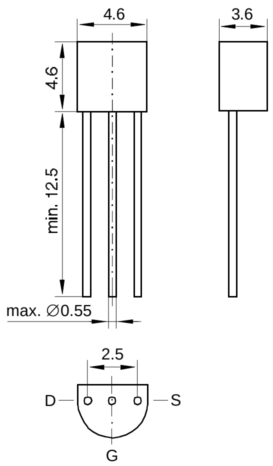
DMOS Transistors (P-Channel)

P-Channel Enhancement Mode DMOS Transistor

Features

– high breakdown voltage
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown
– specially suited for telephone subsets

On special request, this transistor is also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	240	V
Drain-Gate Voltage	$-V_{DGS}$	240	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	$-I_D$	200	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C
1) Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.			

Inverse Diode

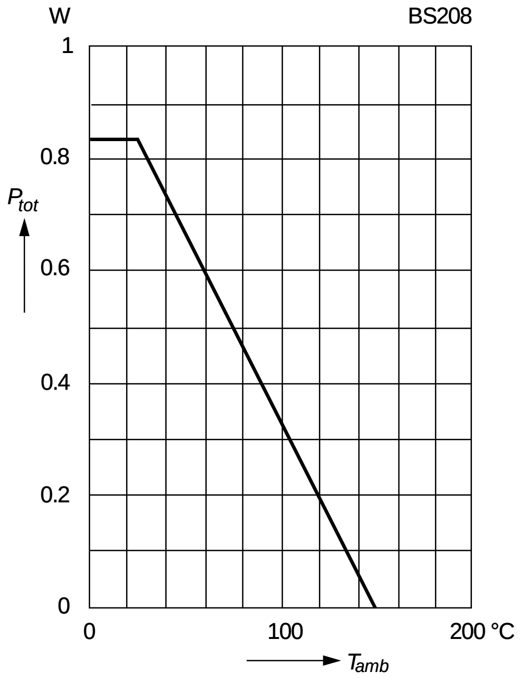
	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.75	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 µA, V_{GS} = 0	$-V_{(BR)DSS}$	240	250	–	V
Gate-Body Leakage Current at $-V_{GS}$ = 15 V, V_{DS} = 0	$-I_{GSS}$	–	–	10	nA
Drain Cutoff Current at $-V_{DS}$ = 130 V, V_{GS} = 0 at $-V_{DS}$ = 70 V, $-V_{GS}$ = 0.2 V	 $-I_{DSS}$ $-I_{DSX}$	 – –	 – –	 1 25	 µA µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 1 mA	$-V_{GS(TO)}$	0.8	1.5	2.5	V
Drain-Source ON Resistance at $-V_{GS}$ = 5 V, $-I_D$ = 100 mA	$r_{DS(ON)}$	–	7	14	Ω
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
Capacitances at $-V_{DS}$ = 20 V, V_{GS} = 0, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 200 30 10	 – – –	 pF pF pF
Switching Times at $-I_D$ = 200 mA, $-U_{GS}$ = 10 V Turn-on Time Fall Time	 t_{on} t_f	 – –	 5 15	 – –	 ns ns
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.					

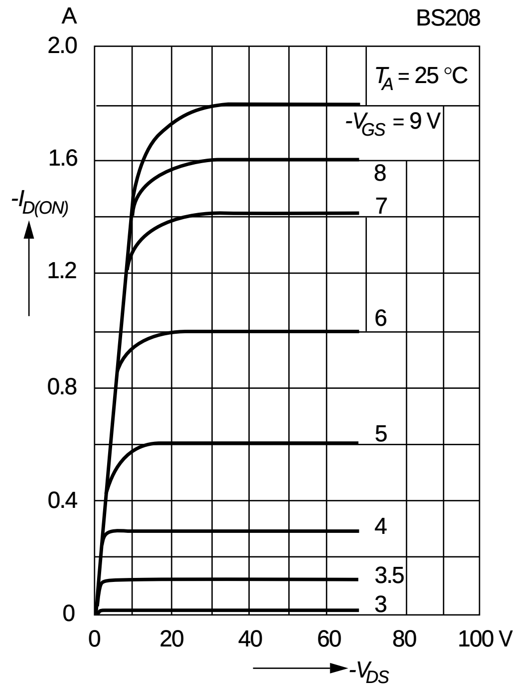
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



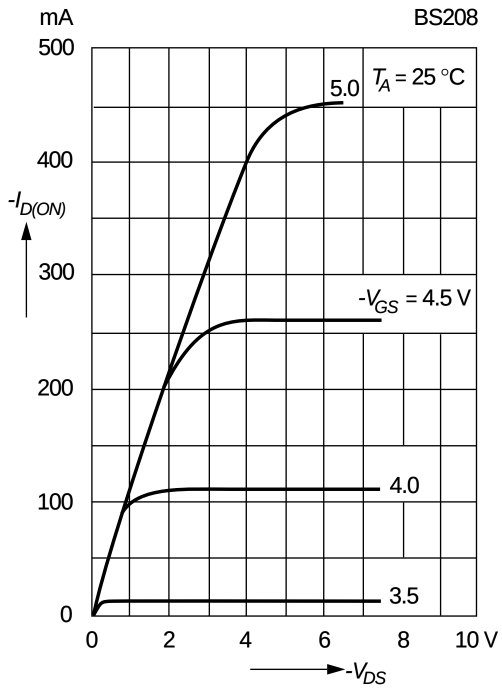
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%

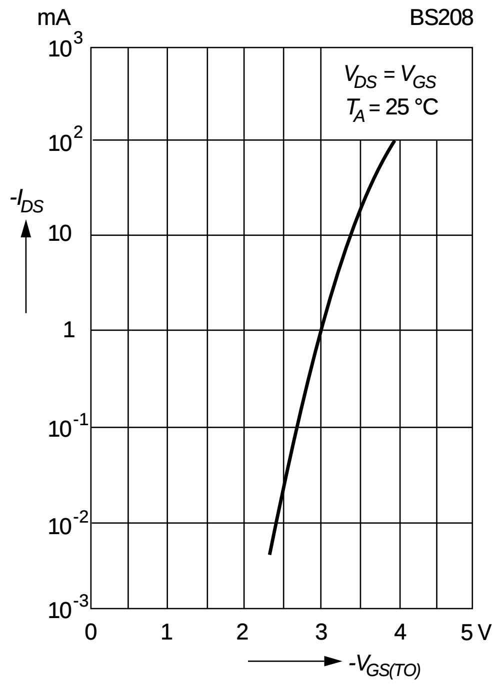


Saturation characteristics

Pulse test width 80 µs; pulse duty factor 1%

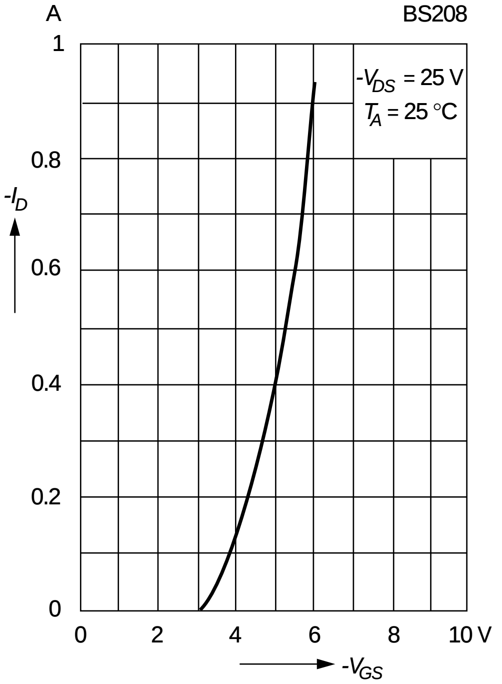


Drain-source current versus gate threshold voltage

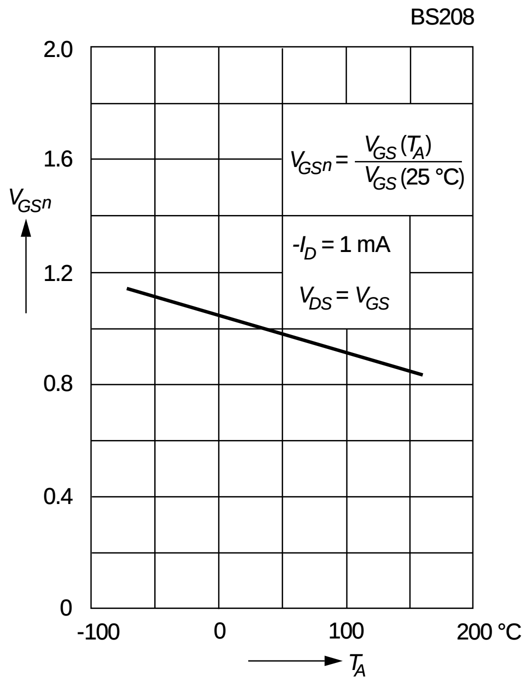


Drain current versus gate-source voltage

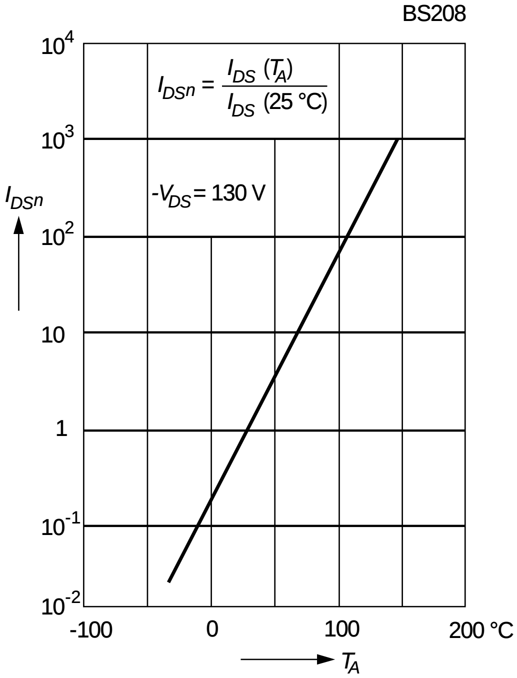
Pulse test width 80 µs; pulse duty factor 1%



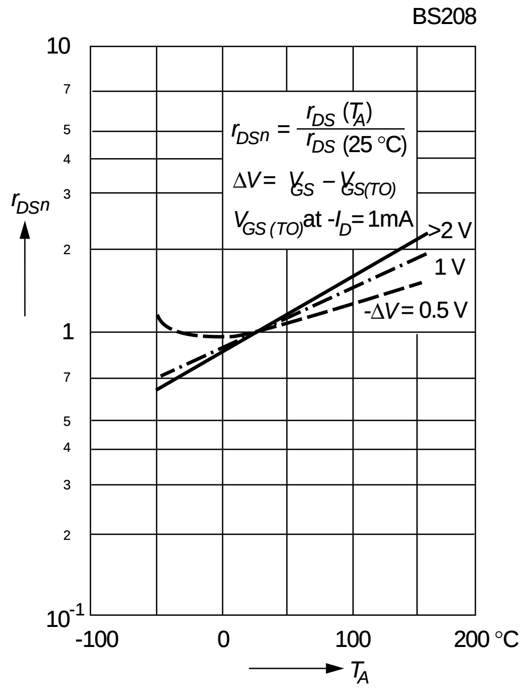
Normalized gate-source voltage versus temperature



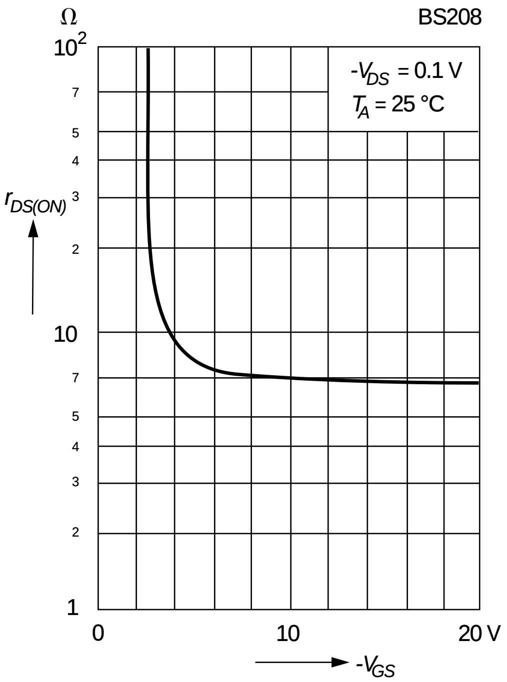
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

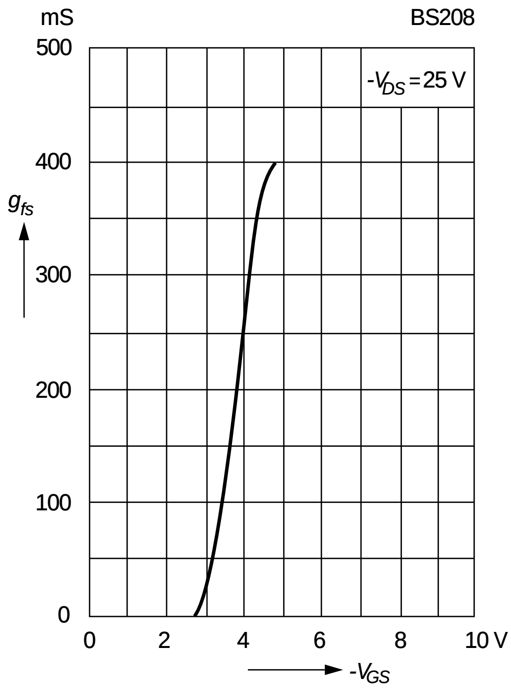


Drain-source resistance versus gate-source voltage



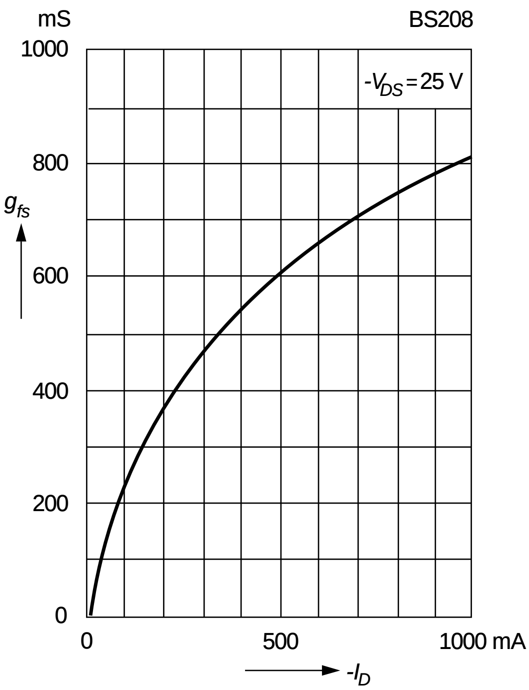
Transconductance versus gate-source voltage

Pulse test width 80 µs; pulse duty factor 1%

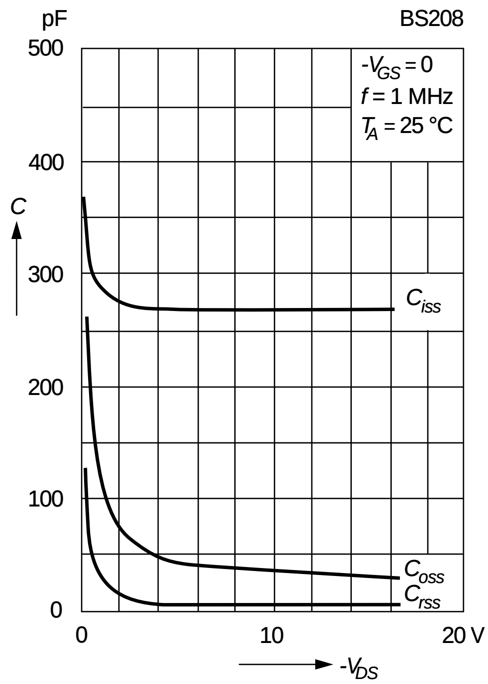


Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%

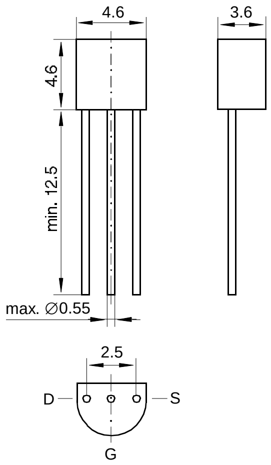


Capacitance versus drain-source voltage



P-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	400	V
Drain-Gate Voltage	$-V_{DGS}$	400	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous) at T_{amb} = 25 °C	$-I_D$	120	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	830[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C
1) Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.			

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	400	mA
Forward Voltage Drop (typ.) at V_{GS} = 0 V, I_F = 400 mA, T_j = 25 °C	V_F	1.0	V

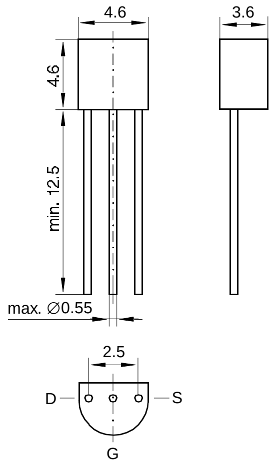
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 µA, V_{GS} = 0 V	$-V_{(BR)DSS}$	400	430	–	V
Gate-Body Leakage Current, Forward at $-V_{GSF}$ = 20 V, V_{DS} = 0 V	$-I_{GSSF}$	–	–	100	nA
Gate-Body Leakage Current, Reverse at $-V_{GSR}$ = 20 V, V_{DS} = 0 V	$-I_{GSSR}$	–	–	100	nA
Drain Cutoff Current at $-V_{DS}$ = 400 V, V_{GS} = 0 V	$-I_{DSS}$	–	–	500	nA
Gate-Source Threshold Voltage at $V_{GS} = V_{DS}$, $-I_D$ = 250 µA	$-V_{GS(th)}$	1	1.5	2.5	V
Drain-Source ON Resistance at $-V_{GS}$ = 5 V, $-I_D$ = 120 mA	$R_{DS(on)}$	–	50	60	Ω
Capacitance at $-V_{DS}$ = 25 V, V_{GS} = 0, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rSS}	 – – –	 200 30 10	 – – –	 pF pF pF
Switching Times at $-V_{GS}$ = 10 V, $-V_{DS}$ = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 10 50	 – –	 ns ns
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

P-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	60	V
Drain-Gate Voltage	$-V_{DGS}$	60	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous) at T_{amb} = 25 °C	$-I_D$	1	A
Power Dissipation at T_{amb} = 25 °C	P_{tot}	830[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	1	A
Forward Voltage Drop (typ.) at V_{GS} = 0 V, I_F = 1 mA, T_j = 25 °C	V_F	1.0	V

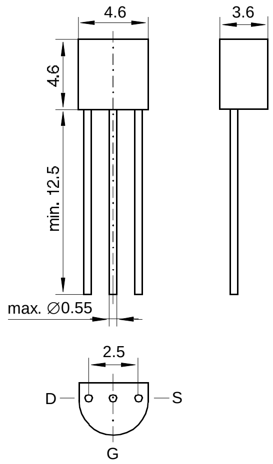
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 µA, V_{GS} = 0 V	$-V_{(BR)DSS}$	60	70	–	V
Gate-Body Leakage Current, Forward at $-V_{GSF}$ = 20 V, V_{DS} = 0 V	$-I_{GSSF}$	–	–	500	nA
Gate-Body Leakage Current, Reverse at $-V_{GSR}$ = 20 V, V_{DS} = 0 V	$-I_{GSSR}$	–	–	500	nA
Drain Cutoff Current at $-V_{DS}$ = 60 V, V_{GS} = 0 V	$-I_{DSS}$	–	–	250	µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 250 µA	$-V_{GS(TO)}$	1	1.5	3	V
Drain-Source ON Resistance at $-V_{GS}$ = 10 V, $-I_D$ = 600 mA	$R_{DS(on)}$	–	0.7	0.8	Ω
Capacitance at $-V_{DS}$ = 25 V, V_{GS} = 0 V, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rSS}	 – – –	 350 150 35	 – – –	 pF pF pF
Switching Times at $-V_{GS}$ = 10 V, $-V_{DS}$ = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 40 100	 – –	 ns ns
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.					

P-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

On special request, this transistor is also manufactured in the pin configuration TO-18.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	60	V
Drain-Gate Voltage	$-V_{DGS}$	60	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	$-I_D$	250	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.3	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.12 A, T_j = 25 °C	V_F	0.85	V

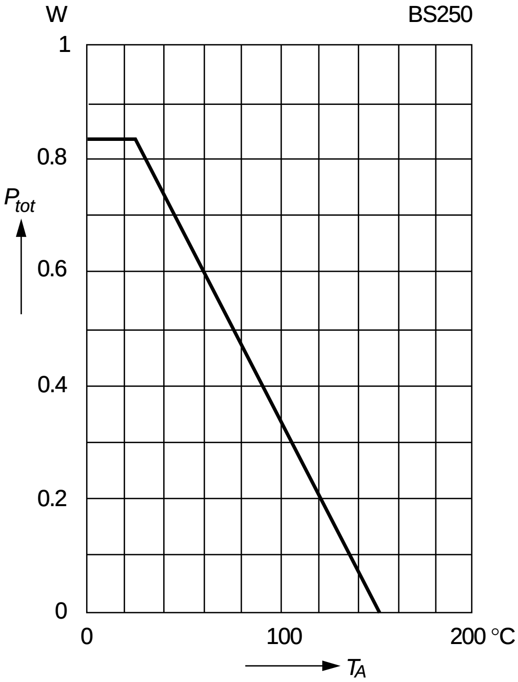
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 µA, V_{GS} = 0	$-V_{(BR)DSS}$	60	70	–	V
Gate Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 1 mA	$-V_{GS(TO)}$	1.0	2.0	3.0	V
Gate-Body Leakage Current at $-V_{GS}$ = 15 V, V_{DS} = 0	$-I_{GSS}$	–	–	20	nA
Drain Cutoff Current at $-V_{DS}$ = 25 V, V_{GS} = 0	$-I_{DSS}$	–	–	0.5	µA
Drain-Source ON Resistance at $-V_{GS}$ = 10 V, $-I_D$ = 0.2 A	$r_{DS(ON)}$	–	3.5	5.0	Ω
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
Forward Transconductance at $-V_{DS}$ = 10 V, $-I_D$ = 0.2 A, f = 1 MHz	g_m	–	150	–	mS
Input Capacitance at $-V_{DS}$ = 10 V, V_{GS} = 0, f = 1 MHz	C_{iss}	–	60	–	pF
Switching Times at $-V_{GS}$ = 10 V, $-V_{DS}$ = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 5 25	 – –	 ns ns

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

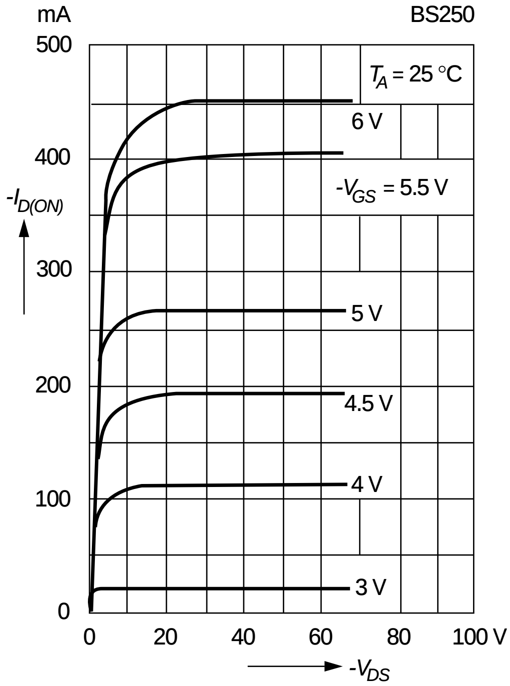
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



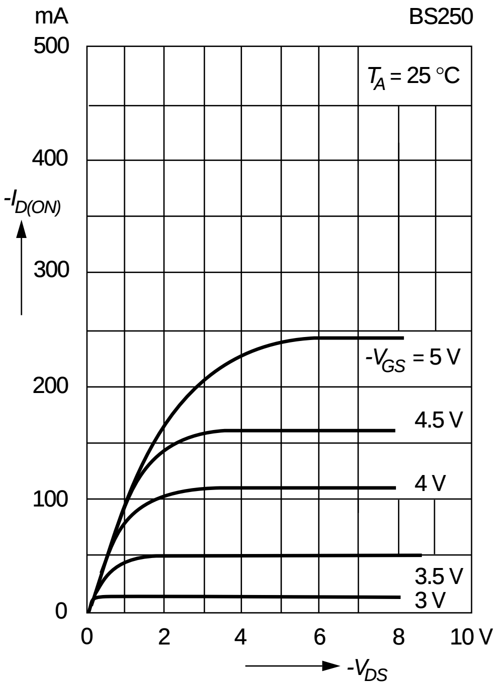
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%

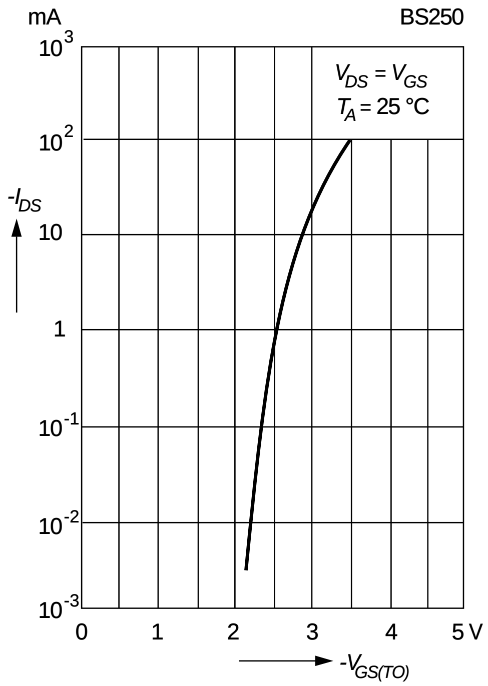


Saturation characteristics

Pulse test width 80 µs; pulse duty factor 1%

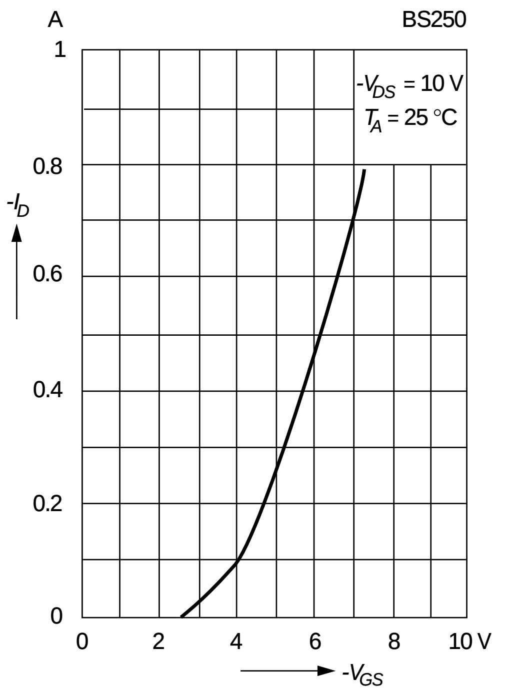


Drain-source current versus gate threshold voltage

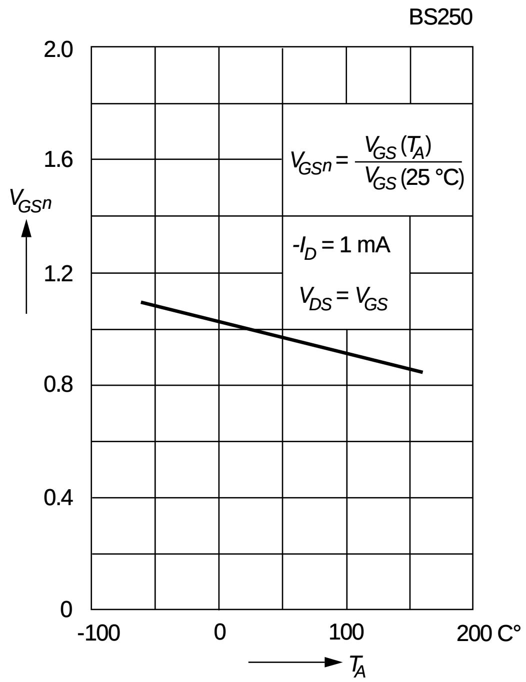


Drain current versus gate-source voltage

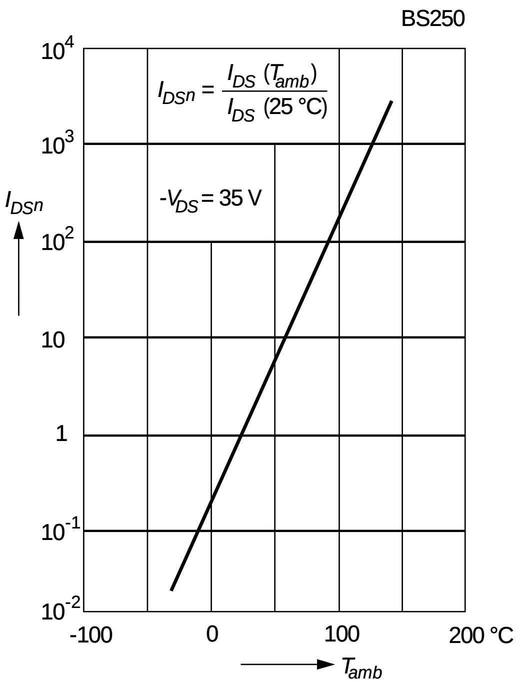
Pulse test width 80 µs; pulse duty factor 1%



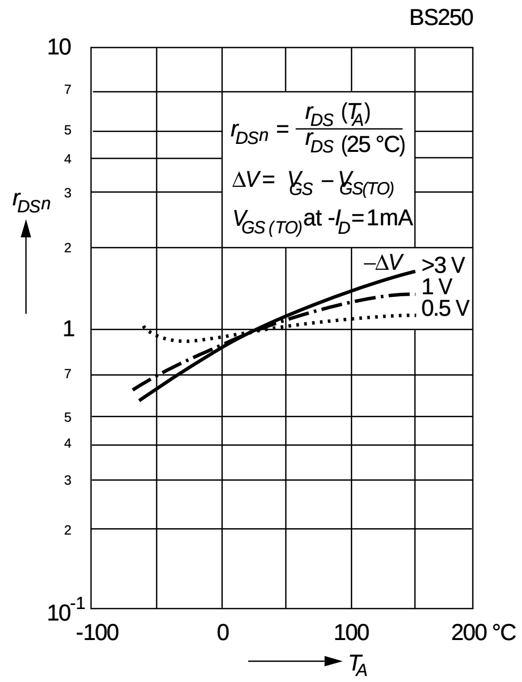
Normalized gate-source voltage versus temperature



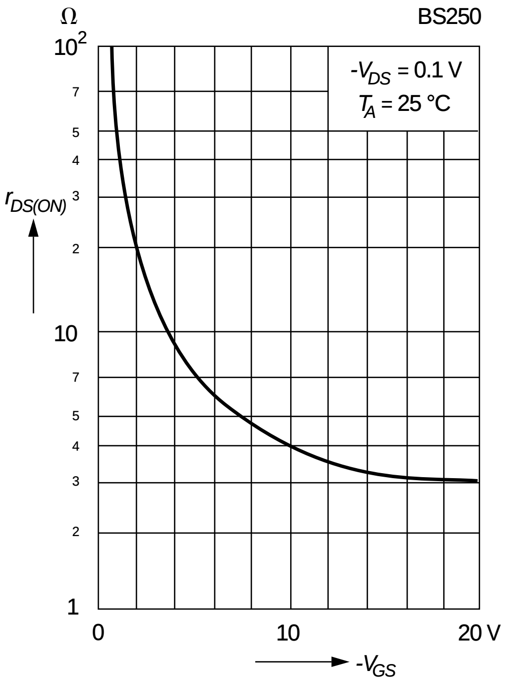
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

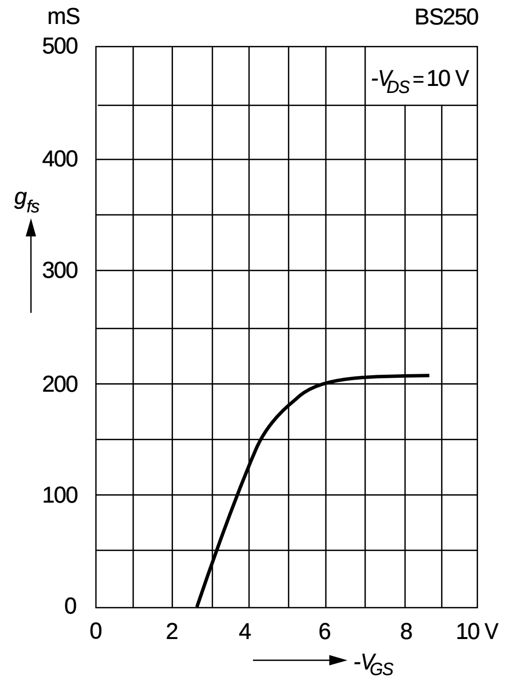


Drain-source resistance versus gate-source voltage



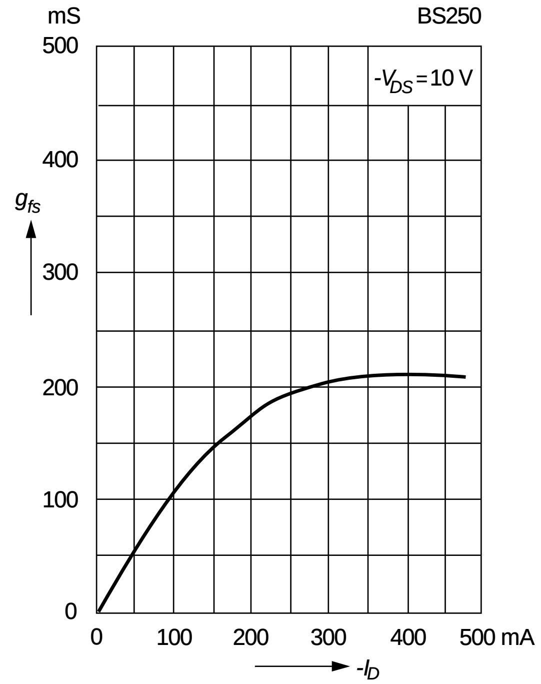
Transconductance versus gate-source voltage

Pulse test width 80 µs; pulse duty factor 1%

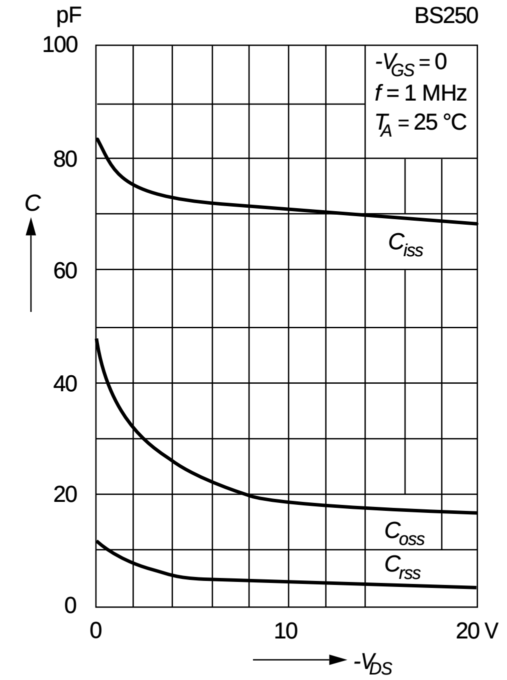


Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%



Capacitance versus drain-source voltage

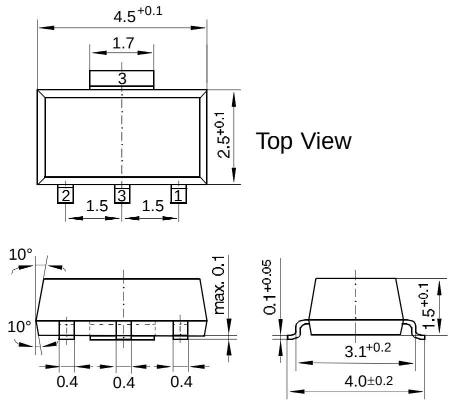


P-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

Pin configuration
1 = Source, 2 = Gate, 3 = Drain

Marking
S23



SOT-89A Plastic Package
Weight approx. 0.04 g
Dimensions in mm

Absolute Maximum Ratings

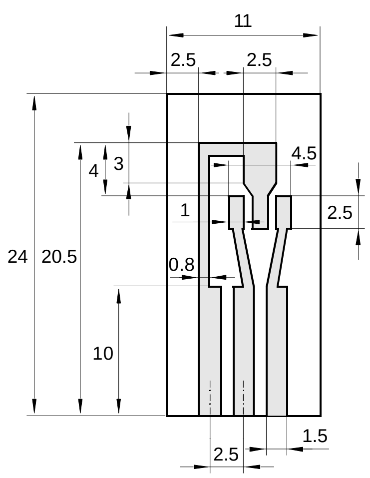
	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	60	V
Drain-Gate Voltage	$-V_{DGS}$	60	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous) at T_{SB} = 50 °C	$-I_D$	1	A
Power Dissipation at T_{SB} = 50 °C	P_{tot}	830[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C
[1)] Device on fiberglass substrate, see layout			

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	1	A
Forward Voltage Drop (typ.) at V_{GS} = 0 V, I_F = 1 A, T_j = 25 °C	V_F	1.0	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 µA, V_{GS} = 0 V	$-V_{(BR)DSS}$	60	70	–	V
Gate-Body Leakage Current, Forward at $-V_{GSF}$ = 20 V, V_{DS} = 0 V	$-I_{GSSF}$	–	–	500	nA
Gate-Body Leakage Current, Reverse at $-V_{GSR}$ = 20 V, V_{DS} = 0 V	$-I_{GSSR}$	–	–	500	nA
Drain Cutoff Current at $-V_{DS}$ = 60 V, V_{GS} = 0 V	$-I_{DSS}$	–	–	250	µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 250 µA	$-V_{GS(th)}$	1	1.5	3	V
Drain-Source ON Resistance at $-V_{GS}$ = 10 V, $-I_D$ = 600 mA	$R_{DS(on)}$	–	0.7	0.8	Ω
Capacitance at $-V_{DS}$ = 25 V, V_{GS} = 0 V, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rSS}	 – – –	 350 150 35	 – – –	 pF pF pF
Switching Times at $-V_{GS}$ = 10 V, $-V_{DS}$ = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 40 100	 – –	 ns ns
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
[1)] Device on fiberglass substrate, see layout					



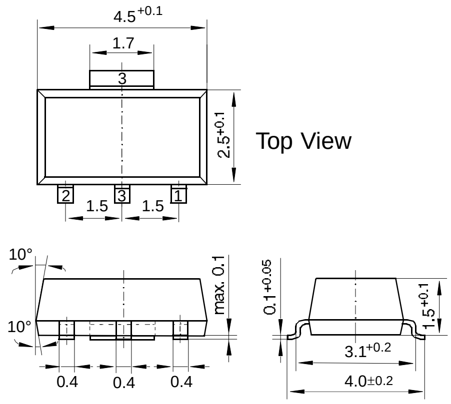
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

P-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

Pin configuration
1 = Source, 2 = Gate, 3 = Drain

Marking
S08



SOT-89A Plastic Package
Weight approx. 0.04 g
Dimensions in mm

Absolute Maximum Ratings

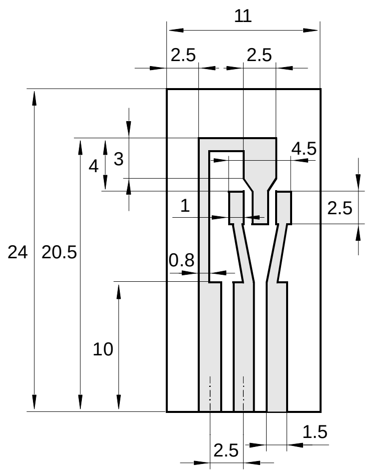
	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	240	V
Drain-Gate Voltage	$-V_{DGS}$	240	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous) at T_{SB} = 50 °C	$-I_D$	200	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	830[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C
[1)] Device on fiberglass substrate, see layout			

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.75	A
Forward Voltage Drop (typ.) at V_{GS} = 0 V, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 µA, V_{GS} = 0 V	$-V_{(BR)DSS}$	240	250	–	V
Gate-Body Leakage Current, Forward at $-V_{GSF}$ = 15 V, V_{DS} = 0 V	$-I_{GSSF}$	–	–	10	nA
Gate-Body Leakage Current, Reverse at $-V_{GSR}$ = 15 V, V_{DS} = 0 V	$-I_{GSSR}$	–	–	10	nA
Drain Cutoff Current at $-V_{DS}$ = 130 V, V_{GS} = 0 V	$-I_{DSS}$	–	–	1	µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 250 µA	$-V_{GS(th)}$	0.8	1.5	2.5	V
Drain-Source ON Resistance at $-V_{GS}$ = 5 V, $-I_D$ = 100 mA	$R_{DS(on)}$	–	7	14	Ω
Capacitance at $-V_{DS}$ = 20 V, V_{GS} = 0 V, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rSS}	 – – –	 200 30 10	 – – –	 pF pF pF
Switching Times at $-V_{GS}$ = 10 V, $-I_D$ = 10 mA Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 5 20	 – –	 ns ns
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	150[1)]	K/W
[1)] Device on fiberglass substrate, see layout					



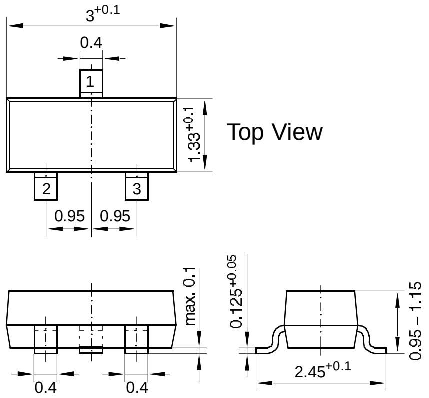
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

P-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– low gate threshold voltage
– low drain-source ON resistance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

Pin configuration
1 = Drain, 2 = Gate, 3 = Source

Marking
S29



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

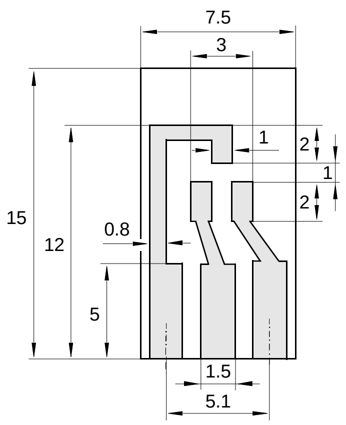
	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	400	V
Drain-Gate Voltage	$-V_{DGS}$	400	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous) at T_{SB} = 50 °C	$-I_D$	70	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	350[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C
[1)] Device on fiberglass substrate, see layout			

Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	350	mA
Forward Voltage Drop (typ.) at V_{GS} = 0 V, I_F = 350 mA, T_j = 25 °C	V_F	1.0	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 µA, V_{GS} = 0 V	$-V_{(BR)DSS}$	400	430	–	V
Gate-Body Leakage Current, Forward at $-V_{GSF}$ = 20 V, V_{DS} = 0 V	$-I_{GSSF}$	–	–	100	nA
Gate-Body Leakage Current, Reverse at $-V_{GSR}$ = 20 V, V_{DS} = 0 V	$-I_{GSSR}$	–	–	100	nA
Drain Cutoff Current at $-V_{DS}$ = 400 V, V_{GS} = 0 V	$-I_{DSS}$	–	–	500	µA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 250 µA	$-V_{GS(th)}$	1	1.5	2.5	V
Drain-Source ON Resistance at V_{GS} = 5 V, $-I_D$ = 100 mA	$R_{DS(on)}$	–	40	50	Ω
Capacitance at $-V_{DS}$ = 25 V, V_{GS} = 0 V, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iSS} C_{OSS} C_{rSS}	 – – –	 200 30 10	 – – –	 pF pF pF
Switching Times at $-V_{GS}$ = 10 V, $-V_{DS}$ = 10 V, R_D = 100 Ω Turn-On Time Turn-Off Time	 t_{on} t_{off}	 – –	 10 50	 – –	 ns ns
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	320[1)]	K/W
[1)] Device on fiberglass substrate, see layout					



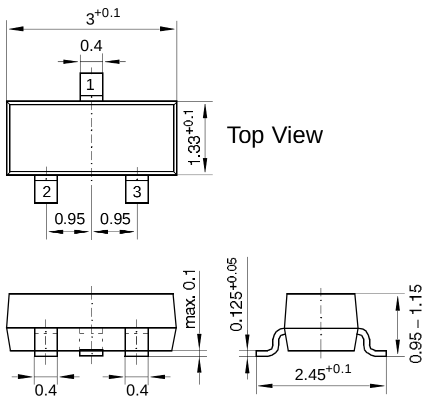
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

P-Channel Enhancement Mode DMOS Transistor

Features
– high input impedance
– high-speed switching
– no minority carrier storage time
– CMOS logic compatible input
– no thermal runaway
– no secondary breakdown

Pin configuration
1 = Drain, 2 = Gate, 3 = Source

Marking
S50



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	60	V
Drain-Gate Voltage	$-V_{DGS}$	60	V
Gate-Source Voltage (pulsed)	V_{GS}	± 20	V
Drain Current (continuous)	$-I_D$	250	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	0.310[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65…+150	°C
[1)] Device on fiberglass substrate, see layout			

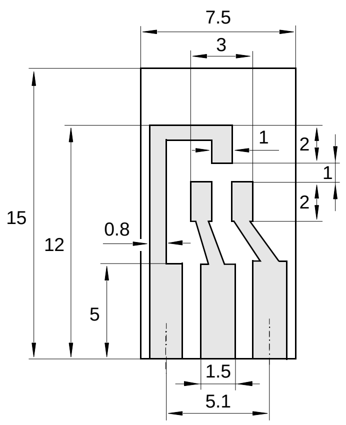
Inverse Diode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.3	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.12 A, T_j = 25 °C	V_F	0.85	V

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 µA, V_{GS} = 0	$-V_{(BR)DSS}$	60	90	–	V
Gate Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 1 mA	$V_{GS(TO)}$	1.0	2	3.0	V
Gate-Body Leakage Current at $-V_{GS}$ = 15 V, V_{DS} = 0	$-I_{GSS}$	–	–	10	nA
Drain Cutoff Current at $-V_{DS}$ = 25 V, V_{GS} = 0	$-I_{DSS}$	–	–	0.5	µA
Drain-Source ON Resistance at $-V_{GS}$ = 10 V, $-I_D$ = 200 mA	$r_{DS(ON)}$	–	3.5	5.0	Ω
Thermal Resistance Junction to Substrate Backside	R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	450[1)]	K/W
Forward Transconductance at $-V_{DS}$ = 10 V, $-I_D$ = 200 mA, f = 1 MHz	g_m	–	200	–	mS
Input Capacitance at $-V_{DS}$ = 10 V, V_{GS} = 0, f = 1 MHz	C_{iss}	–	60	–	pF
Switching Times at $-V_{GS}$ = 10 V, $-V_{DS}$ = 10 V, R_D = 100 Ω					
Turn-On Time	t_{on}	–	5	–	ns
Turn-Off Time	t_{off}	–	25	–	ns

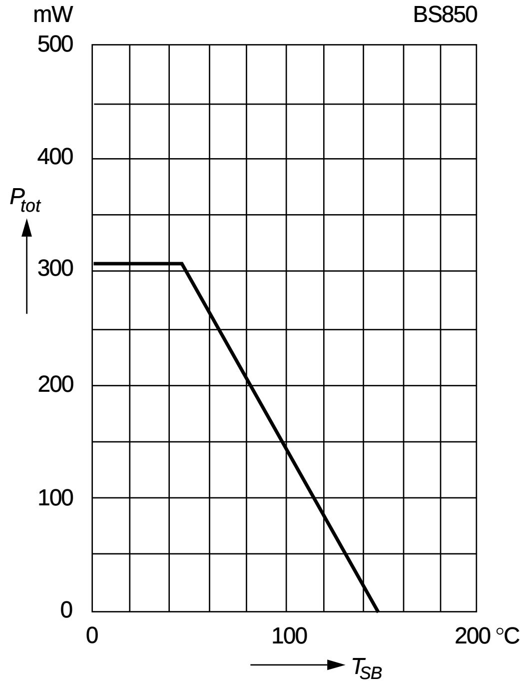
[1)] Device on fiberglass substrate, see layout



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

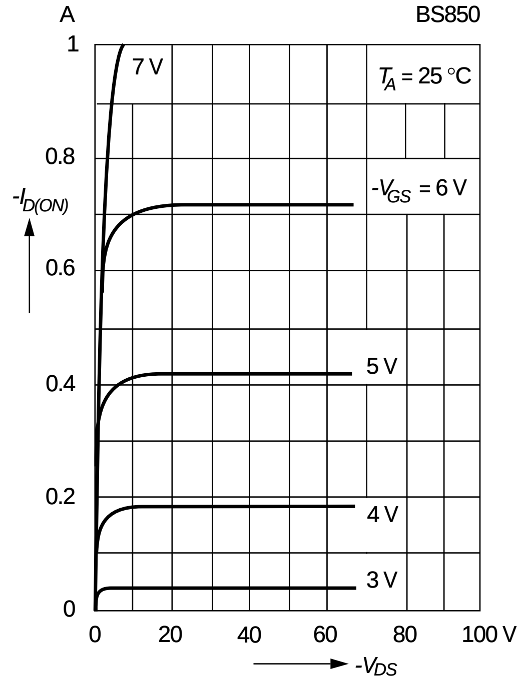
Admissible power dissipation versus temperature of substrate backside

Device on fiberglass substrate, see layout



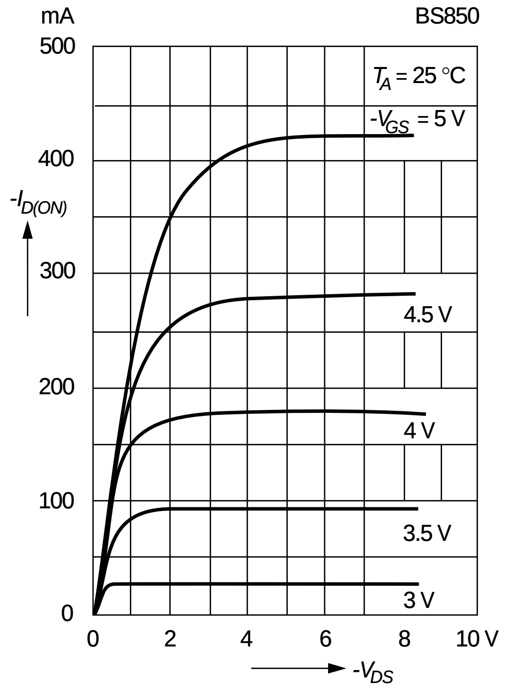
Output characteristics

Pulse test width 80 µs; pulse duty factor 1%

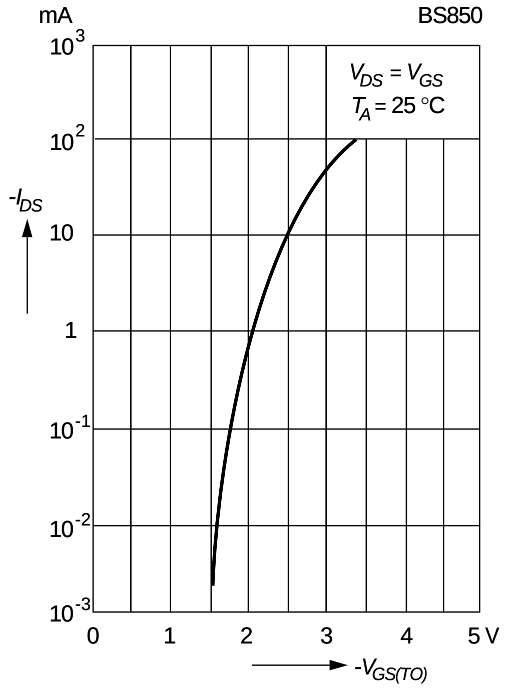


Saturation characteristics

Pulse test width 80 µs; pulse duty factor 1%

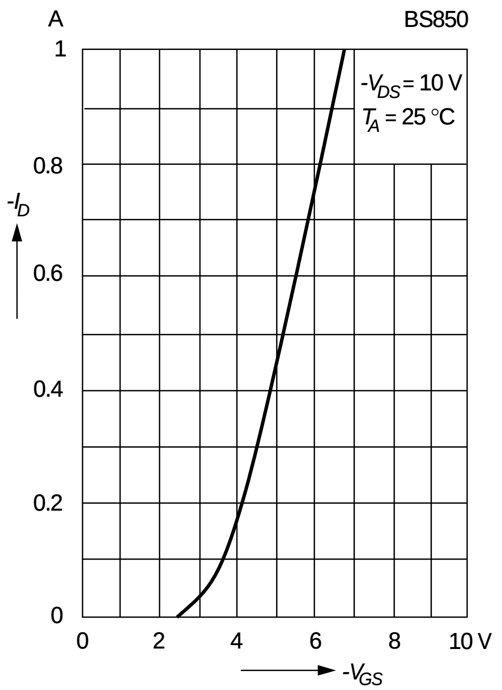


Drain-source current versus gate threshold voltage

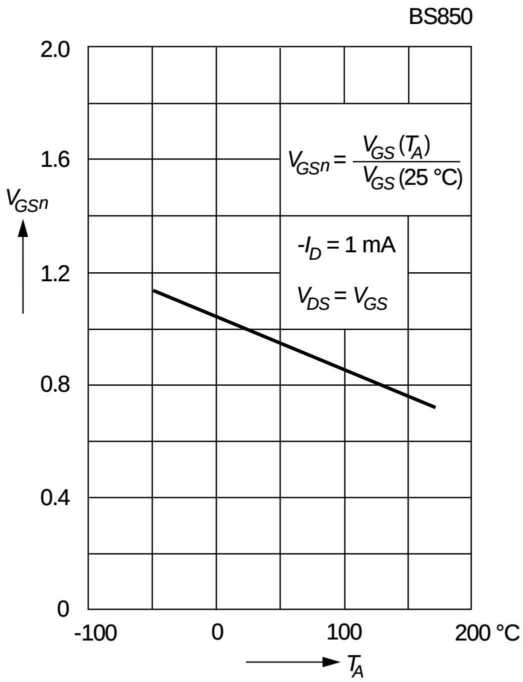


Drain current versus gate-source voltage

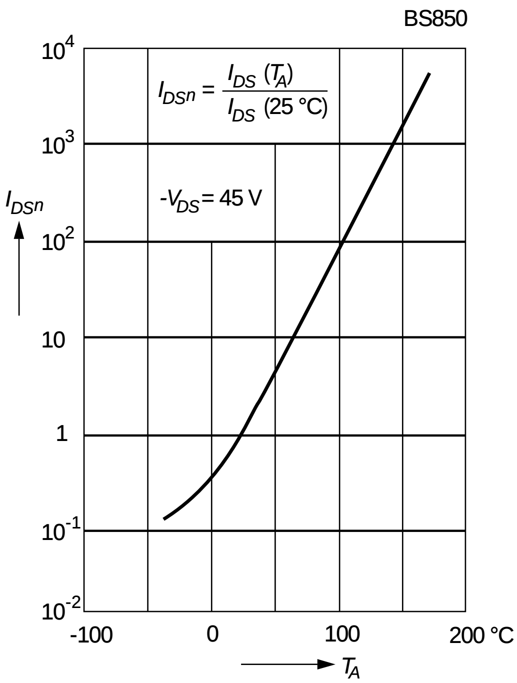
Pulse test width 80 µs; pulse duty factor 1%



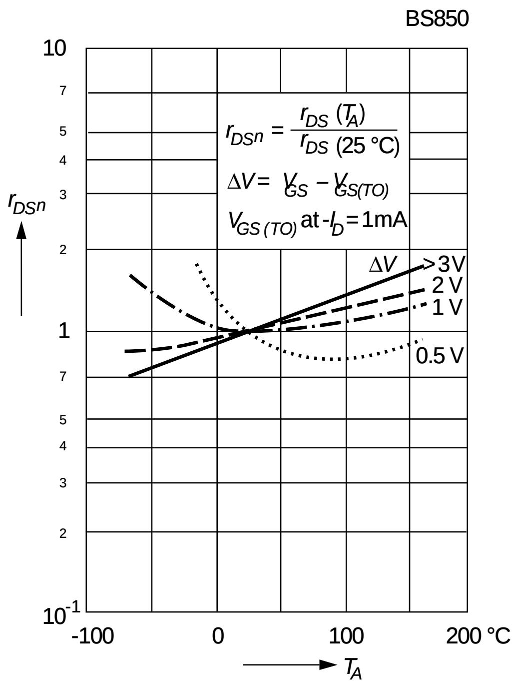
Normalized gate-source voltage versus temperature



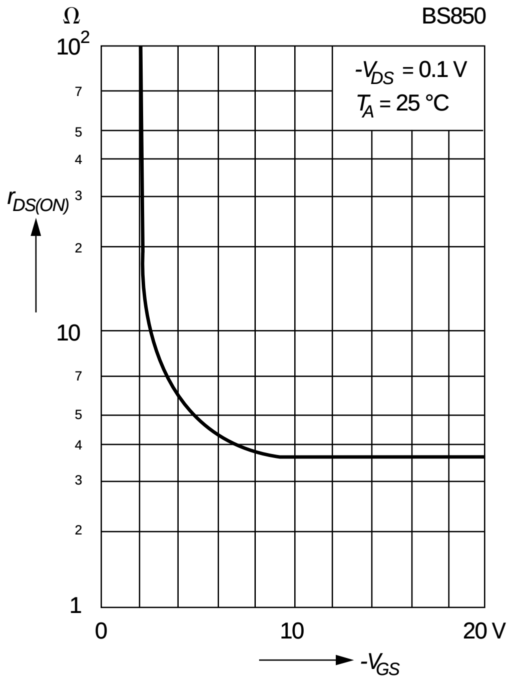
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

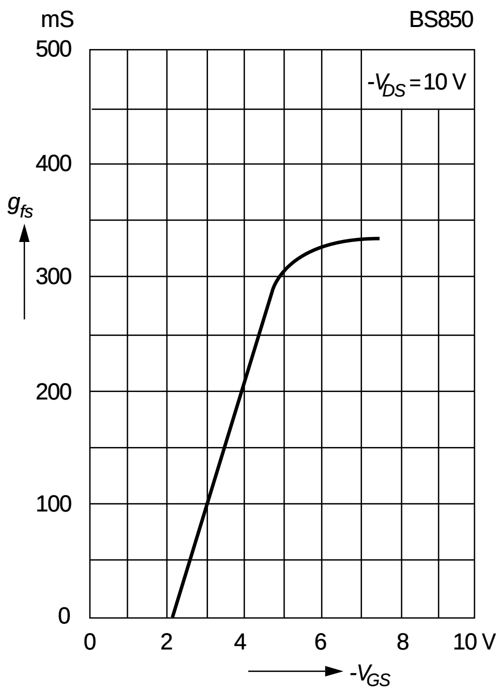


Drain-source resistance versus gate-source voltage



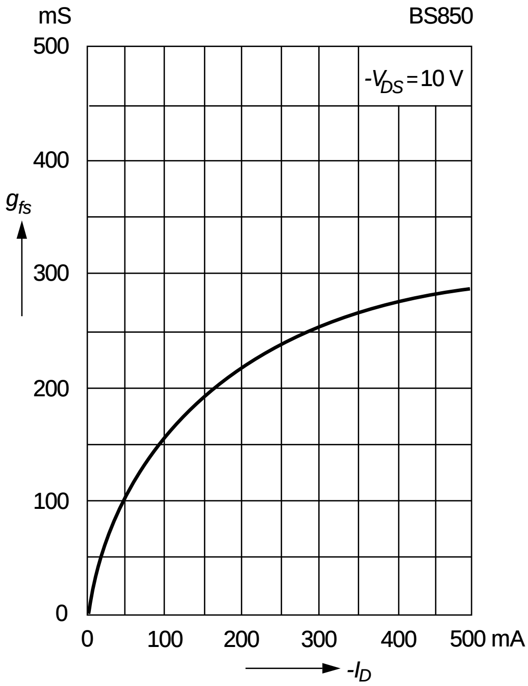
Transconductance versus gate-source voltage

Pulse test width 80 µs; pulse duty factor 1%

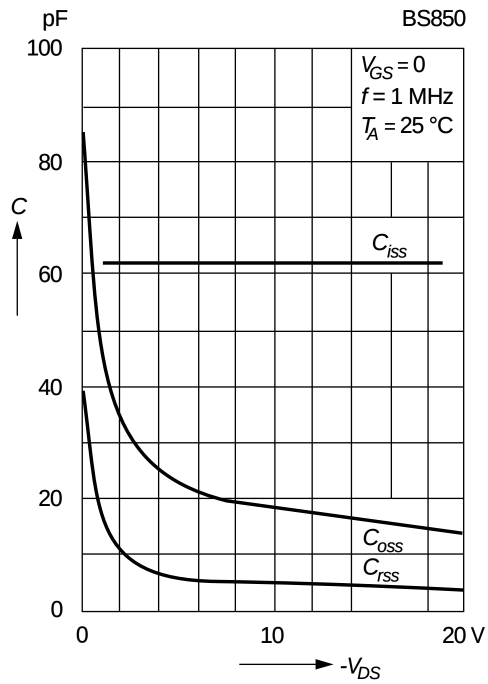


Transconductance versus drain current

Pulse test width 80 µs; pulse duty factor 1%



Capacitance versus drain-source voltage



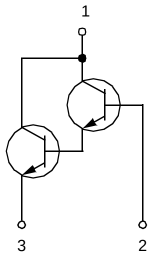
Darlington Transistors

NPN Silicon Planar Darlington Transistor
for general NF applications

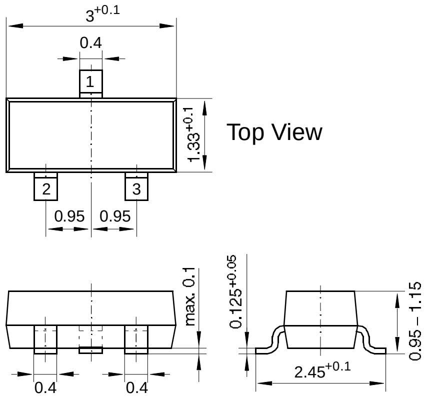
As complementary type, the PNP transistor BCV26 is recommended.

Features
– high collector current
– high current gain

Pin configuration
1 = Collector, 2 = Base, 3 = Emitter



Marking
FF



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

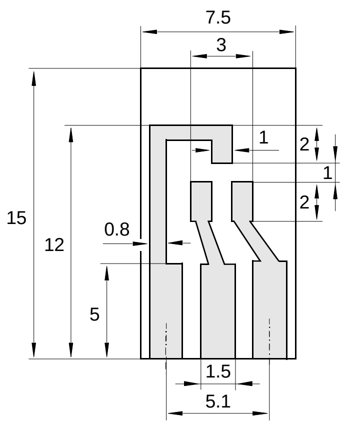
	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	40	V
Emitter-Base Voltage	V_{EBO}	10	V
Collector Current	I_C	300	mA
Peak Collector Current	I_{CM}	800	mA
Base Current	I_B	100	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	300[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	–65 to +150	°C

1) Device on fiberglass substrate, see layout

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Collector-Base Cutoff Current at V_{CBO} = 30 V	I_{CBO}	–	–	0.1	µA
Emitter-Base Cutoff Current at V_{EB} = 10 V	I_{EBO}	–	–	0.1	µA
Collector-Emitter Breakdown Voltage at I_C = 10 mA	$V_{(BR)CEO}$	30	–	–	V
Collector-Base Breakdown Voltage at I_C = 10 µA	$V_{(BR)CBO}$	40	–	–	V
Emitter-Base Breakdown Voltage at I_E = 100 nA	$V_{(BR)EBO}$	10	–	–	V
DC Current Gain at V_{CE} = 5 V, I_C = 1 mA at V_{CE} = 5 V, I_C = 10 mA at V_{CE} = 5 V, I_C = 100 mA	 h_{FE} h_{FE} h_{FE}	 4000 10000 20000	 – – –	 – – –	 – – –
Collector-Emitter Saturation Voltage at I_C = 100 mA, I_B = 0.1 mA	V_{CEsat}	–	–	1.0	V
Base-Emitter Saturation Voltage at I_C = 100 mA, I_B = 0.1 mA	V_{BEsat}	–	–	1.5	V
Gain-Bandwidth Product at V_{CE} = 5 V, I_C = 30 mA, f = 100 MHz	f_T	–	220	–	MHz
Collector-Base Capacitance at V_{CB} = 30 V, I_E = 0, f = 1 MHz	C_{CBO}	–	3.5	–	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	430[1)]	K/W

[1)] Device on fiberglass substrate, see layout below



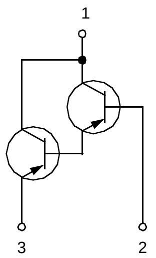
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

PNP Silicon Planar Darlington Transistor
for general NF applications

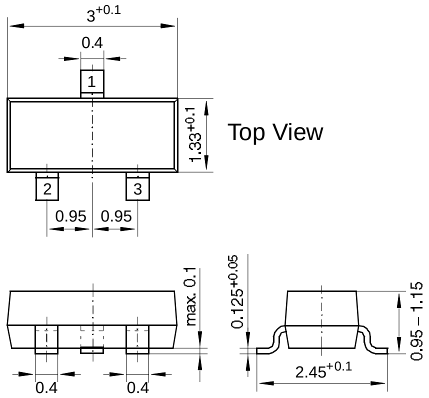
As complementary type, the NPN transistor BCV27 is recommended.

Features
– high collector current
– high current gain

Pin configuration
1 = Collector, 2 = Base, 3 = Emitter



Marking
FD



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

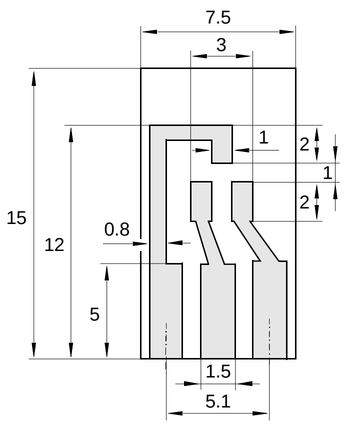
	Symbol	Value	Unit
Collector-Emitter Voltage	$-V_{CEO}$	30	V
Collector-Base Voltage	$-V_{CBO}$	40	V
Emitter-Base Voltage	$-V_{EBO}$	10	V
Collector Current	$-I_C$	300	mA
Peak Collector Current	$-I_{CM}$	800	mA
Base Current	$-I_B$	100	mA
Power Dissipation at T_{SB} = 50 °C	P_{tot}	300[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−65 to +150	°C

[1)] Device on fiberglass substrate, see layout

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Collector-Base Cutoff Current at $-V_{CBO}$ = 30 V	$-I_{CBO}$	–	–	0.1	µA
Emitter-Base Cutoff Current at $-V_{EB}$ = 10 V	$-I_{EBO}$	–	–	0.1	µA
Collector-Emitter Breakdown Voltage at $-I_C$ = 10 mA	$-V_{(BR)CEO}$	30	–	–	V
Collector-Base Breakdown Voltage at I_C = 10 µA	$-V_{(BR)CBO}$	40	–	–	V
Emitter-Base Breakdown Voltage at $-I_E$ = 100 nA	$-V_{(BR)EBO}$	10	–	–	V
DC Current Gain at $-V_{CE}$ = 5 V, $-I_C$ = 1 mA at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA at $-V_{CE}$ = 5 V, $-I_C$ = 100 mA	 h_{FE} h_{FE} h_{FE}	 4000 10000 20000	 – – –	 – – –	 – – –
Collector-Emitter Saturation Voltage at $-I_C$ = 100 mA, $-I_B$ = 0.1 mA	$-V_{CEsat}$	–	–	1.0	V
Base-Emitter Saturation Voltage at $-I_C$ = 100 mA, $-I_B$ = 0.1 mA	$-V_{BEsat}$	–	–	1.5	V
Gain-Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 30 mA, f = 100 MHz	f_T	–	220	–	MHz
Collector-Base Capacitance at $-V_{CB}$ = 30 V, I_E = 0, f = 1 MHz	C_{CBO}	–	3.5	–	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	–	–	430[1)]	K/W

[1)] Device on fiberglass substrate, see layout below



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

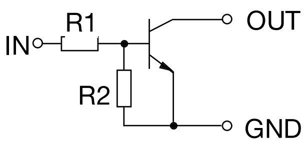
Bias Resistor Transistors

NPN Bias Resistor Transistor

The built-in bias resistor allows inverter circuit configuration without external resistors for input.

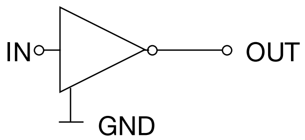
Pin configuration
1 = Collector/OUT
2 = Base/IN
3 = Emitter/GND

Marking
EC4

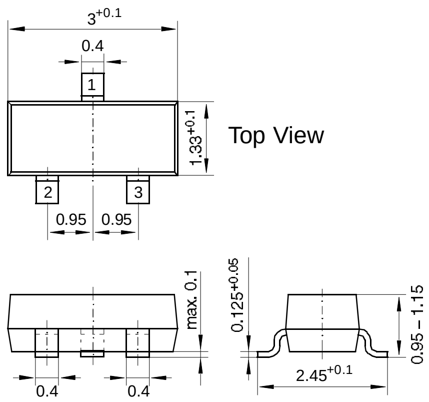


R1 = 10 kΩ

R2 = 10 kΩ



Equivalent circuit



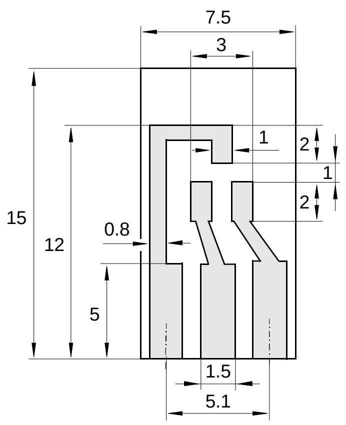
SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Supply Voltage	V_{SUP}	50	V
Input Voltage	V_I	40	V
	$–V_I$	10	V
Collector Current	I_C	50	mA
Peak Collector Current	I_{CM}	100	mA
Power Dissipation	P_{tot}	300[1)]	mW
Junction Temperature	T_j	125	°C
Storage Temperature Range	T_S	–65 to +125	°C
[1)] Device on fiberglass substrate, see layout			

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Input OFF Voltage at V_{SUP} = 5 V, I_O = 100 µA	$V_{I(OFF)}$	–	–	0.5	V
Input ON Voltage at V_O = 0.3 V, I_O = 10 mA	$V_{I(ON)}$	3.0	–	–	V
Output ON Voltage at I_O = 10 mA, I_I = 0.5 mA	$V_{O(ON)}$	–	0.1	0.3	V
Input Current at V_I = 5 V	I_I	–	–	0.88	mA
Output OFF Current at V_{SUP} = 30 V, V_I = 0 V	$I_{O(OFF)}$	–	–	10	µA
DC Current Gain at I_O = 5 mA, V_O = 5 V	G_I	30	–	–	–
Input Resistance	R1	–	10	–	kΩ
Resistance Ratio	R2/R1	0.8	1	1.2	–
Transition Frequency at V_{CE} = 10 V, I_E = –5 mA	f_T	–	250	–	MHz
Collector-Base Capacitance at V_{CB} = 10 V, I_E = 0 mA, f = 1 MHz	C_{ob}	–	5.6	–	pF
Switching Times at V_{SUP} = 5 V, V_I = 5 V, R_L = 1 kΩ Rise Time Storage Time Fall Time	 t_r t_s t_f	 – – –	 0.05 2.0 0.36	 – – –	 µs µs µs



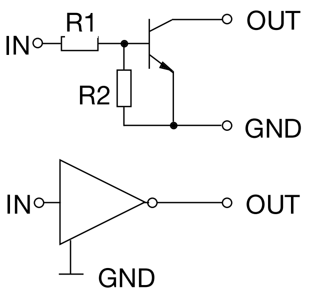
Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

NPN Bias Resistor Transistor

The built-in bias resistor allows inverter circuit configuration without external resistors for input.

Pin configuration
1 = Collector/OUT
2 = Base/IN
3 = Emitter/GND

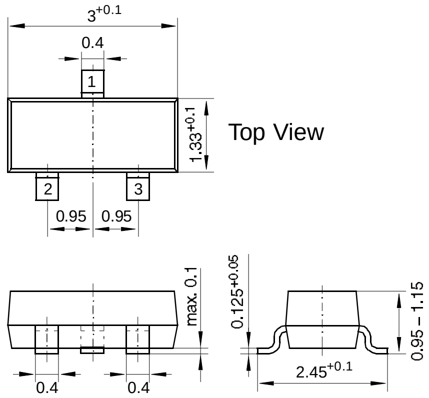
Marking
DC4



R1 = 22 kΩ

R2 = 47 kΩ

Equivalent circuit



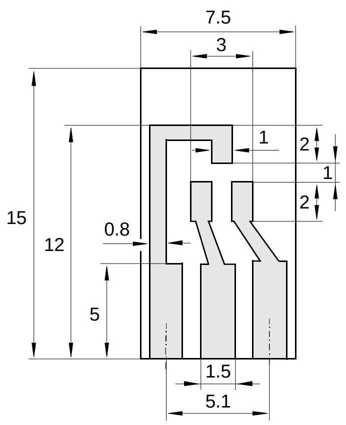
SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Supply Voltage	V_{SUP}	50	V
Input Voltage	V_I	40	V
	$-V_I$	10	V
Collector Current	I_C	100	mA
Peak Collector Current	I_{CM}	100	mA
Power Dissipation	P_{tot}	300[1)]	mW
Junction Temperature	T_j	125	°C
Storage Temperature Range	T_S	–65 to +125	°C
[1)] Device on fiberglass substrate, see layout			

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Input OFF Voltage at V_{SUP} = 5 V, I_O = 100 µA	$V_{I(OFF)}$	–	–	0.4	V
Input ON Voltage at V_O = 0.3 V, I_O = 2 mA	$V_{I(ON)}$	2.5	–	–	V
Output ON Voltage at I_O = 10 mA, I_I = 0.5 mA	$V_{O(ON)}$	–	0.1	0.3	V
Input Current at V_I = 0.5 V	I_I	–	–	0.36	mA
Output OFF Current at V_{SUP} = 30 V, V_I = 0 V	$I_{O(OFF)}$	–	–	10	µA
DC Current Gain at I_O = 5 mA, V_O = 5 V	G_I	68	–	–	–
Input Resistance	R1	–	22	–	kΩ
Resistance Ratio	R2/R1	1.7	2.1	2.6	–
Transition Frequency at V_{CE} = 10 V, I_E = –5 mA	f_T	–	250	–	MHz
Collector-Base Capacitance at V_{CB} = 10 V, I_E = 0 mA, f = 1 MHz	C_{ob}	–	4.3	–	pF
Switching Times at V_{SUP} = 5 V, V_I = 5 V, R_L = 1 kΩ Rise Time Storage Time Fall Time	 t_r t_s t_f	 – – –	 0.12 2.0 0.35	 – – –	 µs µs µs



Layout for R_{thA} test
Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm

Germany
ITT INTERMETALL
Hans-Bunte-Strasse 19
D-79108 Freiburg
P.O. Box 840
D-79008 Freiburg
Tel. ++49-761-517-0
Fax ++49-761-517-2174

Hong Kong
ITT Semiconductors (FE) Ltd.
Room 5, 15th Floor, Block B,
Veristrong Industrial Centre
No. 34-36, Au Pui Wan Street
Fo Tan, Shatin
New Territories
Hong Kong
Tel. ++852-2688-0894
Fax ++852-2687-4861

Japan
ITT Semiconductors (FE) Ltd.
P.O. Box 47
18th Floor, Sumitomo Building
Shinjuku-ku
Tokyo 163-02
Tel. ++81-3-3347-8881
Fax ++81-3-3347-8844

Singapore
ITT Semiconductors (FE) Ltd.
Representative Office
150 Orchard Road # 07-13
Orchard Plaza
Singapore 0923
Tel. ++65-732-65-66
Fax ++65-737-73-92

United Kingdom
ITT Semiconductors UK
(for Discrete Semiconductors)
Ms. Julie Voller
Jays Close
Viables Industrial Estate
Basingstoke
Hampshire RG22 4BW
Tel. ++44-1256-346-394
Fax ++44-1256-346-395

ITT Semiconductors UK
(for Integrated Circuits)
Mr. John Thorogood
P.O. Box 1827
Granborough
Bucks. MK18 3ZT
Tel. ++44-1926-670-670
Fax ++44-1926-670-676

ITT Semiconductors UK
(for Integrated Circuits)
Mr. Julian Richards
P.O. Box 81
Guildford
Surrey GU2 6FY
Tel. ++44-1483-566-333
Fax ++44-1483-566-332

USA
Sales Headquarters:
ITT Semiconductors
2500 West Higgins Road
Suite 1015
Hoffman Estates, IL 60195
Tel. ++1-847-519-9610
Fax ++1-847-519-9615

Central Area:
ITT Semiconductors
909 West Maumee Street
Elmhurst Building
Angola, IN 46703
Tel. ++1-219-833-1960
Fax ++1-219-665-2811

Western Area:
ITT Semiconductors
2635 North First Street
Suite 101
San José, CA 95134
Tel. ++1-408 526-2084
Fax ++1-408 324-1379

ITT INTERMETALL Distributors / Agents

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Padstow NSW 2211
Tel. (02) 792 3922
Fax (02) 792 1446

Austria
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Vertriebsgesellschaft m.b.H.
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A-1232 Wien
Tel. (0431) 6 10 66-0
Fax (0431) 6 10 66-10

SPOERLE ELECTRONIC
Distribution International
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A-1190 Wien
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Fax (02 22) 3 69 22 73

Belgium
SPOERLE ELECTRONIC
Distribution International
GmbH
Keiberg II
Minervastraat, 14/B2
B-1930 Zaventem
Tel. (02) 725 46 60
Fax (02) 725 45 11

Canada
Farnell Electronic Services
300 North Rivermede Road
Concord, Ontario L4K 2Z4
Tel. (416) 798-4884
Fax (416) 798-4889

China
Walasey Ltd.
Shanghai Liaison Office
Room 1708, Block 1
Hu Ban Building
1250, Zhong Shan Rd.,
North, #1
Shanghai
P.R.C.
Tel. (21) 516-1882
or (21) 542-4152
Fax (21) 542-4152

Czech Republic
SPOERLE ELECTRONIC
spol. s.r.o.
Charkovska 24
101 00 Praha
Tel. (2) 73 13 55
Fax (2) 73 13 54

Denmark
Farnell Electronic Services
Naverland 29
DK-2600 Glostrup
Tel. (42) 45 66 45
Fax (42) 45 07 86

Finland
Farnell Electronic Services
Työpajakatu 5
SF-00580 Helsinki
Tel. (0) 4766-0
Fax (0) 4766-6318

France
ARROW ELECTRONIQUE
78-79, rue des Solets
Silic 585
F-94663 Rungis CEDEX
Tel. (1) 49 78 49 78
Fax (1) 49 78 05 96

Farnell Electronic Services
P.O. Box 69 - St. Aubin
F-91192 Gif s/Yvette CEDEX
Tel. (1) 6 98 58-383
Fax (1) 6 98 58-399

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63, rue Jean Jaures
P.O. Box 116
F-95874 Bezons CEDEX
Tel. (1) 34 23 70 00
Fax (1) 30 76 31 97

ITT INTERMETALL
Mr. Francois Boubet
Agent Technico-Commercial
11, rue de Rimoron
F-91650 Breux-Jouy
Tel. (1) 64 58 60 60
Fax (1) 64 58 60 60

Rutronik
Composants Electroniques
Le Saillant
F-19130 Voutezac
Tel. (55) 84 74 83
Fax (55) 84 79 00

Germany
Beck GmbH & Co.
Eltersdorfer Strasse 7
D-90425 Nürnberg
Tel. (0911) 9 34 08-0
Fax (0911) 9 34 08-28

Farnell Electronic Services
Bahnhofstrasse 44
D-71696 Möglingen
Tel. (07141) 487-0
Fax (07141) 487-210

Future Electronics
Deutschland GmbH
Münchner Str. 18
D-85774 Unterföhring
Tel. (089) 957 27-0
Fax (089) 957 27-173

RUTRONIK
Elektronische Bauelemente
GmbH
RSC-Halbleiter GmbH
Industriestrasse 2
D-75228 Ispringen
Tel. (07231) 801-0
Fax (07231) 822 82

SPOERLE ELECTRONIC
Max-Planck-Strasse 1-3
D-63303 Dreieich
Tel. (06103) 304-8
Fax (06103) 304-455

Hong Kong
Walasey Ltd.
Room 1010, 10th Floor
APEC Plaza
No. 49, Hoi Yuen Road
Kwun Tong
Kowloon
Hong Kong
Tel. 2357-1676
Fax 2357-1189

ARRAY Electronics Ltd.
24th Floor, Wyler Centre,
Phase 2
No. 200, Tai Lin Pai Road
Kwai Chung
New Territories
Hong Kong
Tel. 2418-3700 or 2418-3800
Fax 2418-6992 or 2418-6993

Italy
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Viale Milanofiori, E5
I-20090 Assago (Milano)
Tel. (02) 82 470 232
Fax (02) 82 426 31

Silverstar Ltd. S.P.A.
Viale Fulvio Testi, 280
20126 Milano, MI
Tel. (02) 66 12 51
Fax (02) 66 10 13 59

Rebosio Componenti S.P.A.
Viale G. Prati, 3
20051 Limbiate (Milano)
Tel. (02) 99 65 767
Fax (02) 99 62 968

Farnell S.P.A.
Viale Milanofiori E/5
20094 Assago (Milano)
Tel. (02) 82 470
Fax (02) 82 42 631

Eurodis Fanton S.R.L.
Via Olindo Simoni, 8
40011 Anzola d'Emilia, BO
Tel. (05) 17 35 015
Fax (05) 17 35 013

Japan
UNI Electronics Inc.
P.O. Box 68
Sumitomo Building
Shinjuku-ku
Tokyo 163
Tel. (03) 33 47-8878
Fax (03) 33 47-8808

Korea
SOEI KOREA Inc.
WooNam Building, 4th Floor
824-22, Yeoksam-dong
Kangnam-ku
Seoul 135-080
Tel. (02) 508 3221
Fax (02) 508 3229

Netherlands
SPOERLE ELECTRONIC
Distribution International
GmbH
Coltbaan 17
NL-3439 NG Nieuwegein
Tel. (03402) 912 34
Fax (03402) 467 64/359 24

Farnell Electronic Services
Chroomstraat 28
NL-2718 RR Zoetermeer
Tel. (079) 613-161
Fax (079) 613-169

Norway
Farnell Electronic Services
Karihaugun 89
N-1001 Oslo
Tel. (47) 2232-1270
Fax (47) 2232-5120

Poland
SPOERLE ELECTRONIC
Polska Sp. z.o.o.
ul. Domaniewska 41
02-672 Warschau
Tel. (22) 640 03 49
or (22) 640 04 47/48/49
Fax (22) 640 03 48

Singapore
UNI Electronics PTE. Ltd.
1 Tanglin Road #03-260
Orchard Parade Hotel
(Podium Block)
Singapore 1024
Tel. (+65) 235 77 40
or (+65) 235 82 57
Fax (+65) 235 52 98

South Africa
Electronic Building Elements
(Pty) Ltd.
P.O. Box 912-1222
Silverton, 0127
Tel. (012) 803-7680
Fax (012) 803-8294

Spain
AKTA SPAIN S.A.
Roger de Llúria, 155
ENTLO 2.ª
E-08037 Barcelona
Tel. (3) 218 49 49 - 415 22 66
Fax (3) 237 07 80

AMITRON-ARROW S.A.
Albasanz, 75
E-28037 Madrid
Tel. (1) 304 30 40
Fax (1) 327 24 72

Sweden
Farnell Electronic Services
Ankdammsgatan 32
P.O. Box 1330
S-17126 Solna
Tel. (08) 83 00 20
Fax (08) 27 13 03

Ericsson Procomp
Isafjordsgatan 16
S-16481 Kista-Stockholm
Tel. (08) 757 40 40
Fax (08) 757 41 10

Switzerland
Farnell Electronic Services
Brandschenkestrasse 178
CH-8027 Zürich
Tel. (01) 2 04 61 11
Fax (01) 2 04 64 54

AKTA Multikomponent AG
Alte Steinhauserstr. 3
Postfach 5039
CH-6330 Cham
Tel. (041) 740 14 42
Fax (041) 740 13 23

SPOERLE ELECTRONIC
Distribution International
GmbH
Cherstr. 4
Postfach
CH-8152 Opfikon-Glattbrugg
Tel. (01) 1 874 6262
Fax (01) 1 874 6200

SPOERLE ELECTRONIC
Distribution International
GmbH
En Chamard
CH-1442 Montagny s/Yverdon
Tel. (024) 27 01 00
Fax (024) 24 52 45

Taiwan
WesTech Electronics, Inc.
P.O. Box 55-0466
5F, No. 197
Ho Ping E. Road, Sec. 1
Taipei, Taiwan 106, R.O.C.
Tel. (02) 356-0620
Fax (02) 394-2047

Turkey
BIGSTAR
Elektronik Sanayi
ve Ticaret A.S.
Okcu Musa Cad. 69/2
TR-80020 Karaköy-Istanbul
Tel. (0) 212 252 59 15
(3 lines)
Fax (0) 212 252 54 38

INTER A.S.
Kadiköy Hasircibasi
Caddesi No. 55
TR-81310 Istanbul
Tel. (0) 216 349 94 00
(30 lines)
Fax (0) 216 349 94 30

United Kingdom
ARROW Electronics (UK) Ltd.
St. Martins Business Centre
Cambridge Road
Bedford MK42 0LF
Tel. (01234) 34 72 11
Fax (01234) 21 46 74

Farnell Electronic Services
Edinburgh Way
Harlow, Essex
CM20 2DF
Tel. (01279) 44 11 44
Fax (01279) 44 16 87

First Principals Ltd.
2 Walker Road
Bardon Hill
Coalville
Leicestershire LE67 1TU
Tel. (01530) 51 12 95
Fax (01530) 51 12 96

Flint Distribution Ltd.
Enterprise House
Ashby Road
Coalville
Leicestershire LE67 3LA
Tel. (01530) 51 03 35
Fax (01530) 51 02 75

Future Electronics Ltd.
Future House
Poyle Road
Colnbrook Slough, Berks.
SL3 0EZ
Tel. (01075) 368 70 00
Fax (01075) 368 91 00

HB Electronics Ltd.
Lever Street
Bolton, Lancs.
B13 6BJ
Tel. (01204) 38 63 61
Fax (01204) 38 49 11

Farnell Electronic Services
346 Edinburgh Avenue
Slough
SL1 4TU
Tel. (01753) 82 42 12
Fax (01753) 82 41 60

USA
Diodes Incorporated
3050 East Hillcrest Drive
Westlake Village, CA 91362
Tel. (805) 446-4800
Fax (805) 446-4850

Alphanumerical List of Types

ITT INTERMETALL
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-7 61-5 17-0
Fax +49-7 61-5 17-21 74
E-mail: docservice@itt-sc.de
Internet: http://www.itt-sc.de

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