AC4601 芯片规格书

珠海市杰理科技有限公司

版本：V1.1

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AC4601 Features

High performance 32-bit RISC CPU

- RISC CPU
- DC-160MHz operation
- Support DSP instructions
- 32 Vectored interrupts
- 4 Levels interrupt priority

Flexible I/O

- 28 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

Digital Peripheral Feature

- Bluetooth V2.1+EDR baseband and modem
- FM receiver with stereo decoder and 50uS deemphasis
- Four multi-function 16-bit timers, support capture and PWM mode
- One 16-bit active parallel port
- One full-duplex basic UART
- Two full-duplex advanced UART
- Two SPI interface supports host and device mode
- Two SD Card Host controller
- One audio interface supports IIS, left adjusted, right adjusted and DSP mode
- One full speed USB 2.0 OTG controller
- Watchdog

Analog Peripheral Features

- Bluetooth RF with frequency synthesizer
- FM RF with frequency synthesizer，76-108MHz，100KHz step
- Three Crystal Oscillator
- Full speed USB 2.0 PHY
- 160MHz PLL-based clock generator
- 16-bit Stereo DAC, SNR > 93dB
- 4 channels Stereo ADC with 1 channel MIC amplifier, SNR>72dB
- Embedded headphone amplifier
- 2 channels analog MUX
- 8 channels 10-bit ADC
- 2 channels 4 levels Low Voltage Detector
- Built in Cap Sense Key controller

- Power-on reset
- Two LDO: 5V to 1.8V, 5V to 3.3V

Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth 2.1 + EDR specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Provides +4dbm transmitting power
- receiver with -85dBm sensitivity

FM Tuner

- Support worldwide frequency band 76-108MHz
- Digital low-IF tuner
- Fully integrated digital frequency synthesizer
- Autonomous search tuning
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
- Programmable de-emphasis (50/75 ms)
- Receive signal strength indicator (RSSI)
- Bass boost
- Volume control

Power Supply

- VDDLDO is 3.3V to 5.5V
- VDDIO is 3.0V to 3.6V

Packages

- LQFP48 7x7
- DIE form

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

一、引脚定义

1.1 引脚分配

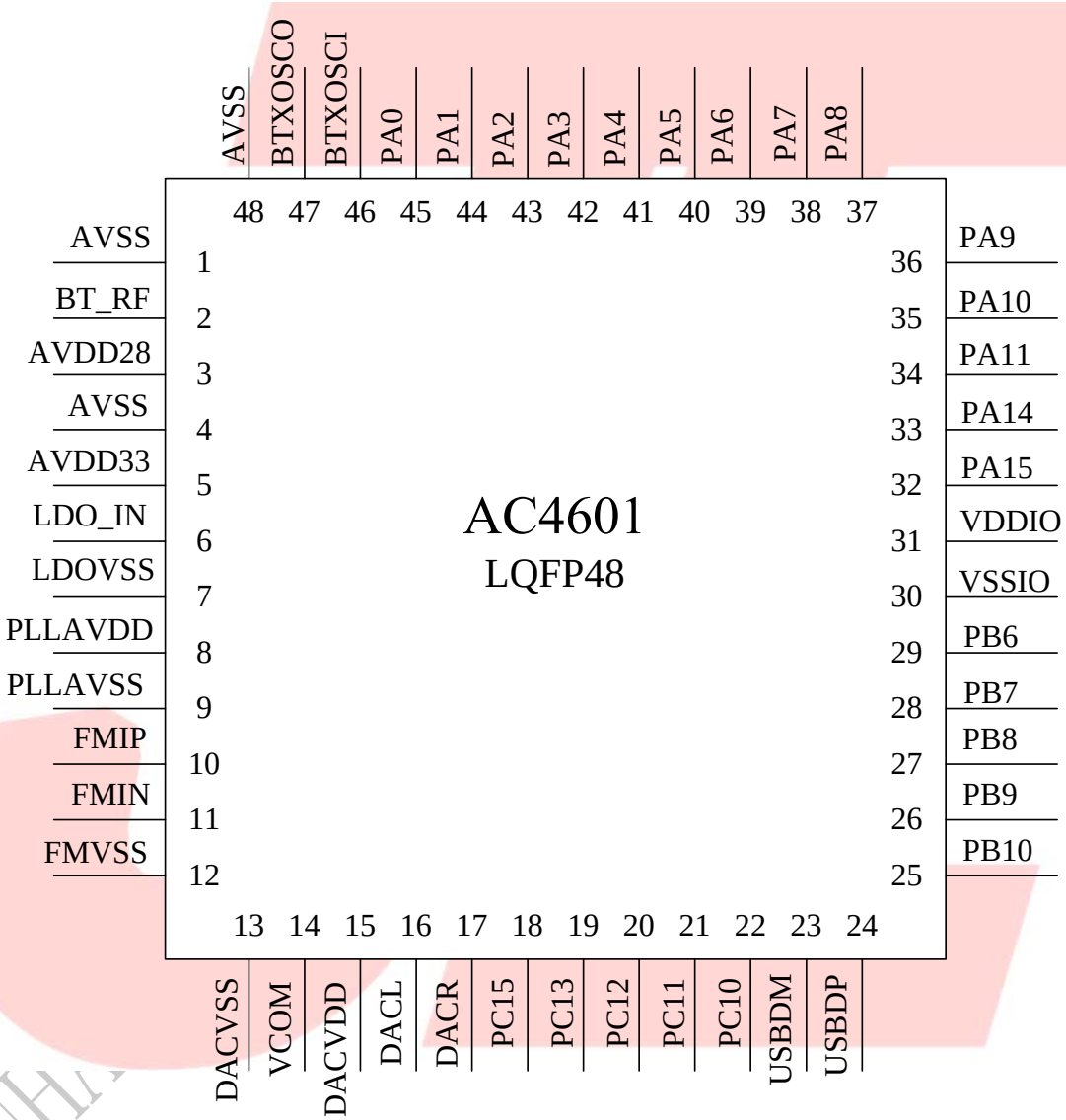


图 1-1 AC4601_LQFP48 引脚分配图

1.2 引脚描述

表 1-1 AC4601_LQFP48 引脚描述

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	AVSS	P	/	Analog Ground	
2	BT_RF	P	/		
3	AVDD28	P	/	Analog Power 2.8v	
4	AVSS	P	/	Analog Ground	
5	AVDD33	P	/	Analog Power 3.3v	
6	LDO_IN	P	/	LDO Power 5v	
7	LDOVSS	P	/	LDO Ground	
8	PLLAVDD	P	/		
9	PLLAVSS	P	/		
10	FMIP	I	/		
11	FMIN	I	/		
12	FMVSS	P	/	FM Analog Ground	
13	DACVSS	P	/	DAC Ground	
14	VCOM	P	/	DAC Reference	
15	DACVDD	P	/	DAC Power	
16	DACL	O	/	DAC Left Channel	
17	DACR	O	/	DAC Right Channel	
18	PC15	I/O	16	GPIO	MIC; AMUX2R：Simulator Channel2 Right; 12BitADC;
19	PC13	I/O	16	GPIO	AMUX1R：Simulator Channel1 Right; 12BitADC; UART2RXD：Uart2 Data Out(D);
20	PC12	I/O	16	GPIO	AMUX1L：Simulator Channel 1 Left; 12BitADC; UART2TXD：Uart2 Data In(D); ALNK_MCLKB：Audio Link Master Clk(B);
21	PC11	I/O	16	GPIO	SD1DAT2A：SD1 Data2(A); AMUX0R：Simulator Channel0

					Right; ALNK_LRCKB：Audio Link Clk(B);
22	PC10	I/O	16	GPIO	SD1DAT3A：SD1 Data3(A); AMUX0L：Simulator Channel0 left; ALNK_SCLKB：Audio Link Clk(B);
23	USBDM	I/O	4	USB Negative Data	
24	USBDP	I/O	4	USB Positive Data	
25	PB10	I/O	16	GPIO	Wakeup12：Port Interrupt/Wakeup12; CAP2：Timer2 Capture; UART0TXB：Uart0 Data Out(B); DACL：DAC Left Channel; COM4：LCD COM Output 4;
26	PB9	I/O	16	GPIO	TMR3：Timer3 Clock Input; UART2RXC：Uart2 Data In(C); DACCK：DAC Clk; COM3：LCD COM Output 3;
27	PB8	I/O	16	GPIO	UART2TXC：Uart2 Data Out(C); COM2：LCD COM Output 2;
28	PB7	I/O	16	GPIO	UART1RXC：Uart1 Data In(C); SPI1DOB：SPI1 Data Out(B); IIC_SDA_B：IIC SDA(B); COM1：LCD COM Output 1;
29	PB6	I/O	16	GPIO	PWM0：Timer0 PWM Output; UART1TXC：Uart1 Data Out(C); SPI1CLKB：SPI1 Clk(B); IIC_SCL_B：IIC SCL(B); COM0：LCD COM Output 0;
30	VSSIO	P	/	IO Ground	
31	VDDIO	P	/	IO Power 3.3v	
32	PA15	I/O	16	GPIO	TMR1：Timer1 Clock Input; SPI1DOA：SPI1 Data Out(A); PAPD15：PAP Data 15; SEG15：LCD SEG Output15;
33	PA14	I/O	16	GPIO	Wakeup13：Port Interrupt /Wakeup 13; ADC7：ADC Input Channel 7; SPI1CLKA：SPI1 Clk(A); PAPD14：PAP Data(14);

					ALNK_MCLKA：Audio Link Master Clk(A); SEG14：LCD SEG Output14;
34	PA11	I/O	16	GPIO	ADC6：ADC Input Channel 6; UART2RXB：Uart2 Data In(B); PAPD11：PAP Data11; ALNK_DAT3A：Audio Link Data3(A); SEG11：LCD SEG Output11;
35	PA10	I/O	16	GPIO	Wakeup10：Port Interrupt /Wakeup 10; CAP3：Timer3 Capture; UART2TXB：Uart2 Data Out(B); PAPD10：PAP Data10; ALNK_DAT2A：Audio Link Data2(A); SEG10：LCD SEG Output10;
36	PA9	I/O	16	GPIO	UART0RX：Uart0 Data In(A); PAPD：PAP Data9; ALNK_DAT1A：Audio Link Data1(A); SEG9：LCD SEG Output9;
37	PA8	I/O	16	GPIO	Wakeup3：Port Interrupt /Wakeup 3; ADC5：ADC Input Channel 5; UART0TXA：Uart0 Data Out(A); PAPD8：PAP Data8; ALNK_DAT0A：Audio Link Data0(A); SEG8：LCD SEG Output8;
38	PA7	I/O	16	GPIO	UART1RXA：Uart1 Data In(A); PAPD7：PAP Data7; SEG7：LCD SEG Output7;
39	PA6	I/O	16	GPIO	Wakeup9：Port Interrupt /Wakeup 9; TMR0：Timer0 Clock Input； UART1TXA：Uart1 Data Out(A); PAPD6：PAP Data6; SEG6：LCD SEG Output6;
40	PA5	I/O	16	GPIO	ADC4：ADC Input Channel 4; CAP0：Timer0 Capture; SD0DAT2B：SD0 Data2(B); PAPD5：PAP Data5; CLKOUT1：Clk Out1; UART2RXA：Uart2 Data In(A);

					SEG5： LCD SEG Output5;
41	PA4	I/O	16	GPIO	Wakeup8：Port Interrupt /Wakeup 8; SD0DAT3B：SD0 Data3(B); PAPD4： PAP Data4; CLKOUT0：Clk Out0; UART2TXA： Uart2 Data Out(A); SEG4：LCD SEG Output4;
42	PA3	I/O	16	GPIO	ADC3：ADC Input Channel 3; SD0CLKB:SD0 Clk(B); PAPD3：PAP Data3; SEG3：LCD SEG Output3;
43	PA2	I/O	16	GPIO	ADC2：ADC Input Channel 2; SD0CMDB：SD0 Command(B); PAPD2：PAP Data1; SEG2：LCD SEG Output2;
44	PA1	I/O	16	GPIO	ADC1：ADC Input Channel 1; PWM3：Timer3 PWM Output; SD0DAT0B：SD0 Data0(B); PAPD1：PAP Data1; SEG1：LCD SEG Output1;
45	PA0	I/O	16	GPIO	Wakeup2：Port Interrupt /Wakeup 2; ADC0：ADC Input Channel 0; CAP1：Timer1 Capture; SD0DAT1B：SD0 Data1(B); PAPD0：PAP Data0; SEG0：LCD SEG Output0;
46	BTXOSCI			OSC In	
47	BTXOSCO			OSC Out	
48	AVSS	P	/	Analog Ground	

二、电气特性

2.1 LDO 电压、电流特性

表 2-1

符号	参数	最小	典型	最大	单位	测试条件
LDO5V	Voltage Input	3.3	4.6	5.5	V	_
$V_{3.3}$	Voltage output	_	3.3	_	V	LDO5V = 5V, 100mA loading
$V_{1.8}$		_	1.8	_	V	LDO5V = 5V, 50mA loading
V_{DACVDD}	DAC Voltage	_	3.1	_	V	LDO5V = 5V, 10mA loading
$I_{L3.3}$	Loading current	_	_	150	mA	LDO5V = 5V

2.2 IO 输入、输出高低逻辑特性

表 2-2

IO 输入特性						
符号	参数	最小	典型	最大	单位	测试条件
V_{IL}	Low-Level Input Voltaget	-0.3	_	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	_	VDDIO+0.3	V	VDDIO = 3.3V
IO 输出特性						
V_{OL}	Low-Level Output Voltaget	_	_	0.33	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltaget	2.7	_	_	V	VDDIO = 3.3V

2.3 IO 输出能力、上下拉电阻特性

表 2-3

Port 口	普通输出	强输出	上拉电阻	下拉电阻	备注
PA0~PA15、PB0~PB15、PR0~PR3	串接 250 欧电阻（寄存器可控制）	16mA	10K	60K	1、PA8 default pulldown 2、内部上下拉阻抗因工艺波动差异，可能存在±20%的偏差
PC0~PC15、PD0~PD7	8mA	24mA	10K	60K	

DAC 特性

表 2-4

参数	最小	典型	最大	单位	测试条件
Frequency Response	20	_	200000	Hz	_
THD+N	_	0.014	_	%	1KHz out = 1V RMS
S/N	_	93	_	dB	1KHz out = 1V RMS
Channel Separation	_	80	_	dB	_
DAC Output Power	_	>15	_	mW	32ohm loading

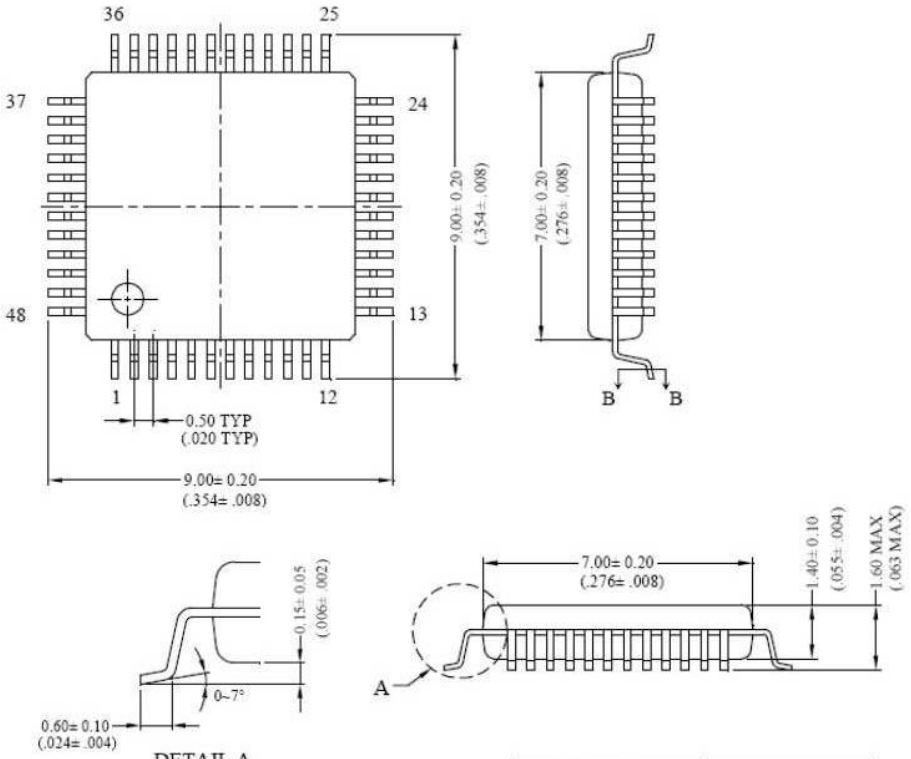
BT 特性

表 2-5

参数	最小	典型	最大	单位	测试条件
Maximum Output Power	_	4	_	dBm	_
RMS DEVM	_	5.3	_	%	Maximum output power
PEAK DEVM	_	12	_	%	
99% DEVM	_	8	_	%	
EDR Relative Power	_	-1.4	_	dB	
BDR Sensitivity	_	-84	_	dBm	BER=0.001
EDR Sensitivity	_	-85	_	dBm	BER=0.0001

三、封装

3.1 LQFP48_7*7



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
J	0.107	0.197	.0042	.0076
J1	0.107	0.147	.0042	.0058
K	0.200	0.250	.0079	.0098
K1	0.200	0.300	.0079	.0118

引线间距 Lead Pitch	0.50mm(19.7mil)
载体尺寸 Pad Size	205mil×205mil
载体打凹深度 Depressed Die Pad	0.120±0.025 (0.007±0.001)
单位 Unit	mm(inch)

图 3-1 AC4601_LQFP48 封装图

四、版本信息

日期	版本号	描述
2015.3.30	V1.0	原始版本
2015.7.28	V1.1	增加内部上下拉电阻误差说明