RDA5830/1

SINGLE-CHIP BROADCAST FM/AM/LW/SW RECEIVER *Rev.2.0–Mar..2009*

1 General Description

The RDA5830/1 is a single-chip broadcast FM/AM/LW/SW (LW/SW only for RDA5830) receiver with fully integrated synthesizer, IF selectivity and MPX decoder. The chip uses the CMOS process, support multi-interface and require the least external component. The package size is 4X4mm and is completely adjustment-free. All these make it very suitable for portable devices.

The RDA5830/1 has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5830/1 use auto frequency calibration, this make it have perfectly performance and agility.

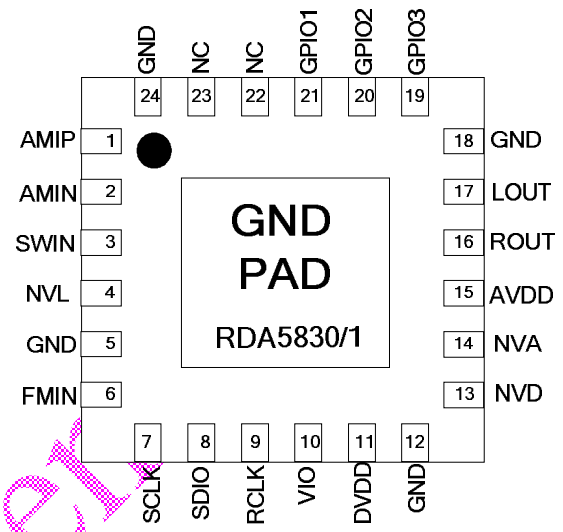


Figure 1-1. RDA5830/1 Top View

The RDA5830/1 support world band FM/AM（RDA5831 alos suppory LW/SW） frequency band receive, support weather band and also support RDS/RBDS receive .

The RDA5830/1 directly support wide power supply range (1.8V~5V).

1.1 Features

- CMOS single-chip fully-integrated FM/AM receiver
- Low power consumption
  - Total current consumption lower than 20mA at FM mode and 23mA at AM mode
- Support worldwide and campus frequency band
  - 500-2000 KHz AM band
  - 65-220 MHz FM band
  - 150-500KHz LW band (RDA5831 only)
  - 2-30MHz SW band (RDA5831 only)
  - Weather band
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support RDS/RBDS receive
- Support SNR FM searching
- Include 4K memory
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
  - Mono/stereo switch
  - Soft mute
  - High cut
- Programmable de-emphasis (50/75 μs)

- Receive signal strength indicator (RSSI)
- Bass boost
- Volume control
- Support I2S digital interface
- Support audio power amplifier (32Ω resistance loading)
- Line-level analog output voltage
- 4X4mm 24 pin QFN package

1.2 Applications

- Cellular handsets
- FM/AM stereo recivers
- CD/DVD

2 Table of Contents

3 Functional Description

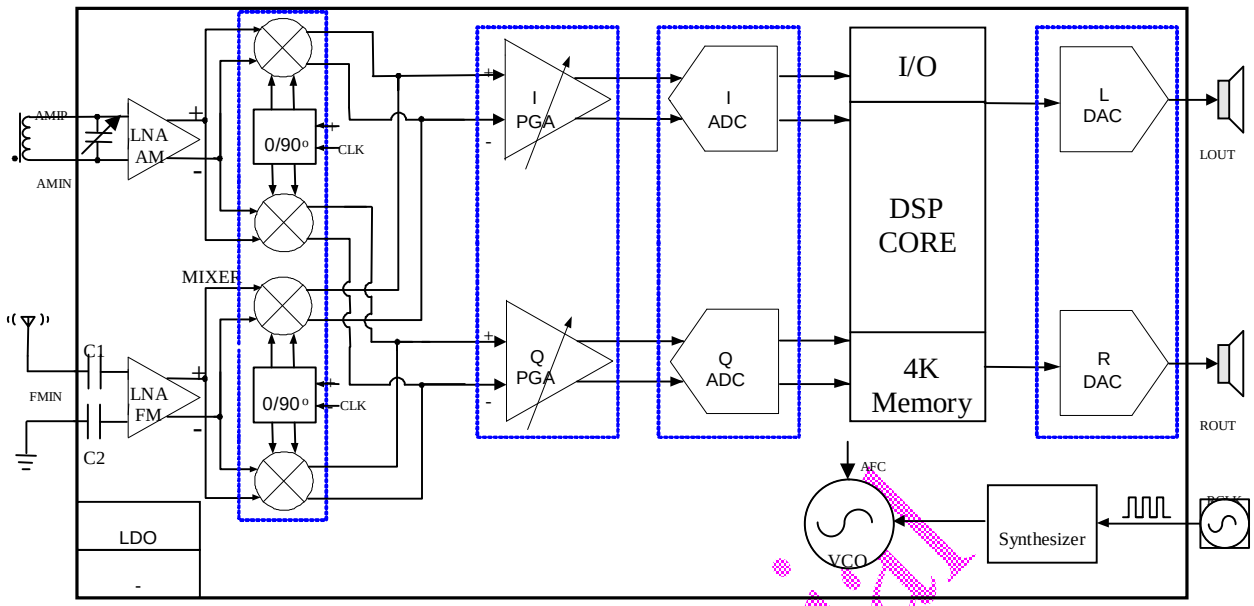


Figure 3-1. RDA5830 FM/AM Receiver Block Diagram

3.1 FM/AM Receiver Structure

The RDA5830/1 is a single-chip FM/AM/LW/SW receiver (FM/AM Rx). It has perfectly FM/AM receive performances, also least external components. The RDA5830/1 integrate 4K memory, this make it have additional advantage such as saving frequency or datas.

Except FM/AM receive , the RDA5830/1 also have RDS/RBDS, I2S input/output, weather band. All these make it very suitable for portable devices.

3.2 FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (FM LNA) supporting the FM broadcast band (65 to 115MHz), a quadrature image-reject mixer, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA_FM has differential input ports, in RDA5830/1, we only use one port as input, and the other port directly connect to gnd.

The quadrature mixer down converts the LNA output differential RF signal to low-IF, it also has image-reject function.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

3.3 AM Receiver

In AM mode, the AM signal would captured by loop stick, and amplified by LNA_AM, down conversed whith AM mixer. The following steps same as FM mode.

3.4 Synthesizer

The frequency synthesizer (including synthesizer and VCO) generates the local oscillator signal which divide to quadrature, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer1 frequency is defined by bits CHAN[9:0] with the range from 65MHz to 115MHz in FM mode and 500K to 1710KHz in AM mode.

3.5 Power Supply

The RDA5830/1 integrated one LDO which supplies power to the chip and a DC-DC which support lower power supply. The external supply voltage range is 1.8-5.5 V when don't use integrated DC-DC. The DC-DC have auto wake-up function when supply voltage lower than 2V, and output constant 2V voltage.

3.6 RESET

The RDA5830/1 is RESET itself When VIO is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1.

3.7 Control Interface

The RDA5830/1 only supports I^2C control interface. User could select either of them to program the chip.

The I^2C interface is compliant to I^2C Bus Specification 2.1. It includes two pins: SCLK and SDIO. A I^2C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010001b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5830/1.

Details refer to *RDA5830/1 Programming Guide*.

3.8 I^2S Audio Data Interface

The RDA5830/1 supports I^2S (Inter_IC Sound Bus) audio interface. The interface is fully compliant with I^2S bus specification. When setting I2SEN bit high, RDA5830/1 will output SCK, WS, SD signals from GPIO3, GPIO1, GPIO2 as I^2S master and transmitter, the sample rate is 42Kbps.

3.9 GPIO Outputs

The RDA5830/1 has three GPIOs. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST. Constant low, high or high-Z functionality is available regardless of the state of VDD supplies or the ENABLE bit.

4 Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Supply Voltage	1.8	3.3	5.5	V
VIO	Interface Supply Voltage	1.5	-	3.6	V
T_{amb}	Ambient Temperature	-20	27	+70	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*DVDD	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDD		DVDD	V
V_{TH}	CMOS Threshold Voltage		0.5*VDD		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VIO	Interface Supply Voltage	-0.5		+4	V
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current (1)	-10		+10	mA
V_{IN}	Input Voltage(1)	-0.3		VIO+0.3	V
V_{lna}	LNA FM Input Level			10	dBm

Notes:

1. For Pin: SCLK, SDIO

Table 4-3 Power Consumption Specification

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 ℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
I_A	Analog Supply Current	ENABLE=1	18	mA
I_D	Digital Supply Current	ENABLE=1	3	mA
I_{VIO}	Interface Supply Current	SCLK and RCLK inactive	5	μA
I_{APD}	Analog Powerdown Current	ENABLE=0	3	μA
I_{DPD}	Digital Powerdown Current	ENABLE=0	1	μA

5 Receiver Characteristics

Table 5-1 FM Receiver Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{in}	FM Input Frequency	BAND=0	87		108	MHz
		BAND=1	76		91	MHz
V_{rf}	Sensitivity[1,2,3]	(S+N)/N=26dB		1.6	2	μV EMF
R_{in}	LNA Input Resistance [7]			150		Ω
C_{in}	LNA Input Capacitance [7]		2	4	6	pF
$IP3_{in}$	Input IP3[4]	AGCD=1	80		-	dBμV
α_{am}	AM Suppression[1,2]	m=0.3	40	-	-	dB
S_{200}	Adjacent Channel Selectivity	±200KHz	45		-	dB
V_{AFL}; V_{AFR}	Left and Right Audio Frequency Output Voltage (Pins LOUT and ROUT)	Volume [3:0] =1111		200		mV
(S+N)/N	Maximum Signal Plus Noise to Noise Ratio[1,2,3,5]		54	60	-	dB
α_{SCS}	Stereo Channel Separation		35	-	-	dB
THD	Audio Total Harmonic Distortion[1,3,6]			0.05	0.1	%
α_{AOI}	Audio Output L/R Imbalance				0.1	dB
R_L	Audio Output Loading Resistance	Single-ended	32	-	-	Ω
Pins AMIP, AMIN, SWIN, FMIN, LOUT, ROUT and NC(22,23)						
V_{com_am}	Pin AMIP/AMIN Input Common Mode Voltage			**1**		V
V_{com_swin}	Pin SWIN Input Common Mode Voltage			**1**		V
V_{com_fmin}	Pin FMIN Input Common Mode Voltage			**floate**		V
$V_{com\_lout/rout}$	Audio Output Common Mode Voltage[8]		0.9	1.0	1.1	V
V_{com_nc}	Pins NC (22, 23) Common Mode Voltage			floate		V
! The NC(22, 23) pins SHOULD BE left floating.						

Notes:

1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;

2. Δf=22.5KHz; 3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz; 4. $|f_2-f_1|$>1MHz, $f_0=2xf_1-f_2$, AGC disable, F_{in}=76 to 108MHz; 5. P_{RF}=60dB$_U$V; 6. Δf=75KHz; 7. Measured at V_{EMF} = 1 m V, f_{RF} = 76 to 108MHz; 8. At LOUT and ROUT pins

Table 5-2 AM Receiver Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{AM}	Input Frequency	Medium Wave (AM)	500	—	2000	kHz
	Sensitivity[1,2,3]	(S+N)/N= 26 dB	—	35	—	μV EMF
	Large Signal Voltage Handling[4]	THD < 8%	—	200	—	mV_{RMS}
	Power Supply Rejection Ratio	ΔV_{DD} = 100 mV_{RMS},100 Hz	—	40	—	dB
	Audio Output Voltage[1,5]		—	200	—	mV_{RMS}
	Audio S/N[1,2,3,5]			48	—	dB
	Audio THD[1,3,5]		—	—	1	%
	Antenna Inductance	Medium Wave (AM)	180	—	400	μH
	Power Up Time	From power down		—	200	ms

NOTE：

1. FMOD = 1kHz , 30%modulation , A-weighted , 2 kHz channel filter.
2. B_{AF} = 300 Hz to 15kHz , A-weighted.
3. f_{RF} = 1000kHz , Δf =10kHz.
4. Guaranteed by characterization.
5. V_{IN} =5 mV_{RMS}.

6 Serial Interface

6.1 I²C Interface Timing

Table 6-1 I²C Interface Timing Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	400	KHz
SCLK High Time	t_{high}		0.6	-	-	µs
SCLK Low Time	t_{low}		1.3	-	-	µs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	µs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	µs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	µs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	µs
SDIO Output Fall Time	$t_{f:out}$		$20+0.1C_b$	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		$20+0.1C_b$	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF

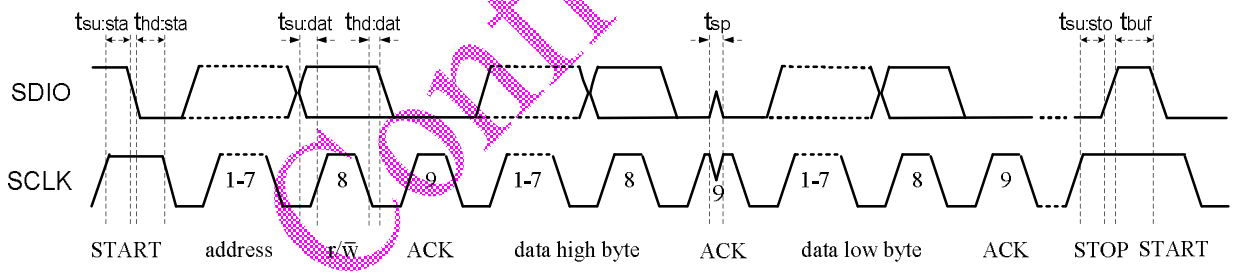


Figure 6-1. I²C Interface Write Timing Diagram

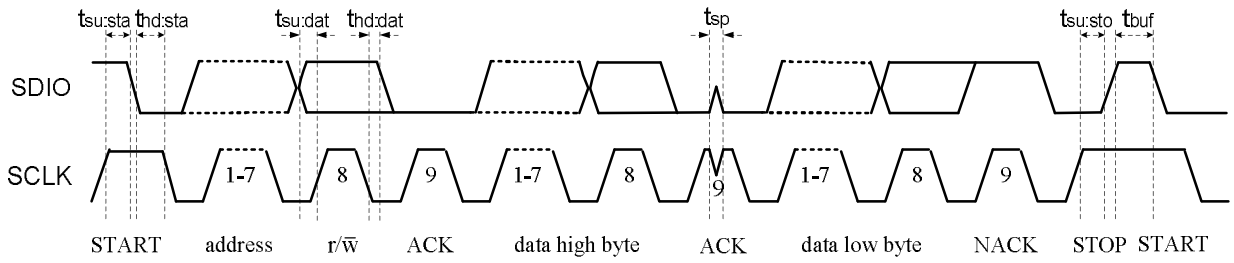


Figure 6-2. I²C Interface Read Timing Diagram

7 Register Definition

REG	BITS	NAME	FUNCTION	DEFAULT
00H	15:8	CHIPID[7:0]	Chip ID.	0x58
02H	15	DHIZ	Audio Output High-Z Disable. *0 = High impedance; 1 = Normal operation*	0
	14	DMUTE	Mute Disable. *0 = Mute; 1 = Normal operation*	0
	13	MONO	Mono Select. *0 = Stereo; 1 = Force mono*	0
	12	BASS	Bass Boost. *0 = Disabled; 1 = Bass boost enabled*	0
	9	SEEKUP	Seek Up. *0 = Seek down; 1 = Seek up*	0
	8	SEEK	Seek. *0 = Disable; 1 = Enable* *Seek begins in the direction specified by SEEKUP and ends when a channel is found with RSSI level above SEEKTH[5:0], or the entire band has been searched.* *The SEEK bit is set low and the STC bit is set high when the seek operation completes.*	0
	7	SKMODE	Seek Mode 0 = wrap at the upper or lower band limit and continue seeking 1 = stop seeking at the upper or lower band limit	0
	6:4	CLK_MODE[2:0]	000=32.768kHz 001=12Mhz 101=24Mhz 010=13Mhz 110=26Mhz 011=19.2Mhz 111=38.4Mhz 100=others(need user define)	000
	3	RDS_EN	RDS Enable 0 = Disabled 1 = Enable	0
	4	RESERVED		0

REG	BITS	NAME	FUNCTION	DEFAULT
	1	SOFT_RESET	Soft reset. If 0, not reset; If 1, reset.	0
	0	ENABLE	Power Up Enable. *0 = Disabled; 1 = Enabled*	0
03H	15:8	FM_CHAN[9:0]	FM_Band Channel Select. BAND = *0* *Frequency = Channel Spacing (kHz) x* CHAN+ *87.5 MHz* BAND = *1* *Frequency = Channel Spacing (kHz) x* CHAN + *76.0 MHz* CHAN *is updated after a seek operation.*	0x00
	4	TUNE	Tune 0 = Disable 1 = Enable The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The tune bit is reset to low automatically when the tune operation completes..	0
	3:2	BAND[1:0]	Band Select. 00 = 87.0–108 MHz (US/Europe) 01 = 76–91 MHz (Japan) 10 = 76–108 MHz (Japan wide)	00
	1:0	SPACE[1:0]	Channel Spacing. 00 = 100 kHz 01 = 200 kHz 10 = 50kHz	00
04H	15	RDSIEN	RDS Interrupt Enable 0 = Disable Interrupt(Default) 1 = Enable Interrupt Setting RDSIEN = 1 and GPIO2[1:0] = 01 will generate a low pulse int on GPIO2 when the RDSR 0Ah[15] bit is set.	0
	14	STCIEN	Seek/Tune Complete Interrupt Enable. 0 = Disable Interrupt	0

REG	BITS	NAME	FUNCTION	DEFAULT
			1 = Enable Interrupt Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs.	
	13	RBDS	1=rbds 0=rds	0
	11	DE	De-emphasis. *0 = 75 μs; 1 = 50 μs*	0
	10	RDSR _MODE	0 = RDSR width fixed 40 ms high 1 = read reg0AH clr RDSR	1
	9	SOFTMUTE_EN	If 1, softmute enable	1
	8	AFCD (auto-frequency calibrate disable)	AFC disable. If 0, afc work; If 1, afc disabled.	0
	7	Gpio1_int_en	Interrupt triggered by GPIO1 enable. If 0, disable interrupt from GPIO1; If 1, enable interrupt from GPIO1.	0
	6	I2S_ENABLED	I2S bus enable If 0, disabled; If 1, enabled.	0
	5:4	GPIO3[1:0]	General Purpose I/O 3. *00 = High impedance* *01 = Mono/Stereo indicator (ST)* *10 = Low* *11 = High*	00
	3:2	GPIO2[1:0]	General Purpose I/O 2. *00 = High impedance* *01 = Interrupt (INT)* *10 = Low* *11 = High*	00
	1:0	GPIO1[1:0]	General Purpose I/O 1. *00 = High impedance* *01 = Reserved* *10 = Low* *11 = High*	00
05H	15	INT _MODE	If 0, generate 5ms interrupt; If 1, interrupt last until read reg0AH action occurs.	1
	14:8	SEEKTH[6:0]	Seek Threshold. RSSI scale is logarithmic. 0000000 = min RSSI	0001000
	7:6	RESERVED		00
	5:4	FM	FM Lna working current bit:	10

REG	BITS	NAME	FUNCTION	DEFAULT
		LNA_ICSEL_BIT[1:0]	00=1.8mA 01=2.1mA 10=2.5mA 11=3.0mA	
	3:0	VOLUME[3:0]	Volume Gain Control Bits. *0000=min; 1111=max* *Volume scale is logarithmic*	1111
0AH	15	RDSR	RDS ready 0 = No RDS/RBDS group ready 1 = New RDS/RBDS group ready	0
	14	STC	Seek/Tune Complete. 0 = Not complete 1 = Complete The seek/tune complete flag is set when the seek or tune operation completes.	0
	13	SF	Seek Fail. *0 = Seek successful; 1 = Seek failure* *The seek fail flag is set when the seek operation fails to find a channel with an* RSSI *level greater than* SEEKTH[5:0].	0
	12	RDSS	RDS Synchronization 0=RDS decoder not synchronized(default) 1 = RDS decoder synchronized Available only in RDS Verbose mode	0
	10	ST	Stereo Indicator. *0 = Mono; 1 = Stereo* *Stereo indication is available on* GPIO3 *by setting* GPIO1[1:0] *=01.*	1
	9:0	READCHAN[9:0]	Read Channel. BAND = 0 Frequency = Channel Spacing (kHz) x READCHAN[7:0]+ 87.5 MHz BAND = 1 Frequency = Channel Spacing (kHz) x READCHAN[7:0]+ 76.0 MHz READCHAN[7:0] is updated after a tune or seek operation.	8'h00
0BH	15:9	RSSI[6:0]	RSSI.	0

REG	BITS	NAME	FUNCTION	DEFAULT
			000000 = min 111111 = max RSSI scale is logarithmic.	
	8	FM TUNE	1 = the current channel is a station 0 = the current channel is not a station	0
	7	SEEK READY	1 = seek ready 0 = not ready	0
	6:5	RESERVED		00
	4	ABCD_E	1 = the block id of register 0cH,0dH,0eH,0fH is E 0 = he block id of register 0cH,0dH,0eH,0fH is A,B,C,D	0
	3:2	BLERA[1:0]	BLK Errors Level of RDS_DATA_0, and is always read as Errors Level of RDS BLOCK A(in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1). 00 = 0 errors requiring correction 01 = 1~2 errors requiring correction 10 = 3~5 errors requiring correction 11 = 6+ errors or error in checkword, correctionnot possible Available only in RDS Verbose mode	00
	1:0	BLERB[1:0]	BLK Errors Level of RDS_DATA_1, and is always read as Errors Level of RDS BLOCK B(in RDS mode) or E(in RBDS mode when ABCD_E flag is 1). 00 = 0 errors requiring correction 01 = 1~2 errors requiring correction 10 = 3~5 errors requiring correction	00

REG	BITS	NAME	FUNCTION	DEFAULT
			11 = 6+ errors or error in checkword, correctionnot possible Available only in RDS Verbose mode	
0CH	15:0	RDSA[15:0]	BLOCK A (in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1)	0
0DH	15:0	RDSB[15:0]	BLOCK B (in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1)	0
0EH	15:0	RDSC[15:0]	BLOCK C/c' (in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1)	0
0FH	15:0	RDSD[15:0]	BLOCK D (in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1)	0
10H	15:14	BLERC[1:0]	BLK Errors Level of RDS_DATA_2, and is always read as Errors Level of RDS BLOCK C/c'(in RDS mode) or BLOCK E(in RBDS mdoe when ABCD_E flag is 1). 00 = 0 errors requiring correction 01 = 1~2 errors requiring correction 10 = 3~5 errors requiring correction 11 = 6+ errors or error in checkword, correctionnot possible Available only in RDS Verbose mode	00
	13:12	BLERD[1:0]	BLK Errors Level of RDS_DATA_3, and is always read as Errors Level of RDS BLOCK D(in RDS mode) or BLOCK E(in RBDS mdoe when ABCD_E flag is 1). 00 = 0 errors requiring correction 01 = 1~2 errors requiring correction 10 = 3~5 errors requiring	00

REG	BITS	NAME	FUNCTION	DEFAULT
			correction 11 = 6+ errors or error in checkword, correctionnot possible Available only in RDS Verbose mode	
40H	15	AUTO_SEEK	AM Auto Seek	0
	14	RESERVED		0
	13	Weather_band	For weather band	0
	12:4	RESERVED		0
	3:0	CHIP_FUNC[3:0]	0000 = fm rx 0001 = fm tx (reserved for RDA5820) 1000 = pa (reserved for RDA5820) 1100 = dac 0010 = am/lw 0011 = sw Others = reserved	0000
72H	15 :0	FREQ_AM[15 :0]	AM Band Frequency (Unit, KHz)	0000_0100_0000_0000
7AH	15:0	Read CURRENT AM FREQUENCY	Current AM Frequency in chip	

8 Pins Description

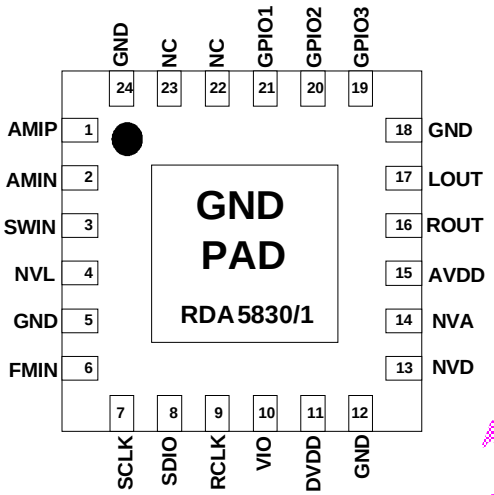
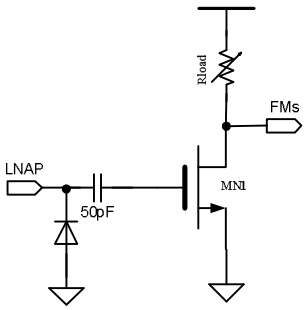
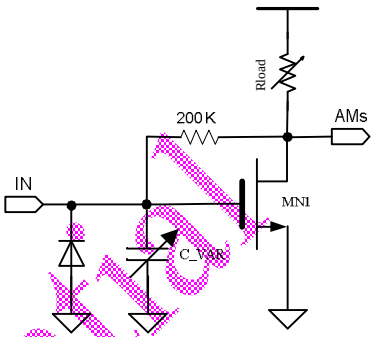
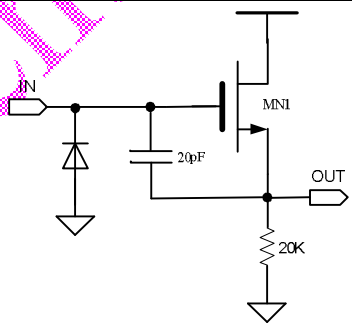
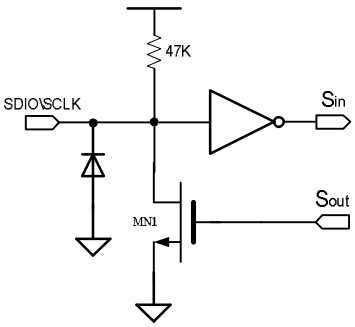
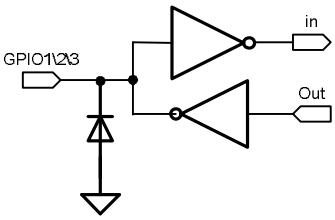


Figure 8-1. RDA5830/1 Top View

Table 8-1 RDA5830/1 Pins Description

SYMBOL	PIN	DESCRIPTION
GND	5,12,18,24	Ground. Connect to ground plane on PCB
FMIN	6	FM Band LNA input port.
SWIN	3	SW Band LNA input port
AMIP,AMIN	1,2	AM Band LNA differential input port.
SCLK	7	Clock input for serial control bus
SDIO	8	Data input/output for serial control bus
RCLK	9	32.768KHz crystal oscillator and reference clock input
VIO	10	Power supply for I/O
DVDD/AVDD	11/15	Power supply for DSP and analog section
ROUT,LOUT	16,17	Right/Left audio output
NVL	4	LNA reference voltage
NVD	13	DSP reference voltage
NVA	14	Analog reference voltage
GPIO1,GPIO2,GPIO3	21,20,19	General purpose input/output
NC	22,23	No Connect

Table 8-2 Internal Pin Configuration

SYMBOL	PIN	DESCRIPTION
FMIN	6	
AMIP/AMIN/SWIN	1/2/3	
RCLK	9	
SCLK/SDIO	7/8	
GPIO1/GPIO2/GPIO3	21/20/19	

9 Application Diagram

9.1 Common application diagram:

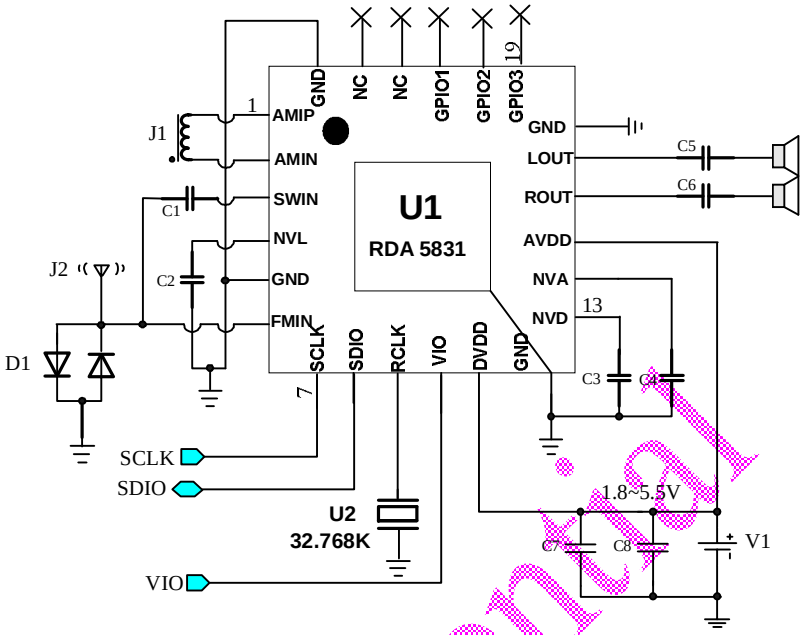


Figure 9-1. RDA5831 FM/AM/LW/SW Receiver Application Diagram

9.1.1 Bill of Materials:

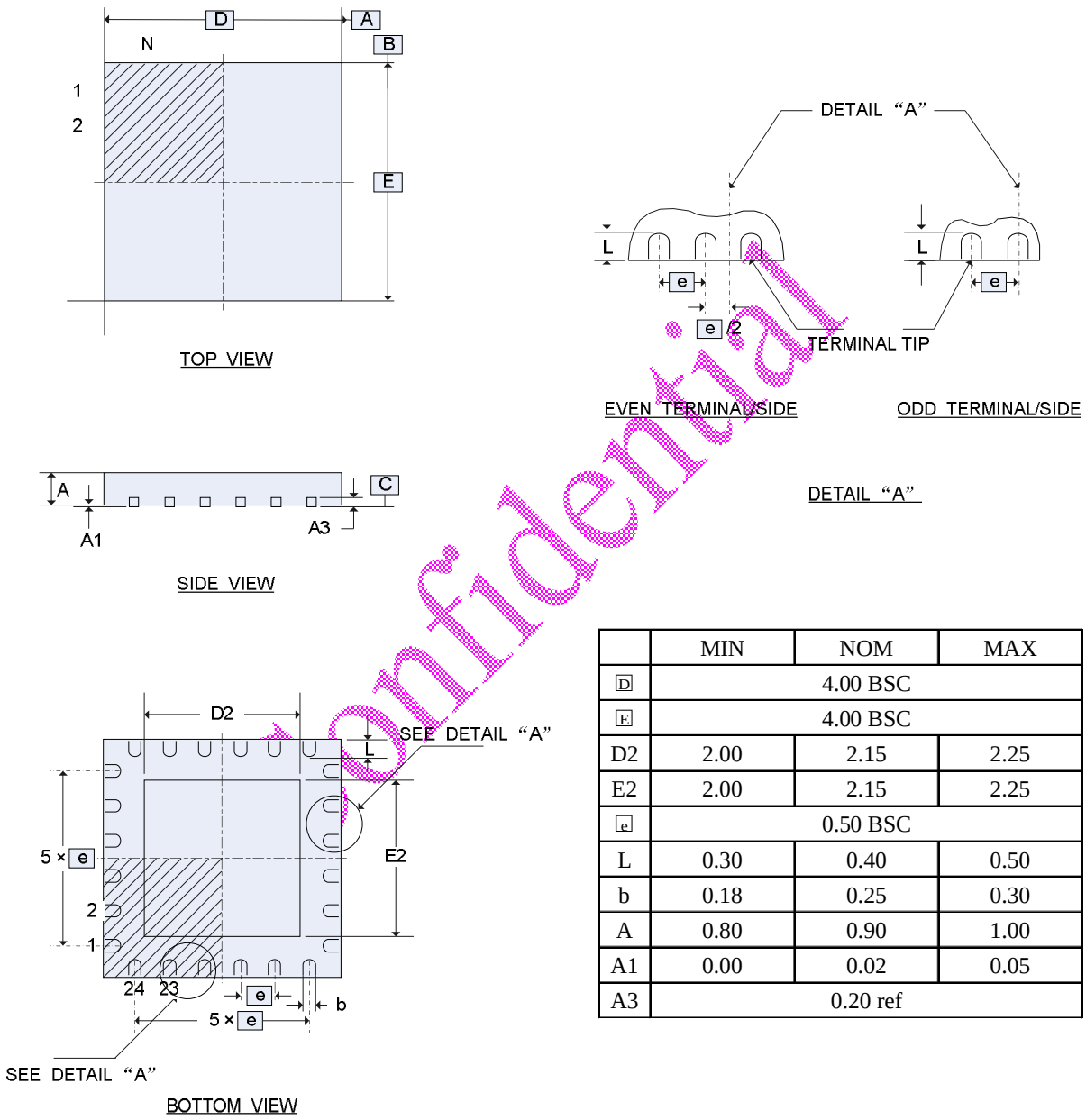
COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5831	FM/AM/LW/SW Receiver	RDA
U2	DCXO	Crystal oscillator 32.768KHz	<=50PPM
J1	180~600uH	Ferrite Loop Stick, for LW and AM	
J2		FM/SW Band Antenna	
D1		ESD protect diode	
C1	1uF	SW Input Couple Capacitor	Murata
C2/C3/C4	22nF	Reference Bypass Capacitor	Murata
C5,C6	125μF	Audio AC Couple Capacitors	Murata
C7/C8	24nF/1uF	Power Supply Bypass Capacitor	Murata

! Pins NC(22,23) should be leaved floating;

! Place C7/C8 Close to AVDD pin.

10 Package Physical Dimension

Figure 10-1 illustrates the package details for the RDA5830/1. The package is lead-free and RoHS-compliant.



	MIN	NOM	MAX
D		4.00 BSC	
E		4.00 BSC	
D2	2.00	2.15	2.25
E2	2.00	2.15	2.25
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 ref	

Figure 10-2. 24-Pin 4x4 Quad Flat No-Lead (QFN)

11 PCB Land Pattern

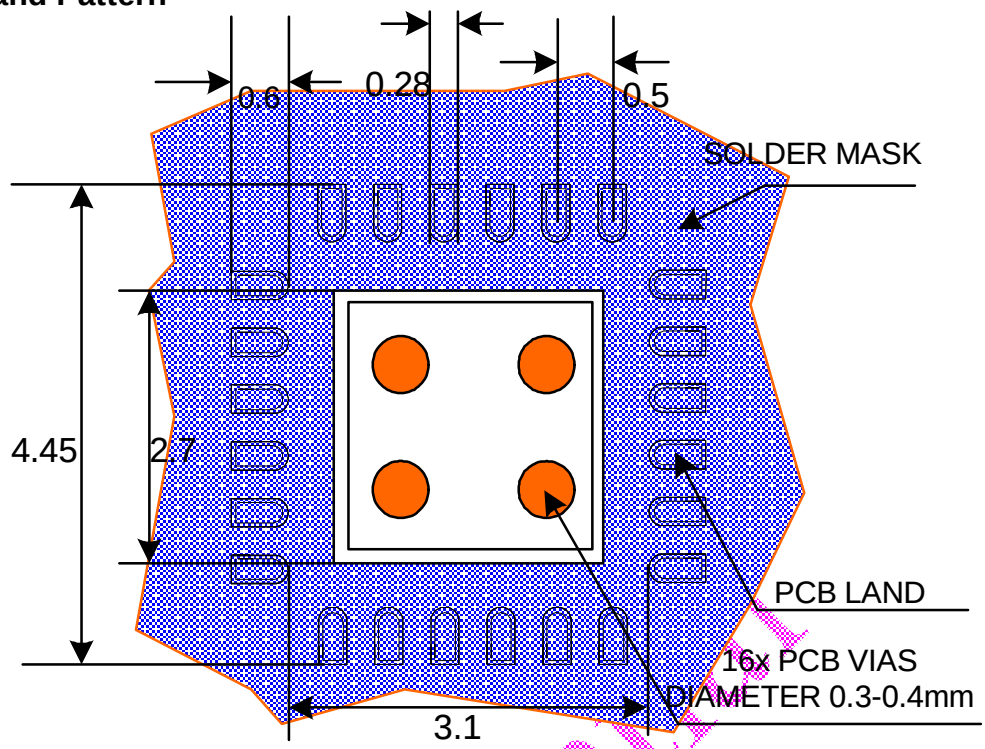


Figure 11-1. PCB Land Pattern for 24-Pin QFN

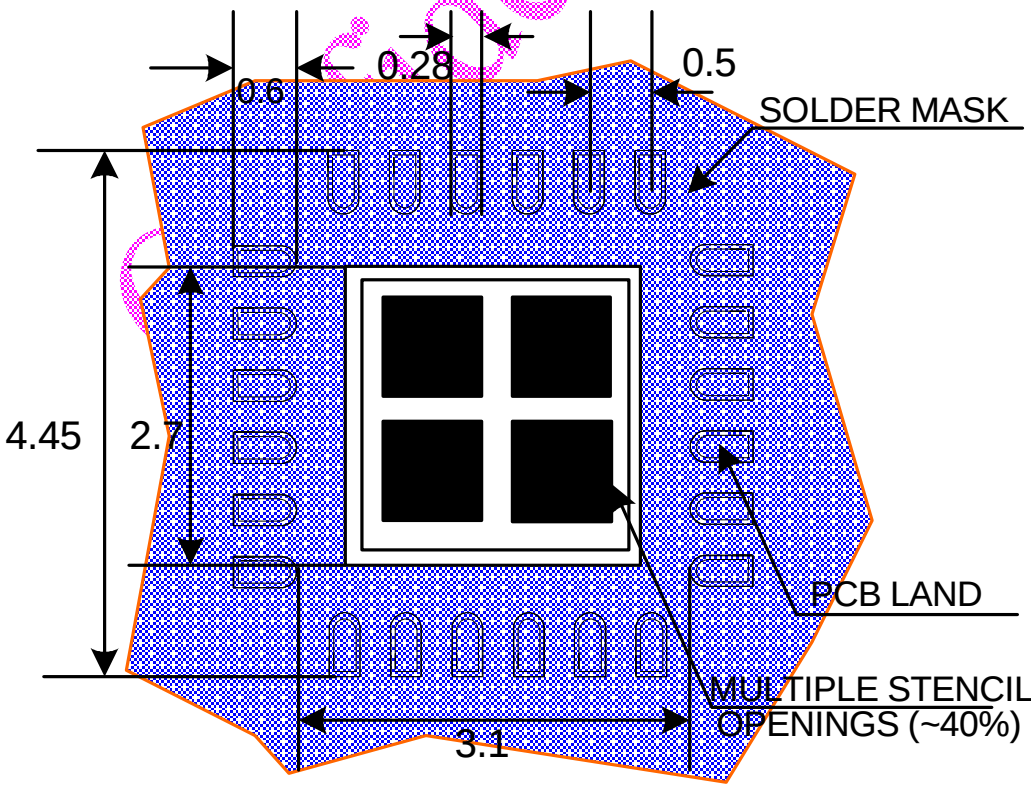


Figure 11-2. PCB Solder Paste Stencil Openings

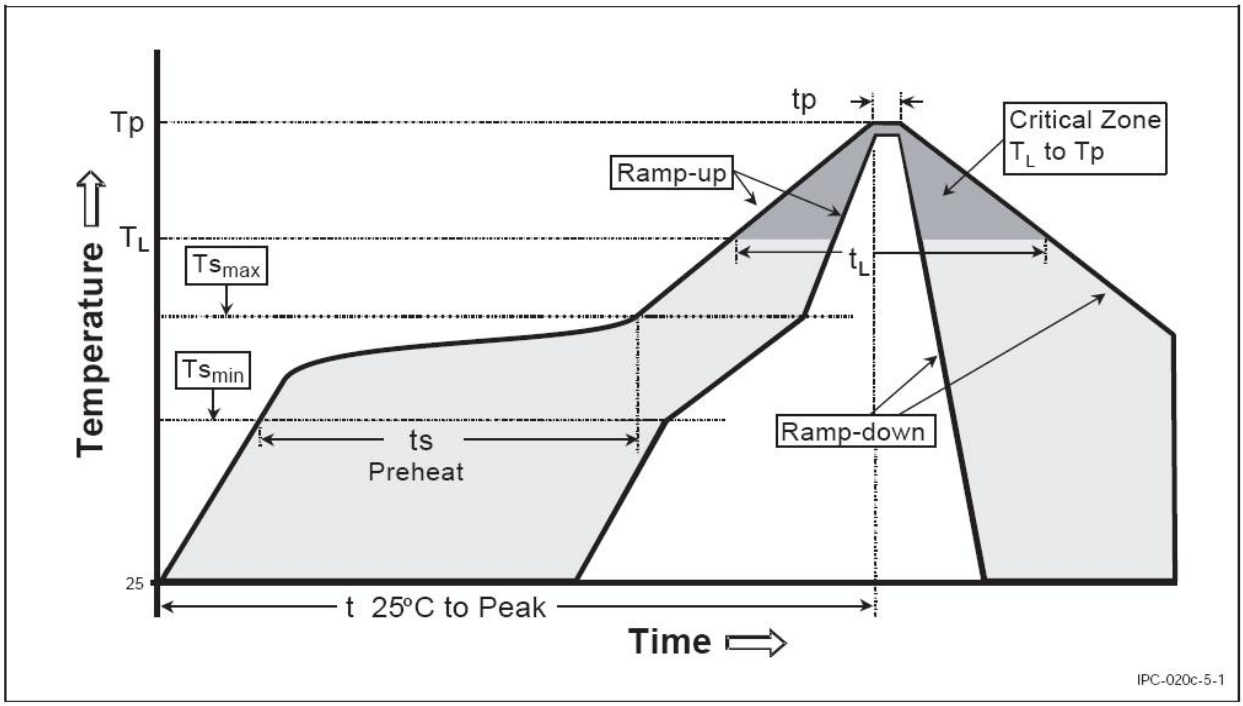


Figure 17.Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-I Classification Reflow Profiles

Package Thickness	Volume mm^3 <350	Volume mm^3 ⩾350
＜2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
⩾2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 ＜350	Volume mm^3 350-2000	Volume mm^3 ＞2000
＜1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
⩾2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Gallium Arsenide integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

12 Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2008-12-27	ChunZhao,YananLiu	Original Draft.
V2.0	2009-03-25	ChunZhao	Add LW/SW

13 Contact Information

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