Dual JK flip-flop with set and reset; negative-edge trigger

Description：

The74HC112isahigh-speedSi-gateCMOSdevices and are pin compatible with low power Schottky TTL
(LSTTL). They are specified in compliance with JEDEC
standard no. 7A.
The 74HC112 is dual negative-edge triggered
JK-type flip-flops featuring individual nJ, nK, clock (nCP),set (nSD) and reset (nRD) inputs.
The set and reset inputs, when LOW, set or reset the
outputs as shown in the function table regardless of the
levels at the other inputs.

Features：

-Asynchronous set and reset

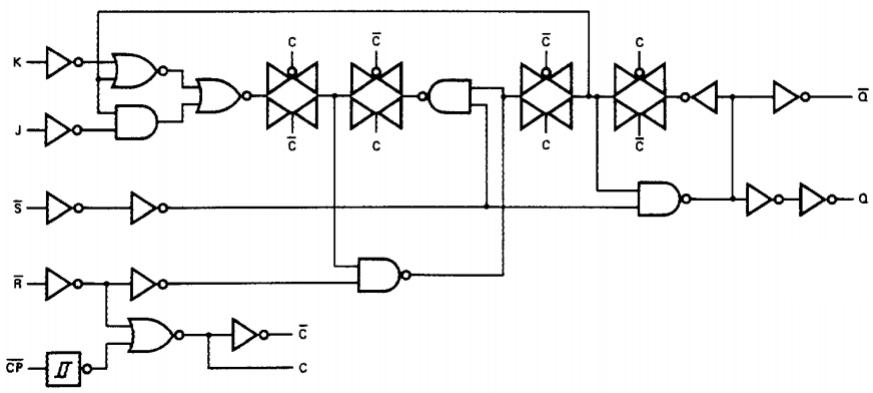
-Output capability: standard

-I_{CC} category: flip-flops

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge triggered)
2, 12	1K, 2K	data inputs; flip-flops 1 and 2
3, 11	1J, 2J	data inputs; flip-flops 1 and 2
4, 10	$1\overline{S}_D$, $2\overline{S}_D$	set inputs (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 7	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
15, 14	$1\overline{R}_D$, $2\overline{R}_D$	reset inputs (active LOW)
16	V_{CC}	positive supply voltage

Logic diagram:



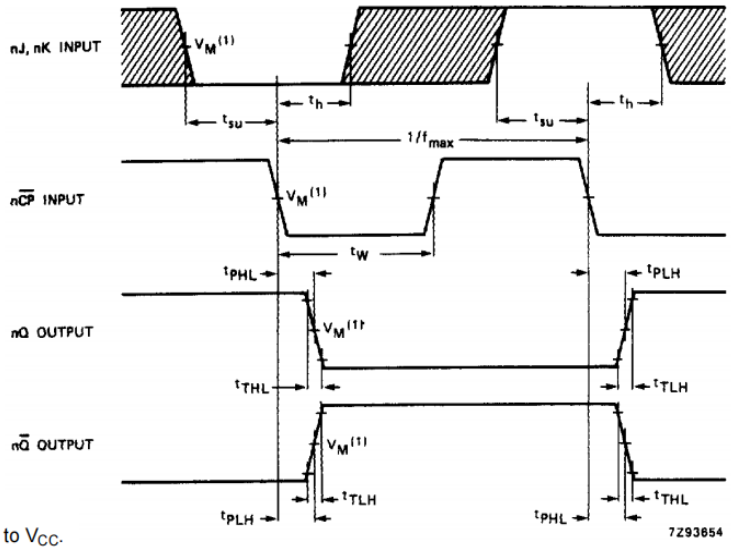
FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	$n\overline{CP}$	nJ	nK	nQ	$n\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	L
toggle	H	H	↓	h	h	$\overline{q}$	q
load “0” (reset)	H	H	↓	l	h	L	H
load “1” (set)	H	H	↓	h	l	H	L
hold “no change”	H	H	↓	l	l	q	$\overline{q}$

AC CHARACTERISTICS

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		50 18 14	155 31 26		295 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	set or reset pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{CP}$	80 16 14	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time $n\overline{S}_D$ to $n\overline{CP}$	80 16 14	−19 −7 −6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_h	hold time nJ, nK to $n\overline{CP}$	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.6
f_{max}	maximum clock pulse frequency	6 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

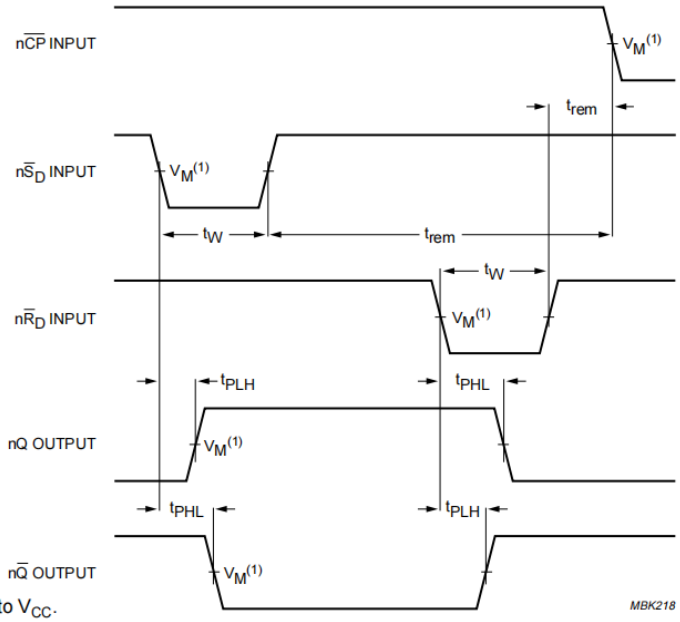
AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.6 Waveforms showing the clock ($n\overline{CP}$) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the nJ, nK to $n\overline{CP}$ set-up times, the $n\overline{CP}$ to nJ, nK hold times, the output transition times and the maximum clock pulse frequency.

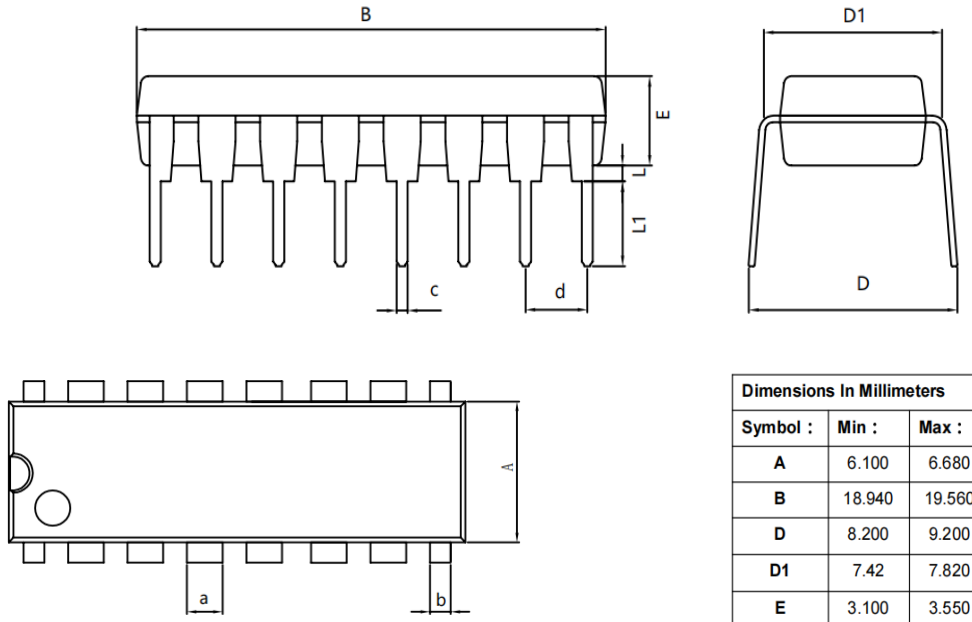


(1) HC : V_M = 50%; V_I = GND to V_{CC}.

Fig.7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse width and the $n\overline{R}_D$ and $n\overline{S}_D$ to $n\overline{CP}$ removal time.

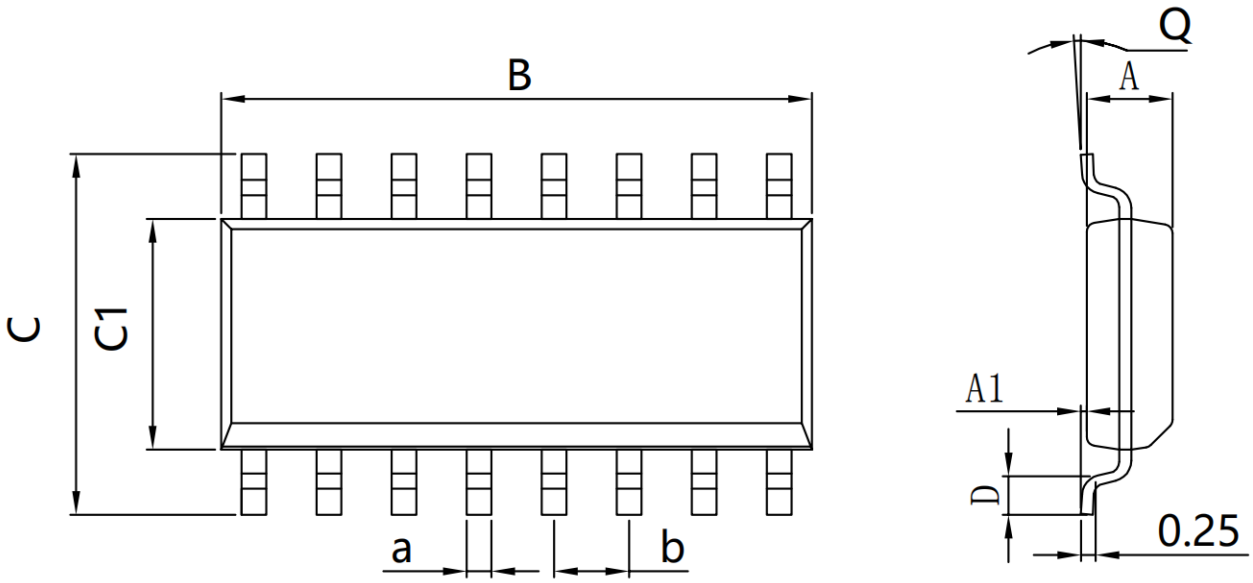
PACKAGE MECHANICAL DATA

DIP16



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	6.100	6.680	L	0.500	0.800
B	18.940	19.560	a	1.524 TYP	
D	8.200	9.200	b	0.889 TYP	
D1	7.42	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.800			

SOP16



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	9.800	10.00	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			