SN74LS191(LX)
Presettable Synchronous 4-bit Binary up/down Counter

Product Specification

Specification Revision History：

Version	Date	Description
2022-06-A1	2022-06	New
2023-04-B1	2023-04	Update the template

Contents

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1、General Description

The SN74LS191 is an asynchronously presettable 4-bit binary up/down counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired value. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. This operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}$/D) input signal determines the direction of counting as indicated in the function table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH.

Also, the $\overline{U}$/D input should be changed only when either $\overline{CE}$ or CP is HIGH. Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches '15' in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the $\overline{RC}$ output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figure 4 and Figure 5.

In Figure 4, each $\overline{RC}$ output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Figure 5 shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Figure 6, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage it not affected by its own $\overline{CE}$ signal therefore the simple inhibit scheme of Figure 4 and 5 does not apply. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

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Features:

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
SN74LS191N(LX)	DIP16	SN74LS191N	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
SN74LS191DR(LX)	SOP16	LS191	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74LS191PW(LX)	TSSOP16	LS191	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

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Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
SN74LS191DR	SOP16	LS191	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
SN74LS191PW	TSSOP16	LS191	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

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2、Block Diagram And Pin Description

2.1、Block Diagram

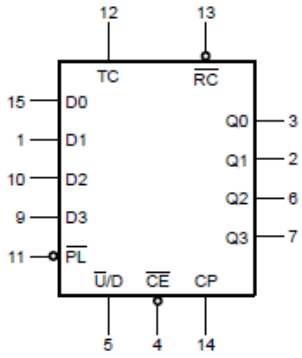

Figure 1. Logic symbol

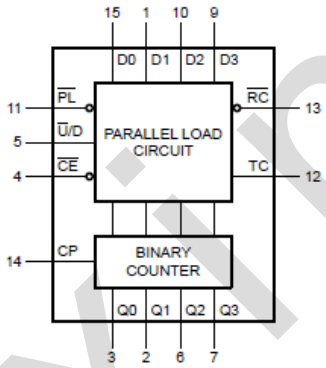

Figure 2. Functional diagram

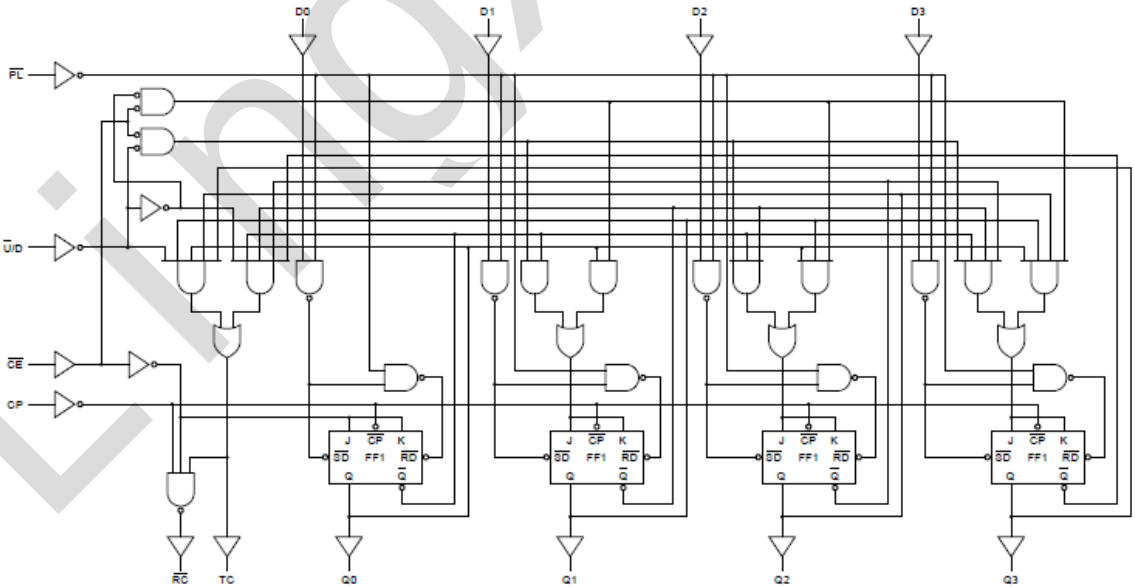

Figure 3. Logic diagram

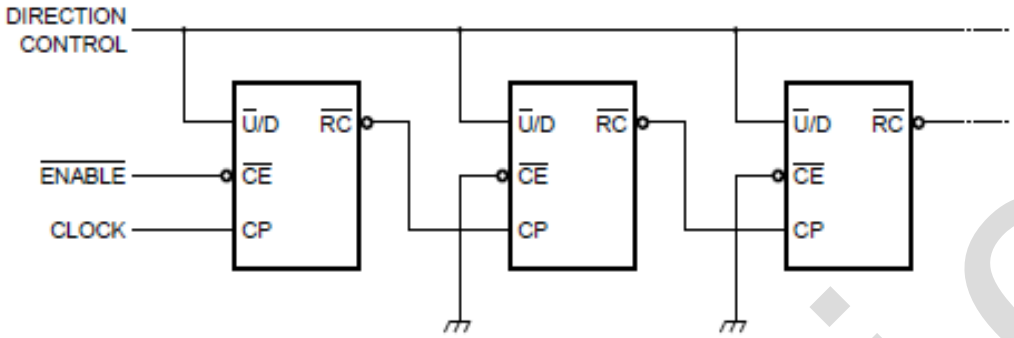

Figure 4. N-stage ripple counter using ripple clock

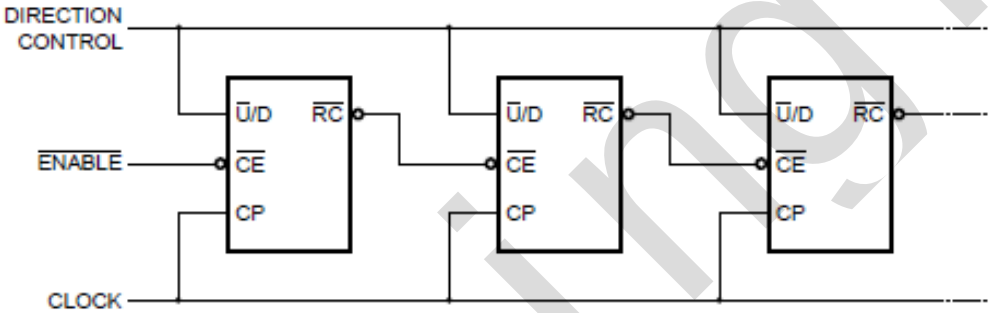

Figure 5. Synchronous n-stage counter using ripple carry/borrow

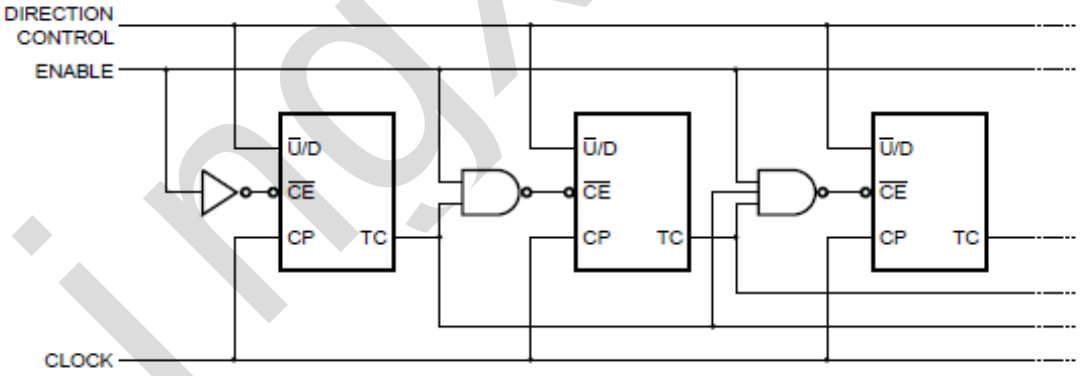

Figure 6. Synchronous n-stage counter with parallel gated carry/borrow

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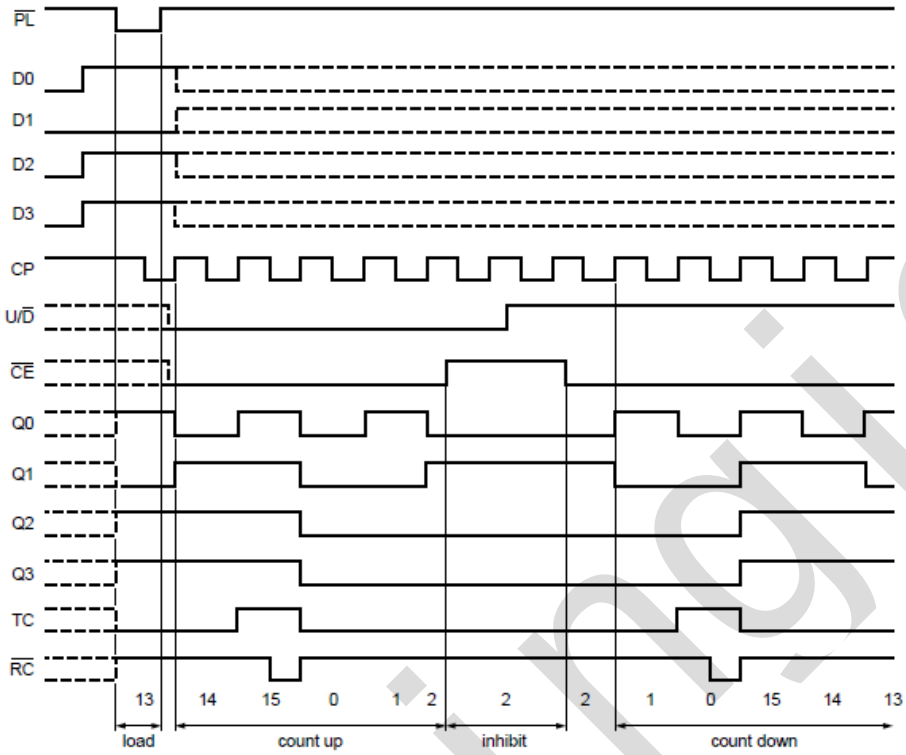
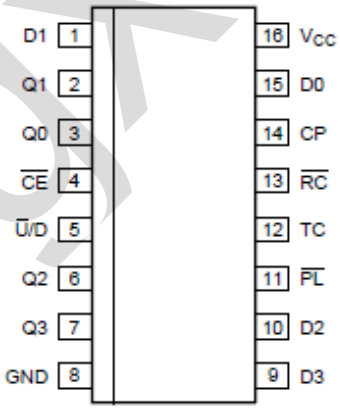


Figure 7. Typical timing sequence

2.2、Pin Configurations



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2.3、Pin Description

Pin No.	Pin Name	Description
1	D1	data input
2	Q1	flip-flop output
3	Q0	flip-flop output
4	$\overline{CE}$	count enable input (active LOW)
5	$\overline{U}$/D	up/down input
6	Q2	flip-flop output
7	Q3	flip-flop output
8	GND	ground (0V)
9	D3	data input
10	D2	data input
11	$\overline{PL}$	parallel load input (active LOW)
12	TC	terminal count output
13	$\overline{RC}$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge-triggered)
15	D0	data input
16	V_{CC}	supply voltage

2.4、Function Table

Operating mode	Input					Output
	$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	Dn	Qn
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition; l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

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Input			Terminal count state				Output	
$\overline{U}$/D	$\overline{CE}$	CP	Q0	Q1	Q2	Q3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓	H	H	H	H	⌐	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	⌐	⊓

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care.

[2] ⊓ =one LOW level output pulse.

[3] ⌐ =TC goes LOW on a LOW-to-HIGH clock transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	V_O= -0.5V to V_{CC}+0.5V		-	±25	mA
supply current	I_{CC}	-		-	+50	mA
ground current	I_{GND}	-		-50	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

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3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA

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3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA

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3.3.4、AC Characteristics 1

(T_{amb}=25℃, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Qn; see Figure 9	V_{CC}=2.0V	-	72	220	ns
			V_{CC}=4.5V	-	26	44	ns
			V_{CC}=5.0V; C_L=15pF	-	22	-	ns
			V_{CC}=6.0V	-	21	37	ns
		CP to TC; see Figure 9	V_{CC}=2.0V	-	83	255	ns
			V_{CC}=4.5V	-	30	51	ns
			V_{CC}=6.0V	-	24	43	ns
		CP to $\overline{RC}$; see Figure 10	V_{CC}=2.0V	-	47	150	ns
			V_{CC}=4.5V	-	17	30	ns
			V_{CC}=6.0V	-	14	26	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 10	V_{CC}=2.0V	-	33	130	ns
			V_{CC}=4.5V	-	12	26	ns
			V_{CC}=6.0V	-	10	22	ns
		Dn to Qn; see Figure 11	V_{CC}=2.0V	-	61	220	ns
			V_{CC}=4.5V	-	22	44	ns
			V_{CC}=6.0V	-	18	37	ns
		$\overline{PL}$ to Qn; see Figure 12	V_{CC}=2.0V	-	61	220	ns
			V_{CC}=4.5V	-	22	44	ns
			V_{CC}=6.0V	-	18	37	ns
		$\overline{U}$/D to TC; see Figure 13	V_{CC}=2.0V	-	44	190	ns
			V_{CC}=4.5V	-	16	38	ns
			V_{CC}=6.0V	-	13	32	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 13	V_{CC}=2.0V	-	50	210	ns
			V_{CC}=4.5V	-	18	42	ns
			V_{CC}=6.0V	-	14	36	ns
transition time	t_t	see Figure 14	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP; HIGH or LOW; see Figure 9	V_{CC}=2.0V	125	28	-	ns
			V_{CC}=4.5V	25	10	-	ns
			V_{CC}=6.0V	21	8	-	ns
		$\overline{PL}$; LOW; see Figure 14	V_{CC}=2.0V	100	22	-	ns
			V_{CC}=4.5V	20	8	-	ns
			V_{CC}=6.0V	17	6	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; see Figure 14	V_{CC}=2.0V	35	8	-	ns
			V_{CC}=4.5V	7	3	-	ns
			V_{CC}=6.0V	6	2	-	ns
set-up time	t_{su}	$\overline{U}$/D to CP; see Figure 15	V_{CC}=2.0V	205	50	-	ns
			V_{CC}=4.5V	41	18	-	ns
			V_{CC}=6.0V	35	14	-	ns
		Dn to $\overline{PL}$;	V_{CC}=2.0V	100	19	-	ns

		see Figure 16	V_{CC}=4.5V	20	7	-	ns
			V_{CC}=6.0V	17	6	-	ns
		$\overline{CE}$ to CP; see Figure 15	V_{CC}=2.0V	140	44	-	ns
			V_{CC}=4.5V	28	16	-	ns
			V_{CC}=6.0V	24	13	-	ns
hold time	t_h	$\overline{U}$/D to CP; see Figure 15	V_{CC}=2.0V	0	-39	-	ns
			V_{CC}=4.5V	0	-14	-	ns
			V_{CC}=6.0V	0	-11	-	ns
		Dn to $\overline{PL}$; see Figure 16	V_{CC}=2.0V	0	-11	-	ns
			V_{CC}=4.5V	0	-4	-	ns
			V_{CC}=6.0V	0	-3	-	ns
		$\overline{CE}$ to CP; see Figure 15	V_{CC}=2.0V	0	-28	-	ns
			V_{CC}=4.5V	0	-10	-	ns
			V_{CC}=6.0V	0	-8	-	ns
maximum frequency	f_{max}	CP; see Figure 9	V_{CC}=2.0V	4.0	11	-	MHz
			V_{CC}=4.5V	20	33	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	36	-	MHz
			V_{CC}=6.0V	24	39	-	MHz
power dissipation capacitance	C_{PD}	V_I=GND to V_{CC}		-	31	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

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3.3.5、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Qn; see Figure 9	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns
		CP to TC; see Figure 9	V_{CC}=2.0V	-	-	320	ns
			V_{CC}=4.5V	-	-	64	ns
			V_{CC}=6.0V	-	-	54	ns
		CP to $\overline{RC}$; see Figure 10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 10	V_{CC}=2.0V	-	-	165	ns
			V_{CC}=4.5V	-	-	33	ns
			V_{CC}=6.0V	-	-	28	ns
		Dn to Qn; see Figure 11	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns
		$\overline{PL}$ to Qn; see Figure 12	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	55	ns
			V_{CC}=6.0V	-	-	47	ns
		$\overline{U}$/D to TC; see Figure 13	V_{CC}=2.0V	-	-	240	ns
			V_{CC}=4.5V	-	-	48	ns
			V_{CC}=6.0V	-	-	41	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 13	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
transition time	t_t	see Figure 14	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	CP; HIGH or LOW; see Figure 9	V_{CC}=2.0V	155	-	-	ns
			V_{CC}=4.5V	31	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		$\overline{PL}$; LOW; see Figure 14	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP; see Figure 14	V_{CC}=2.0V	45	-	-	ns
			V_{CC}=4.5V	9	-	-	ns
			V_{CC}=6.0V	8	-	-	ns

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set-up time	t_{su}	$\overline{U}$/D to CP; see Figure 15	V_{CC}=2.0V	255	-	-	ns
			V_{CC}=4.5V	51	-	-	ns
			V_{CC}=6.0V	43	-	-	ns
		Dn to $\overline{PL}$; see Figure 16	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
		$\overline{CE}$ to CP; see Figure 15	V_{CC}=2.0V	175	-	-	ns
			V_{CC}=4.5V	35	-	-	ns
			V_{CC}=6.0V	30	-	-	ns
hold time	t_h	$\overline{U}$/D to CP; see Figure 15	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		Dn to $\overline{PL}$; see Figure 16	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		$\overline{CE}$ to CP; see Figure 15	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 9	V_{CC}=2.0V	3.2	-	-	MHz
			V_{CC}=4.5V	16	-	-	MHz
			V_{CC}=6.0V	19	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

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3.3.6、AC Characteristics 3

(T_{amb}=-40℃ to +125℃, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Qn; see Figure 9	V_{CC}=2.0V	-	-	330	ns
			V_{CC}=4.5V	-	-	66	ns
			V_{CC}=6.0V	-	-	56	ns
		CP to TC; see Figure 9	V_{CC}=2.0V	-	-	395	ns
			V_{CC}=4.5V	-	-	77	ns
			V_{CC}=6.0V	-	-	65	ns
		CP to $\overline{RC}$; see Figure 10	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
		$\overline{CE}$ to $\overline{RC}$; see Figure 10	V_{CC}=2.0V	-	-	195	ns
			V_{CC}=4.5V	-	-	39	ns
			V_{CC}=6.0V	-	-	33	ns
		Dn to Qn; see Figure 11	V_{CC}=2.0V	-	-	330	ns
			V_{CC}=4.5V	-	-	66	ns
			V_{CC}=6.0V	-	-	56	ns
		$\overline{PL}$ to Qn; see Figure 12	V_{CC}=2.0V	-	-	330	ns
			V_{CC}=4.5V	-	-	66	ns
			V_{CC}=6.0V	-	-	56	ns
		$\overline{U}$/D to TC; see Figure 13	V_{CC}=2.0V	-	-	285	ns
			V_{CC}=4.5V	-	-	57	ns
			V_{CC}=6.0V	-	-	48	ns
		$\overline{U}$/D to $\overline{RC}$; see Figure 13	V_{CC}=2.0V	-	-	315	ns
			V_{CC}=4.5V	-	-	63	ns
			V_{CC}=6.0V	-	-	54	ns
transition time	t_t	see Figure 14	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
pulse width	t_W	CP; HIGH or LOW; see Figure 9	V_{CC}=2.0V	195	-	-	ns
			V_{CC}=4.5V	39	-	-	ns
			V_{CC}=6.0V	33	-	-	ns
		$\overline{PL}$; LOW; see Figure 14	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns

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recovery time	t_{rec}	$\overline{PL}$ to CP; see Figure 14	V_{CC}=2.0V	55	-	-	ns
			V_{CC}=4.5V	11	-	-	ns
			V_{CC}=6.0V	9	-	-	ns
set-up time	t_{su}	$\overline{U}$/D to CP; see Figure 15	V_{CC}=2.0V	310	-	-	ns
			V_{CC}=4.5V	62	-	-	ns
			V_{CC}=6.0V	53	-	-	ns
		Dn to $\overline{PL}$; see Figure 16	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		$\overline{CE}$ to CP; see Figure 15	V_{CC}=2.0V	210	-	-	ns
			V_{CC}=4.5V	42	-	-	ns
			V_{CC}=6.0V	36	-	-	ns
hold time	t_h	$\overline{U}$/D to CP; see Figure 15	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		Dn to $\overline{PL}$; see Figure 16	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		$\overline{CE}$ to CP; see Figure 15	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 9	V_{CC}=2.0V	2.6	-	-	MHz
			V_{CC}=4.5V	13	-	-	MHz
			V_{CC}=6.0V	15	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

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4、Testing Circuit

4.1、AC Testing Circuit

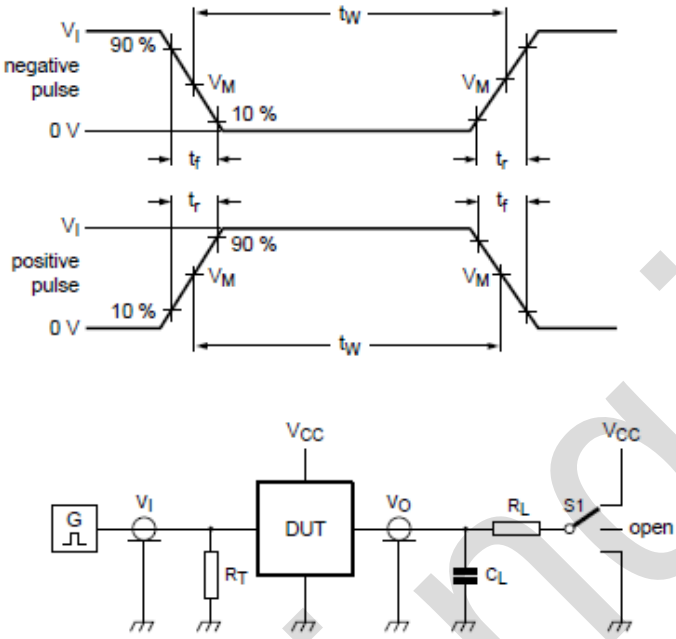

Figure 8. Test circuit for measuring switching times

Definitions for test circuit:

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

S1=Test selection switch

4.2、AC Testing Waveforms

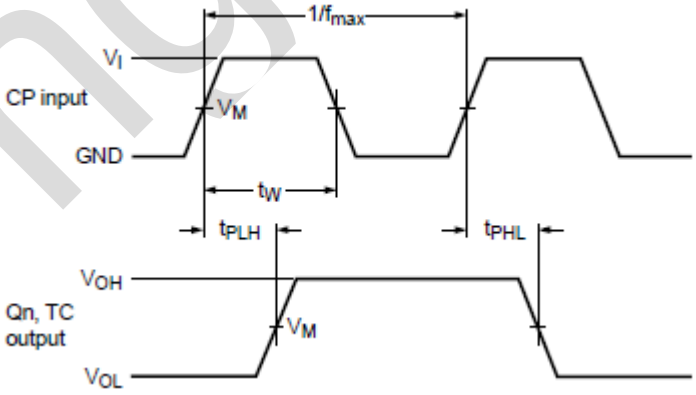

Figure 9. The clock input (CP) to outputs (Qn, TC) propagation delays, clock pulse width and maximum clock frequency

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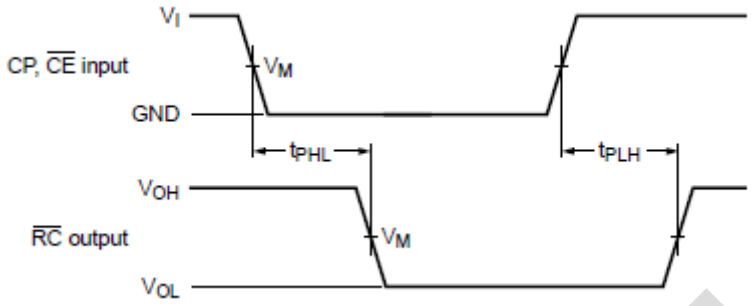

Figure 10. The clock and count enable inputs (CP, $\overline{CE}$) to ripple clock output ($\overline{RC}$) propagation delays

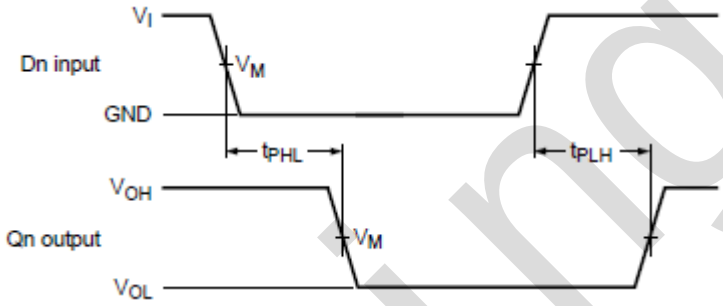

Figure 11. The input (Dn) to output (Qn) propagation delays

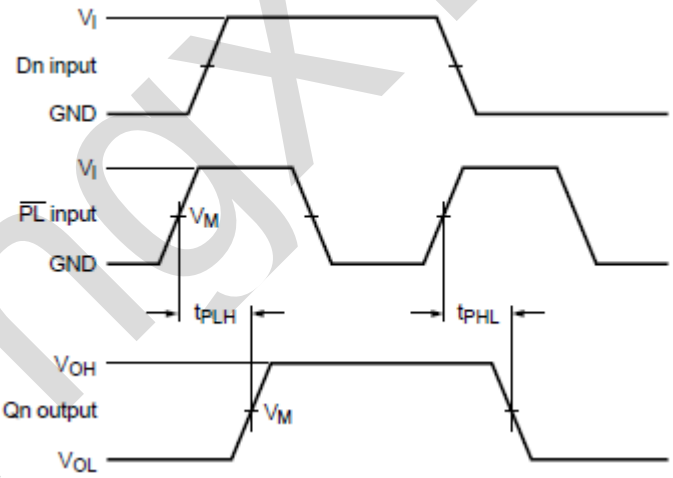

Figure 12. The parallel load input ($\overline{PL}$) to output (Qn) propagation delays

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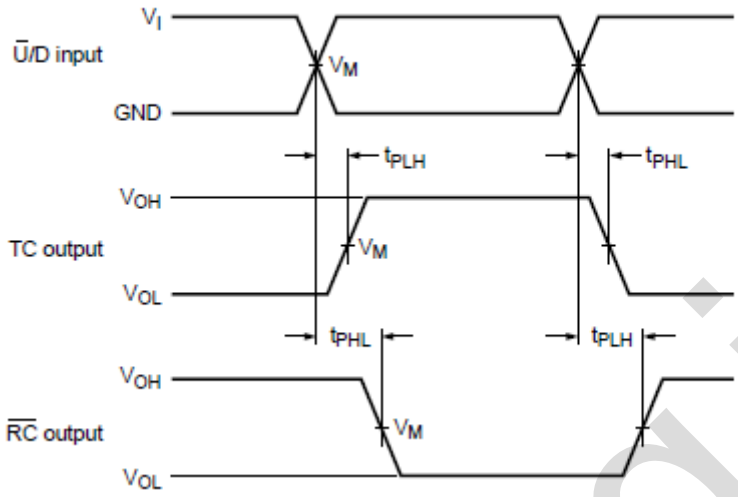

Figure 13. The up/down count input ($\overline{U}$/D) to terminal count and ripple clock output (TC, $\overline{RC}$) propagation delays

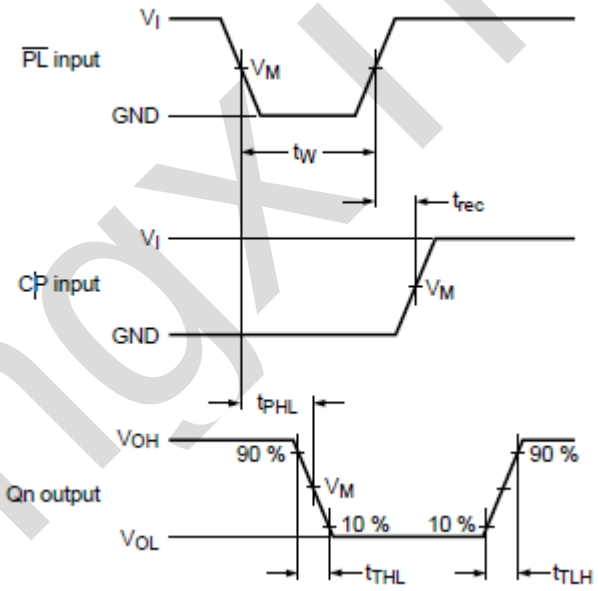

Figure 14. The parallel load input ($\overline{PL}$) to clock (CP) recovery times, parallel load pulse width and output (Qn) transition times

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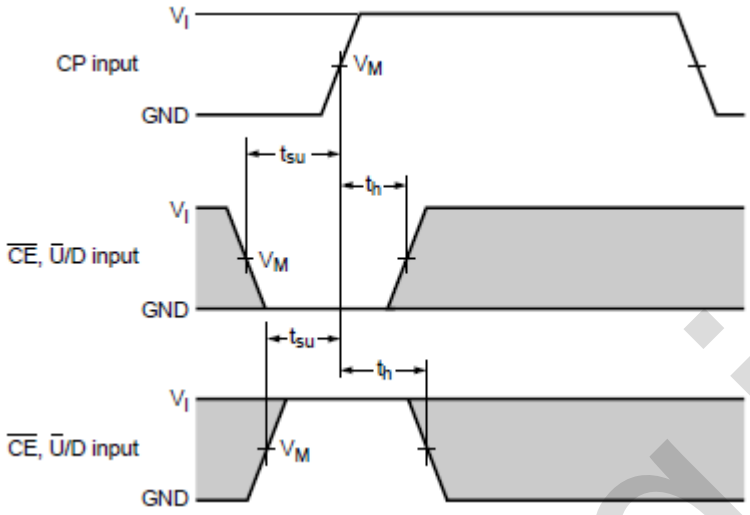


Figure 15. The count enable and up/down count inputs ($\overline{CE}$, $\overline{U}$/D) to clock input (CP) set-up and hold times

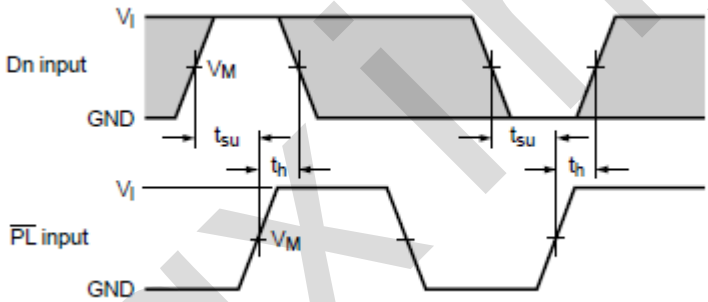


Figure 16. The parallel load input ($\overline{PL}$) to data input (Dn) set-up and hold times

4.3、Measurement Points

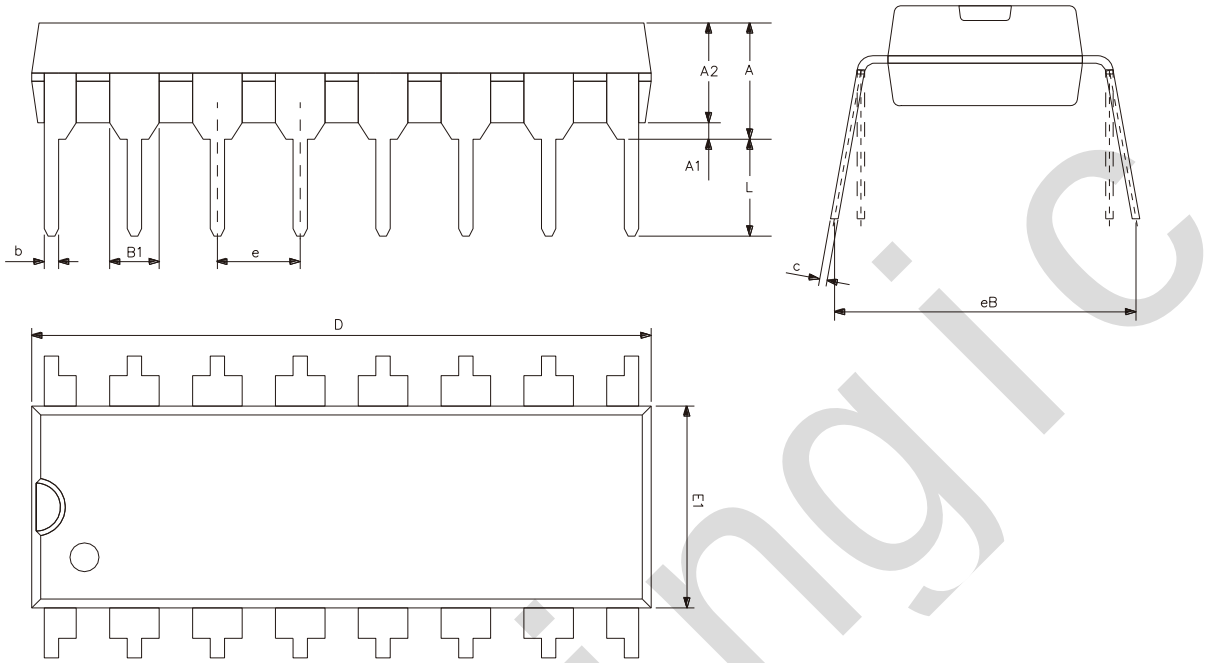
Input	Output
V_M	V_M
$0.5\times V_{CC}$	$0.5\times V_{CC}$

4.4、Test Data

Input		Load		S1 position
V_I	t_r , t_f	C_L	R_L	t_{PLH}, t_{PHL}
V_{CC}	6ns	15pF, 50pF	1kΩ	open

5、Package Information

5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

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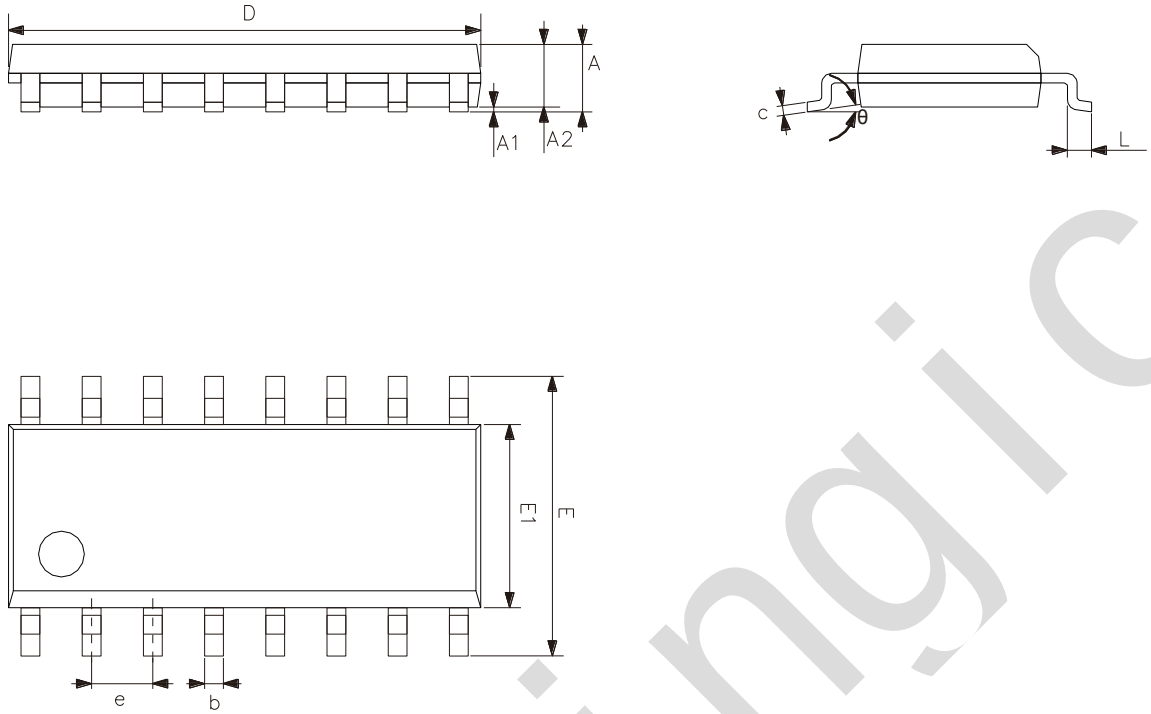
5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

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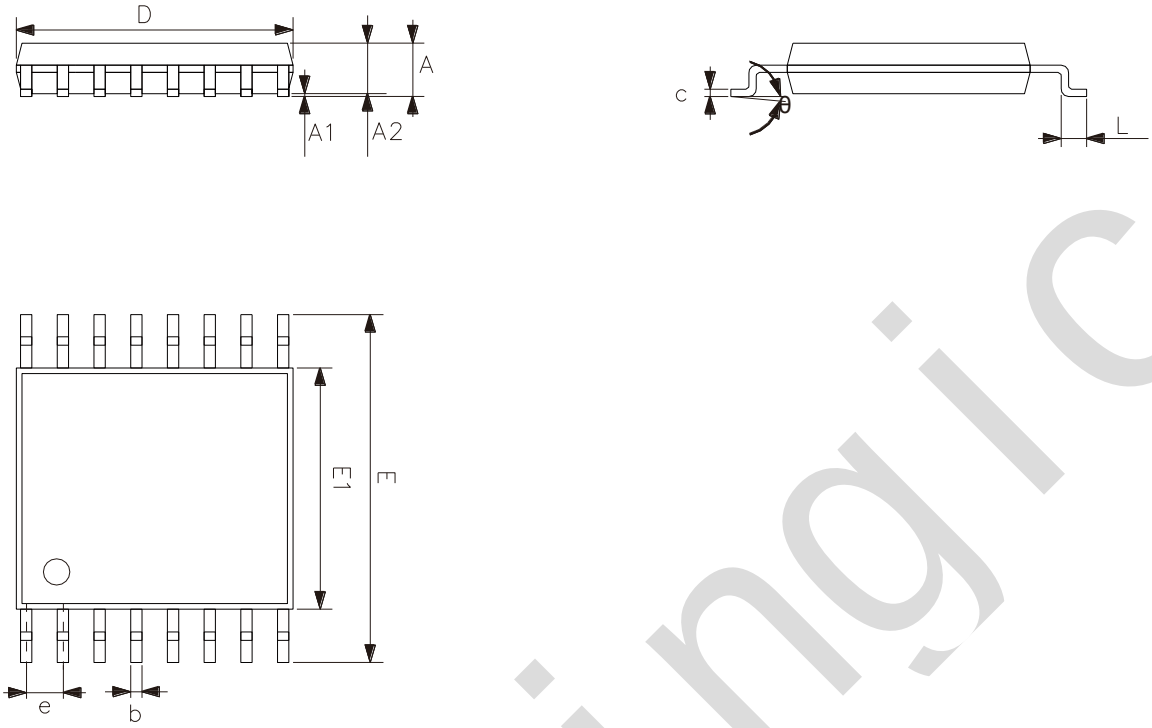
5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

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6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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