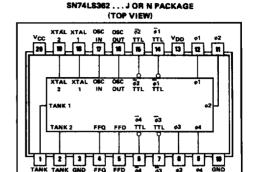
### MSI

### TYPE SN74LS382 (TIM9904) FOUR-PHASE CLOCK GENERATOR/DRIVER

BULLETIN NO. DL-S 7712476, OCTOBER 1976-REVISED AUGUST 1977

- Clock Generator/Driver for The TMS 9900 or Other Microprocessors
- High-Level 4-Phase Outputs
- Complementary TTL 4-Phase Outputs
- Self-Contained Oscillator Can be Crystal or Capacitor Controlled
- External Oscillator Can Be Used
- Clocked D-Type Flip-Flop With Schmitt-Trigger Input For Reset Signal Synchronization

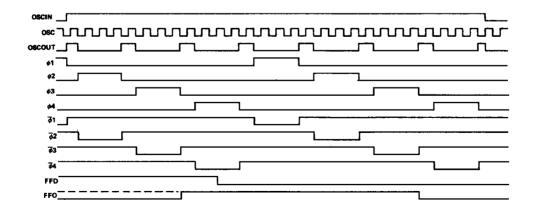
### description



The 'LS362 consists of an oscillator, divide-by-four counter, a second divide-by-four counter with gating to generate four clock phases, high-level (12-volt) output drivers, low-level (5-volt) complementary output drivers, and a D-type flip-flop controlled by an external signal and the  $\phi3$  clock. The four high-level clock phases provide clock inputs to a TMS 9900 microprocessor. The four complementary TTL-level clocks can be used to time memory or other logic functions in a TMS 9900 computer system. The D-type flip-flop can be used to provide (for example) a reset signal to a TMS 9900, timed by  $\phi3$ , on receipt of an input to the FFD input from power turn-on or a manual switch closure. Other applications are possible. A safety feature has been incorporated in the  $\phi$  outputs such that if an open occurs in the VCC supply common to 'LS362 and TMS 9900, the  $\phi$  outputs will go low thus protecting the TMS 9900.

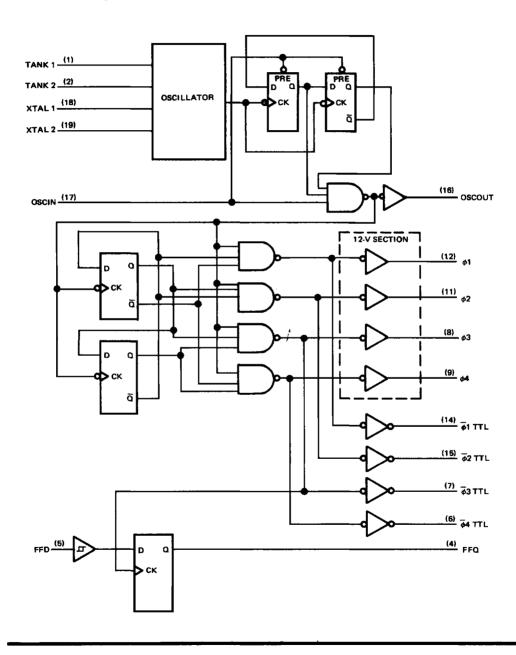
The frequency of the internal oscillator can be established by a quartz crystal or capacitor and LC circuit. Either a fundamental or overtone crystal may be used. The LC circuit connected to the tank inputs selects the desired crystal overtone or establishes the internal oscillator frequency when a capacitor is used instead of a crystal. An LC circuit must always be used at the tank inputs when using the internal oscillator. An external oscillator can be used, if desired, see "Applications Information" for details.

#### typical phase relationships of inputs and outputs (OSC is internal)



# TYPE SN74LS362 (TIM9964) FOUR-PHASE CLOCK GENERATOR/DRIVER

### functional block diagram



# TYPE \$N74L\$362 (TIM9804) FOUR-PHASE CLOCK GENERATOR/DRIVER

### schematics of inputs and outputs

EQUIVALENT OF D INPUT	EQUIVALENT OF OSCIN INPUT	EQUIVALENT OF XTAL 1 AND XTAL 2 INPUTS
VCC 20 kΩ NOM INPUT GND 1	VCC 2.3 kΩ NOM	INPUT GND 1
EQUIVALENT OF TANK INPUTS	TYPICAL OF ¢1,¢2,¢3 AND ¢4 OUTPUTS	TYPICAL OF OSCOUT, Q, AND ALL ottl outputs
INPUT GND 1	VDD OUTPUT	OUTPUT

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage: VCC (see Note 1)																		. 7 V
V <sub>DD</sub> (see Note 1)																		13 V
Input voltage: OSCIN																		5.5 V
FFD															-0	).5	٧	to 7 V
Operating free-air temperature range	•														(	٥°c	to	70°C
Storage temperature range																		

NOTE 1: Voltage values are with respect to the network ground terminals connected together.

#### recommended operating conditions

		MIN	NOM	MAX	UNIT
Construction	Vcc	4,75	5	5.25	V
Supply voltages	V <sub>DD</sub>	11.4	12	12.6	V
High lands are a second land	φ1, φ2, φ3, φ4			-100	μА
High-level output current, IOH	All others			-400	μA
	φ1, φ2, φ3, φ4			4	mA
Low-level output current, IOL	All others			8	mÄ
Internal oscillator frequency, fosc	•		48	54	MHz
External oscillator pulse width, tw(osc)		25			ns
Setup time, FFD input (with respect to felling edge of φ3), t <sub>SU</sub>		50			ns
Hold time, FFD input (with respect to falling edge of φ3), th		-30			ns.
Operating free-air temperature, TA		0		70	°C

# TYPE \$N74L\$362 (TIM9904) FOUR-PHASE CLOCK GENERATOR/DRIVER

REVISED AUGUST 1977

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIO	NS	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			V
	Low-level	FFD					0.5	V
VIL	input voltage	OSCIN					0.8	1 °
V <sub>T+</sub> - V <sub>T-</sub>	Hysteresis	FFD			0.4	0.8		V
VłK	input clamp voltage		VCC = 4.75 V, VDD = 11.4 V,	i <sub>j</sub> = -18 mA			-1.5	V
V	High-level	φ1, φ2, φ3, φ4	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = -100 µA	V <sub>DD</sub> -2	V <sub>DD</sub> -1.5	Voo	l v
VOH	output voltage	Other outputs	V <sub>DD</sub> ≈ 11,4 V to 12.6 V	1 <sub>OH</sub> = -400 µA	2.7	3.4		l Y
	Low-level	φ1, φ2, φ3, φ4		IQL = 4 mA		0.25	0.4	
VOL	output voltage	Other outputs	V <sub>CC</sub> = 4.75 V, V <sub>DD</sub> = 11.4 V	IOL = 4 mA		0.25	0.4	mA
	output voltage	Other outputs		IOL = 8 mA		0.35	0.5	
1.	Input current at	FFD	V <sub>CC</sub> = 5.25 V, V <sub>DD</sub> = 12.6 V	V <sub>I</sub> = 7 V	•		0.1	mA
l)	maximum input voltage	OSCIŅ	VCC - 8.25 V, VDD - 12.6 V	V <sub>I</sub> ≈ 5.5 V			0.3	] ""^
	High-level	FFD	V <sub>CC</sub> = 5.25 V, V <sub>DD</sub> = 12.6 V,	V. = 27V			20	μA
чн	input current	OSCIN	VCC - 5.25 V, VDD - 12.6 V,	V   - 2.7 V			60	] "^
	Low-level	FFD	V	V = 0.4 V			-0.4	
lŧL.	input current	OSCIN	V <sub>CC</sub> = 5.25 V, V <sub>DD</sub> = 12.6 V,	V  = 0.4 V			-3.2	mA
	Short-circuit	All except	V <sub>CC</sub> ≈ 5.25 V		~20		-100	
los	output current‡	φ1, φ2, φ3, φ4	VCC - 5.25 V		~20		-100	mA
	Cumply assurant from Va	_	V <sub>CC</sub> = 5.25 V, FFD and OSCI	N at GND,		105	175	
1cc	Supply current from Vo	iC .	Outputs open			105	1/5	mA
1	Supply current from V		V <sub>CC</sub> = 5.25 V, V <sub>DD</sub> = 12.6 V,		12	20		
ססי	and bis correct from A C	D	FFD and OSCIN at GND, Outputs open					mA

 $<sup>^{\</sup>uparrow}\text{All typical values are at V}_{CC}$  = 5 V, V $_{DD}$  = 12 V, T $_{A}$  = 25°C.

### switching characteristics, TA = 25°C, VCC = 5 V, VDD = 12 V, fosc = 48 MHz, see figure 1

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>out</sub>	Output frequency, any φ or φ TTL			3		MHz
out	Output frequency, OSCOUT	1		12		MHz
<sup>t</sup> c(ø)	Cycle time, any φ output	1		333		ns
t <sub>r(<math>\phi</math>)</sub>	Riss time, any φ output	1	5		20	ns
<sup>t</sup> f(φ)	Fall time, any φ output	1	5		20	ns
<sup>t</sup> w(φ)	Pulse width, any φ output high	1	40			ns
<sup>t</sup> φ1L, φ2H	Delay time, ¢1 low to ¢2 high		0	5	15	ns.
<sup>1</sup> φ2L, φ3H	Delay time, ¢2 low to ¢3 high	1	0	5	15	ns
φ3L, φ4H	Delay time, ¢3 low to ¢4 high	1	0	5	15	ns
φ4L, φ1H	Delay time, $\phi4$ low to $\phi1$ high	Output loads:	0	5	15	ns
φ1H, φ2H	Delay time, ¢1 high to ¢2 high	φ1, φ3, φ4: 100 pF to GND	70	83		n <b>s</b>
φ2H, φ3H	Delay time, ø2 high to ø3 high	¢2: 200 pF to GND	70	83		ns
<b>φ3H, φ4H</b>	Delay time, ¢3 high to ¢4 high	Others: R <sub>L</sub> = 2 kΩ,	70	83		กร
<sup>t</sup> φ4H, φ1H	Delay time, φ4 high to φ1 high	C <sub>L</sub> = 15 pF	70	83		ns
tøH, ØTL	Delay time, φ <sub>n</sub> high to φ <sub>n</sub> TTL low	See Note 2		-8		ns
<sup>t</sup> φL, ΦTH	Delay time, φ <sub>n</sub> low to φ <sub>n</sub> TTL high	1		-19		ns
<b>'</b> ∮3 <b>L</b> , ΩН	Delay time, \$\phi 3 low to FFQ output high	1		-7		ns
¹ø3L, QL	Delay time, \$3 low to FFQ output low	1		-12		ns
<sup>t</sup> øŁ, OSOH	Delay time, $\phi$ low to OSCOUT high			-5		ns
toH, OSOL	Delay time, FFQ high to OSCOUT low	1		-13		ns

NOTE 2: Use load circuit for bi-state totem-pole outputs, page 3-11.

<sup>‡</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Outputs \$\phi1\$, \$\phi2\$, \$\phi3\$, and \$\phi4\$ do not have short-circuit protection.

### TYPE SN74LS362 (TIM9994) FOUR-PHASE CLOCK GENERATOR/DRIVER

#### **APPLICATION INFORMATION**

Figure 2 shows the 'LS362 connected to a TMS9900. The oscillator is shown operating with a quartz crystal and an LC circuit connected to the tank terminals.

For operation of the TMS 9900 microprocessor at 3 MHz, the frequency reference will need a resonant frequency of 48 MHz (16 x 3 MHz). A quartz crystal used as a frequency reference should be made for series-mode operation with a resistance in the 20- to 75-ohm range and be capable of a minimum of 2 mW power dissipation. Typical frequency tolerance is  $\pm 0.005\%$ . For 48-MHz operation a third-overtone crystal is used. The inductance L connected across the tank terminals should be 0.47  $\mu$ H  $\pm$  10%, and the capacitance C (including board capacity) should be 22 pF  $\pm$  5%. The LC circuit should be tuned to the third-overtone crystal frequency for best results. A 0.1- $\mu$ F capacitor can be substituted for the quartz crystal. With a capacitor rather than a crystal, the LC tuned circuit establishes the operating frequencies. LC component values for operation at any frequency can be computed from  $f_{OSC} = 1/(2\pi\sqrt{LC})$  where  $f_{OSC}$  is the oscillator frequency, L is the inductance value in henries, and C is the capacitance value in farads.

When the internal oscillator is being used, OSCIN should be connected to  $V_{CC}$  through a resistor (1  $k\Omega$  nominal) and an LC tank circuit must be connected to the tank inputs. An external oscillator can be used by connecting it to OSCIN and disabling the internal oscillator by connecting the crystal terminals to  $V_{CC}$  and leaving the tank inputs open. An external oscillator must have a frequency four times the desired output clock frequency and a 25% duty cycle. See Figure 3.

The first low-level external clock pulse will preset the divide-by-four counter, allowing the external oscillator signal to directly drive the phase generator. Figure 3 is a timing diagram illustrating operation with an external oscillator.

Resistors between  $\phi$ 1,  $\phi$ 2,  $\phi$ 3, and  $\phi$ 4 outputs of the 'LS362 and the corresponding clock input terminals of the TMS 9900 should be in the 10- to 20-ohm range (See Figure 2). Their purpose is to minimize overshoot and undershoot. The required resistance value is dependent on circuit layout. Clock signal interconnections should be as short as possible.

The D-type flip-flop associated with pins FFD and FFQ can be used to provide a power-on reset and a manual reset to the TMS 9900 as shown in Figure 4. A Schmitt-trigger circuit driving the D input generates a fast-rising waveform when the input voltage rises to a specific value. At power turn-on, voltage across the  $0.1~\mu F$  capacitor in Figure 4 will rise towards  $V_{CC}$ . This circuit provides a delay that resets the TMS 9900 after  $V_{CC}$  has stabilized. An optional manual reset switch can be connected to the delay circuit for resetting the TMS 9900 at any time. The TMS 9900 HOLD signal could alternately be actuated by FFD.

The ground terminals GND1 and GND2 should be connected together and to system ground.

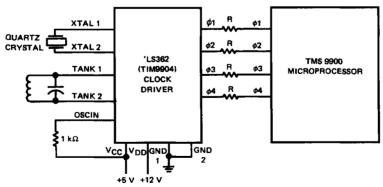


FIGURE 2-'LS362 CRYSTAL-CONTROLLED OPERATION

# TYPE SN74L8362 (TIM9904) FOUR-PHASE CLOCK GENERATOR/DRIVER

#### **APPLICATION INFORMATION**

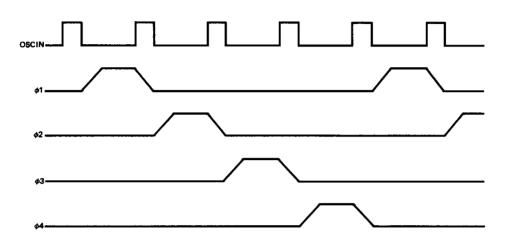


FIGURE 3-EXTERNAL OSCILLATOR TIMING

