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ILI6485

Single Chip for 480RGBx272 TFT Panel 720x544 Driver with Timing Controller

Preliminary Specification

Version: V001
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ILI TECHNOLOGY CORP.
10F, No.1, Taiyuan 2nd St., Zhubei City, Hsinchu
Taiwan 302, R.O.C.
Tel.886-3-5600099; Fax.886-3-5600055
http://www.ilitek.com

Table of Contents

1. GENERAL DESCRIPTION

ILI6485 offers all-in-one chip solution of 480RGBx272 for color TFT-LCD panel. This chip incorporated with digital timing generator, source and gate driver, power supply circuit and embedded serial communication interface for function setting. The source output support real 8-bit resolution and 256-gray scale with small output deviation are designed to support higher color resolution. The power supply circuit incorporated with step-up circuit, regulators and operational amplifiers to generate power supply voltages to drive TFT LCD.

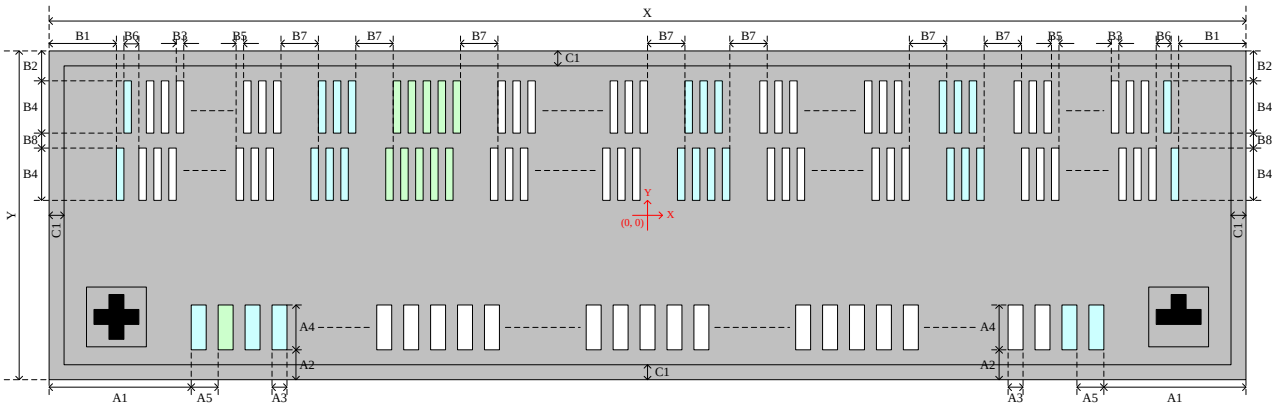
2. FEATURES

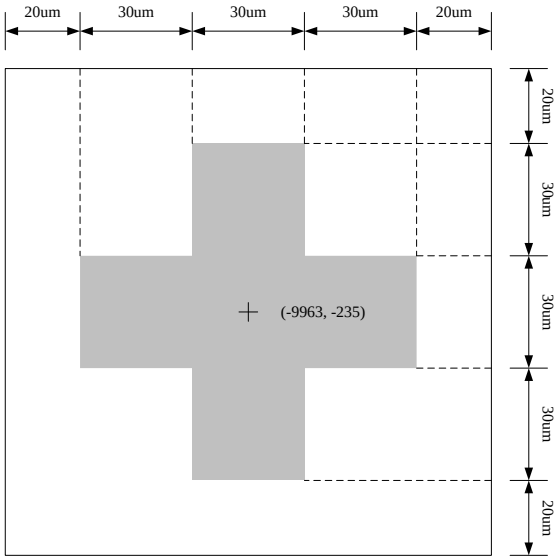
- Display Maximum Resolution: 480*RGB (H) *272(V).
  - ✓ Support dual gate panel resolution:
    480RGB*272 / 320RGB*240 / 240RGB*240
  - ✓ Support single gate panel resolution:
    240RGB*320 / 240RGB*240
- LCD Driver Output Circuits.
  - ✓ Source Outputs: 720 Channels.
  - ✓ Gate Outputs: 544 Channels.
  - ✓ Common Electrode Output.
- 256 gray scale with true 8 bit DAC.
- Support SYNC, SYNC-DE and DE mode RGB interface input timing.
- Support 8-bit serial and 24-bit parallel RGB interface.
- Support 3- wire Serial Peripheral Interface to config and control display.
- On Chip Build-In Circuits.
  - ✓ DC/DC Converter.
  - ✓ Multi-OTP Circuit.
  - ✓ Timing Controller.
- Driving Algorithm.
  - ✓ Dot Inversion.
- Wide Supply Voltage Range.
  - ✓ I/O Voltage (VDDI to VSSD): 3.0V ~ VCI.
  - ✓ Analog Voltage (VCI to VSSA): 3.0V ~ 3.6V.
  - ✓ Charge pump Voltage (VCIP to VSSP): 3.0V ~ 3.6V.
- On-Chip Power System.
  - ✓ VGMP: +4.672 ~ +6.704V.
  - ✓ VGMN: -4.992V ~ -2.9600V.
  - ✓ Gate driver HIGH level (VGH to VSSA): +10.16V ~ +18V.
  - ✓ Gate driver LOW level (VGL to VSSA): -13V ~ -7V.
- Optimized layout for COG Assembly.

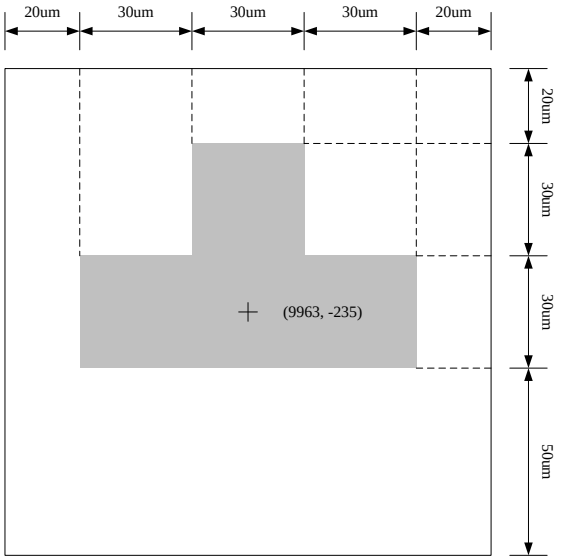
- The multi-OTP provides three times programming to set LCD initial parameters.
  - ✓ 6-bit VCOM offset adjustment.
  - ✓ 7-bit ID setting for end user use.
  - ✓ **2-bit resolution setting.**
  - ✓ **1-bit Dual gate / Single gate setting.**
  - ✓ Positive and negative gamma voltage setting.

3. PAD ARRANGEMENT

3.1 Bump&Align_Mark Information







Chip thickness→300um

Symbol	Dimensions(um)	Symbol	Dimensions (um)	Symbol	Dimensions (um)
A1	343	B2	51.5	B8	33
A2	51.5	B3	12	C1	30
A3	32	B4	97	X	20188
A4	97	B5	15	Y	714
A5	59	B6	30		
B1	143	B7	75		

***Remark: Chip dimension include scribe line**

4. PAD CENTER COORDINATES

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
1	DUMMY	-9735	-257	51	VSSD	-6785	-257	101	VDIR	-3835	-257
2	VSSD	-9676	-257	52	VSSD	-6726	-257	102	VDIR	-3776	-257
3	DUMMY	-9617	-257	53	VSSD	-6667	-257	103	TEST_X[3]	-3717	-257
4	DUMMY	-9558	-257	54	VDDD	-6608	-257	104	TEST_X[3]	-3658	-257
5	VSSD	-9499	-257	55	VDDD	-6549	-257	105	TEST_X[4]	-3599	-257
6	VPP	-9440	-257	56	VDDD	-6490	-257	106	TEST_X[4]	-3540	-257
7	VPP	-9381	-257	57	VDDD	-6431	-257	107	CSX	-3481	-257
8	VPP	-9322	-257	58	VDDD	-6372	-257	108	CSX	-3422	-257
9	VPP	-9263	-257	59	VDDD	-6313	-257	109	SDA	-3363	-257
10	VPP	-9204	-257	60	VDDI	-6254	-257	110	SDA	-3304	-257
11	VPP	-9145	-257	61	VDDI	-6195	-257	111	SCL	-3245	-257
12	VSSD	-9086	-257	62	VDDI	-6136	-257	112	SCL	-3186	-257
13	DUMMY	-9027	-257	63	VDDI	-6077	-257	113	STBYB	-3127	-257
14	DUMMY	-8968	-257	64	VDDI	-6018	-257	114	STBYB	-3068	-257
15	DUMMY	-8909	-257	65	VDDI	-5959	-257	115	TEST_X[5]	-3009	-257
16	DUMMY	-8850	-257	66	VCI	-5900	-257	116	TEST_X[5]	-2950	-257
17	VSSD	-8791	-257	67	VCI	-5841	-257	117	RESX	-2891	-257
18	VGMP	-8732	-257	68	VCI	-5782	-257	118	RESX	-2832	-257
19	VGMP	-8673	-257	69	VCI	-5723	-257	119	SYNC	-2773	-257
20	VGMP	-8614	-257	70	VCI	-5664	-257	120	SYNC	-2714	-257
21	VGMP	-8555	-257	71	VCI	-5605	-257	121	TEST_X[6]	-2655	-257
22	VGMP	-8496	-257	72	VCI	-5546	-257	122	TEST_X[6]	-2596	-257
23	VGMP	-8437	-257	73	VCI	-5487	-257	123	DUMMY	-2537	-257
24	VGMN	-8378	-257	74	TEST_ANA[0]	-5428	-257	124	DUMMY	-2478	-257
25	VGMN	-8319	-257	75	VSYNC	-5369	-257	125	VSSD	-2419	-257
26	VGMN	-8260	-257	76	VSYNC	-5310	-257	126	DR7	-2360	-257
27	VGMN	-8201	-257	77	HSYNC	-5251	-257	127	DR7	-2301	-257
28	VGMN	-8142	-257	78	HSYNC	-5192	-257	128	DR6	-2242	-257
29	VGMN	-8083	-257	79	DCLK	-5133	-257	129	DR6	-2183	-257
30	VCOM	-8024	-257	80	DCLK	-5074	-257	130	DR5	-2124	-257
31	VCOM	-7965	-257	81	VDPOL	-5015	-257	131	DR5	-2065	-257
32	VCOM	-7906	-257	82	VDPOL	-4956	-257	132	DR4	-2006	-257
33	VCOM	-7847	-257	83	HDPOL	-4897	-257	133	DR4	-1947	-257
34	VCOM	-7788	-257	84	HDPOL	-4838	-257	134	DR3	-1888	-257
35	VCOM	-7729	-257	85	DCLKPOL	-4779	-257	135	DR3	-1829	-257
36	VSSD	-7670	-257	86	DCLKPOL	-4720	-257	136	DR2	-1770	-257
37	DUMMY	-7611	-257	87	SBGR	-4661	-257	137	DR2	-1711	-257
38	DUMMY	-7552	-257	88	SBGR	-4602	-257	138	DR1	-1652	-257
39	VSSD	-7493	-257	89	DE	-4543	-257	139	DR1	-1593	-257
40	DUAL	-7434	-257	90	DE	-4484	-257	140	DR0	-1534	-257
41	DUAL	-7375	-257	91	DUMMY	-4425	-257	141	DR0	-1475	-257
42	RES[1]	-7316	-257	92	DUMMY	-4366	-257	142	DG7	-1416	-257
43	RES[1]	-7257	-257	93	DUMMY	-4307	-257	143	DG7	-1357	-257
44	RES[0]	-7198	-257	94	DUMMY	-4248	-257	144	DG6	-1298	-257
45	RES[0]	-7139	-257	95	PARA_SERI	-4189	-257	145	DG6	-1239	-257
46	VSSD	-7080	-257	96	PARA_SERI	-4130	-257	146	DG5	-1180	-257
47	VSSD	-7021	-257	97	EXTC	-4071	-257	147	DG5	-1121	-257
48	VSSD	-6962	-257	98	EXTC	-4012	-257	148	DG4	-1062	-257
49	VSSD	-6903	-257	99	HDIR	-3953	-257	149	DG4	-1003	-257
50	VSSD	-6844	-257	100	HDIR	-3894	-257	150	DG3	-944	-257

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
151	DG3	-885	-257	201	TEST_OUT[11]	2065	-257	251	VSSP	5015	-257
152	DG2	-826	-257	202	TEST_OUT[11]	2124	-257	252	VSSP	5074	-257
153	DG2	-767	-257	203	TEST_OUT[12]	2183	-257	253	VSSP	5133	-257
154	DG1	-708	-257	204	TEST_OUT[12]	2242	-257	254	VSSP	5192	-257
155	DG1	-649	-257	205	TEST_OUT[13]	2301	-257	255	VSSP	5251	-257
156	DG0	-590	-257	206	TEST_OUT[13]	2360	-257	256	VSSP	5310	-257
157	DG0	-531	-257	207	TEST_IN[0]	2419	-257	257	VSSP	5369	-257
158	DB7	-472	-257	208	TEST_IN[1]	2478	-257	258	DUMMY	5428	-257
159	DB7	-413	-257	209	TEST_IN[2]	2537	-257	259	DUMMY	5487	-257
160	DB6	-354	-257	210	TEST_IN[3]	2596	-257	260	DUMMY	5546	-257
161	DB6	-295	-257	211	DUMMY	2655	-257	261	DUMMY	5605	-257
162	DB5	-236	-257	212	DUMMY	2714	-257	262	VSP_DC	5664	-257
163	DB5	-177	-257	213	DUMMY	2773	-257	263	VSP_DC	5723	-257
164	DB4	-118	-257	214	DUMMY	2832	-257	264	VSP_DC	5782	-257
165	DB4	-59	-257	215	DUMMY	2891	-257	265	VSP_DC	5841	-257
166	DB3	0	-257	216	DUMMY	2950	-257	266	VSP_DC	5900	-257
167	DB3	59	-257	217	VSSA	3009	-257	267	VSP_DC	5959	-257
168	DB2	118	-257	218	VSSA	3068	-257	268	TEST_ANA[5]	6018	-257
169	DB2	177	-257	219	VSSA	3127	-257	269	TEST_ANA[5]	6077	-257
170	DB1	236	-257	220	VSSA	3186	-257	270	TEST_ANA[5]	6136	-257
171	DB1	295	-257	221	VSSA	3245	-257	271	TEST_ANA[6]	6195	-257
172	DB0	354	-257	222	VSSA	3304	-257	272	TEST_ANA[6]	6254	-257
173	DB0	413	-257	223	VSSA	3363	-257	273	TEST_ANA[6]	6313	-257
174	DUMMY	472	-257	224	VSN_AC	3422	-257	274	VSN_DC	6372	-257
175	DUMMY	531	-257	225	VSN_AC	3481	-257	275	VSN_DC	6431	-257
176	DUMMY	590	-257	226	VSN_AC	3540	-257	276	VSN_DC	6490	-257
177	DUMMY	649	-257	227	VSN_AC	3599	-257	277	VSN_DC	6549	-257
178	DUMMY	708	-257	228	VSN_AC	3658	-257	278	VSN_DC	6608	-257
179	TEST_OUT[0]	767	-257	229	VSN_AC	3717	-257	279	VSN_DC	6667	-257
180	TEST_OUT[0]	826	-257	230	TEST_ANA[1]	3776	-257	280	TEST_ANA[7]	6726	-257
181	TEST_OUT[1]	885	-257	231	TEST_ANA[1]	3835	-257	281	TEST_ANA[7]	6785	-257
182	TEST_OUT[1]	944	-257	232	TEST_ANA[1]	3894	-257	282	TEST_ANA[7]	6844	-257
183	TEST_OUT[2]	1003	-257	233	TEST_ANA[2]	3953	-257	283	TEST_ANA[8]	6903	-257
184	TEST_OUT[2]	1062	-257	234	TEST_ANA[2]	4012	-257	284	TEST_ANA[8]	6962	-257
185	TEST_OUT[3]	1121	-257	235	TEST_ANA[2]	4071	-257	285	TEST_ANA[8]	7021	-257
186	TEST_OUT[3]	1180	-257	236	TEST_ANA[3]	4130	-257	286	VCIP	7080	-257
187	TEST_OUT[4]	1239	-257	237	TEST_ANA[3]	4189	-257	287	VCIP	7139	-257
188	TEST_OUT[4]	1298	-257	238	TEST_ANA[3]	4248	-257	288	VCIP	7198	-257
189	TEST_OUT[5]	1357	-257	239	TEST_ANA[4]	4307	-257	289	VCIP	7257	-257
190	TEST_OUT[5]	1416	-257	240	TEST_ANA[4]	4366	-257	290	VCIP	7316	-257
191	TEST_OUT[6]	1475	-257	241	TEST_ANA[4]	4425	-257	291	VCIP	7375	-257
192	TEST_OUT[6]	1534	-257	242	VSP_AC	4484	-257	292	VCIP	7434	-257
193	TEST_OUT[7]	1593	-257	243	VSP_AC	4543	-257	293	VCIP	7493	-257
194	TEST_OUT[7]	1652	-257	244	VSP_AC	4602	-257	294	VGSP	7552	-257
195	TEST_OUT[8]	1711	-257	245	VSP_AC	4661	-257	295	VGSP	7611	-257
196	TEST_OUT[8]	1770	-257	246	VSP_AC	4720	-257	296	VGSP	7670	-257
197	TEST_OUT[9]	1829	-257	247	VSP_AC	4779	-257	297	VGSP	7729	-257
198	TEST_OUT[9]	1888	-257	248	VSP_AC	4838	-257	298	VGSP	7788	-257
199	TEST_OUT[10]	1947	-257	249	VSP_AC	4897	-257	299	VGSP	7847	-257
200	TEST_OUT[10]	2006	-257	250	VSSP	4956	-257	300	TEST_ANA[9]	7906	-257

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
301	TEST_ANA[9]	7965	-257	351	G[36]	9645	257	401	G[136]	8895	257
302	TEST_ANA[9]	8024	-257	352	G[38]	9630	127	402	G[138]	8880	127
303	TEST_ANA[10]	8083	-257	353	G[40]	9615	257	403	G[140]	8865	257
304	TEST_ANA[10]	8142	-257	354	G[42]	9600	127	404	G[142]	8850	127
305	TEST_ANA[10]	8201	-257	355	G[44]	9585	257	405	G[144]	8835	257
306	VGH	8260	-257	356	G[46]	9570	127	406	G[146]	8820	127
307	VGH	8319	-257	357	G[48]	9555	257	407	G[148]	8805	257
308	VGH	8378	-257	358	G[50]	9540	127	408	G[150]	8790	127
309	VGH	8437	-257	359	G[52]	9525	257	409	G[152]	8775	257
310	VGH	8496	-257	360	G[54]	9510	127	410	G[154]	8760	127
311	VGH	8555	-257	361	G[56]	9495	257	411	G[156]	8745	257
312	TEST_ANA[11]	8614	-257	362	G[58]	9480	127	412	G[158]	8730	127
313	TEST_ANA[11]	8673	-257	363	G[60]	9465	257	413	G[160]	8715	257
314	TEST_ANA[11]	8732	-257	364	G[62]	9450	127	414	G[162]	8700	127
315	TEST_ANA[11]	8791	-257	365	G[64]	9435	257	415	G[164]	8685	257
316	TEST_ANA[11]	8850	-257	366	G[66]	9420	127	416	G[166]	8670	127
317	TEST_ANA[11]	8909	-257	367	G[68]	9405	257	417	G[168]	8655	257
318	TEST_ANA[12]	8968	-257	368	G[70]	9390	127	418	G[170]	8640	127
319	TEST_ANA[12]	9027	-257	369	G[72]	9375	257	419	G[172]	8625	257
320	TEST_ANA[12]	9086	-257	370	G[74]	9360	127	420	G[174]	8610	127
321	TEST_ANA[12]	9145	-257	371	G[76]	9345	257	421	G[176]	8595	257
322	TEST_ANA[12]	9204	-257	372	G[78]	9330	127	422	G[178]	8580	127
323	TEST_ANA[12]	9263	-257	373	G[80]	9315	257	423	G[180]	8565	257
324	VGL	9322	-257	374	G[82]	9300	127	424	G[182]	8550	127
325	VGL	9381	-257	375	G[84]	9285	257	425	G[184]	8535	257
326	VGL	9440	-257	376	G[86]	9270	127	426	G[186]	8520	127
327	VGL	9499	-257	377	G[88]	9255	257	427	G[188]	8505	257
328	VGL	9558	-257	378	G[90]	9240	127	428	G[190]	8490	127
329	VGL	9617	-257	379	G[92]	9225	257	429	G[192]	8475	257
330	DUMMY	9676	-257	380	G[94]	9210	127	430	G[194]	8460	127
331	DUMMY	9735	-257	381	G[96]	9195	257	431	G[196]	8445	257
332	VSSA	9945	127	382	G[98]	9180	127	432	G[198]	8430	127
333	VSSA	9930	257	383	G[100]	9165	257	433	G[200]	8415	257
334	G[2]	9900	127	384	G[102]	9150	127	434	G[202]	8400	127
335	G[4]	9885	257	385	G[104]	9135	257	435	G[204]	8385	257
336	G[6]	9870	127	386	G[106]	9120	127	436	G[206]	8370	127
337	G[8]	9855	257	387	G[108]	9105	257	437	G[208]	8355	257
338	G[10]	9840	127	388	G[110]	9090	127	438	G[210]	8340	127
339	G[12]	9825	257	389	G[112]	9075	257	439	G[212]	8325	257
340	G[14]	9810	127	390	G[114]	9060	127	440	G[214]	8310	127
341	G[16]	9795	257	391	G[116]	9045	257	441	G[216]	8295	257
342	G[18]	9780	127	392	G[118]	9030	127	442	G[218]	8280	127
343	G[20]	9765	257	393	G[120]	9015	257	443	G[220]	8265	257
344	G[22]	9750	127	394	G[122]	9000	127	444	G[222]	8250	127
345	G[24]	9735	257	395	G[124]	8985	257	445	G[224]	8235	257
346	G[26]	9720	127	396	G[126]	8970	127	446	G[226]	8220	127
347	G[28]	9705	257	397	G[128]	8955	257	447	G[228]	8205	257
348	G[30]	9690	127	398	G[130]	8940	127	448	G[230]	8190	127
349	G[32]	9675	257	399	G[132]	8925	257	449	G[232]	8175	257
350	G[34]	9660	127	400	G[134]	8910	127	450	G[234]	8160	127

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
451	G[236]	8145	257	501	G[336]	7395	257	551	G[436]	6645	257
452	G[238]	8130	127	502	G[338]	7380	127	552	G[438]	6630	127
453	G[240]	8115	257	503	G[340]	7365	257	553	G[440]	6615	257
454	G[242]	8100	127	504	G[342]	7350	127	554	G[442]	6600	127
455	G[244]	8085	257	505	G[344]	7335	257	555	G[444]	6585	257
456	G[246]	8070	127	506	G[346]	7320	127	556	G[446]	6570	127
457	G[248]	8055	257	507	G[348]	7305	257	557	G[448]	6555	257
458	G[250]	8040	127	508	G[350]	7290	127	558	G[450]	6540	127
459	G[252]	8025	257	509	G[352]	7275	257	559	G[452]	6525	257
460	G[254]	8010	127	510	G[354]	7260	127	560	G[454]	6510	127
461	G[256]	7995	257	511	G[356]	7245	257	561	G[456]	6495	257
462	G[258]	7980	127	512	G[358]	7230	127	562	G[458]	6480	127
463	G[260]	7965	257	513	G[360]	7215	257	563	G[460]	6465	257
464	G[262]	7950	127	514	G[362]	7200	127	564	G[462]	6450	127
465	G[264]	7935	257	515	G[364]	7185	257	565	G[464]	6435	257
466	G[266]	7920	127	516	G[366]	7170	127	566	G[466]	6420	127
467	G[268]	7905	257	517	G[368]	7155	257	567	G[468]	6405	257
468	G[270]	7890	127	518	G[370]	7140	127	568	G[470]	6390	127
469	G[272]	7875	257	519	G[372]	7125	257	569	G[472]	6375	257
470	G[274]	7860	127	520	G[374]	7110	127	570	G[474]	6360	127
471	G[276]	7845	257	521	G[376]	7095	257	571	G[476]	6345	257
472	G[278]	7830	127	522	G[378]	7080	127	572	G[478]	6330	127
473	G[280]	7815	257	523	G[380]	7065	257	573	G[480]	6315	257
474	G[282]	7800	127	524	G[382]	7050	127	574	G[482]	6300	127
475	G[284]	7785	257	525	G[384]	7035	257	575	G[484]	6285	257
476	G[286]	7770	127	526	G[386]	7020	127	576	G[486]	6270	127
477	G[288]	7755	257	527	G[388]	7005	257	577	G[488]	6255	257
478	G[290]	7740	127	528	G[390]	6990	127	578	G[490]	6240	127
479	G[292]	7725	257	529	G[392]	6975	257	579	G[492]	6225	257
480	G[294]	7710	127	530	G[394]	6960	127	580	G[494]	6210	127
481	G[296]	7695	257	531	G[396]	6945	257	581	G[496]	6195	257
482	G[298]	7680	127	532	G[398]	6930	127	582	G[498]	6180	127
483	G[300]	7665	257	533	G[400]	6915	257	583	G[500]	6165	257
484	G[302]	7650	127	534	G[402]	6900	127	584	G[502]	6150	127
485	G[304]	7635	257	535	G[404]	6885	257	585	G[504]	6135	257
486	G[306]	7620	127	536	G[406]	6870	127	586	G[506]	6120	127
487	G[308]	7605	257	537	G[408]	6855	257	587	G[508]	6105	257
488	G[310]	7590	127	538	G[410]	6840	127	588	G[510]	6090	127
489	G[312]	7575	257	539	G[412]	6825	257	589	G[512]	6075	257
490	G[314]	7560	127	540	G[414]	6810	127	590	G[514]	6060	127
491	G[316]	7545	257	541	G[416]	6795	257	591	G[516]	6045	257
492	G[318]	7530	127	542	G[418]	6780	127	592	G[518]	6030	127
493	G[320]	7515	257	543	G[420]	6765	257	593	G[520]	6015	257
494	G[322]	7500	127	544	G[422]	6750	127	594	G[522]	6000	127
495	G[324]	7485	257	545	G[424]	6735	257	595	G[524]	5985	257
496	G[326]	7470	127	546	G[426]	6720	127	596	G[526]	5970	127
497	G[328]	7455	257	547	G[428]	6705	257	597	G[528]	5955	257
498	G[330]	7440	127	548	G[430]	6690	127	598	G[530]	5940	127
499	G[332]	7425	257	549	G[432]	6675	257	599	G[532]	5925	257
500	G[334]	7410	127	550	G[434]	6660	127	600	G[534]	5910	127

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
601	G[536]	5895	257	651	S[40]	5025	257	701	S[90]	4275	257
602	G[538]	5880	127	652	S[41]	5010	127	702	S[91]	4260	127
603	G[540]	5865	257	653	S[42]	4995	257	703	S[92]	4245	257
604	G[542]	5850	127	654	S[43]	4980	127	704	S[93]	4230	127
605	G[544]	5835	257	655	S[44]	4965	257	705	S[94]	4215	257
606	DUMMY	5760	127	656	S[45]	4950	127	706	S[95]	4200	127
607	DUMMY	5745	257	657	S[46]	4935	257	707	S[96]	4185	257
608	DUMMY	5730	127	658	S[47]	4920	127	708	S[97]	4170	127
609	DUMMY	5715	257	659	S[48]	4905	257	709	S[98]	4155	257
610	DUMMY	5700	127	660	S[49]	4890	127	710	S[99]	4140	127
611	DUMMY	5685	257	661	S[50]	4875	257	711	S[100]	4125	257
612	S[1]	5610	127	662	S[51]	4860	127	712	S[101]	4110	127
613	S[2]	5595	257	663	S[52]	4845	257	713	S[102]	4095	257
614	S[3]	5580	127	664	S[53]	4830	127	714	S[103]	4080	127
615	S[4]	5565	257	665	S[54]	4815	257	715	S[104]	4065	257
616	S[5]	5550	127	666	S[55]	4800	127	716	S[105]	4050	127
617	S[6]	5535	257	667	S[56]	4785	257	717	S[106]	4035	257
618	S[7]	5520	127	668	S[57]	4770	127	718	S[107]	4020	127
619	S[8]	5505	257	669	S[58]	4755	257	719	S[108]	4005	257
620	S[9]	5490	127	670	S[59]	4740	127	720	S[109]	3990	127
621	S[10]	5475	257	671	S[60]	4725	257	721	S[110]	3975	257
622	S[11]	5460	127	672	S[61]	4710	127	722	S[111]	3960	127
623	S[12]	5445	257	673	S[62]	4695	257	723	S[112]	3945	257
624	S[13]	5430	127	674	S[63]	4680	127	724	S[113]	3930	127
625	S[14]	5415	257	675	S[64]	4665	257	725	S[114]	3915	257
626	S[15]	5400	127	676	S[65]	4650	127	726	S[115]	3900	127
627	S[16]	5385	257	677	S[66]	4635	257	727	S[116]	3885	257
628	S[17]	5370	127	678	S[67]	4620	127	728	S[117]	3870	127
629	S[18]	5355	257	679	S[68]	4605	257	729	S[118]	3855	257
630	S[19]	5340	127	680	S[69]	4590	127	730	S[119]	3840	127
631	S[20]	5325	257	681	S[70]	4575	257	731	S[120]	3825	257
632	S[21]	5310	127	682	S[71]	4560	127	732	S[121]	3810	127
633	S[22]	5295	257	683	S[72]	4545	257	733	S[122]	3795	257
634	S[23]	5280	127	684	S[73]	4530	127	734	S[123]	3780	127
635	S[24]	5265	257	685	S[74]	4515	257	735	S[124]	3765	257
636	S[25]	5250	127	686	S[75]	4500	127	736	S[125]	3750	127
637	S[26]	5235	257	687	S[76]	4485	257	737	S[126]	3735	257
638	S[27]	5220	127	688	S[77]	4470	127	738	S[127]	3720	127
639	S[28]	5205	257	689	S[78]	4455	257	739	S[128]	3705	257
640	S[29]	5190	127	690	S[79]	4440	127	740	S[129]	3690	127
641	S[30]	5175	257	691	S[80]	4425	257	741	S[130]	3675	257
642	S[31]	5160	127	692	S[81]	4410	127	742	S[131]	3660	127
643	S[32]	5145	257	693	S[82]	4395	257	743	S[132]	3645	257
644	S[33]	5130	127	694	S[83]	4380	127	744	S[133]	3630	127
645	S[34]	5115	257	695	S[84]	4365	257	745	S[134]	3615	257
646	S[35]	5100	127	696	S[85]	4350	127	746	S[135]	3600	127
647	S[36]	5085	257	697	S[86]	4335	257	747	S[136]	3585	257
648	S[37]	5070	127	698	S[87]	4320	127	748	S[137]	3570	127
649	S[38]	5055	257	699	S[88]	4305	257	749	S[138]	3555	257
650	S[39]	5040	127	700	S[89]	4290	127	750	S[139]	3540	127

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
751	S[140]	3525	257	801	S[190]	2775	257	851	S[240]	2025	257
752	S[141]	3510	127	802	S[191]	2760	127	852	S[241]	2010	127
753	S[142]	3495	257	803	S[192]	2745	257	853	S[242]	1995	257
754	S[143]	3480	127	804	S[193]	2730	127	854	S[243]	1980	127
755	S[144]	3465	257	805	S[194]	2715	257	855	S[244]	1965	257
756	S[145]	3450	127	806	S[195]	2700	127	856	S[245]	1950	127
757	S[146]	3435	257	807	S[196]	2685	257	857	S[246]	1935	257
758	S[147]	3420	127	808	S[197]	2670	127	858	S[247]	1920	127
759	S[148]	3405	257	809	S[198]	2655	257	859	S[248]	1905	257
760	S[149]	3390	127	810	S[199]	2640	127	860	S[249]	1890	127
761	S[150]	3375	257	811	S[200]	2625	257	861	S[250]	1875	257
762	S[151]	3360	127	812	S[201]	2610	127	862	S[251]	1860	127
763	S[152]	3345	257	813	S[202]	2595	257	863	S[252]	1845	257
764	S[153]	3330	127	814	S[203]	2580	127	864	S[253]	1830	127
765	S[154]	3315	257	815	S[204]	2565	257	865	S[254]	1815	257
766	S[155]	3300	127	816	S[205]	2550	127	866	S[255]	1800	127
767	S[156]	3285	257	817	S[206]	2535	257	867	S[256]	1785	257
768	S[157]	3270	127	818	S[207]	2520	127	868	S[257]	1770	127
769	S[158]	3255	257	819	S[208]	2505	257	869	S[258]	1755	257
770	S[159]	3240	127	820	S[209]	2490	127	870	S[259]	1740	127
771	S[160]	3225	257	821	S[210]	2475	257	871	S[260]	1725	257
772	S[161]	3210	127	822	S[211]	2460	127	872	S[261]	1710	127
773	S[162]	3195	257	823	S[212]	2445	257	873	S[262]	1695	257
774	S[163]	3180	127	824	S[213]	2430	127	874	S[263]	1680	127
775	S[164]	3165	257	825	S[214]	2415	257	875	S[264]	1665	257
776	S[165]	3150	127	826	S[215]	2400	127	876	S[265]	1650	127
777	S[166]	3135	257	827	S[216]	2385	257	877	S[266]	1635	257
778	S[167]	3120	127	828	S[217]	2370	127	878	S[267]	1620	127
779	S[168]	3105	257	829	S[218]	2355	257	879	S[268]	1605	257
780	S[169]	3090	127	830	S[219]	2340	127	880	S[269]	1590	127
781	S[170]	3075	257	831	S[220]	2325	257	881	S[270]	1575	257
782	S[171]	3060	127	832	S[221]	2310	127	882	S[271]	1560	127
783	S[172]	3045	257	833	S[222]	2295	257	883	S[272]	1545	257
784	S[173]	3030	127	834	S[223]	2280	127	884	S[273]	1530	127
785	S[174]	3015	257	835	S[224]	2265	257	885	S[274]	1515	257
786	S[175]	3000	127	836	S[225]	2250	127	886	S[275]	1500	127
787	S[176]	2985	257	837	S[226]	2235	257	887	S[276]	1485	257
788	S[177]	2970	127	838	S[227]	2220	127	888	S[277]	1470	127
789	S[178]	2955	257	839	S[228]	2205	257	889	S[278]	1455	257
790	S[179]	2940	127	840	S[229]	2190	127	890	S[279]	1440	127
791	S[180]	2925	257	841	S[230]	2175	257	891	S[280]	1425	257
792	S[181]	2910	127	842	S[231]	2160	127	892	S[281]	1410	127
793	S[182]	2895	257	843	S[232]	2145	257	893	S[282]	1395	257
794	S[183]	2880	127	844	S[233]	2130	127	894	S[283]	1380	127
795	S[184]	2865	257	845	S[234]	2115	257	895	S[284]	1365	257
796	S[185]	2850	127	846	S[235]	2100	127	896	S[285]	1350	127
797	S[186]	2835	257	847	S[236]	2085	257	897	S[286]	1335	257
798	S[187]	2820	127	848	S[237]	2070	127	898	S[287]	1320	127
799	S[188]	2805	257	849	S[238]	2055	257	899	S[288]	1305	257
800	S[189]	2790	127	850	S[239]	2040	127	900	S[289]	1290	127

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
901	S[290]	1275	257	951	S[340]	525	257	1001	S[383]	-345	257
902	S[291]	1260	127	952	S[341]	510	127	1002	S[384]	-360	127
903	S[292]	1245	257	953	S[342]	495	257	1003	S[385]	-375	257
904	S[293]	1230	127	954	S[343]	480	127	1004	S[386]	-390	127
905	S[294]	1215	257	955	S[344]	465	257	1005	S[387]	-405	257
906	S[295]	1200	127	956	S[345]	450	127	1006	S[388]	-420	127
907	S[296]	1185	257	957	S[346]	435	257	1007	S[389]	-435	257
908	S[297]	1170	127	958	S[347]	420	127	1008	S[390]	-450	127
909	S[298]	1155	257	959	S[348]	405	257	1009	S[391]	-465	257
910	S[299]	1140	127	960	S[349]	390	127	1010	S[392]	-480	127
911	S[300]	1125	257	961	S[350]	375	257	1011	S[393]	-495	257
912	S[301]	1110	127	962	S[351]	360	127	1012	S[394]	-510	127
913	S[302]	1095	257	963	S[352]	345	257	1013	S[395]	-525	257
914	S[303]	1080	127	964	S[353]	330	127	1014	S[396]	-540	127
915	S[304]	1065	257	965	S[354]	315	257	1015	S[397]	-555	257
916	S[305]	1050	127	966	S[355]	300	127	1016	S[398]	-570	127
917	S[306]	1035	257	967	S[356]	285	257	1017	S[399]	-585	257
918	S[307]	1020	127	968	S[357]	270	127	1018	S[400]	-600	127
919	S[308]	1005	257	969	S[358]	255	257	1019	S[401]	-615	257
920	S[309]	990	127	970	S[359]	240	127	1020	S[402]	-630	127
921	S[310]	975	257	971	S[360]	225	257	1021	S[403]	-645	257
922	S[311]	960	127	972	DUMMY	150	127	1022	S[404]	-660	127
923	S[312]	945	257	973	DUMMY	135	257	1023	S[405]	-675	257
924	S[313]	930	127	974	DUMMY	120	127	1024	S[406]	-690	127
925	S[314]	915	257	975	DUMMY	105	257	1025	S[407]	-705	257
926	S[315]	900	127	976	DUMMY	90	127	1026	S[408]	-720	127
927	S[316]	885	257	977	DUMMY	75	257	1027	S[409]	-735	257
928	S[317]	870	127	978	DUMMY	60	127	1028	S[410]	-750	127
929	S[318]	855	257	979	S[361]	-15	257	1029	S[411]	-765	257
930	S[319]	840	127	980	S[362]	-30	127	1030	S[412]	-780	127
931	S[320]	825	257	981	S[363]	-45	257	1031	S[413]	-795	257
932	S[321]	810	127	982	S[364]	-60	127	1032	S[414]	-810	127
933	S[322]	795	257	983	S[365]	-75	257	1033	S[415]	-825	257
934	S[323]	780	127	984	S[366]	-90	127	1034	S[416]	-840	127
935	S[324]	765	257	985	S[367]	-105	257	1035	S[417]	-855	257
936	S[325]	750	127	986	S[368]	-120	127	1036	S[418]	-870	127
937	S[326]	735	257	987	S[369]	-135	257	1037	S[419]	-885	257
938	S[327]	720	127	988	S[370]	-150	127	1038	S[420]	-900	127
939	S[328]	705	257	989	S[371]	-165	257	1039	S[421]	-915	257
940	S[329]	690	127	990	S[372]	-180	127	1040	S[422]	-930	127
941	S[330]	675	257	991	S[373]	-195	257	1041	S[423]	-945	257
942	S[331]	660	127	992	S[374]	-210	127	1042	S[424]	-960	127
943	S[332]	645	257	993	S[375]	-225	257	1043	S[425]	-975	257
944	S[333]	630	127	994	S[376]	-240	127	1044	S[426]	-990	127
945	S[334]	615	257	995	S[377]	-255	257	1045	S[427]	-1005	257
946	S[335]	600	127	996	S[378]	-270	127	1046	S[428]	-1020	127
947	S[336]	585	257	997	S[379]	-285	257	1047	S[429]	-1035	257
948	S[337]	570	127	998	S[380]	-300	127	1048	S[430]	-1050	127
949	S[338]	555	257	999	S[381]	-315	257	1049	S[431]	-1065	257
950	S[339]	540	127	1000	S[382]	-330	127	1050	S[432]	-1080	127

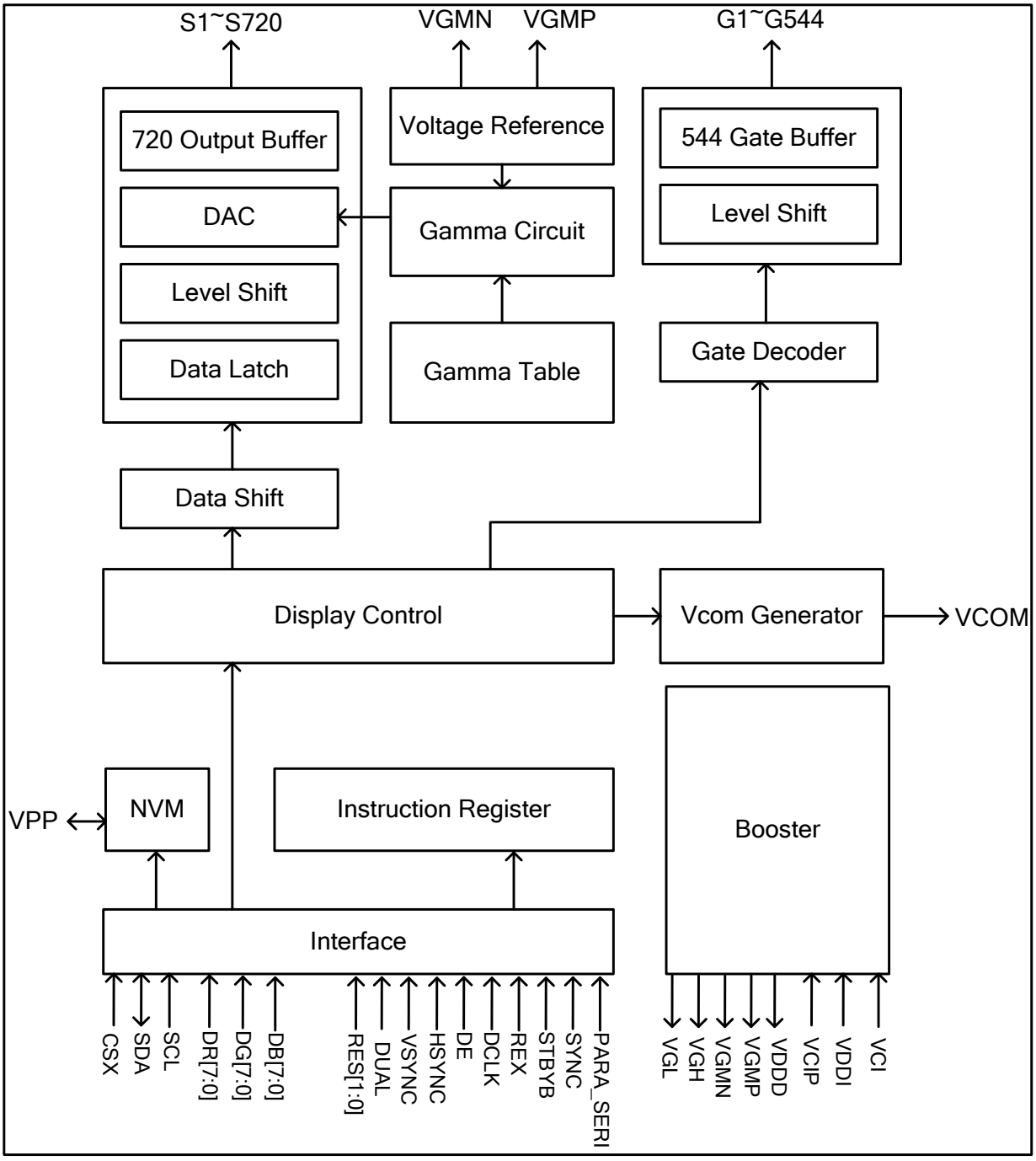
Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
1051	S[433]	-1095	257	1101	S[483]	-1845	257	1151	S[533]	-2595	257
1052	S[434]	-1110	127	1102	S[484]	-1860	127	1152	S[534]	-2610	127
1053	S[435]	-1125	257	1103	S[485]	-1875	257	1153	S[535]	-2625	257
1054	S[436]	-1140	127	1104	S[486]	-1890	127	1154	S[536]	-2640	127
1055	S[437]	-1155	257	1105	S[487]	-1905	257	1155	S[537]	-2655	257
1056	S[438]	-1170	127	1106	S[488]	-1920	127	1156	S[538]	-2670	127
1057	S[439]	-1185	257	1107	S[489]	-1935	257	1157	S[539]	-2685	257
1058	S[440]	-1200	127	1108	S[490]	-1950	127	1158	S[540]	-2700	127
1059	S[441]	-1215	257	1109	S[491]	-1965	257	1159	S[541]	-2715	257
1060	S[442]	-1230	127	1110	S[492]	-1980	127	1160	S[542]	-2730	127
1061	S[443]	-1245	257	1111	S[493]	-1995	257	1161	S[543]	-2745	257
1062	S[444]	-1260	127	1112	S[494]	-2010	127	1162	S[544]	-2760	127
1063	S[445]	-1275	257	1113	S[495]	-2025	257	1163	S[545]	-2775	257
1064	S[446]	-1290	127	1114	S[496]	-2040	127	1164	S[546]	-2790	127
1065	S[447]	-1305	257	1115	S[497]	-2055	257	1165	S[547]	-2805	257
1066	S[448]	-1320	127	1116	S[498]	-2070	127	1166	S[548]	-2820	127
1067	S[449]	-1335	257	1117	S[499]	-2085	257	1167	S[549]	-2835	257
1068	S[450]	-1350	127	1118	S[500]	-2100	127	1168	S[550]	-2850	127
1069	S[451]	-1365	257	1119	S[501]	-2115	257	1169	S[551]	-2865	257
1070	S[452]	-1380	127	1120	S[502]	-2130	127	1170	S[552]	-2880	127
1071	S[453]	-1395	257	1121	S[503]	-2145	257	1171	S[553]	-2895	257
1072	S[454]	-1410	127	1122	S[504]	-2160	127	1172	S[554]	-2910	127
1073	S[455]	-1425	257	1123	S[505]	-2175	257	1173	S[555]	-2925	257
1074	S[456]	-1440	127	1124	S[506]	-2190	127	1174	S[556]	-2940	127
1075	S[457]	-1455	257	1125	S[507]	-2205	257	1175	S[557]	-2955	257
1076	S[458]	-1470	127	1126	S[508]	-2220	127	1176	S[558]	-2970	127
1077	S[459]	-1485	257	1127	S[509]	-2235	257	1177	S[559]	-2985	257
1078	S[460]	-1500	127	1128	S[510]	-2250	127	1178	S[560]	-3000	127
1079	S[461]	-1515	257	1129	S[511]	-2265	257	1179	S[561]	-3015	257
1080	S[462]	-1530	127	1130	S[512]	-2280	127	1180	S[562]	-3030	127
1081	S[463]	-1545	257	1131	S[513]	-2295	257	1181	S[563]	-3045	257
1082	S[464]	-1560	127	1132	S[514]	-2310	127	1182	S[564]	-3060	127
1083	S[465]	-1575	257	1133	S[515]	-2325	257	1183	S[565]	-3075	257
1084	S[466]	-1590	127	1134	S[516]	-2340	127	1184	S[566]	-3090	127
1085	S[467]	-1605	257	1135	S[517]	-2355	257	1185	S[567]	-3105	257
1086	S[468]	-1620	127	1136	S[518]	-2370	127	1186	S[568]	-3120	127
1087	S[469]	-1635	257	1137	S[519]	-2385	257	1187	S[569]	-3135	257
1088	S[470]	-1650	127	1138	S[520]	-2400	127	1188	S[570]	-3150	127
1089	S[471]	-1665	257	1139	S[521]	-2415	257	1189	S[571]	-3165	257
1090	S[472]	-1680	127	1140	S[522]	-2430	127	1190	S[572]	-3180	127
1091	S[473]	-1695	257	1141	S[523]	-2445	257	1191	S[573]	-3195	257
1092	S[474]	-1710	127	1142	S[524]	-2460	127	1192	S[574]	-3210	127
1093	S[475]	-1725	257	1143	S[525]	-2475	257	1193	S[575]	-3225	257
1094	S[476]	-1740	127	1144	S[526]	-2490	127	1194	S[576]	-3240	127
1095	S[477]	-1755	257	1145	S[527]	-2505	257	1195	S[577]	-3255	257
1096	S[478]	-1770	127	1146	S[528]	-2520	127	1196	S[578]	-3270	127
1097	S[479]	-1785	257	1147	S[529]	-2535	257	1197	S[579]	-3285	257
1098	S[480]	-1800	127	1148	S[530]	-2550	127	1198	S[580]	-3300	127
1099	S[481]	-1815	257	1149	S[531]	-2565	257	1199	S[581]	-3315	257
1100	S[482]	-1830	127	1150	S[532]	-2580	127	1200	S[582]	-3330	127

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
1201	S[583]	-3345	257	1251	S[633]	-4095	257	1301	S[683]	-4845	257
1202	S[584]	-3360	127	1252	S[634]	-4110	127	1302	S[684]	-4860	127
1203	S[585]	-3375	257	1253	S[635]	-4125	257	1303	S[685]	-4875	257
1204	S[586]	-3390	127	1254	S[636]	-4140	127	1304	S[686]	-4890	127
1205	S[587]	-3405	257	1255	S[637]	-4155	257	1305	S[687]	-4905	257
1206	S[588]	-3420	127	1256	S[638]	-4170	127	1306	S[688]	-4920	127
1207	S[589]	-3435	257	1257	S[639]	-4185	257	1307	S[689]	-4935	257
1208	S[590]	-3450	127	1258	S[640]	-4200	127	1308	S[690]	-4950	127
1209	S[591]	-3465	257	1259	S[641]	-4215	257	1309	S[691]	-4965	257
1210	S[592]	-3480	127	1260	S[642]	-4230	127	1310	S[692]	-4980	127
1211	S[593]	-3495	257	1261	S[643]	-4245	257	1311	S[693]	-4995	257
1212	S[594]	-3510	127	1262	S[644]	-4260	127	1312	S[694]	-5010	127
1213	S[595]	-3525	257	1263	S[645]	-4275	257	1313	S[695]	-5025	257
1214	S[596]	-3540	127	1264	S[646]	-4290	127	1314	S[696]	-5040	127
1215	S[597]	-3555	257	1265	S[647]	-4305	257	1315	S[697]	-5055	257
1216	S[598]	-3570	127	1266	S[648]	-4320	127	1316	S[698]	-5070	127
1217	S[599]	-3585	257	1267	S[649]	-4335	257	1317	S[699]	-5085	257
1218	S[600]	-3600	127	1268	S[650]	-4350	127	1318	S[700]	-5100	127
1219	S[601]	-3615	257	1269	S[651]	-4365	257	1319	S[701]	-5115	257
1220	S[602]	-3630	127	1270	S[652]	-4380	127	1320	S[702]	-5130	127
1221	S[603]	-3645	257	1271	S[653]	-4395	257	1321	S[703]	-5145	257
1222	S[604]	-3660	127	1272	S[654]	-4410	127	1322	S[704]	-5160	127
1223	S[605]	-3675	257	1273	S[655]	-4425	257	1323	S[705]	-5175	257
1224	S[606]	-3690	127	1274	S[656]	-4440	127	1324	S[706]	-5190	127
1225	S[607]	-3705	257	1275	S[657]	-4455	257	1325	S[707]	-5205	257
1226	S[608]	-3720	127	1276	S[658]	-4470	127	1326	S[708]	-5220	127
1227	S[609]	-3735	257	1277	S[659]	-4485	257	1327	S[709]	-5235	257
1228	S[610]	-3750	127	1278	S[660]	-4500	127	1328	S[710]	-5250	127
1229	S[611]	-3765	257	1279	S[661]	-4515	257	1329	S[711]	-5265	257
1230	S[612]	-3780	127	1280	S[662]	-4530	127	1330	S[712]	-5280	127
1231	S[613]	-3795	257	1281	S[663]	-4545	257	1331	S[713]	-5295	257
1232	S[614]	-3810	127	1282	S[664]	-4560	127	1332	S[714]	-5310	127
1233	S[615]	-3825	257	1283	S[665]	-4575	257	1333	S[715]	-5325	257
1234	S[616]	-3840	127	1284	S[666]	-4590	127	1334	S[716]	-5340	127
1235	S[617]	-3855	257	1285	S[667]	-4605	257	1335	S[717]	-5355	257
1236	S[618]	-3870	127	1286	S[668]	-4620	127	1336	S[718]	-5370	127
1237	S[619]	-3885	257	1287	S[669]	-4635	257	1337	S[719]	-5385	257
1238	S[620]	-3900	127	1288	S[670]	-4650	127	1338	S[720]	-5400	127
1239	S[621]	-3915	257	1289	S[671]	-4665	257	1339	VSSA	-5475	257
1240	S[622]	-3930	127	1290	S[672]	-4680	127	1340	VSSA	-5490	127
1241	S[623]	-3945	257	1291	S[673]	-4695	257	1341	VSSA	-5505	257
1242	S[624]	-3960	127	1292	S[674]	-4710	127	1342	VSSA	-5520	127
1243	S[625]	-3975	257	1293	S[675]	-4725	257	1343	VSSA	-5535	257
1244	S[626]	-3990	127	1294	S[676]	-4740	127	1344	VSSA	-5550	127
1245	S[627]	-4005	257	1295	S[677]	-4755	257	1345	VSSA	-5565	257
1246	S[628]	-4020	127	1296	S[678]	-4770	127	1346	VSSA	-5580	127
1247	S[629]	-4035	257	1297	S[679]	-4785	257	1347	VSSA	-5595	257
1248	S[630]	-4050	127	1298	S[680]	-4800	127	1348	VSSA	-5610	127
1249	S[631]	-4065	257	1299	S[681]	-4815	257	1349	DUMMY	-5685	257
1250	S[632]	-4080	127	1300	S[682]	-4830	127	1350	DUMMY	-5700	127

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
1351	DUMMY	-5715	257	1401	G[451]	-6525	257	1451	G[351]	-7275	257
1352	DUMMY	-5730	127	1402	G[449]	-6540	127	1452	G[349]	-7290	127
1353	DUMMY	-5745	257	1403	G[447]	-6555	257	1453	G[347]	-7305	257
1354	DUMMY	-5760	127	1404	G[445]	-6570	127	1454	G[345]	-7320	127
1355	G[543]	-5835	257	1405	G[443]	-6585	257	1455	G[343]	-7335	257
1356	G[541]	-5850	127	1406	G[441]	-6600	127	1456	G[341]	-7350	127
1357	G[539]	-5865	257	1407	G[439]	-6615	257	1457	G[339]	-7365	257
1358	G[537]	-5880	127	1408	G[437]	-6630	127	1458	G[337]	-7380	127
1359	G[535]	-5895	257	1409	G[435]	-6645	257	1459	G[335]	-7395	257
1360	G[533]	-5910	127	1410	G[433]	-6660	127	1460	G[333]	-7410	127
1361	G[531]	-5925	257	1411	G[431]	-6675	257	1461	G[331]	-7425	257
1362	G[529]	-5940	127	1412	G[429]	-6690	127	1462	G[329]	-7440	127
1363	G[527]	-5955	257	1413	G[427]	-6705	257	1463	G[327]	-7455	257
1364	G[525]	-5970	127	1414	G[425]	-6720	127	1464	G[325]	-7470	127
1365	G[523]	-5985	257	1415	G[423]	-6735	257	1465	G[323]	-7485	257
1366	G[521]	-6000	127	1416	G[421]	-6750	127	1466	G[321]	-7500	127
1367	G[519]	-6015	257	1417	G[419]	-6765	257	1467	G[319]	-7515	257
1368	G[517]	-6030	127	1418	G[417]	-6780	127	1468	G[317]	-7530	127
1369	G[515]	-6045	257	1419	G[415]	-6795	257	1469	G[315]	-7545	257
1370	G[513]	-6060	127	1420	G[413]	-6810	127	1470	G[313]	-7560	127
1371	G[511]	-6075	257	1421	G[411]	-6825	257	1471	G[311]	-7575	257
1372	G[509]	-6090	127	1422	G[409]	-6840	127	1472	G[309]	-7590	127
1373	G[507]	-6105	257	1423	G[407]	-6855	257	1473	G[307]	-7605	257
1374	G[505]	-6120	127	1424	G[405]	-6870	127	1474	G[305]	-7620	127
1375	G[503]	-6135	257	1425	G[403]	-6885	257	1475	G[303]	-7635	257
1376	G[501]	-6150	127	1426	G[401]	-6900	127	1476	G[301]	-7650	127
1377	G[499]	-6165	257	1427	G[399]	-6915	257	1477	G[299]	-7665	257
1378	G[497]	-6180	127	1428	G[397]	-6930	127	1478	G[297]	-7680	127
1379	G[495]	-6195	257	1429	G[395]	-6945	257	1479	G[295]	-7695	257
1380	G[493]	-6210	127	1430	G[393]	-6960	127	1480	G[293]	-7710	127
1381	G[491]	-6225	257	1431	G[391]	-6975	257	1481	G[291]	-7725	257
1382	G[489]	-6240	127	1432	G[389]	-6990	127	1482	G[289]	-7740	127
1383	G[487]	-6255	257	1433	G[387]	-7005	257	1483	G[287]	-7755	257
1384	G[485]	-6270	127	1434	G[385]	-7020	127	1484	G[285]	-7770	127
1385	G[483]	-6285	257	1435	G[383]	-7035	257	1485	G[283]	-7785	257
1386	G[481]	-6300	127	1436	G[381]	-7050	127	1486	G[281]	-7800	127
1387	G[479]	-6315	257	1437	G[379]	-7065	257	1487	G[279]	-7815	257
1388	G[477]	-6330	127	1438	G[377]	-7080	127	1488	G[277]	-7830	127
1389	G[475]	-6345	257	1439	G[375]	-7095	257	1489	G[275]	-7845	257
1390	G[473]	-6360	127	1440	G[373]	-7110	127	1490	G[273]	-7860	127
1391	G[471]	-6375	257	1441	G[371]	-7125	257	1491	G[271]	-7875	257
1392	G[469]	-6390	127	1442	G[369]	-7140	127	1492	G[269]	-7890	127
1393	G[467]	-6405	257	1443	G[367]	-7155	257	1493	G[267]	-7905	257
1394	G[465]	-6420	127	1444	G[365]	-7170	127	1494	G[265]	-7920	127
1395	G[463]	-6435	257	1445	G[363]	-7185	257	1495	G[263]	-7935	257
1396	G[461]	-6450	127	1446	G[361]	-7200	127	1496	G[261]	-7950	127
1397	G[459]	-6465	257	1447	G[359]	-7215	257	1497	G[259]	-7965	257
1398	G[457]	-6480	127	1448	G[357]	-7230	127	1498	G[257]	-7980	127
1399	G[455]	-6495	257	1449	G[355]	-7245	257	1499	G[255]	-7995	257
1400	G[453]	-6510	127	1450	G[353]	-7260	127	1500	G[253]	-8010	127

Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY	Pad No.	Designation	CX	CY
1501	G[251]	-8025	257	1551	G[151]	-8775	257	1601	G[51]	-9525	257
1502	G[249]	-8040	127	1552	G[149]	-8790	127	1602	G[49]	-9540	127
1503	G[247]	-8055	257	1553	G[147]	-8805	257	1603	G[47]	-9555	257
1504	G[245]	-8070	127	1554	G[145]	-8820	127	1604	G[45]	-9570	127
1505	G[243]	-8085	257	1555	G[143]	-8835	257	1605	G[43]	-9585	257
1506	G[241]	-8100	127	1556	G[141]	-8850	127	1606	G[41]	-9600	127
1507	G[239]	-8115	257	1557	G[139]	-8865	257	1607	G[39]	-9615	257
1508	G[237]	-8130	127	1558	G[137]	-8880	127	1608	G[37]	-9630	127
1509	G[235]	-8145	257	1559	G[135]	-8895	257	1609	G[35]	-9645	257
1510	G[233]	-8160	127	1560	G[133]	-8910	127	1610	G[33]	-9660	127
1511	G[231]	-8175	257	1561	G[131]	-8925	257	1611	G[31]	-9675	257
1512	G[229]	-8190	127	1562	G[129]	-8940	127	1612	G[29]	-9690	127
1513	G[227]	-8205	257	1563	G[127]	-8955	257	1613	G[27]	-9705	257
1514	G[225]	-8220	127	1564	G[125]	-8970	127	1614	G[25]	-9720	127
1515	G[223]	-8235	257	1565	G[123]	-8985	257	1615	G[23]	-9735	257
1516	G[221]	-8250	127	1566	G[121]	-9000	127	1616	G[21]	-9750	127
1517	G[219]	-8265	257	1567	G[119]	-9015	257	1617	G[19]	-9765	257
1518	G[217]	-8280	127	1568	G[117]	-9030	127	1618	G[17]	-9780	127
1519	G[215]	-8295	257	1569	G[115]	-9045	257	1619	G[15]	-9795	257
1520	G[213]	-8310	127	1570	G[113]	-9060	127	1620	G[13]	-9810	127
1521	G[211]	-8325	257	1571	G[111]	-9075	257	1621	G[11]	-9825	257
1522	G[209]	-8340	127	1572	G[109]	-9090	127	1622	G[9]	-9840	127
1523	G[207]	-8355	257	1573	G[107]	-9105	257	1623	G[7]	-9855	257
1524	G[205]	-8370	127	1574	G[105]	-9120	127	1624	G[5]	-9870	127
1525	G[203]	-8385	257	1575	G[103]	-9135	257	1625	G[3]	-9885	257
1526	G[201]	-8400	127	1576	G[101]	-9150	127	1626	G[1]	-9900	127
1527	G[199]	-8415	257	1577	G[99]	-9165	257	1627	VSSA	-9930	257
1528	G[197]	-8430	127	1578	G[97]	-9180	127	1628	VSSA	-9945	127
1529	G[195]	-8445	257	1579	G[95]	-9195	257				
1530	G[193]	-8460	127	1580	G[93]	-9210	127				
1531	G[191]	-8475	257	1581	G[91]	-9225	257				
1532	G[189]	-8490	127	1582	G[89]	-9240	127				
1533	G[187]	-8505	257	1583	G[87]	-9255	257				
1534	G[185]	-8520	127	1584	G[85]	-9270	127				
1535	G[183]	-8535	257	1585	G[83]	-9285	257				
1536	G[181]	-8550	127	1586	G[81]	-9300	127				
1537	G[179]	-8565	257	1587	G[79]	-9315	257				
1538	G[177]	-8580	127	1588	G[77]	-9330	127				
1539	G[175]	-8595	257	1589	G[75]	-9345	257				
1540	G[173]	-8610	127	1590	G[73]	-9360	127				
1541	G[171]	-8625	257	1591	G[71]	-9375	257				
1542	G[169]	-8640	127	1592	G[69]	-9390	127				
1543	G[167]	-8655	257	1593	G[67]	-9405	257				
1544	G[165]	-8670	127	1594	G[65]	-9420	127				
1545	G[163]	-8685	257	1595	G[63]	-9435	257				
1546	G[161]	-8700	127	1596	G[61]	-9450	127				
1547	G[159]	-8715	257	1597	G[59]	-9465	257				
1548	G[157]	-8730	127	1598	G[57]	-9480	127				
1549	G[155]	-8745	257	1599	G[55]	-9495	257				
1550	G[153]	-8760	127	1600	G[53]	-9510	127				

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 Pin Function

Pin Name	I/O	Descriptions
CSX	I (VDDI)	Serial communication chip select, Internal pull high.
SDA	I/O (VDDI)	Serial communication data input and output ,Internal pull low.
SCL	I (VDDI)	Serial communication clock input, Internal pull low.
PARA_SERI	I (VDDI)	PARA_SERI=”Low”, Serial 8-bit RGB input through DG0~DG7. PARA_SERI=”High”, Parallel 24-bit RGB input through DR0~ DR7, DB0~DB7, DG0~DG7.
DR7~DR0	I (VDDI)	8-bit digital Red data input.
DG7~DG0	I (VDDI)	8-bit digital Green data input
DB7~DB0	I (VDDI)	8-bit digital Blue data input.
DCLK	I (VDDI)	Clock signal; latching data at the falling edge.
HSYNC	I (VDDI)	Horizontal sync signal; negative polarity. When not used, user should connect it to “Low”.
VSYNC	I (VDDI)	Vertical sync signal; negative polarity. When not used, user should connect it to “Low”.
DE	I (VDDI)	Data input enable. Active High to enable the data input. When not used, user should connect it to “Low”.
SYNC	I (VDDI)	No Function. User should connect it to “Low”.
HDIR	I (VDDI)	Horizontal scan direction control. HDIR = “High”: Shift from left to right. HDIR = “Low” : Shift from right to left. When not used, user should connect it to “High”. (Please refer to the register setting : HDIR).
VDIR	I (VDDI)	Vertical scan direction control. VDIR = “High”: Shift from up to down. VDIR = “Low”: Shift from down to up. When not used, user should connect it to “High”.
VDPOL	I (VDDI)	VSYNC polarity control. VDPOL=”High”, negative polarity. VDPOL=Low, positive polarity. When not used, user should connect it to “High”. (Please refer to the register setting : VDPOL).
HDPOL	I (VDDI)	HSYNC polarity control. HDPOL=”High”, negative polarity. HDPOL=”Low”, positive polarity. When not used, user should connect it to “High”. (Please refer to the register setting : VDPOL).
DCLKPOL	I (VDDI)	DCLK polarity control. DCLKPOL=”High”, negative polarity. DCLKPOL=”Low”, positive polarity. (Please refer to the register setting : DCLKPOL).

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>SBGR</td><td>I
(VDDI)</td><td>Data R[7:0] & B[7:0] exchanged internally.
SBGR=”1” R[7:0]→B[7:0] B[7:0]→R[7:0].
SBGR=”0” R[7:0]→R[7:0] B[7:0]→B[7:0].</td></tr>
<tr><td>RESX</td><td>I
(VDDI)</td><td>Global reset. Active low, Internal pull high.</td></tr>
<tr><td>STBYB</td><td>I
(VDDI)</td><td>Display control / standby mode selection. Internal pull low.
STBYB = “Low” : Standby.
STBYB = “High” : Normal display.</td></tr>
<tr><td>EXTC</td><td>I
(VDDI)</td><td>No Function. User should connect it to “Low”.</td></tr>
<tr><td>DUAL</td><td>I
(VDDI)</td><td>Dual gate / Single gate control. Internal pull high.
DUAL = “High”: Dual gate
DUAL = “Low”: Single gate
When not used, User should leave it open or connect it to “High”.</td></tr>
<tr><td>RES[1:0]</td><td>I
(VDDI)</td><td>Resolution control. Internal pull high.
When not used, User should leave it open or connect it to “High”.
<table>
<tr><th>DUAL</th><th>RES[1:0]</th><th>Description</th><th>Enable Channel</th></tr>
<tr><td rowspan="4">Low</td><td>00</td><td>Single gate,
240RGB*240.</td><td>S[1]~S[720]
G[1]~G[240]</td></tr>
<tr><td>01</td><td>Single gate,
240RGB*320.</td><td>S[1]~S[720]
G[1]~G[320]</td></tr>
<tr><td>10</td><td>Prohibit.</td><td>-</td></tr>
<tr><td>11</td><td>Prohibit.</td><td>-</td></tr>
<tr><td rowspan="4">High</td><td>00</td><td>Dual gate,
240RGB*240</td><td>S[1]~S[180]&S[541]~S[720]
G[1]~G[480]</td></tr>
<tr><td>01</td><td>Prohibit.</td><td>-</td></tr>
<tr><td>10</td><td>Dual gate,
320RGB*240</td><td>S[1]~S[240]&S[481]~S[720]
G[1]~G[480]</td></tr>
<tr><td>11</td><td>Dual gate,
480RGB*272</td><td>S[1]~S[720]
G[1]~G[544]</td></tr>
</table></td></tr>
<tr><td colspan="3">Source/Gate Drive</td></tr>
<tr><td>S[1]~S[720]</td><td>O</td><td>Source driver output signals</td></tr>
<tr><td>G[1]~G[544]</td><td>O</td><td>Gate driver output signals.</td></tr>
<tr><td colspan="3">VCOM Generator</td></tr>
<tr><td>VCOM</td><td>O</td><td>A power supply for the TFT-LCD common electrode. Frame polarity output for VCOM.</td></tr>
<tr><td colspan="3">Power Supply</td></tr>
<tr><td>VCI</td><td>P</td><td>Power supply for digital circuit</td></tr>
<tr><td>VDDI</td><td>P</td><td>Power supply for digital interface I/O pins.</td></tr>
<tr><td>VCIP</td><td>P</td><td>Power supply for charge pump circuit</td></tr>
<tr><td>VSSD</td><td>P</td><td>Ground pin for digital circuit.</td></tr>
<tr><td>VSSA</td><td>P</td><td>Ground pin for analog circuit.</td></tr>
<tr><td>VSSP</td><td>P</td><td>Ground pin for charge pump circuit.</td></tr>
<tr><td>VPP</td><td>P</td><td>Power input pin for NVM. When writing NVM, it needs external power supply voltage (10.5V). If not used, let this pin open.</td></tr>
<tr><td>VSP_AC</td><td>C</td><td>A power supply pin for positive source OP-AMP driver. Connect a capacitor for stabilization.</td></tr>
<tr><td>VSP_DC</td><td>PO</td><td>A power supply pin for generating positive Gamma and VGMP reference</td></tr>
</table>

Pin Name	I/O	Descriptions
		voltage.
VSN_AC	C	A power supply pin for negative source OP-AMP driver. Connect a capacitor for stabilization.
VSN_DC	C	A power supply pin for generating negative Gamma and VGMN reference voltage. Connect a capacitor for stabilization.
VDDD	PO	Monitoring pin of internal digital power.
VGH	C	Positive power supply for gate driver output. Connect a capacitor for stabilization. (Default NC).
VGL	C	Negative power supply for gate driver output. Connect a capacitor for stabilization. (Default NC).
VGMP	PO	A reference positive voltage of grayscale voltage generator.
VGMN	PO	A reference negative voltage of grayscale voltage generator.
VGSP	PO	Internal VCOM offset monitor pin for feed-through voltage.
Others		
TEST_OUT[13:0]	T	Test pins for internal testing only. User should leave it open.
TEST_IN[3:0]	T	Test pins for internal testing only. Internal pull low. User should leave it open or connect it to “Low”.
TEST_ANA[12:1]	T	Test pins for internal testing only. User should leave it open.
TEST_X[4:3]	T	Test pins for internal testing only. Internal pull low. User should leave it open or connect it to “Low”.
TEST_X[5]	T	Test pins for internal testing only. Internal pull high. User should leave it open or connect it to “High”.
TEST_X[6]	T	Test pins for internal testing only. User should leave it open.
DUMMY	D	Dummy pin. User should leave it open.

Note.. I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, T: test pin, C: capacitor pin

If unused pin don’t floating, the pin fix to VDDI or VSSD

Hardeare pins option mapping software register option table

HDIR			*VDIR*		
PIN_HDIR	*REG_HDIR*	*HDIR*	*PIN_VDIR*	*REG_VDIR*	*VDIR*
0	*0*	*1*	*0*	*0*	*1*
0	*1*	*0*	*0*	*1*	*0*
1	*0*	*0*	*1*	*0*	*0*
1	*1*	*1*	*1*	*1*	*1*

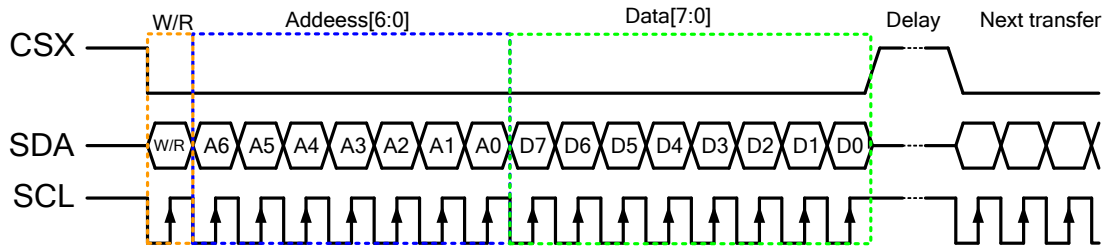
VDPOL			*HDPOL*		
PIN_VDPOL	*REG_VDPOL*	*VDPOL*	*PIN_HDPOL*	*REG_HDPOL*	*HDPOL*
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	1	1	1

DCLKPOL			*DUAL*		
Pin_DCLKPOL	*REG_DCLKPOL*	*DCLKPOL*	*PIN_DUAL*	*REG_DUAL*	*DUAL*
0	*0*	*1*	*0*	*0*	*1*
0	*1*	*0*	*0*	*1*	*0*
1	*0*	*0*	*1*	*0*	*0*
1	*1*	*1*	*1*	*1*	*1*

RES[0]			*RES[1]*		
PIN_RES[0]	*REG_RES[0]*	*RES[0]*	*PIN_RES[1]*	*REG_RES[1]*	*RES[1]*
0	*0*	*1*	*0*	*0*	*1*
0	*1*	*0*	*0*	*1*	*0*
1	*0*	*0*	*1*	*0*	*0*
1	*1*	*1*	*1*	*1*	*1*

STBYB			*RBSWAP*		
PIN_STBYB	*REG_STBYB*	*STBYB*	*PIN_RBSWAP*	*REG_RBSWAP*	*RBSWAP*
0	*0*	*0*	*0*	*0*	*0*
0	*1*	*1*	*0*	*1*	*1*
1	*0*	*1*	*1*	*0*	*1*
1	*1*	*0*	*1*	*1*	*0*

7. 3-WIRE SERIAL INTERFACE



Bit	Description
W/R	W/R control bit. “0” for Write; “1” for Read
A[6:0]	Register Address [6:0].
D[7:0]	Data for the W/R operation to the address indicated by Address phase

a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CSX and is completed at the next rising edge of CSX.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CSX is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CSX is low, the previous 16 bits of transferred data before the rising edge of CSX pulse are valid data.

f. Serial block operates with the SCL clock.

g. Serial data can be accepted in the power save mode.

h. After power on reset or RESX reset, it is required 100ms delay to begin SPI communication.

8. REGISTER LIST

8.1 Register Summary

NO	R/W	Address							Parameter Data								Default
		A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R00H	R/W	0	0	0	0	0	0	0	0	VDIR	HDIR	0	RGBIF[1:0]		0	GM_SWAP	64H
	1/0																
R01H	R/W	0	0	0	0	0	0	1	0	0	0	0	GRB	0	0	STBYB	08H
	1/0																
R02H	R/W	0	0	0	0	0	1	0	CONTRAST[7:0]								40H
	1/0																
R03H	R/W	0	0	0	0	0	1	1	0	SUB_CONTRAST_R[6:0]							40H
	1/0																
R04H	R/W	0	0	0	0	1	0	0	0	SUB_CONTRAST_B[6:0]							40H
	1/0																
R05H	R/W	0	0	0	0	1	0	1	BRIGHTNESS[7:0]								40H
	1/0																
R06H	R/W	0	0	0	0	1	1	0	0	SUB_BRIGHTNESS_R[6:0]							40H
	1/0																
R07H	R/W	0	0	0	0	1	1	1	0	SUB_BRIGHTNESS_B[6:0]							40H
	1/0																
R08H	R/W	0	0	0	1	0	0	0	H_BLANKING[7:0]								2BH
	1/0																
R09H	R/W	0	0	0	1	0	0	1	VDPOL	HDPOL	V_BLANKING[5:0]						CCH
	1/0																
R0AH	R/W	0	0	0	1	0	1	0	DEPOL	DCLKPOL	1	1	REV	NBW	INVSEL[1:0]		77H
	1/0																
R0BH	R/W	0	0	0	1	0	1	1	0	0	0	0	0	DUAL	RES[1:0]		07H
	1/0																
R0DH	R/W	0	0	0	1	1	0	1	0	0	0	1	RBSWAP	0	0	0	10H
	1/0																
R0EH	R/W	0	0	0	1	1	1	0	0	0	0	0	0	0	1	OTP_NO_LOAD	02H
	1/0																
R10H	R/W	0	0	1	0	0	0	0	0	VP255[2:0]			0	VP0[2:0]			50H
	1/0																
R11H	R/W	0	0	1	0	0	0	1	0	0	0	VP3[4:0]					0BH
	1/0																
R12H	R/W	0	0	1	0	0	1	0	0	0	0	VP7[4:0]					16H
	1/0																
R13H	R/W	0	0	1	0	0	1	1	0	0	0	VP11[4:0]					07H
	1/0																
R14H	R/W	0	0	1	0	1	0	0	0	0	0	VP15[4:0]					08H
	1/0																
R15H	R/W	0	0	1	0	1	0	1	0	0	0	VP27[4:0]					0AH
	1/0																
R16H	R/W	0	0	1	0	1	1	0	0	0	0	VP51[4:0]					13H
	1/0																
R17H	R/W	0	0	1	0	1	1	1	VP111[3:0]				VP79[3:0]				BBH
	1/0																
R18H	R/W	0	0	1	1	0	0	0	VP176[3:0]				VP144[3:0]				72H
	1/0																
R19H	R/W	0	0	1	1	0	0	1	0	0	0	VP204[4:0]					14H
	1/0																
R1AH	R/W	0	0	1	1	0	1	0	0	0	0	VP228[4:0]					0BH
	1/0																
R1BH	R/W	0	0	1	1	0	1	1	0	0	0	VP240[4:0]					0EH
	1/0																
R1CH	R/W	0	0	1	1	1	0	0	0	0	0	VP244[4:0]					0AH
	1/0																
R1DH	R/W	0	0	1	1	1	0	1	0	0	0	VP248[4:0]					0FH
	1/0																

NO	R/W	Address							Parameter Data								Default
		A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R1EH	R/W	0	0	1	1	1	1	0	0	0	0	VP252[4:0]					10H
	1/0																
R1FH	R/W	0	0	1	1	1	1	1	0	VN255[2:0]		0	VN0[2:0]				50H
	1/0																
R20H	R/W	0	1	0	0	0	0	0	0	0	0	VN3[4:0]					0BH
	1/0																
R21H	R/W	0	1	0	0	0	0	1	0	0	0	VN7[4:0]					16H
	1/0																
R22H	R/W	0	1	0	0	0	1	0	0	0	0	VN11[4:0]					07H
	1/0																
R23H	R/W	0	1	0	0	0	1	1	0	0	0	VN15[4:0]					06H
	1/0																
R24H	R/W	0	1	0	0	1	0	0	0	0	0	VN27[4:0]					07H
	1/0																
R25H	R/W	0	1	0	0	1	0	1	0	0	0	VN51[4:0]					0DH
	1/0																
R26H	R/W	0	1	0	0	1	1	0	VN111[3:0]				VN79[3:0]				44H
	1/0																
R27H	R/W	0	1	0	0	1	1	1	VN176[3:0]				VN144[3:0]				7CH
	1/0																
R28H	R/W	0	1	0	1	0	0	0	0	0	0	VN204[4:0]					0AH
	1/0																
R29H	R/W	0	1	0	1	0	0	1	0	0	0	VN228[4:0]					12H
	1/0																
R2AH	R/W	0	1	0	1	0	1	0	0	0	0	VN240[4:0]					0FH
	1/0																
R2BH	R/W	0	1	0	1	0	1	1	0	0	0	VN244[4:0]					0BH
	1/0																
R2CH	R/W	0	1	0	1	1	0	0	0	0	0	VN248[4:0]					0FH
	1/0																
R2DH	R/W	0	1	0	1	1	0	1	0	0	0	VN252[4:0]					10H
	1/0																
R2EH	R/W	0	1	0	1	1	1	0	SD_BIAS_SEL_H[2:0]			VSP_DC_RATIO	0	1	0	1	95H
	1/0																
R2FH	R/W	0	1	0	1	1	1	1	CP_VGH_CLP_EN	CP_VGL_CLP_EN	VSPAC_DETVCI[1:0]		0	1	1	0	F6H
	1/0																
R30H	R/W	0	1	1	0	0	0	0	VREF_VREG1_SEL[7:0]								4EH
	1/0																
R31H	R/W	0	1	1	0	0	0	1	VREF_VREG2_SEL[7:0]								61H
	1/0																
R32H	R/W	0	1	1	0	0	1	0	0	VREF_VGSP_SEL[6:0]							42H
	1/0																
R33H	R/W	0	1	1	0	0	1	1	0	VREF_VGL_SEL[2:0]			VREF_VGH_SEL[3:0]				3AH
	1/0																
R34H	R/W	0	1	1	0	1	0	0	0	VREF_VSP_AC_SEL[2:0]			0	VREF_VSP_DC_SEL[2:0]			33H
	1/0																
R35H	R/W	0	1	1	0	1	0	1	0	VREF_VSN_AC_SEL[2:0]			0	VREF_VSN_DC_SEL[2:0]			22H
	1/0																
R36H	R/W	0	1	1	0	1	1	0	0	0	0	0	VREF_VDDN_AC_SEL[1:0]		VREF_VDDN_DC_SEL[1:0]		00H
	1/0																
R3CH	R/W	0	1	1	1	1	0	0	0	0	0	0	0	0	DUAL_SEL[1:0]		00H
	1/0																
R3EH	R/W	0	1	1	1	1	1	0	0	ID[6:0]							7FH
	1/0																

NO	R/W	Address							Parameter Data								Default
		A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R40H	R/W	1	0	0	0	0	0	0	VMF_SET	VMF[6:0]							C0H
	1/0																
R45H	R	1	0	0	0	1	0	1	0	OTP2REG_GAMMA_MARK[2:0]			0	OTP2REG_RES_MARK[2:0]			--
	1																
R46H	R	1	0	0	0	1	1	0	0	OTP2REG_VCMC_MARK[2:0]			0	OTP2REG_CHIPID_MARK[2:0]			--
	1																
R48H	W	1	0	0	1	0	0	0	OTP_KEY[7:0]								--
	0																
R49H	R/W	1	0	0	1	0	0	1	0	OTP_TARGET[6:0]							40H
	1/0																
R4AH	R	1	0	0	1	0	1	0	0	0	0	0	0	0	0	OTP_TRIM_FAIL _FLAG	--
	1																

8.2 Command Table 1 Register description

Register R00H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VDIR	HDIR	-	RGBIF[1:0]		-	GM_SWAP
Default	0	1	1	0	0	1	0	0

VDIR:Vertical shift direction setting

0: Shift from bottom to top, last line=L1← L2…L543←L544=first line

1: Shift from top to bottom, first line=L1→ L2…L543→L544=last line (Default)

HDIR:Horizontal shift direction setting

0: Shift from right to left, last data=Y1← Y2…Y719←Y720=first data

1: Shift from left to right, first data=Y1→ Y2…Y719→Y720=last data (Default)

RGBIF[1:0]:RGB Interface Input Timing

00:SYNC Mode

01:DE Mode (Default)

1x:SYNC-DE Mode

GM_SWAP:Gate line and color filter mapping selection

0: Normal (Default)

1: Swap the gate line and color filter mapping

Register R01H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	GRB	-	-	STBYB
Default	0	0	0	0	1	0	0	0

GRB:Software reset

0: Reset

1: Normal operation (Default)

STBYB:Standby mode control

0: Standby, timing control, DAC, and DC/DC converter are off, and register data should be kept (Default)

1: Normal operation

Register R02H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CONTRAST[7:0]							
Default	0	1	0	0	0	0	0	0

CONTRAST[7:0]:RGB contrast level setting, the gain changes (1/64)/ bit

00h: contrast gain=0

40h: contrast gain=1 (Default)

FFh: contrast gain=3.984

Register R03H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	SUB_CONTRAST_R[6:0]						
Default	0	1	0	0	0	0	0	0

SUB_CONTRAST_R[6:0]:R sub-contrast level setting, the gain changes (1/256) / bit

00h: contrast gain=0.75

40h: contrast gain=1 (Default)

7Fh: contrast gain=1.246

Register R04H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	SUB_CONTRAST_B[6:0]						
Default	0	1	0	0	0	0	0	0

SUB_CONTRAST_B[6:0]:B sub-contrast level setting, the gain changes (1/256) / bit

00h: contrast gain=0.75

40h: contrast gain=1 (Default)

7Fh: contrast gain=1.246

Register R05H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BRIGHTNESS[7:0]							
Default	0	1	0	0	0	0	0	0

BRIGHTNESS[7:0]:RGB brightness level setting, the accuracy 1 step/ bit
00h: -64
40h: 0 (Default)
FFh: +191

Register R06H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	SUB_BRIGHTNESS_R[6:0]						
Default	0	1	0	0	0	0	0	0

SUB_BRIGHTNESS_R[6:0]:R sub-brightness level setting, the accuracy 1 step / bit

00h: -64

40h: 0 (Default)

7Fh: +63

Register R07H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	SUB_BRIGHTNESS_B[6:0]						
Default	0	1	0	0	0	0	0	0

SUB_BRIGHTNESS_B[6:0]:B sub-brightness level setting, the accuracy 1 step / bit

00h: -64

40h: 0 (Default)

7Fh: +63

Register R08H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	H_BLANKING[7:0]							
Default	0	0	1	0	1	0	1	1

H_BLANKING[7:0]:RGB interface SYNC Mode, HSYNC back porch setting (unit: DCLK)

*. H_BLANKING >=3

Register R09H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VDPOL	HDPOL	V_BLANKING[5:0]					
Default	1	1	0	0	1	1	0	0

VDPOL:VSYNC polarity setting

0: Positive polarity

1: Negative polarity (Default)

HDPOL:HSYNC polarity setting

0: Positive polarity

1: Negative polarity (Default)

V_BLANKING[5:0]:RGB interface SYNC Mode, VSYNC back porch setting (unit: HSYNC)

*.V_BLANKING>=1

Register R0AH

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	DEPOL	DCLKPOL	-	-	REV	NBW	INVSEL[1:0]	
Default	0	1	1	1	0	1	1	1

DEPOL:DE polarity control

0: Positive polarity (Default)

1: Negative polarity

DCLKPOL:DCLK polarity setting

0: Positive Polarity

1: Negative Polarity (Default)

REV:Data Invert

0: Disable (Default)

1: Enable

NBW:Normal Black/White

0: Normal Black

1: Normal White (Default)

INVSEL[1:0]:Inversion selection

Single gate

00: 1+2 dot inversion (vertical)

01: Column inversion (vertical)

10: 4 Dot inversion (vertical)

11: Dot inversion (vertical) (Default)

Dual gate

00: 1 +2 dot inversion (horizontal)

01: 2 dot inversion (horizontal)

10: 1 +2 dot inversion (horizontal)

11: 2 dot inversion (horizontal) (Default)

Register R0BH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	DUAL	RES[1:0]	
Default	0	0	0	0	0	1	1	1

DUAL:Single Gate/Dual Gate Select

0: Single Gate

1: Dual Gate (Default)

RES[1:0]:Resolution setting

00: 240RGBx240

01: 240RGBx320

10: 320RGBx240

11: 480RGBx272 (Default)

Register R0DH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	RBSWAP	-	-	-
Default	0	0	0	1	0	0	0	0

RBSWAP:R data and B data exchange

0: R data and B data no exchange (Default)

1: R data and B data exchange

Register R0EH

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	-	-	-	-	-	-	-	OTP_NO_LOAD
Default	0	0	0	0	0	0	1	0

OTP_NO_LOAD:OTP Reload Control

0: Enable OTP reload (Default)

1: Disable OTP reload

Register R10H~R2DH

Gamma Register

Register	D7	D6	D5	D4	D3	D2	D1	D0	Default
R10H	-	VP255[2:0]			-	VP0[2:0]			50H
R11H	-	-	-	VP3[4:0]					0BH
R12H	-	-	-	VP7[4:0]					16H
R13H	-	-	-	VP11[4:0]					07H
R14H	-	-	-	VP15[4:0]					08H
R15H	-	-	-	VP27[4:0]					0AH
R16H	-	-	-	VP51[4:0]					13H
R17H	VP111[3:0]				VP79[3:0]				BBH
R18H	VP176[3:0]				VP144[3:0]				72H
R19h	-	-	-	VP204[4:0]					14H
R1AH	-	-	-	VP228[4:0]					0BH
R1BH	-	-	-	VP240[4:0]					0EH
R1CH	-	-	-	VP244[4:0]					0AH
R1DH	-	-	-	VP248[4:0]					0FH
R1EH	-	-	-	VP252[4:0]					10H
R1FH	-	VN255[2:0]			-	VN0[2:0]			50H
R20H	-	-	-	VN3[4:0]					0BH
R21H	-	-	-	VN7[4:0]					16H
R22H	-	-	-	VN11[4:0]					07H
R23H	-	-	-	VN15[4:0]					06H
R24H	-	-	-	VN27[4:0]					07H
R25H	-	-	-	VN51[4:0]					0DH
R26H	VN111[3:0]				VN79[3:0]				44H
R27H	VN176[3:0]				VN144[3:0]				7CH
R28H	-	-	-	VN204[4:0]					0AH
R29H	-	-	-	VN228[4:0]					12H
R2AH	-	-	-	VN240[4:0]					0FH
R2BH	-	-	-	VN244[4:0]					0BH
R2CH	-	-	-	VN248[4:0]					0FH
R2DH	-	-	-	VN252[4:0]					10H

Parameter Data	Description	Parameter Data	Description
VP/N0	V0 Gamma selection.	VP/N144	V144 Gamma selection.
VP/N3	V3 Gamma selection.	VP/N176	V176 Gamma selection.
VP/N7	V7 Gamma selection.	VP/N204	V204 Gamma selection.
VP/N11	V11 Gamma selection.	VP/N228	V228 Gamma selection.
VP/N15	V15 Gamma selection.	VP/N240	V240 Gamma selection.
VP/N27	V27 Gamma selection.	VP/N244	V244 Gamma selection.
VP/N51	V51 Gamma selection.	VP/N248	V248 Gamma selection.
VP/N79	V79 Gamma selection.	VP/N252	V252 Gamma selection.
VP/N111	V111 Gamma selection.	VP/N255	V255 Gamma selection.

Register R2EH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SD_BIAS_SEL_H[2:0]			VSP_DC_RATIO	-	-	-	-
Default	1	0	0	1	0	1	0	1

SD_BIAS_SEL_H[2:0]:Source bias current select

000: Level (Least)

001: Level (Smaller)

010: Level (Small)

011: Level (Small to Medium)

100: Level (Medium)(Default)

101: Level (Medium to Large)

110: Level (Large to Maximum)

111: Level (Maximum)

VSP_DC_RATIO: VSP_DC ratio select

0: 2X (Default)

1: 3X

Register R2FH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CP_VGH_CLP_EN	CP_VGL_CLP_EN	VSPAC_DETVCI[1:0]		-	-	-	-
Default	1	1	1	1	0	1	1	0

CP_VGH_CLP_EN: VGH clamp function enable

0: Disable

1: Enable (Default)

CP_VGL_CLP_EN: VGL clamp function enable

0: Disable

1: Enable (Default)

VSPAC_DETVCI[1:0]: VSP_AC boost mode setting

00: 3X

01: 2X

10: Auto-switching when VCI lower than 3.0V

11: Auto-switching when VCI lower than 3.1V (Default)

Register R30H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VREF_VREG1_SEL[7:0]							
Default	0	1	0	0	1	1	1	0

VREF_VREG1_SEL[7:0]: Control signal to select VGMP

10h~8Fh: VGMP from 6.704V to 4.672V, -16mV/Step

4Eh: VGMP = 5.712V (Default)

VGMP level adjustment (Unit:V)															
VERG1[7:0]	VGMP	VERG1[7:0]	VGMP	VERG1[7:0]	VGMP	VERG1[7:0]	VGMP	VERG1[7:0]	VGMP	VERG1[7:0]	VGMP	VERG1[7:0]	VGMP	VERG1[7:0]	VGMP
10h	6.704	20h	6.448	30h	6.192	40h	5.936	50h	5.680	60h	5.424	70h	5.168	80h	4.912
11h	6.688	21h	6.432	31h	6.176	41h	5.920	51h	5.664	61h	5.408	71h	5.152	81h	4.896
12h	6.672	22h	6.416	32h	6.160	42h	5.904	52h	5.648	62h	5.392	72h	5.136	82h	4.88
13h	6.656	23h	6.400	33h	6.144	43h	5.888	53h	5.632	63h	5.376	73h	5.120	83h	4.864
14h	6.640	24h	6.384	34h	6.128	44h	5.872	54h	5.616	64h	5.360	74h	5.104	84h	4.848
15h	6.624	25h	6.368	35h	6.112	45h	5.856	55h	5.600	65h	5.344	75h	5.088	85h	4.832
16h	6.608	26h	6.352	36h	6.096	46h	5.840	56h	5.584	66h	5.328	76h	5.072	86h	4.816
17h	6.592	27h	6.336	37h	6.080	47h	5.824	57h	5.568	67h	5.312	77h	5.056	87h	4.8
18h	6.576	28h	6.320	38h	6.064	48h	5.808	58h	5.552	68h	5.296	78h	5.040	88h	4.784
19h	6.560	29h	6.304	39h	6.048	49h	5.792	59h	5.536	69h	5.280	79h	5.024	89h	4.768
1Ah	6.544	2Ah	6.288	3Ah	6.032	4Ah	5.776	5Ah	5.520	6Ah	5.264	7Ah	5.008	8Ah	4.752
1Bh	6.528	2Bh	6.272	3Bh	6.016	4Bh	5.760	5Bh	5.504	6Bh	5.248	7Bh	4.992	8Bh	4.736
1Ch	6.512	2Ch	6.256	3Ch	6.000	4Ch	5.744	5Ch	5.488	6Ch	5.232	7Ch	4.976	8Ch	4.72
1Dh	6.496	2Dh	6.240	3Dh	5.984	4Dh	5.728	5Dh	5.472	6Dh	5.216	7Dh	4.960	8Dh	4.704
1Eh	6.480	2Eh	6.224	3Eh	5.968	4Eh	5.712	5Eh	5.456	6Eh	5.200	7Eh	4.944	8Eh	4.688
1Fh	6.464	2Fh	6.208	3Fh	5.952	4Fh	5.696	5Fh	5.440	6Fh	5.184	7Fh	4.928	8Fh	4.672

Register R31H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VREF_VREG2_SEL[7:0]							
Default	0	1	1	0	0	0	0	1

VREF_VREG2_SEL[7:0]: Control signal to select VGMN

10h~8Fh: VGMN from -4.992V to -2.960V, 16mV/Step

61h: VGMN = -3.696V (Default)

VGMN level adjustment (Unit:V)

VREG2[7:0]	VGMN	VREG2[7:0]	VGMN	VREG2[7:0]	VGMN	VREG2[7:0]	VGMN	VREG2[7:0]	VGMN	VREG2[7:0]	VGMN	VREG2[7:0]	VGMN	VREG2[7:0]	VGMN
10h	-4.992	20h	-4.736	30h	-4.480	40h	-4.224	50h	-3.968	60h	-3.712	70h	-3.456	80h	-3.2
11h	-4.976	21h	-4.720	31h	-4.464	41h	-4.208	51h	-3.952	61h	-3.696	71h	-3.440	81h	-3.184
12h	-4.960	22h	-4.704	32h	-4.448	42h	-4.192	52h	-3.936	62h	-3.680	72h	-3.424	82h	-3.168
13h	-4.944	23h	-4.688	33h	-4.432	43h	-4.176	53h	-3.920	63h	-3.664	73h	-3.408	83h	-3.152
14h	-4.928	24h	-4.672	34h	-4.416	44h	-4.160	54h	-3.904	64h	-3.648	74h	-3.392	84h	-3.136
15h	-4.912	25h	-4.656	35h	-4.400	45h	-4.144	55h	-3.888	65h	-3.632	75h	-3.376	85h	-3.12
16h	-4.896	26h	-4.640	36h	-4.384	46h	-4. 128	56h	-3.872	66h	-3.616	76h	-3.360	86h	-3.104
17h	-4.880	27h	-4.624	37h	-4.368	47h	-4.112	57h	-3.856	67h	-3.600	77h	-3.344	87h	-3.088
18h	-4.864	28h	-4.608	38h	-4.352	48h	-4.096	58h	-3.840	68h	-3.584	78h	-3.328	88h	-3.072
19h	-4.848	29h	-4.592	39h	-4.336	49h	-4.080	59h	-3.824	69h	-3.568	79h	-3.312	89h	-3.056
1Ah	-4.832	2Ah	-4.576	3Ah	-4.320	4Ah	-4.064	5Ah	-3.808	6Ah	-3.552	7Ah	-3.296	8Ah	-3.04
1Bh	-4.816	2Bh	-4.560	3Bh	-4.304	4Bh	-4.048	5Bh	-3.792	6Bh	-3.536	7Bh	-3.280	8Bh	-3.024
1Ch	-4.800	2Ch	-4.544	3Ch	-4.288	4Ch	-4.032	5Ch	-3.776	6Ch	-3.520	7Ch	-3.264	8Ch	-3.008
1Dh	-4.784	2Dh	-4.528	3Dh	-4.272	4Dh	-4.016	5Dh	-3.760	6Dh	-3.504	7Dh	-3.248	8Dh	-2.992
1Eh	-4.768	2Eh	-4.512	3Eh	-4.256	4Eh	-4.000	5Eh	-3.744	6Eh	-3.488	7Eh	-3.232	8Eh	-2.976
1Fh	-4.752	2Fh	-4.496	3Fh	-4.240	4Fh	-3.984	5Fh	-3.728	6Fh	-3.472	7Fh	-3.216	8Fh	-2.96

Register R32H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VREF_VGSP_SEL[6:0]						
Default	0	1	0	0	0	0	1	0

VREF_VGSP_SEL[6:0]: Control signal to select VGSP

08h~7Bh: VGSP from 1.936V to 0.096V, -16mV/Step

42h: VGSP = 1.008V (Default)

VGSP level adjustment (Unit:V)

VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP
00h	-	10h	1.808	20h	1.552	30h	1.296	40h	1.040	50h	0.784	60h	0.528	70h	0.272
01h	-	11h	1.792	21h	1.536	31h	1.280	41h	1.024	51h	0.768	61h	0.512	71h	0.256
02h	-	12h	1.776	22h	1.520	32h	1.264	42h	1.008	52h	0.752	62h	0.496	72h	0.240
03h	-	13h	1.760	23h	1.504	33h	1.248	43h	0.992	53h	0.736	63h	0.480	73h	0.224
04h	-	14h	1.744	24h	1.488	34h	1.232	44h	0.976	54h	0.720	64h	0.464	74h	0.208
05h	-	15h	1.728	25h	1.472	35h	1.216	45h	0.960	55h	0.704	65h	0.448	75h	0.192
06h	-	16h	1.712	26h	1.456	36h	1.200	46h	0.944	56h	0.688	66h	0.432	76h	0.176
07h	-	17h	1.696	27h	1.440	37h	1.184	47h	0.928	57h	0.672	67h	0.416	77h	0.160
08h	1.936	18h	1.680	28h	1.424	38h	1.168	48h	0.912	58h	0.656	68h	0.400	78h	0.144
09h	1.920	19h	1.664	29h	1.408	39h	1.152	49h	0.896	59h	0.640	69h	0.384	79h	0.128
0Ah	1.904	1Ah	1.648	2Ah	1.392	3Ah	1.136	4Ah	0.880	5Ah	0.624	6Ah	0.368	7Ah	0.112
0Bh	1.888	1Bh	1.632	2Bh	1.376	3Bh	1.120	4Bh	0.864	5Bh	0.608	6Bh	0.352	7Bh	0.096
0Ch	1.872	1Ch	1.616	2Ch	1.360	3Ch	1.104	4Ch	0.848	5Ch	0.592	6Ch	0.336	7Ch	-
0Dh	1.856	1Dh	1.600	2Dh	1.344	3Dh	1.088	4Dh	0.832	5Dh	0.576	6Dh	0.320	7Dh	-
0Eh	1.840	1Eh	1.584	2Eh	1.328	3Eh	1.072	4Eh	0.816	5Eh	0.560	6Eh	0.304	7Eh	-
0Fh	1.824	1Fh	1.568	2Fh	1.312	3Fh	1.056	4Fh	0.800	5Fh	0.544	6Fh	0.288	7Fh	-

Register R33H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VREF_VGL_SEL[2:0]			VREF_VGH_SEL[3:0]			
Default	0	0	1	1	1	0	1	0

VREF_VGL_SEL[2:0]:Control signal to select VGL

VREF_VGH_SEL[3:0]:Control signal to select VGH

VREF_VGL_SEL[2:0]	VGL	VREF_VGH_SEL[3:0]	VGH	VREF_VGH_SEL[3:0]	VGH
0h	-7V	0h	10.16V	8h	13V
1h	-8V	1h	10.24V	9h	14V
2h	-9V	2h	10.32V	Ah (Default)	15V
3h (Default)	-10V	3h	10.40V	Bh	16V
4h	-11V	4h	10.48V	Ch	17V
5h	-12V	5h	10.56V	Dh	18V
6h	-13V	6h	10.64V	Eh	18V
7h	-13V	7h	10.72V	Fh	18V

Register R34H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VREF_VSP_AC_SEL[2:0]			-	VREF_VSP_DC_SEL[2:0]		
Default	0	0	1	1	0	0	1	1

VREF_VSP_AC_SEL[2:0]: Control signal to select VSP_AC

VREF_VSP_DC_SEL[2:0]: Control signal to select VSP_DC

VREF_VSP_AC_SEL[2:0]	VSP_AC	VREF_VSP_DC_SEL[2:0]	VSP_DC
0h	5.600V	0h	5.600V
1h	5.808V	1h	5.808V
2h	6.000V	2h	6.000V
3h (Default)	6.208V	3h (Default)	6.208V
4h	6.400V	4h	6.400V
5h	6.608V	5h	6.608V
6h	6.800V	6h	6.800V
7h	7.008V	7h	7.008V

Register R35H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VREF_VSN_AC_SEL[2:0]			-	VREF_VSN_DC_SEL[2:0]		
Default	0	0	1	0	0	0	1	0

VREF_VSN_AC_SEL[2:0]: Control signal to select VSN_AC

VREF_VSN_DC_SEL[2:0]: Control signal to select VSN_DC

VREF_VSN_AC_SEL[2:0]	VSN_AC	VREF_VSN_DC_SEL[2:0]	VSN_DC
0h	-4.0V	0h	-4.0V
1h	-4.2V	1h	-4.2V
2h (Default)	-4.4V	2h (Default)	-4.4V
3h	-4.6V	3h	-4.6V
4h	-4.8V	4h	-4.8V
5h	-5.0V	5h	-5.0V
6h	-5.2V	6h	-5.2V
7h	-5.4V	7h	-5.4V

Register R36H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	VREF_VDDN_AC_SEL[1:0]		VREF_VDDN_DC_SEL[1:0]	
Default	0	0	0	0	0	0	0	0

VREF_VDDN_AC_SEL[1:0]: Control signal to select VDDN_AC

VREF_VDDN_DC_SEL[1:0]: Control signal to select VDDN_DC

VREF_VDDN_AC_SEL[1:0]	VDDN_AC	VREF_VDDN_DC_SEL[1:0]	VDDN_DC
0h (Default)	1.8V	0h (Default)	1.8V
1h	2.0V	1h	2.0V
2h	2.2V	2h	2.2V
3h	2.4V	3h	2.4V

Register R3CH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	DUAL_SEL[1:0]	
Default	0	0	0	0	0	0	0	0

DUAL_SEL[1:0]:Dual gate on sequence selection

00: Z scan (Default)

01: Bow scan

10: Inv_Z scan

11: Z + Inv_Z

Register R3EH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	ID[6:0]						
Default	0	1	1	1	1	1	1	1

ID[6:0]:ID Setting

Register R40H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VMF_SET	VMF[6:0]						
Default	1	1	0	0	0	0	0	0

VMF_SET:VMF setting

VMF[6:0]:VMF setting adjustment

VMF[6]	VMF[5:0]	VGSP	VGMP	VGMN
0	0h	VGSP+64d	VGMP+64d	VGMN+64d
	1h	VGSP+63d	VGMP+63d	VGMN+63d
	2h	VGSP+62d	VGMP+62d	VGMN+62d
	20h	VGSP+31d	VGMP+31d	VGMN+31d
	3Eh	VGSP+2d	VGMP+2d	VGMN+2d
	3Fh	VGSP+1d	VGMP+1d	VGMN+1d
1	0h	VGSP	VGMP	VGMN
	1h	VGSP-1d	VGMP-1d	VGMN-1d
	2h	VGSP-2d	VGMP-2d	VGMN-2d
	20h	VGSP-32d	VGMP-32d	VGMN-32d
	3Eh	VGSP-62d	VGMP-62d	VGMN-62d
	3Fh	VGSP-63d	VGMP-63d	VGMN-63d

Note: d=16mV

Register R45H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	OTP2REG_GAMMA_MARK[2:0]			-	OTP2REG_RES_MARK[2:0]		
Default	None	None	None	None	None	None	None	None

OTP2REG_GAMMA_MARK[2:0]:Read Only. Gamma Registers OTP Program Flag

OTP2REG_RES_MARK[2:0]:Read Only. RES[1:0] & DUAL Registers OTP Program Flag

Register R46H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	OTP2REG_VCMC_MARK[2:0]			-	OTP2REG_CHIPID_MARK[2:0]		
Default	None	None	None	None	None	None	None	None

OTP2REG_VCMC_MARK[2:0]:Read Only. VCM Registers OTP Program Flag

OTP2REG_CHIPID_MARK[2:0]:Read Only. ID Registers OTP Program Flag

Register R48H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OTP_KEY[7:0]							
Default	None	None	None	None	None	None	None	None

OTP_KEY[7:0]:OTP Program Key

Register R49H

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	OTP_TARGET[6:0]						
Default	0	1	0	0	0	0	0	0

OTP_TARGET[6:0]:OTP Program Target

Register R4AH

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	OTP_TRIM_FAIL_FLAG
Default	None	None	None	None	None	None	None	None

OTP_TRIM_FAIL_FLAG:Read Only. OTP Trim Fail Flag

9. LECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Item	Symbol	*Rating*	Unit
Power Supply Voltage	VCI	*- 0.3 ~ +4.6*	V
IO Supply Voltage	VDDI	*- 0.3 ~ +4.6*	V
Charge Pump Supply Voltage	VCIP	*- 0.3 ~ +4.6*	V
Logic Input Voltage Range	VIN	*-0.3 ~ VDDI + 0.3*	V
Logic Output Voltage Range	VO	*-0.3 ~ VDDI + 0.3*	V
Operating Temperature Range	TOPR	*-30 ~ +85*	℃
Storage Temperature Range	TSTG	*-40 ~ +125*	℃

Note:

1. That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/AC Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.

2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

3. VIN should be less than or equal to 3.6V. (VIN ≤ 3.6V)

9.2 DC Characteristics

9.2.1 Recommended Operating Range

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCI	3.0	3.3	3.6	V	
IO Supply Voltage	VDDI	3.0	3.3	3.6	V	VDDI<=VCI
Charge Pump Supply Voltage	VCIP	3.0	3.3	3.6	V	VCIP<=VCI
NVM Supply Voltage	VPP	10	10.25	10.5	V	

9.2.2 DC Characteristics for Digital Circuit

DC Electrical Characteristics (VCIP=VCI=VDDI= 3.3V, VSSA= 0V, TA=25°C).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	VSSD	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	VSSD	-	VSSD+0.4	V	

9.2.3 DC Characteristics for Analog Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-voltage power	VGH	10.16	15	18	V	
Negative High-voltage power	VGL	-13	-10	-7	V	
Output Voltage Deviation	Vod	-	±35	±45	mV	
Standby Current	Isc	-	-	50	uA	
Operation Current	Ioc	-	20	-	mA	No Load@ FR=60Hz

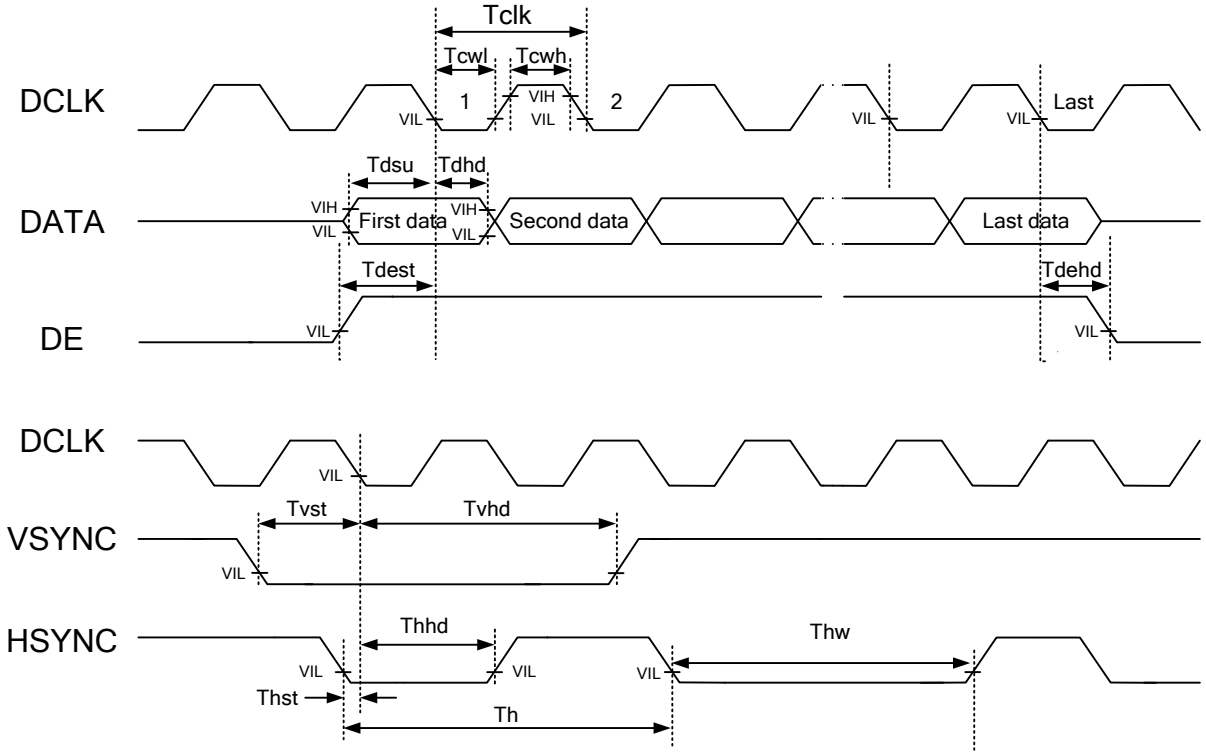
9.3 AC Characteristics

AC Electrical Characteristics (VCIP=VCI=VDDI= 3.3V, VSSA= 0V, TA=25°C).

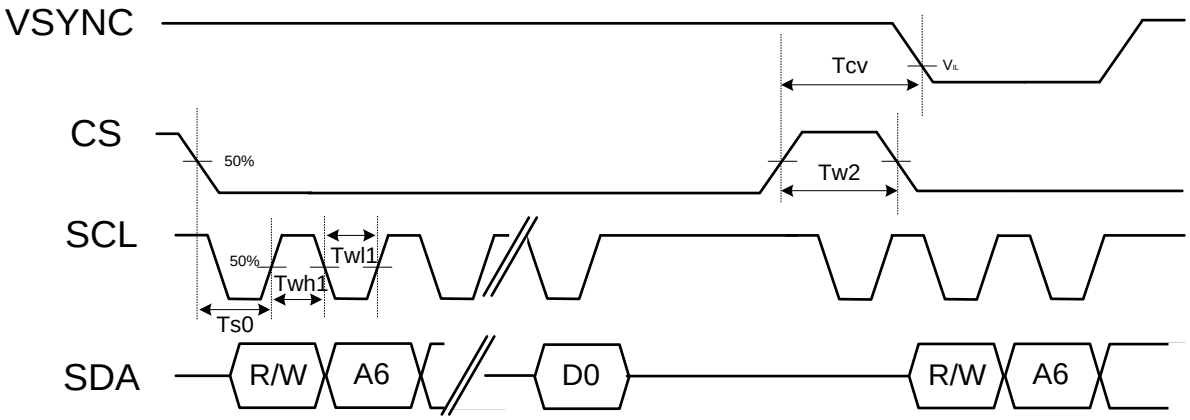
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
System operation timing						
VCI power source slew time	TPOR	-	-	20	ms	From 0V to 99% VCI
RESX pulse width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
Input/ Output timing						
CLK pulse duty	Tcw	40	50	60	%	
Hsync width	Thw	2	-	-	DCLK	
Hsync period	Th	55	60	65	us	
Vsync setup time	Tvst	12	-	-	ns	
Vsync hold time	Tvhd	12	-	-	ns	
Hsync setup time	Thst	12	-	-	ns	
Hsync hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
DE setup time	Tdest	10	-	-	ns	
DE setup time	Tdehd	10	-	-	ns	
SD output stable time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD output rise and fall time	Tgst	-	-	6	ns	Output settled (5%~95%), Loading = 4.7k+29.8pF
3-wire serial communication						
Delay between CSX and VSYNC	Tcv	1	-	-	us	
CSX input setup time	Ts0	50	-	-	ns	
Serial data input setup time	Ts1	50	-	-	ns	
CSX input hold time	Th0	50	-	-	ns	
Serial data input hold time	Th1	50	-	-	ns	
SCL pulse high width	Twh1	50	-	-	ns	
SCL pulse low width	Twl1	50	-	-	ns	
CSX pulse high width	Tw2	400	-	-	ns	

9.4 AC Timing Diagram

9.4.1 Clock and Data Input Timing Diagram



9.4.2 3-Wire Communication Timing Diagram



10. INPUT DATA FORMAT

10.1 RGB Input Timing Table

RGB input timing table (VCIP=VCI=VDDI= 3.3V, VSSA= 0V, TA=25°C).

10.1.1 Parallel 24-bit RGB Timing Table

480RGB X 272 Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	8	9	12	MHz	
DCLK Period		Tclk	125	111	83	ns	
HSYNC	Period Time	Th	487	531	598	DCLK	
	Display Period	Thdisp	-	480	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	4	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	276	292	321	H	
	Display Period	Tvdisp	-	272	-	H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

Note: 1.It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

2.Thbp+Thfp >=7

320RGB X 240 Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	5	6	8	MHz	
DCLK Period		Tclk	200	167	125	ns	
HSYNC	Period Time	Th	327	371	438	DCLK	
	Display Period	Thdisp	-	320	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	4	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	244	260	289	H	
	Display Period	Tvdisp	-	240	-	H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

Note: 1.It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

2.Thbp+Thfp >=7

240RGB X 320 Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	5	6	8	MHz	
DCLK Period		Tclk	200	167	125	ns	
HSYNC	Period Time	Th	247	291	358	DCLK	
	Display Period	Thdisp	-	240	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	4	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	326	340	369	H	
	Display Period	Tvdisp	-	320	-	H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	4	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

Note: 1.It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

2.Thbp+Thfp >=7

240RGB X 240 Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	4	5	6	MHz	
DCLK Period		Tclk	250	200	167	ns	
HSYNC	Period Time	Th	247	291	358	DCLK	
	Display Period	Thdisp	-	240	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	4	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	246	260	289	H	
	Display Period	Tvdisp	-	240	-	H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	4	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

Note: 1.It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

2.Thbp+Thfp >=7

10.1.2 Serial 8-bit RGB Timing Table

480RGB X 272 Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	24	27	30	MHz	
DCLK Period		Tclk	42	37	33	ns	
HSYNC	Period Time	Th	1461	1491	1558	DCLK	
	Display Period	Thdisp	-	1440	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	18	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	276	292	321	H	
	Display Period	Tvdisp	-	272	-	H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

Note:1. It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

2.Thbp+Thfp >=21

320RGB X 240Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	15	16	19	MHz	
DCLK Period		Tclk	67	63	53	ns	
HSYNC	Period Time	Th	981	1011	1078	DCLK	
	Display Period	Thdisp	-	960	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	18	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	244	260	289	H	
	Display Period	Tvdisp	-	240	-	H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

Note:1. It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

2.Thbp+Thfp >=21

240RGB X 320Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	14	16	19	MHz	
DCLK Period		Tclk	71	63	53	ns	
HSYNC	Period Time	Th	741	771	838	DCLK	
	Display Period	Thdisp	-	720	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	18	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	324	340	369	H	
	Display Period	Tvdisp	-	320	-	H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

Note:1. It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

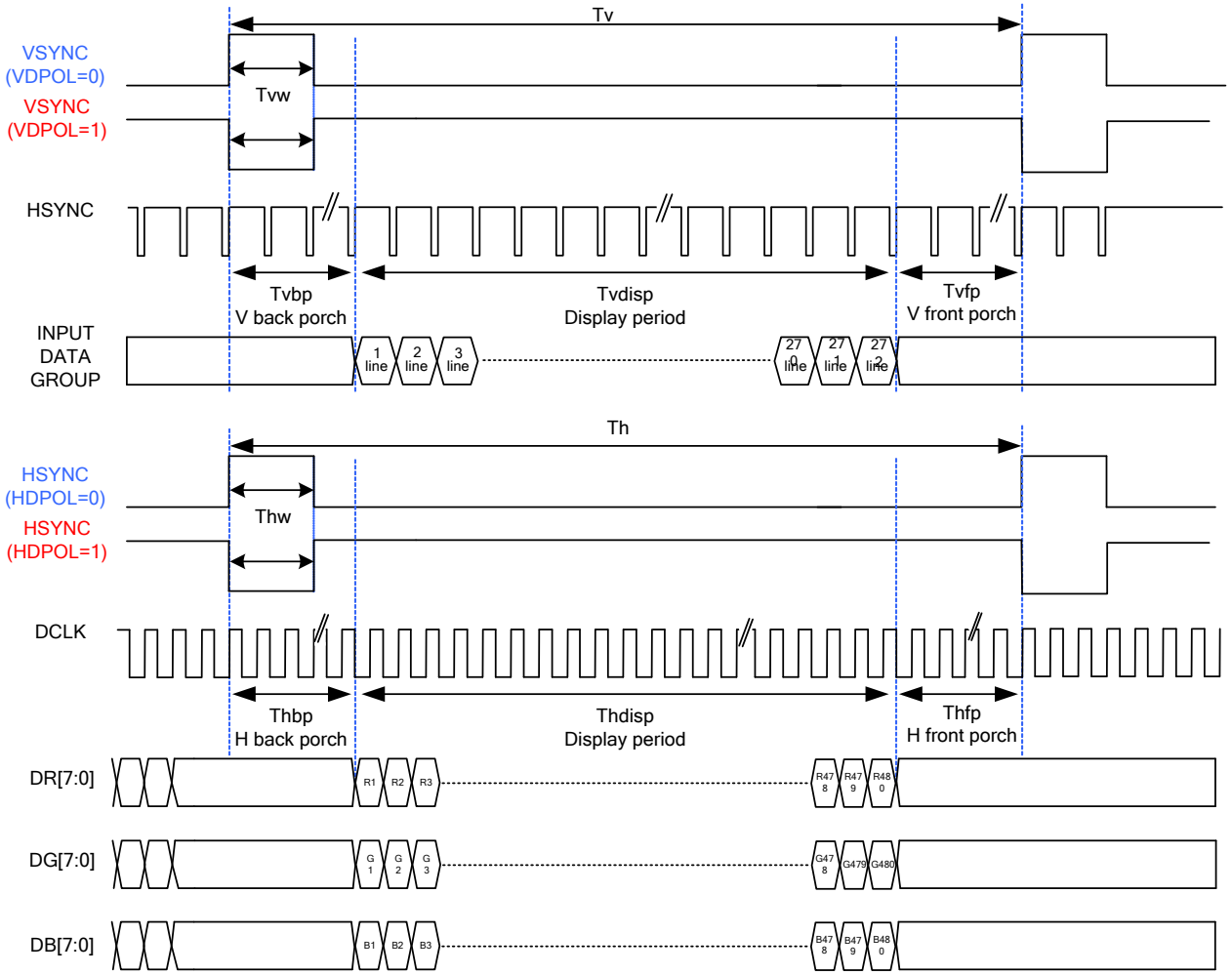
2.Thbp+Thfp >=21

240RGB X 240Resolution Timing Table							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	11	12	15	MHz	
DCLK Period		Tclk	91	83	67	ns	
HSYNC	Period Time	Th	741	771	838	DCLK	
	Display Period	Thdisp	-	720	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	18	8	75	DCLK	
	Pulse Width	Thw	2	4	75	DCLK	
VSYNC	Period Time	Tv	244	260	289	H	
	Display Period	Tvdisp	-	240	-	H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	37	H	

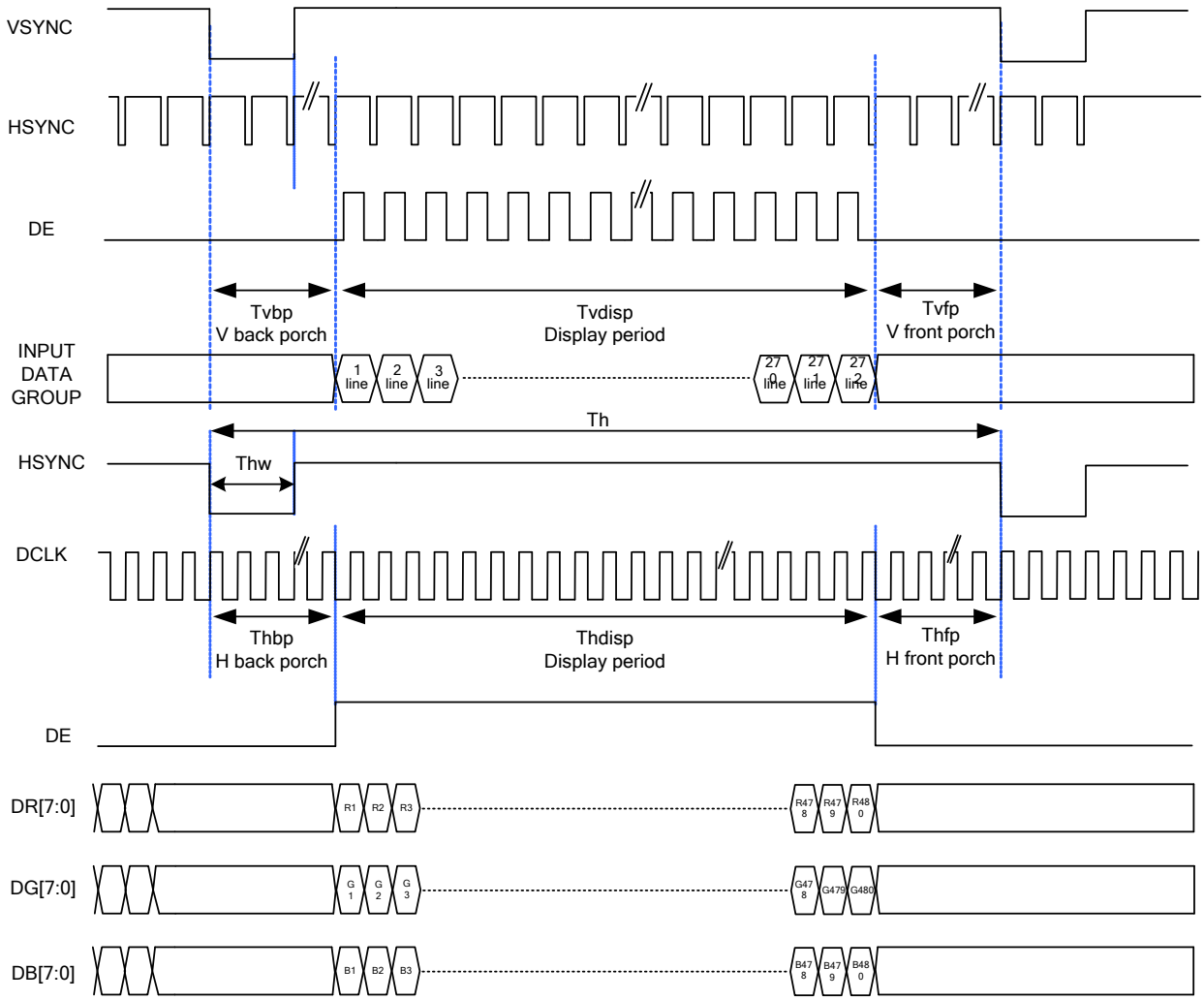
Note:1. It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

2.Thbp+Thfp >=21

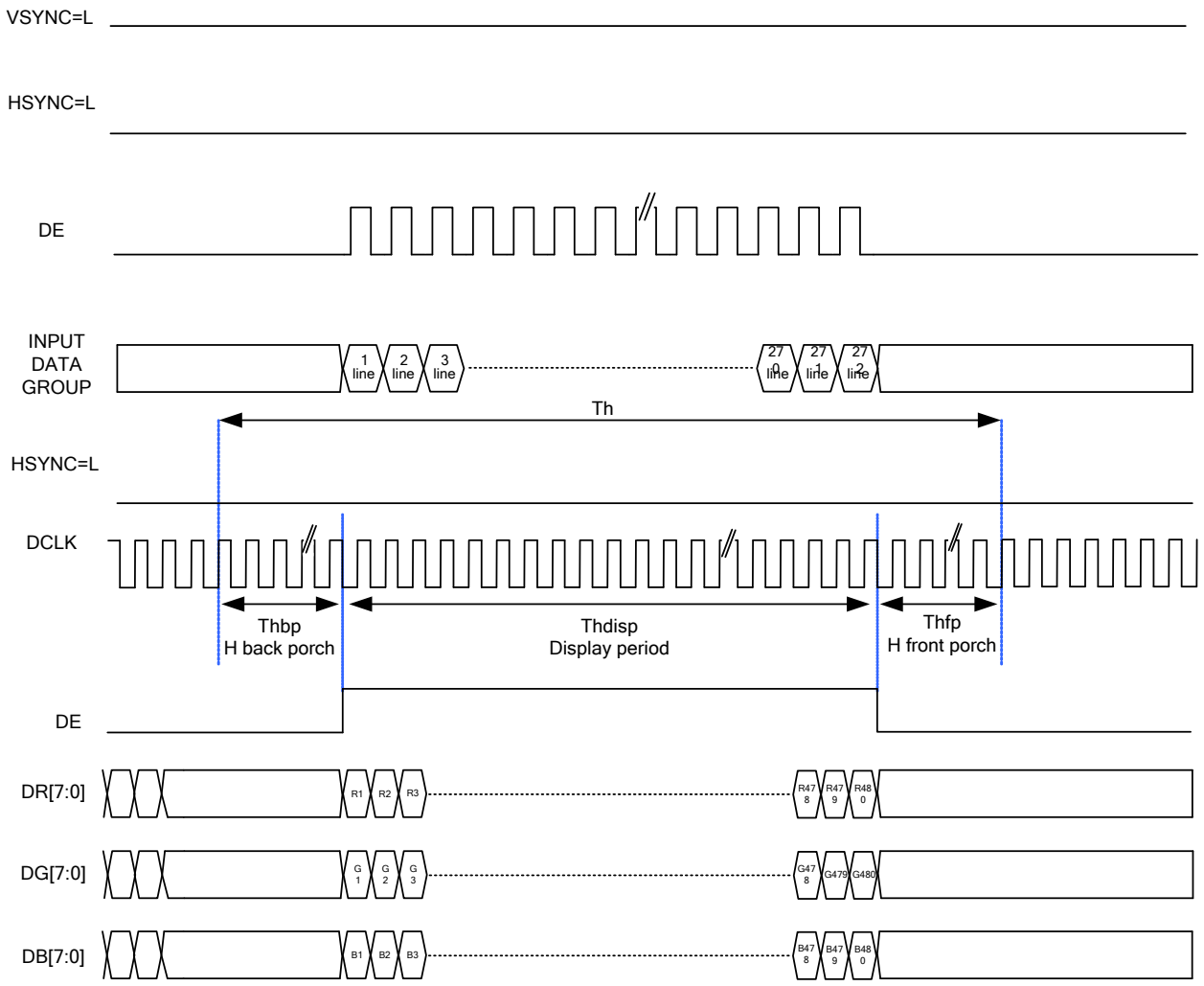
10.2 SYNC Mode Timing Diagram



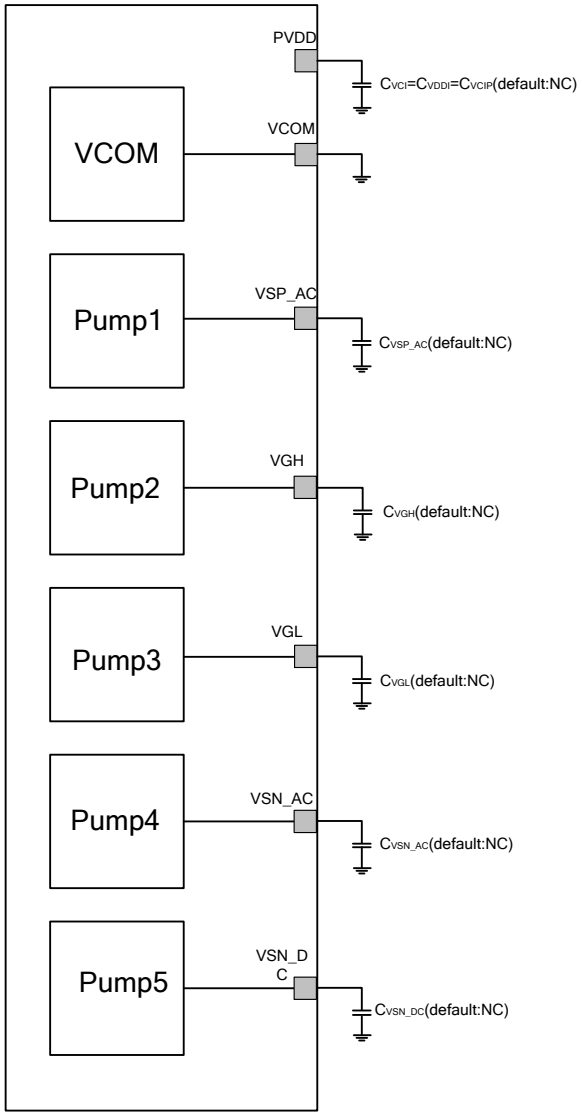
10.3 SYNC-DE Mode Timing Diagram



10.4 DE Mode Timing Diagram



11. POWER APPLICATION CIRCUIT



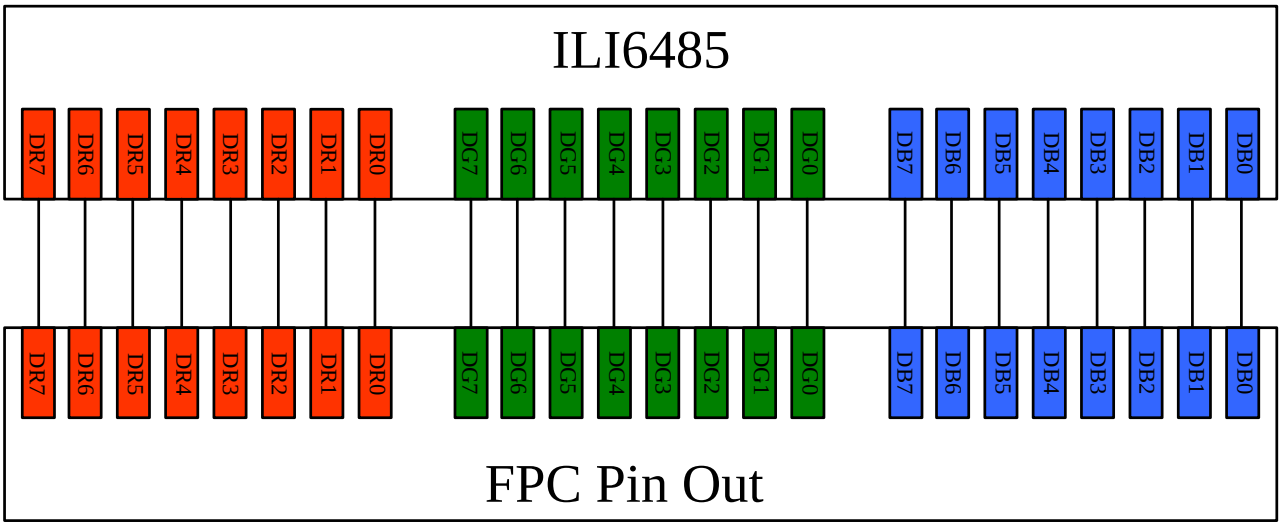
Suggestion of external component

Component	Recommended Value	Voltage proof
CVCI=CVDDI=CVCIP	1uF	> 6.3V (default: NC)
CVSP_AC	1uF	> 10V (default: NC)
CVSN_AC	1uF	> 10V (default: NC
CVSN_DC	1uF	> 10V (default: NC)
CVGH	1uF	> 25V (default: NC)
CVGL	1uF	> 16V (default: NC)

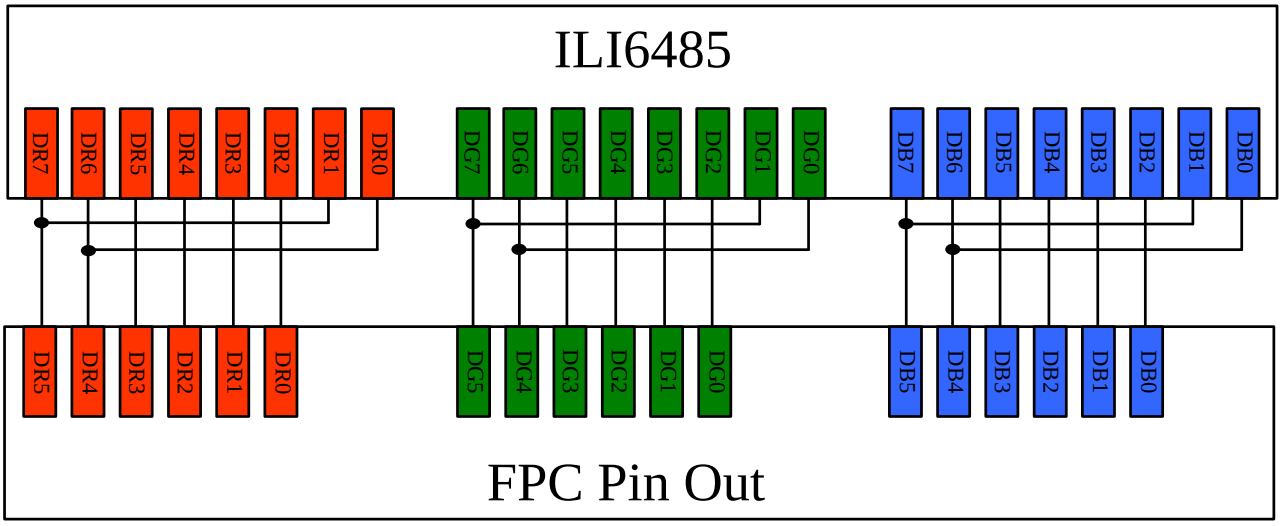
Note: Default NC, The components would be needed depend on the system power, panel loading and display quality.

12. INPUT COLOR FORMAT APPLICATION CIRCIT

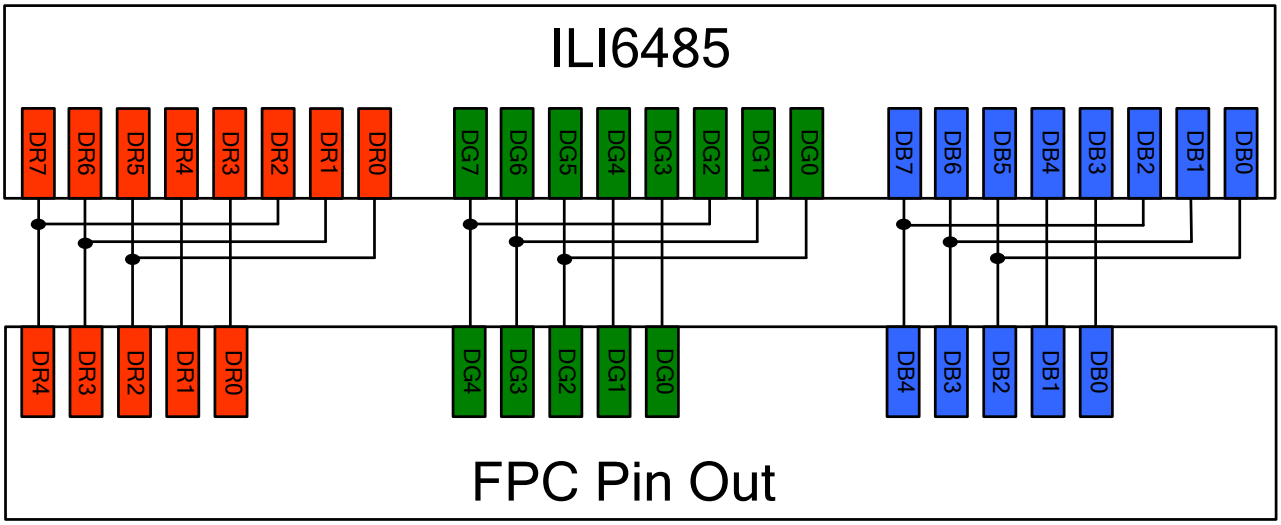
12.1 16.7M Input Color Format



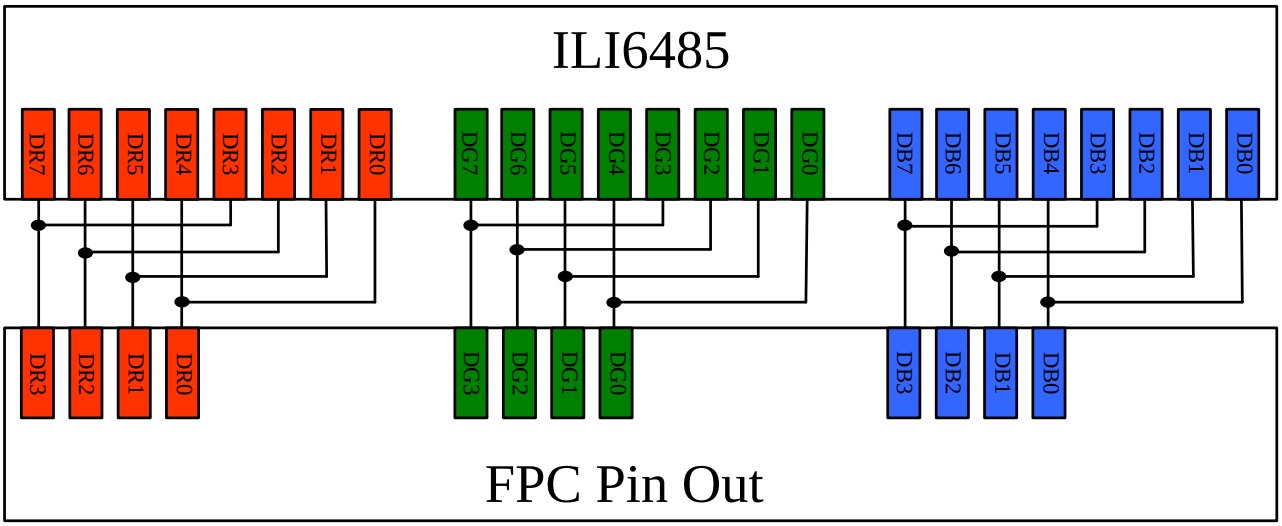
12.2 262K Input Color Format



12.3 65K Input Color Format



12.4 4K Input Color Format



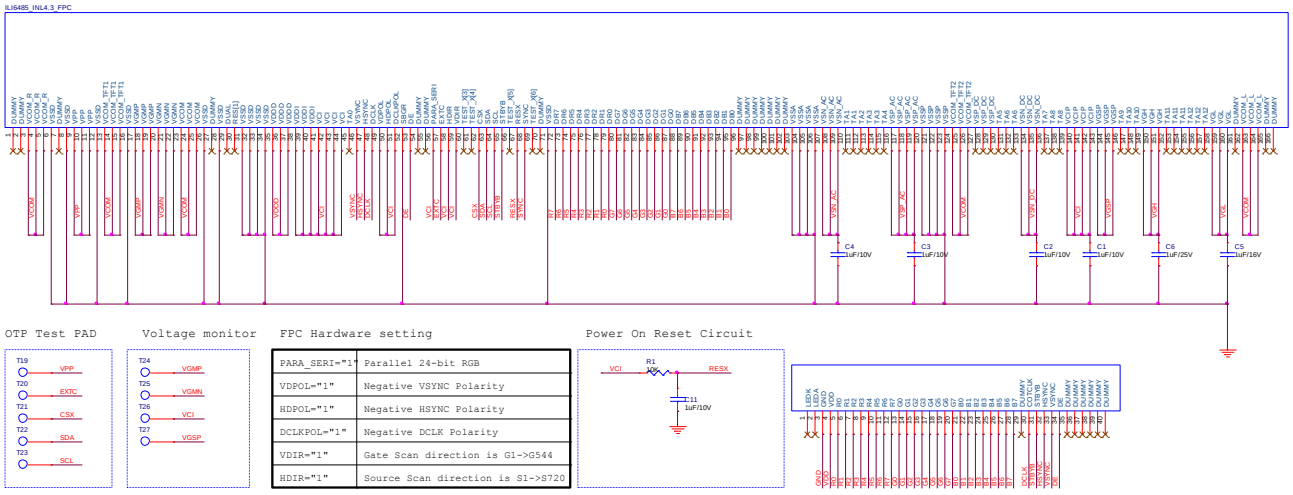
13. FPC APPLICATION CIRCUIT

13.1 RGB Mode Selection Table

RGB Mode	DCLK	HSYNC	VSYNC	DE	DR[0:7]	DG[0:7]	DB[0:7]
Parallel RGB SYNC-DE Mode	Input	Input	Input	Input	Input	Input	Input
Parallel RGB SYNC Mode	Input	Input	Input	VSSD	Input	Input	Input
Parallel RGB DE Mode	Input	VSSD	VSSD	Input	Input	Input	Input
Serial RGB SYNC-DE Mode	Input	Input	Input	Input	VSSD	Input	VSSD
Serial RGB SYNC Mode	Input	Input	Input	VSSD	VSSD	Input	VSSD
Serial RGB DE Mode	Input	VSSD	VSSD	Input	VSSD	Input	VSSD

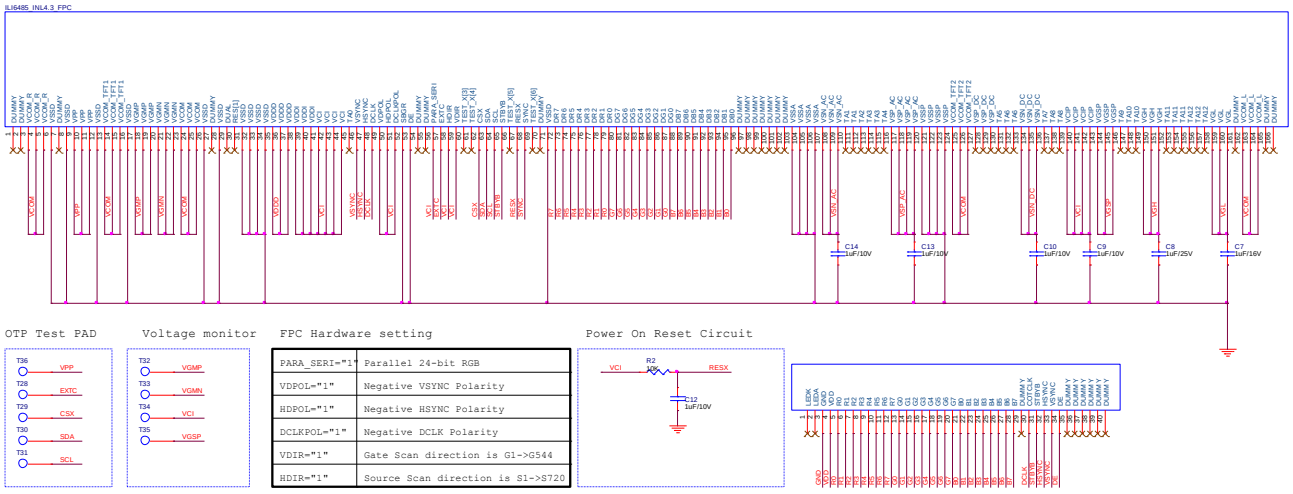
13.2 Type C Panel (I-company panel)

13.2.1 Parallel RGB SYNC-DE Mode Reference Circuit



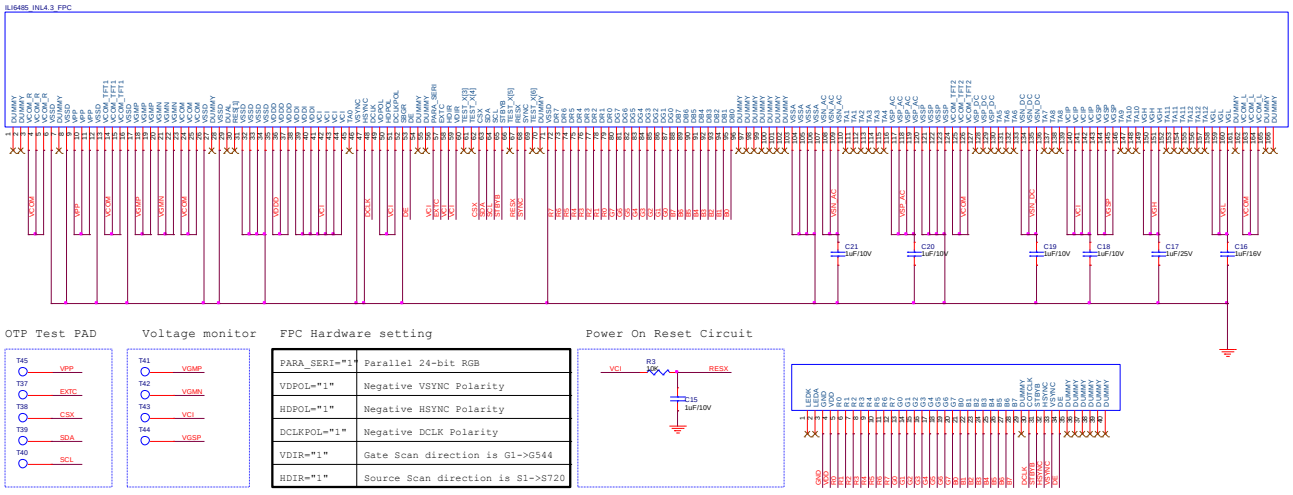
PARA_SERI="1"	Parallel 24-bit RGB
VDPOL="1"	Negative VSYNC Polarity
HDPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720

13.2.2 Parallel RGB SYNC Mode Reference Circuit



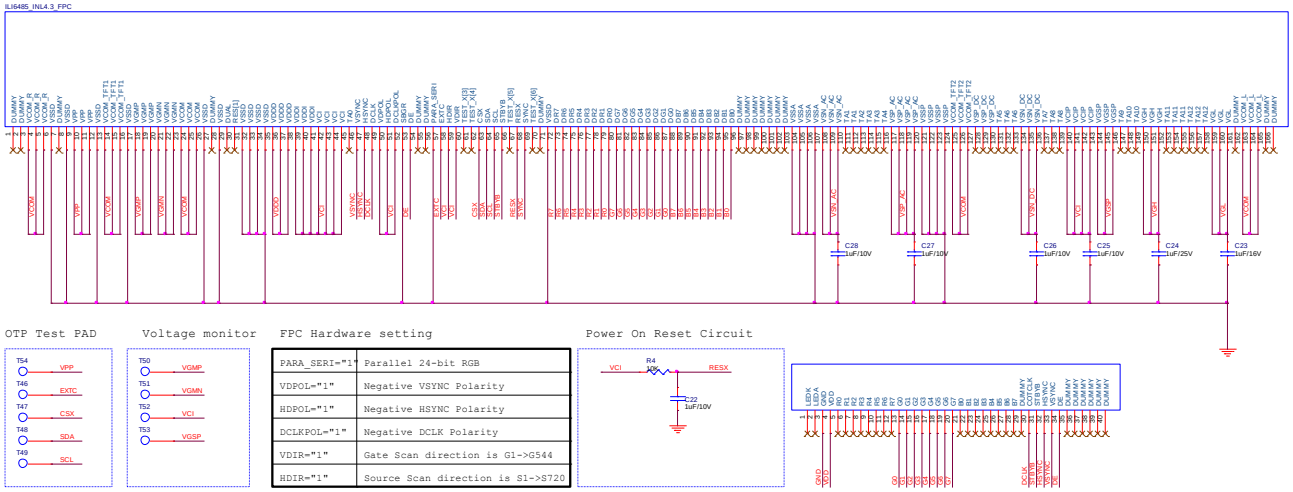
PARA_SERI="1"	Parallel 24-bit RGB
VDPOL="1"	Negative VSYNC Polarity
HDPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720

13.2.3 Parallel RGB DE Mode Reference Circuit



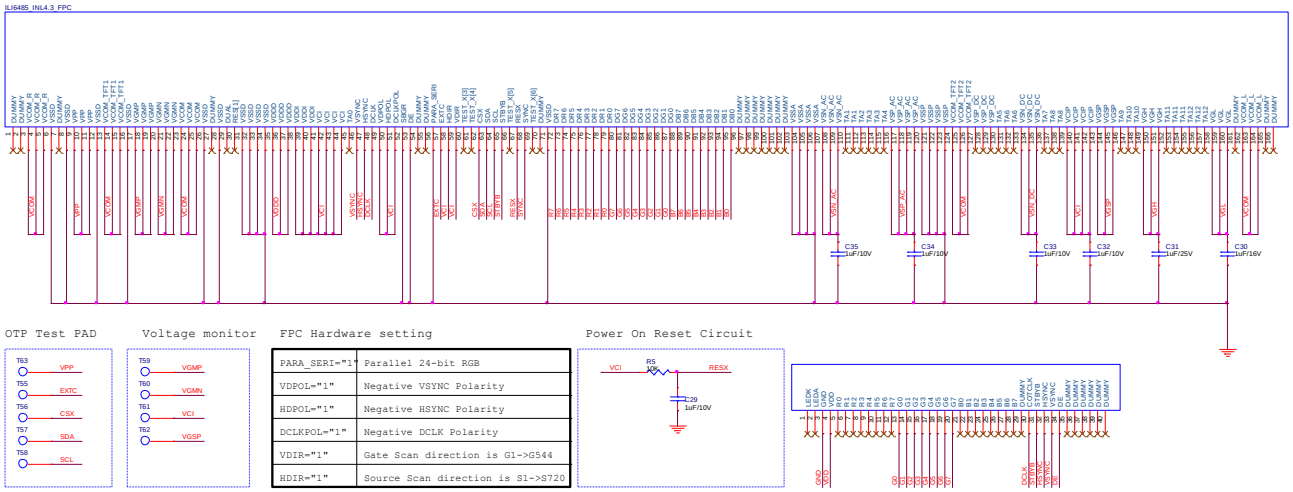
PARA_SERI="1"	Parallel 24-bit RGB
VDPOL="1"	Negative VSYNC Polarity
HDPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720

13.2.4 Serial RGB SYNC-DE Mode Reference Circuit



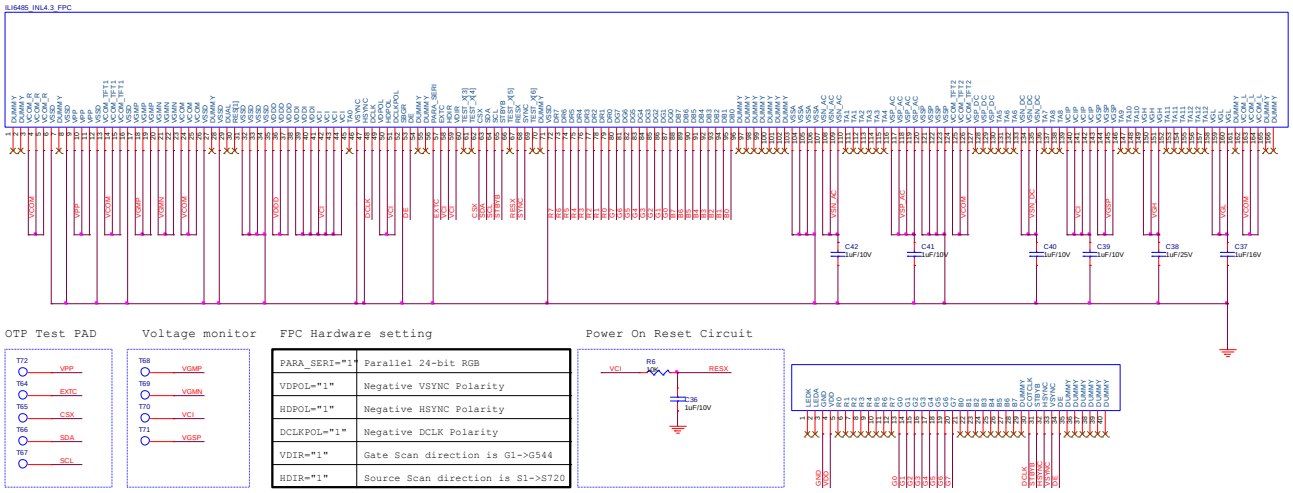
PARA_SERI="1"	Parallel 24-bit RGB
VDPOL="1"	Negative VSYNC Polarity
HDPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720

13.2.5 Serial RGB SYNC Mode Reference Circuit



PARA_SERI="1"	Parallel 24-bit RGB
VDPOL="1"	Negative VSYNC Polarity
HDPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720

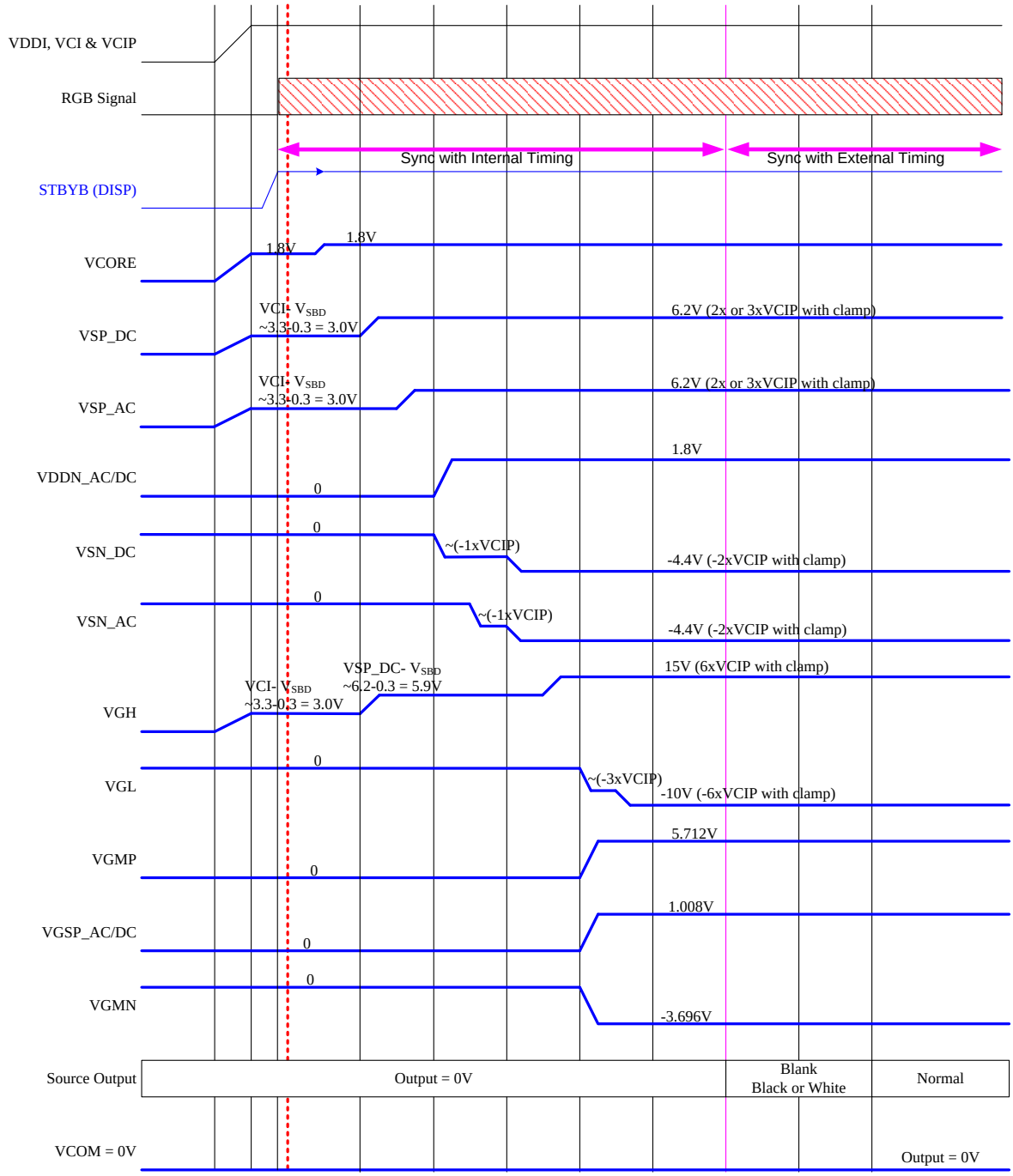
13.2.6 Serial RGB DE Mode Reference Circuit



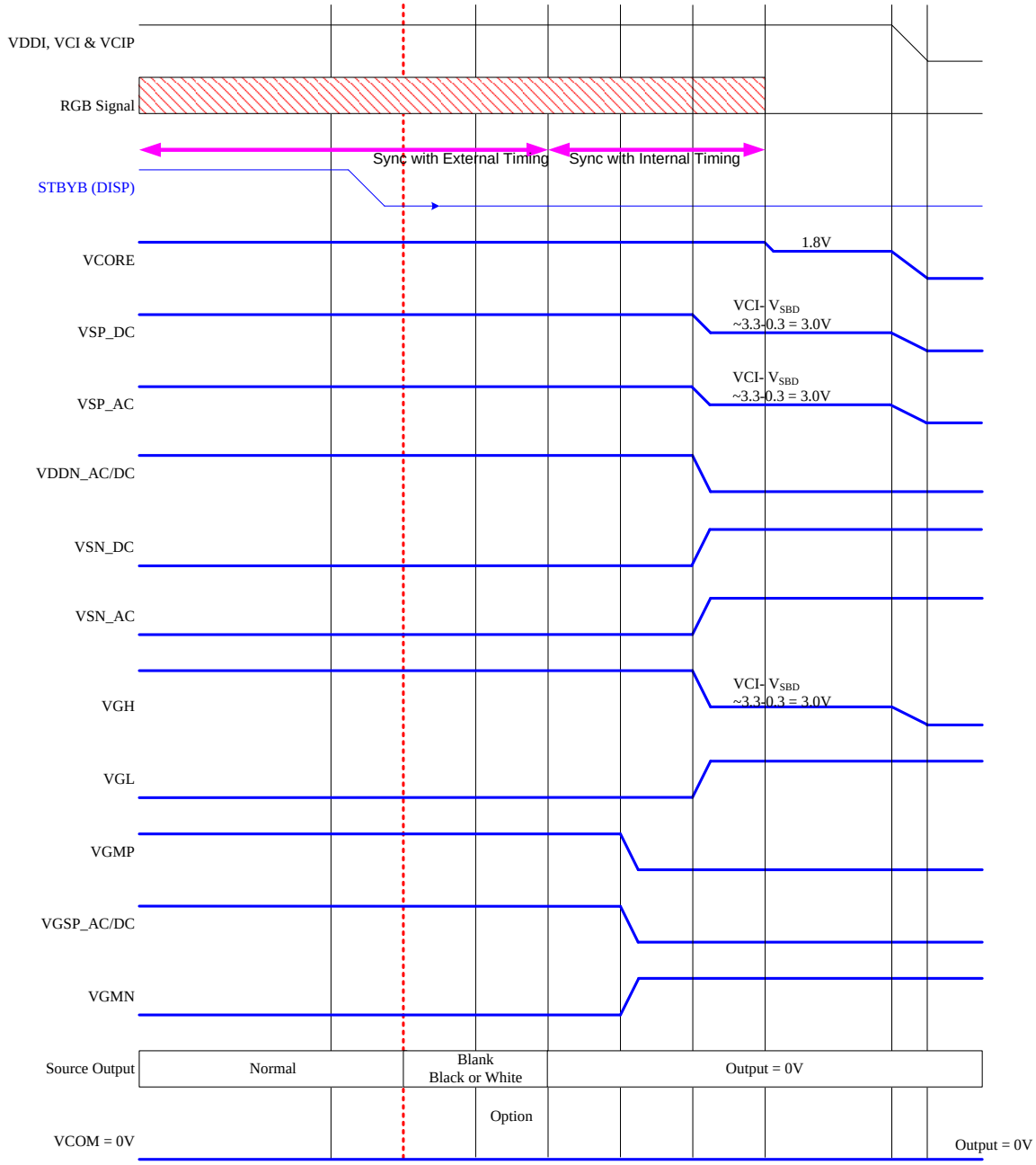
PARA_SERI="1"	Parallel 24-bit RGB
VDPOL="1"	Negative VSYNC Polarity
HDPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720

14. POWER ON/OFF SEQUENCE

14.1 Power On Sequence



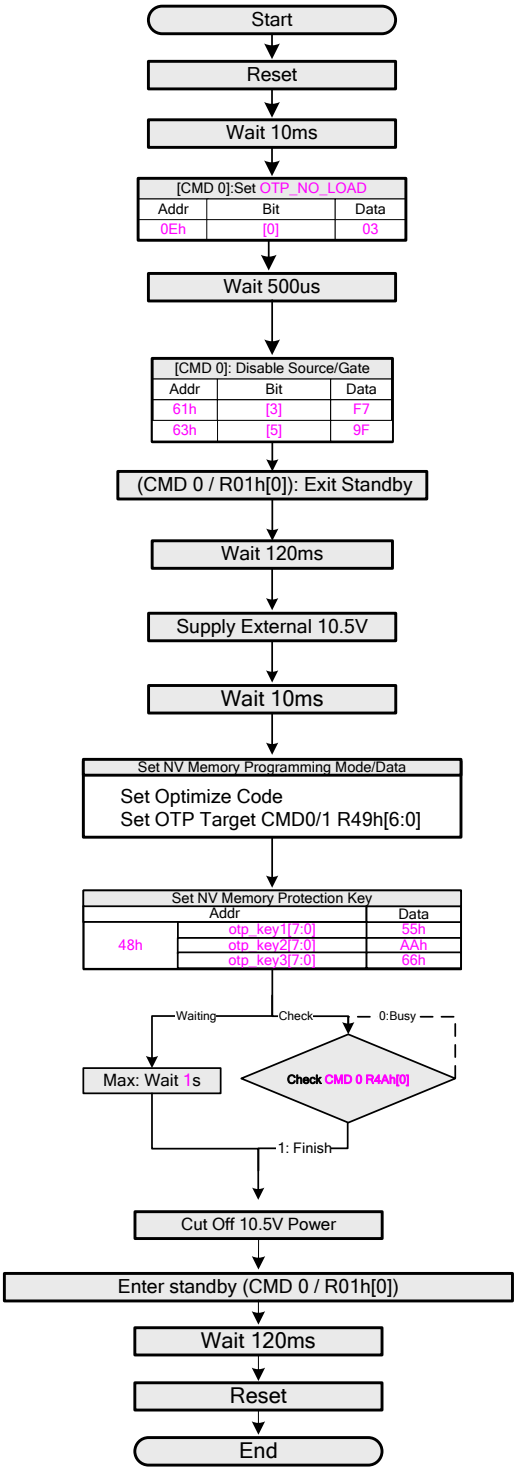
14.2 Power Off Sequence



15. OTP Flow

· Auto Program

OTP Supply Voltage: Min:10.25V Typ:10.5V Max:10.6V



16. RECOMMENDED PANEL ROUTING RESISTANCE

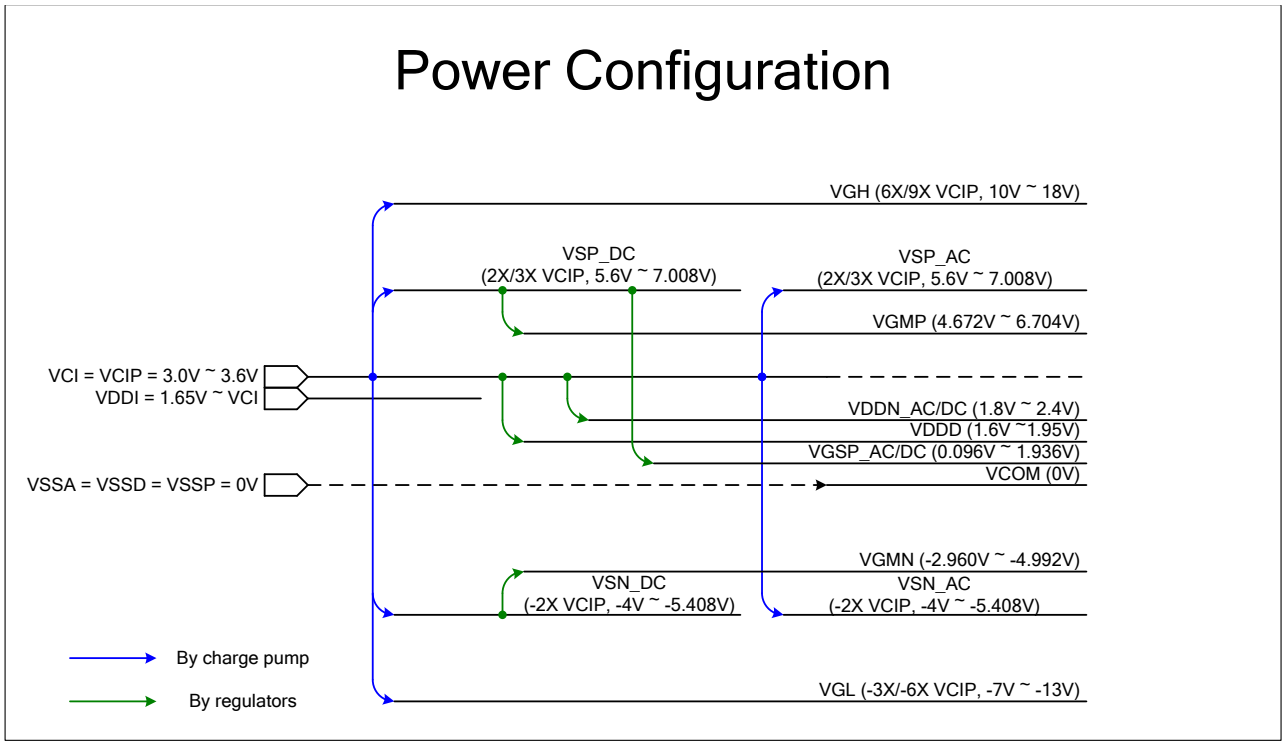
The recommended wiring resistance values are given below. The wiring resistance values affect the current capability of the power supply blocks and thus must be designed within the given range.

Pin Name	Unit: ohm		Pin Name	Unit: ohm
VPP	<3		CSX	<50
VGMP	<50		SDA	<50
VGMN	<50		SCL	<50
VCOM	<3		STBYB	<50
VSSD	<3		RESX	<50
VDDD	<50		SYNC	<50
VDDI	<3		DR7-DR0	<50
VCI	<3		DG7-DG0	<50
VSYNC	<50		DB7-DB0	<50
HSYNC	<50		VSSA	<3
DCLK	<50		VSN_AC	<50
VDPOL	<50		VSN_DC	<50
HDPOL	<50		VSP_AC	<50
DCLKPOL	<50		VSP_DC	<50
SBGR	<50		VGSP	<50
DE	<50		VSSP	<3
PARA_SERI	<50		VCIP	<3
EXTC	<50		VGH	<50
HDIR	<50		VGL	<50
VDIR	<50		RES1	<50
DUAL	<50		RES0	<50

17. POWER STRUCTURE

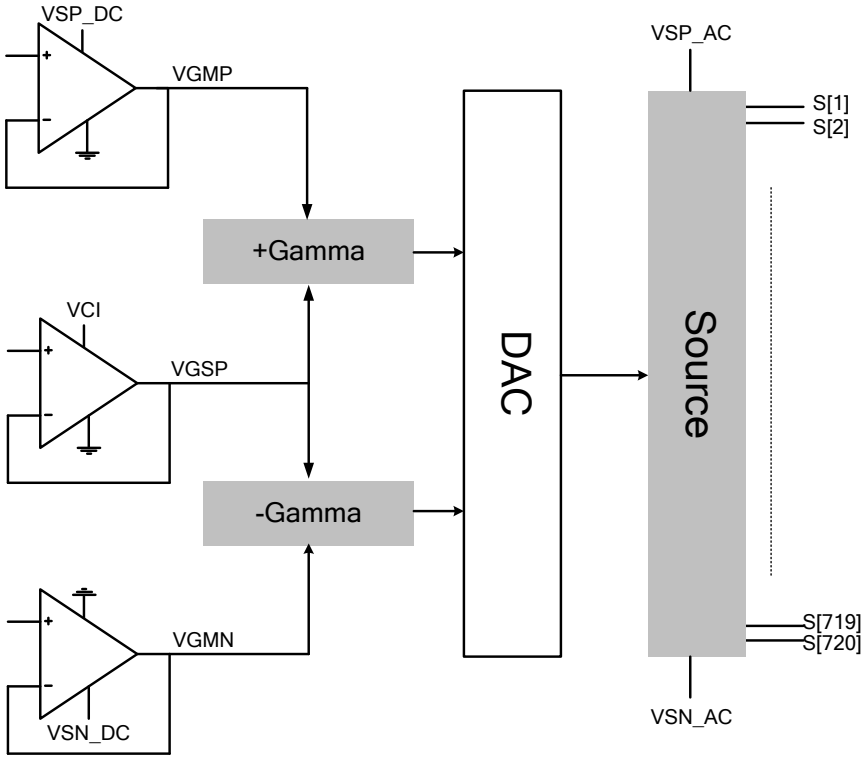
17.1 Voltage Generation

The following figure is relations of analog voltage.

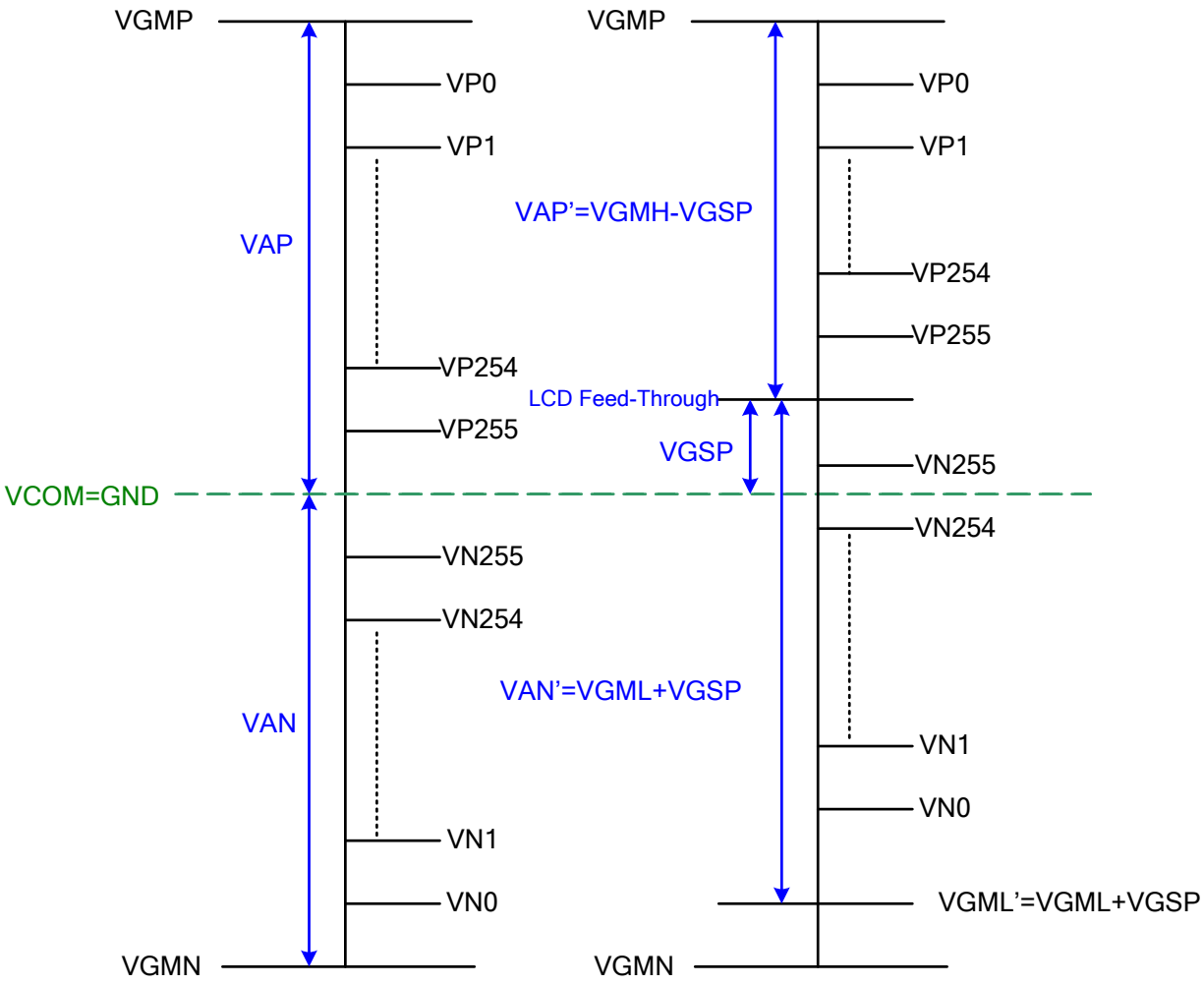


The figure of the below describe the relations of VSP_DC to VGMH, and VSN_DC to VGML.

The power supply for Source output is from VSP_AC and VSN_AC.

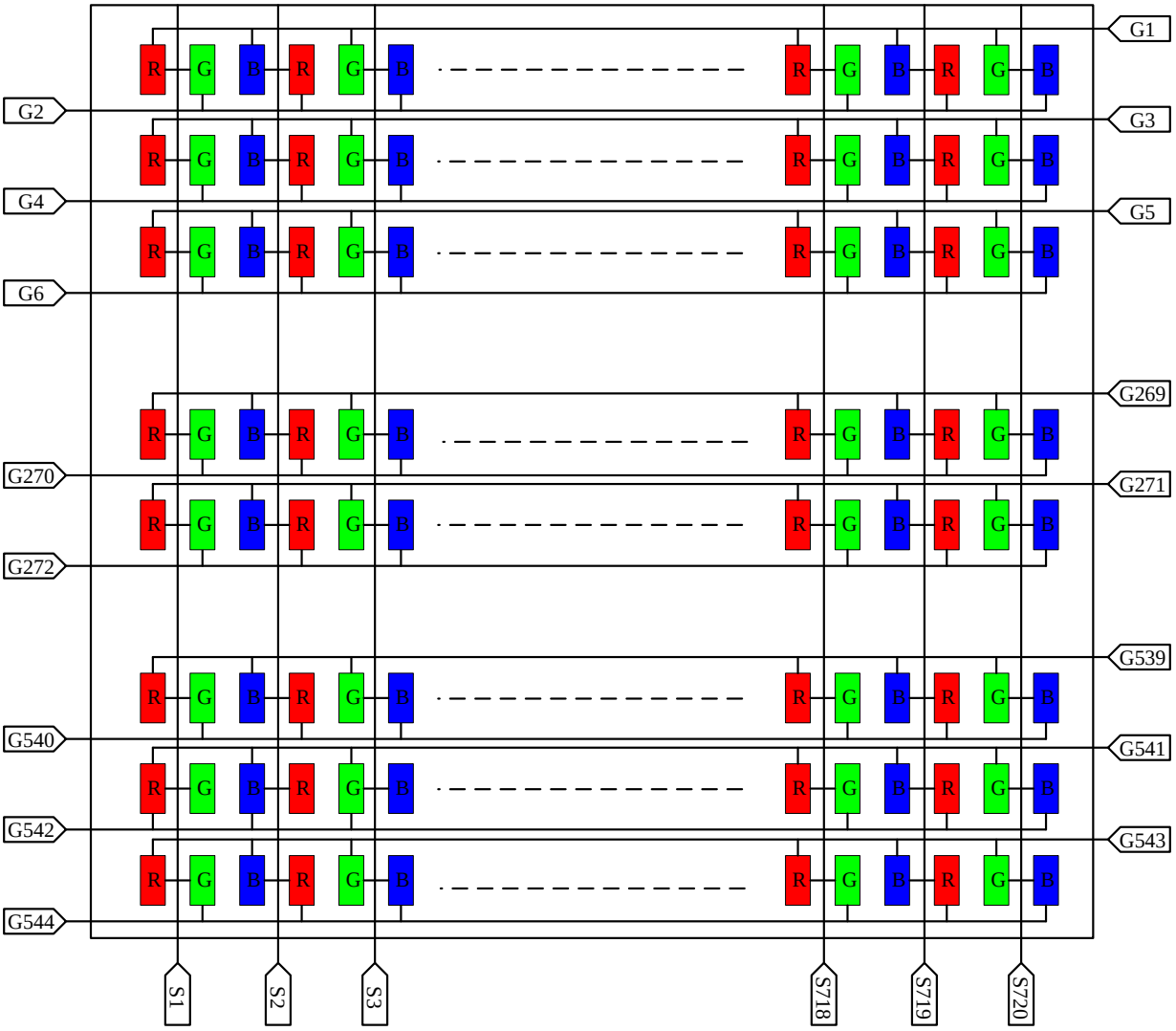


17.2 Source Voltage Relations



Note: VAP' = VGMP-VGSP and VAN'= VGMN+VGSP is LC voltage. Applied maximum voltage between LC is 6.2~ 5.2V, and the difference depends on panel feed-through voltage (panel feed-through voltage estimation is 0.5~ 1.5V).

18. COLOR FILTER ARRANGEMENT



19. REVISION HISTORY

Version No.	Date	Page	Description
001	2018/04/03	All	New Create