

#### NCE N-Channel Enhancement Mode Power MOSFET

#### **Description**

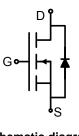
The NCE0106Z uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

#### **General Features**

- $V_{DS}$  = 100V, $I_D$  = 6A  $R_{DS(ON)}$  < 140mΩ @  $V_{GS}$ =10V (Typ:110mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

#### **Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply







TO-92 view

### **Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
0106Z	NCE0106Z	TO-92	-	-	-

Absolute Maximum Ratings (T<sub>A</sub>=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	VDS	100	V	
Gate-Source Voltage	V <sub>GS</sub>	±20	V	
Drain Current-Continuous	I <sub>D</sub>	6	Α	
Drain Current-Pulsed (Note 1)	I <sub>DM</sub>	24	Α	
Maximum Power Dissipation	P <sub>D</sub>	3	W	
Operating Junction and Storage Temperature Range	$T_{J},T_{STG}$	-55 To 150	$^{\circ}$	

#### **Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{ hetaJA}$	41.7	°C/W

#### Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	100	110	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V,V <sub>GS</sub> =0V	-	-	1	μA



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# **NCE0106Z**

Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)	1	1				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =5A	-	110	140	mΩ
Forward Transconductance	<b>g</b> FS	V <sub>DS</sub> =5V,I <sub>D</sub> =2.9A	-	8	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>lss</sub>	)/ OF)/)/ O)/	-	690	-	PF
Output Capacitance	C <sub>oss</sub>	- V <sub>DS</sub> =25V,V <sub>GS</sub> =0V, - F=1.0MHz	-	120	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>	F=1.UIVITZ	-	90	-	PF
Switching Characteristics (Note 4)			•	•		
Turn-on Delay Time	t <sub>d(on)</sub>		-	11	-	nS
Turn-on Rise Time	t <sub>r</sub>	$V_{DD}$ =30V, $I_{D}$ =2A, $R_{L}$ =15 $\Omega$ $V_{GS}$ =10V, $R_{G}$ =2.5 $\Omega$	-	7.4	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	35	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	9.1	-	nS
Total Gate Charge	Qg	\/ 20\/ L 24	-	15.5		nC
Gate-Source Charge	$Q_{gs}$	$V_{DS}=30V,I_{D}=3A,$	-	3.2	-	nC
Gate-Drain Charge	$Q_{gd}$	- V <sub>GS</sub> =10V	-	4.7	-	nC
Drain-Source Diode Characteristics	•		•	•		
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =6A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	6	Α

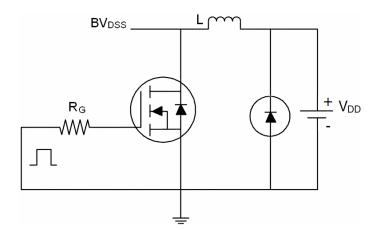
#### Notes:

- $\textbf{1.} \ \textbf{Repetitive Rating: Pulse width limited by maximum junction temperature}.$
- **2.** Surface Mounted on FR4 Board,  $t \le 10$  sec.
- **3.** Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2%.
- 4. Guaranteed by design, not subject to production

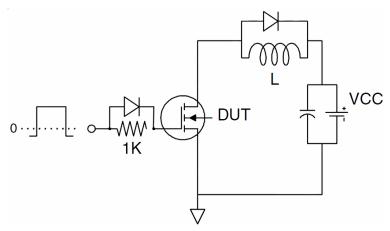


## **Test Circuit**

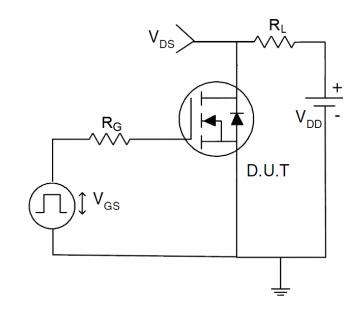
#### 1) E<sub>AS</sub> test circuit



#### 2) Gate charge test circuit



#### 3) Switch Time Test Circuit



#### Typical Electrical and Thermal Characteristics (curves)

Figure 1. Source-Drain Diode Forward Voltage

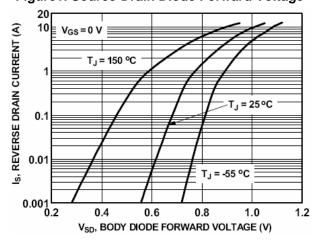


Figure3. Output characteristics

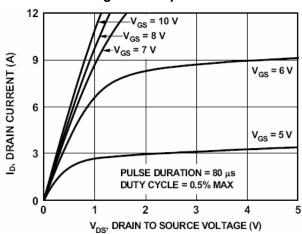


Figure 5. Static drain-source on resistance

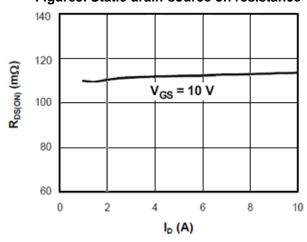


Figure 2. Safe operating area

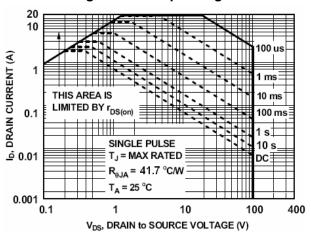


Figure 4. Transfer characteristics

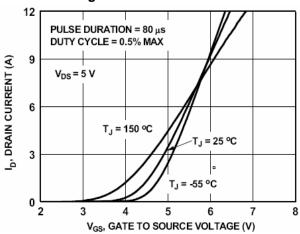


Figure 6. R<sub>DS(ON)</sub> vs Junction Temperature

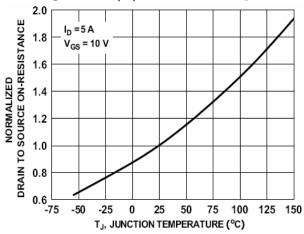


Figure 7. BV<sub>DSS</sub> vs Junction Temperature

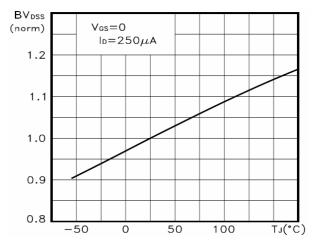


Figure 8. V<sub>GS(th)</sub> vs Junction Temperature

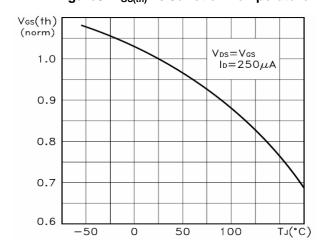


Figure9. Gate charge waveforms

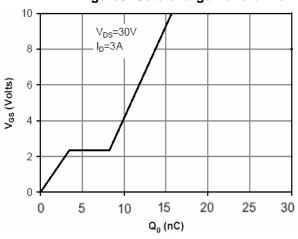
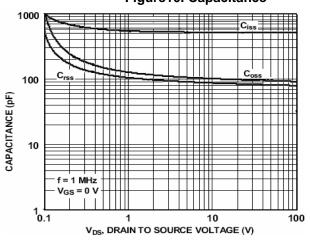


Figure10. Capacitance



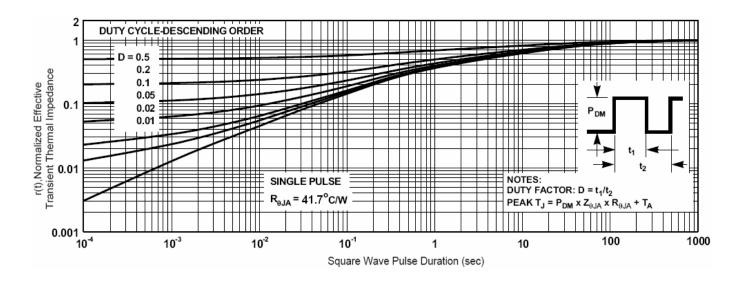
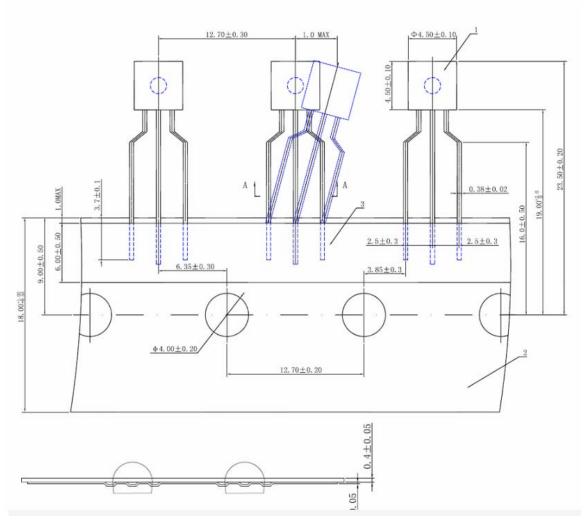
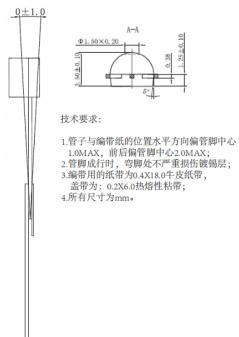


Figure 11. Normalized Maximum Transient Thermal Impedance

## **TO-92 Package Information**





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